

MM5452,MM5453

MM5452/MM5453 Liquid Crystal Display Drivers



Literature Number: SNLS367B

MM5452/MM5453

Liquid Crystal Display Drivers

General Description

The MM5452 is a monolithic integrated circuit utilizing CMOS metal gate, low threshold enhancement mode devices. It is available in a 40-pin molded package. The chip can drive up to 32 segments of LCD and can be paralleled to increase this number. The chip is capable of driving a 4½-digit 7-segment display with minimal interface between the display and the data source.

The MM5452 stores display data in latches after it is clocked in, and holds the data until new display data is received.

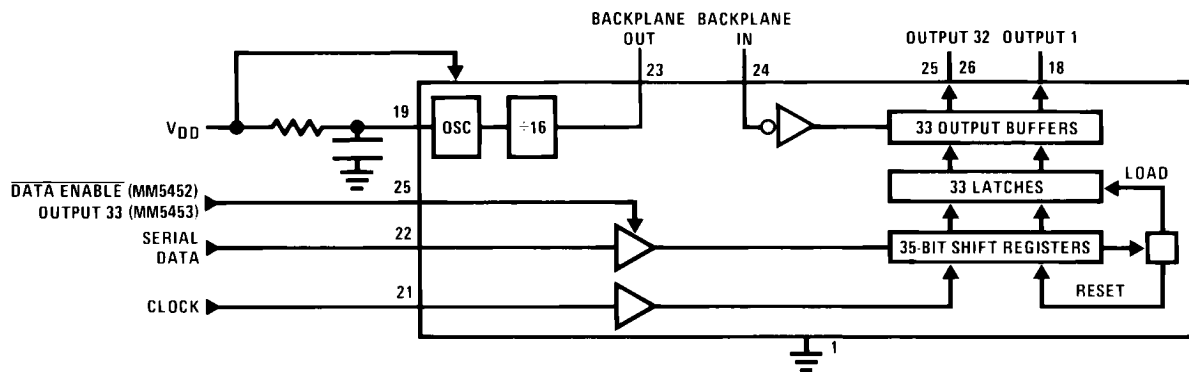
Features

- Serial data input
- No load signal required
- $\overline{\text{DATA ENABLE}}$ (MM5452)
- Wide power supply operation
- TTL compatibility
- 32 or 33 outputs
- Alphanumeric and bar graph capability
- Cascaded operation capability

Applications

- COPS™ or microprocessor displays
- Industrial control indicator
- Digital clock, thermometer, counter, voltmeter
- Instrumentation readouts
- Remote displays

Block Diagram



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FIGURE 1.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin, Referenced to Gnd	-0.3V to +10V
Storage Temperature	-65°C to +150°C
Power Dissipation at 25°C	350mW
Power Dissipation at 70°C	300mW
Junction Temperature	+150°C
Lead Temperature (Soldering, 10s)	300°C

Recommended Operating Conditions

V_{DD}	3V to 10V
Operating Temperature	-40°C to 85°C

Electrical Characteristics T_A within operating range, $V_{DD} = 3.0V$ to $10V$, $V_{SS} = 0V$ unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage, V_{DD}		3		10	V
Average Supply Current, I_{DD}	All Outputs Open, Clock=Gnd, Data=Gnd, OSC=Gnd, BP_IN @ 32Hz				
	$V_{DD} = 5V$			10	μA
	$V_{DD} = 10V$			40	μA
Input Logical '0' Voltage, V_{IL}	$V_{DD} = 3V$			0.4	V
	$V_{DD} = 5V$			0.8	V
	$V_{DD} = 10V$			0.8	V
Input Logical '1' Voltage, V_{IH}	$V_{DD} = 3V$	2.0			V
	$V_{DD} = 5V$	2.0			V
	$V_{DD} = 10V$	8.0			V
Segment Sink Current, I_{OL}	$V_{DD} = 3V$, $V_{OUT} = 0.3V$	-20	-40		μA
Segment Source Current, I_{OH}	$V_{DD} = 3V$, $V_{OUT} = 2.7V$	20	40		μA
Backplane Out Sink Current, I_{OL}	$V_{DD} = 3V$, $V_{OUT} = 0.3V$	-320	-500		μA
Backplane Out Source Current, I_{OH}	$V_{DD} = 3V$, $V_{OUT} = 2.7V$	320	500		μA
Segment Output Offset Voltage	Segment Load = 250pF (Note 2)			+/-50	mV
Backplane Output Offset Voltage	Backplane Load = 8750pF (Note 2)			+/-50	mV
Backplane Out Frequency	$R_{OSC_IN} = 50k\Omega$, $C_{OSC_IN} = 0.01\mu F$		75		Hz
Clock Input Frequency, f_{CLOCK}	$V_{DD} = 3V$ (Notes 2, 3)			500	kHz
	$V_{DD} = 5V$ (Note 2)			750	kHz
	$V_{DD} = 10V$ (Note 2)			1.0	MHz
Clock Input Duty Cycle		40		60	%
Data Input Set-Up Time, t_{DS}		300			ns
Data Input Hold Time, t_{DH}		300			ns
DataEnable Set-up Time, t_{DES}		100			ns

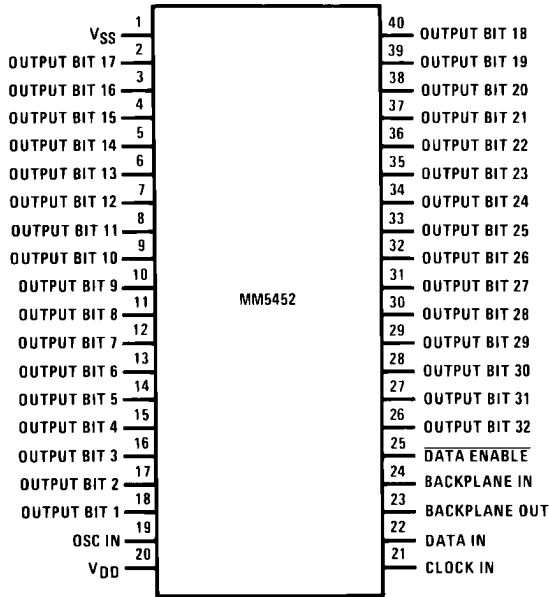
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: This parameter is guaranteed (but not production tested) over the operating temperature range and the operating supply voltage range. Not to be used in Q.A. testing.

Note 3: AC input waveform for test purposes: $t_r \leq 20ns$, $t_f \leq 20ns$, $f_{CLOCK} = 500kHz$, Duty Cycle = 50% $\pm$ 10%

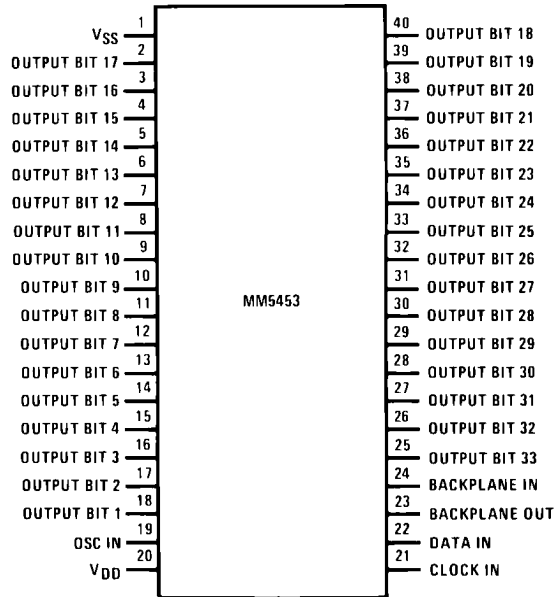
Note 4: Clock input rise time (t_r) and fall time (t_f) must not exceed 300ns

Connection Diagrams



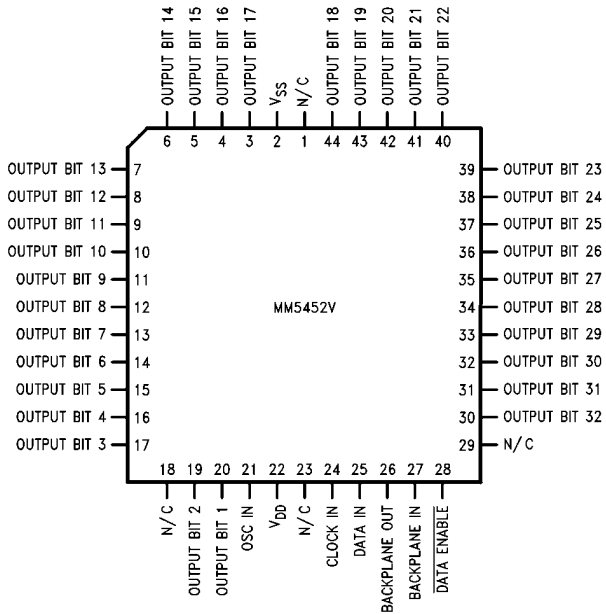
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Top View
Order Number MM5452N
 See NS Package Number N40A



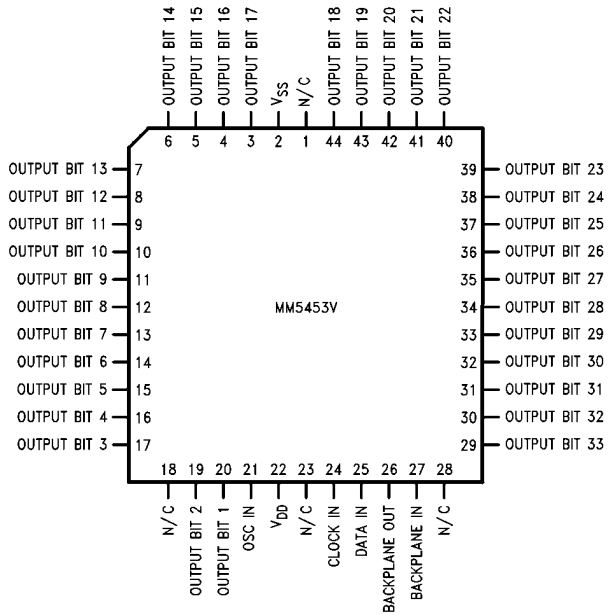
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Top View
Order Number MM5453N
 See NS Package Number N40A



613711

Top View
Order Number MM5452V
 See NS Package Number V44A



613712

Top View
Order Number MM5453V
 See NS Package Number V44A

Functional Description

The MM5452 is specifically designed to operate 4½-digit 7-segment displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Since the MM5452 does not contain a character generator, the formatting of the segment information must be done prior to inputting the data to the MM5452. Using a format of a leading "1" followed by the 32 data bits allows data transfer without an additional load signal. The 32 data bits are latched after the 36th clock is complete, thus providing non-multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time.

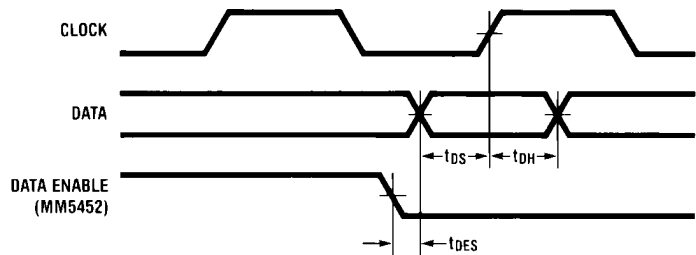
A block diagram is shown in *Figure 1*. For the MM5452 a DATA ENABLE is used instead of the 33rd output. If the DATA ENABLE signal is not required, the 33rd output can be brought out. This is the MM5453 device.

Figure 3 shows the input data format. A start bit of logical "1" precedes the 32 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 32 bits of the shift registers into the latches. At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master-slave configuration. There is no clear for the master portion of the first shift register, thus allowing continuous operation.

If the clock is not continuous, there must be at least a complete set of 36 clocks otherwise the shift registers will not load and clear.

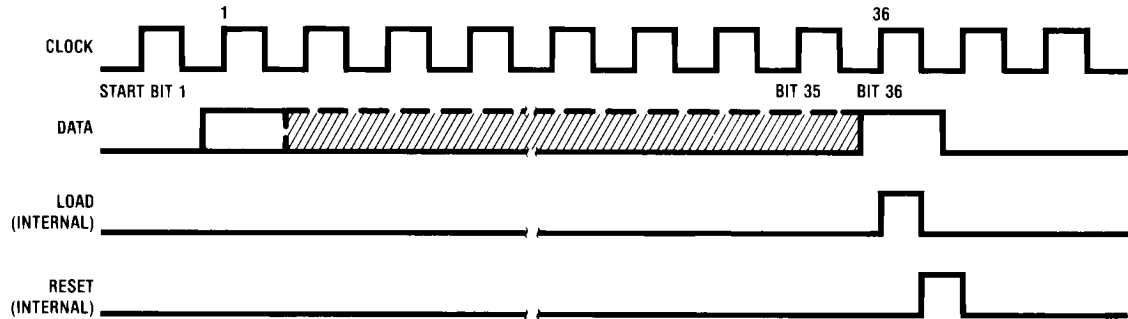
Bit 1 is the first bit following the start bit and it will appear on device pin 18 of the MM5452N and MM5453N, and on device pin 20 of the MM5452V and MM5453V.

Figure 2 shows the timing relationships between data, clock and DATA ENABLE.



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FIGURE 2. Timing Diagram



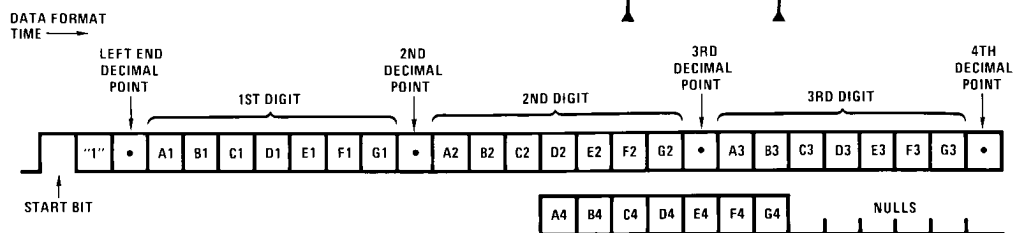
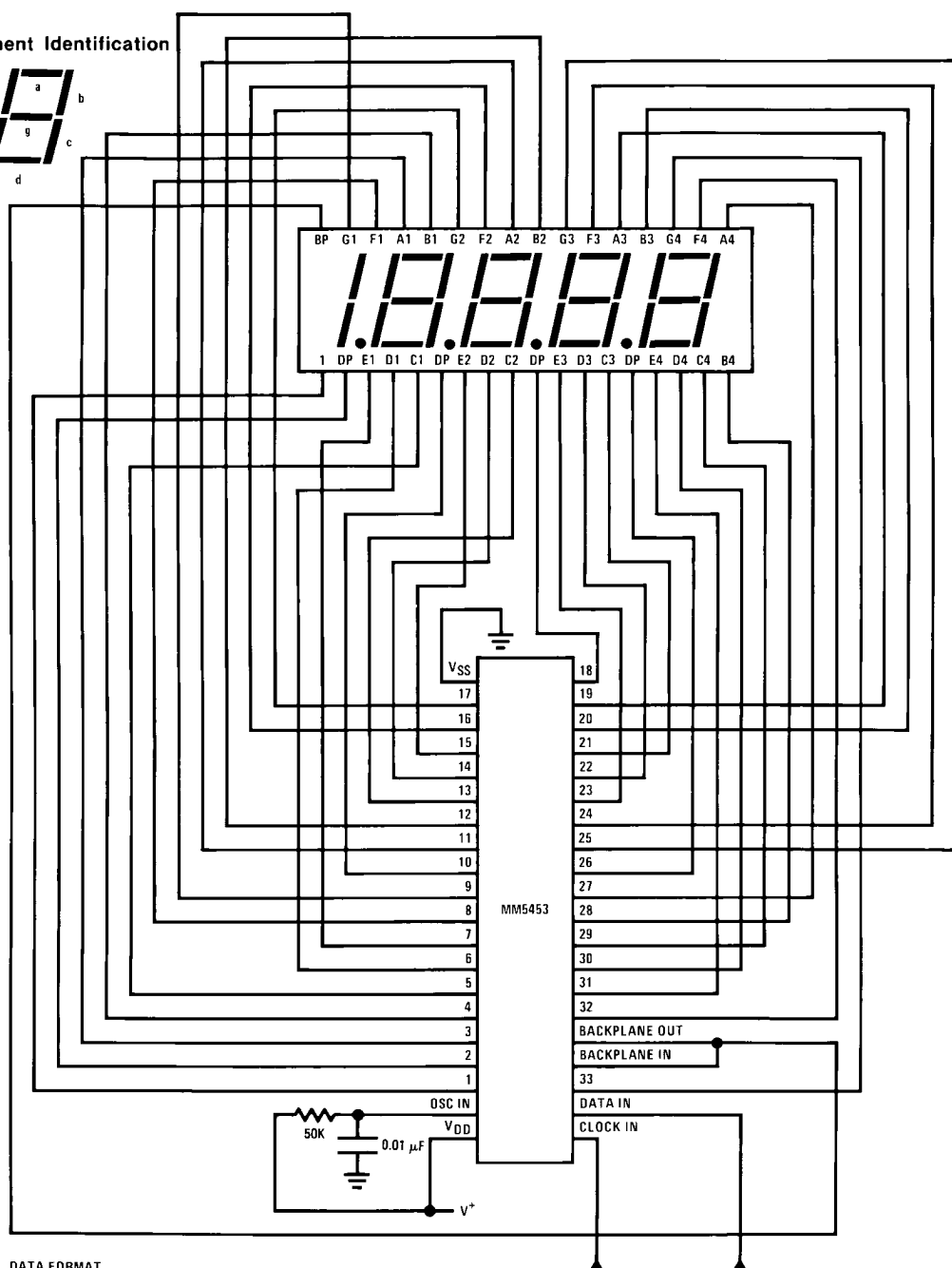
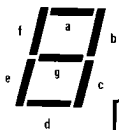
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FIGURE 3. Input Data Format

Figure 4 shows a typical application. Note how the input data maps to the output pins and the display. The MM5452 and MM5453 do not have format restrictions, as all outputs are

controllable. The application assumes a specific display pinout. Different display/driver connection patterns will, of course, yield a different input data format.

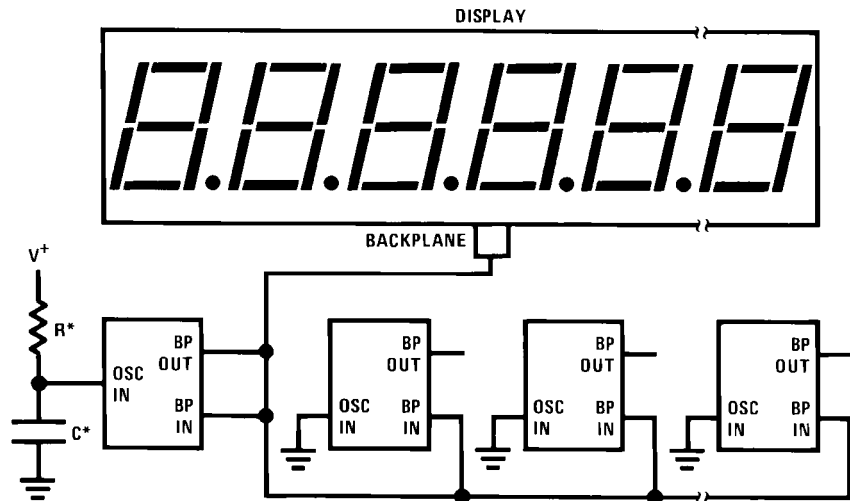
Segment Identification



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Consult LCD manufacturer's data sheet for specific pinouts.

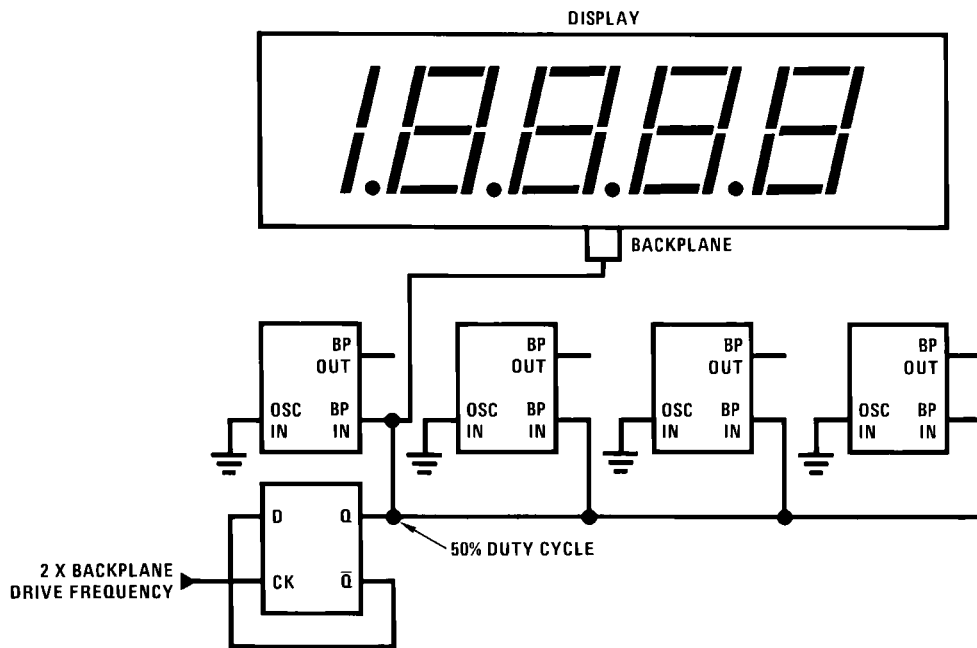
FIGURE 4. Typical 4½-Digit Display Application



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*The minimum recommended value for R for the oscillator input is 9 k Ω . An RC time constant of approximately 4.91×10^{-4} should produce a backplane frequency between 30 Hz and 150 Hz.

FIGURE 5. Parallel Backplane Outputs



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FIGURE 6. External Backplane Clock

Figure 7 shows a four wire remote display that takes advantage of the device's serial input to move many bits of display information on a few wires.

USING AN EXTERNAL CLOCK

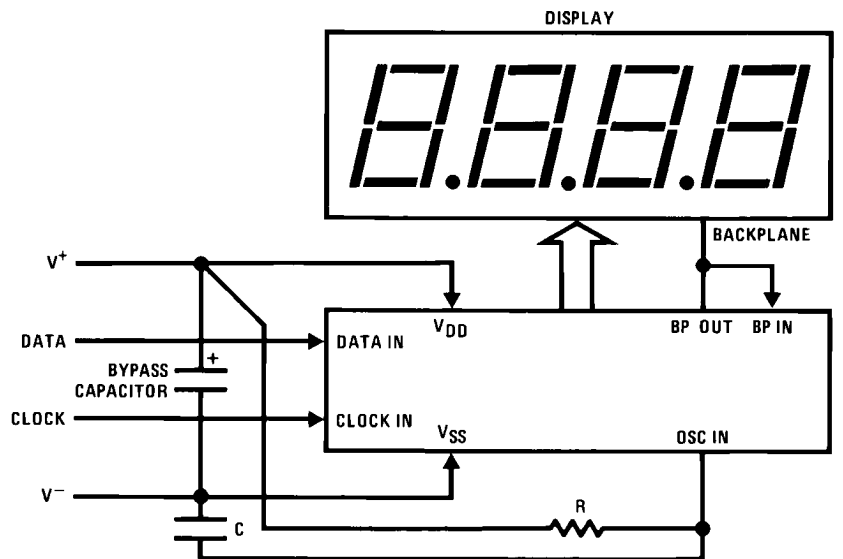
The MM5452/MM5453 LCD Drivers can be used with an externally supplied clock, provided it has a duty cycle of 50%. Deviations from a 50% duty cycle result in an offset voltage on the LCD. In Figure 6, a flip-flop is used to assure a 50% duty cycle. The oscillator input is grounded to prevent oscillation and reduce current consumptions in the chips. The oscillator is not used.

Using an external clock allows synchronizing the display drive with AC power, internal clocks, or DVM integration time to reduce interference from the display.

Figure 8 is a general block diagram that shows how the device's serial input can be used to advantage in an analog display. The analog voltage input is compared with a staircase voltage generated by a counter and a digital-to-analog converter or resistor array. The result of this comparison is clocked into the MM5452, MM5453. The next clock pulse increments the staircase and clocks the new data in.

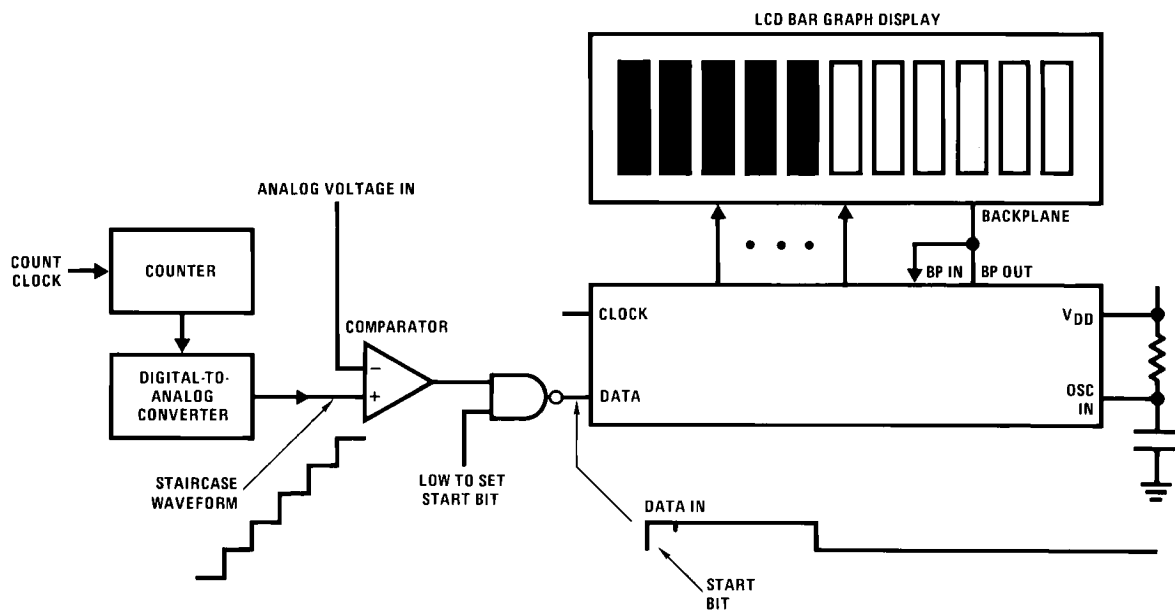
With a buffer amplifier, the same staircase waveform can be used for many displays. The digital-to-analog converter need not be linear; logarithmic or other non-linear functions can be displayed by using weighted resistors or special DACs. This

system can be used for status indicators, spectrum analyzers, audio level and power meters, tuning indicators, and other applications.



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FIGURE 7. Four Wire Remote Display

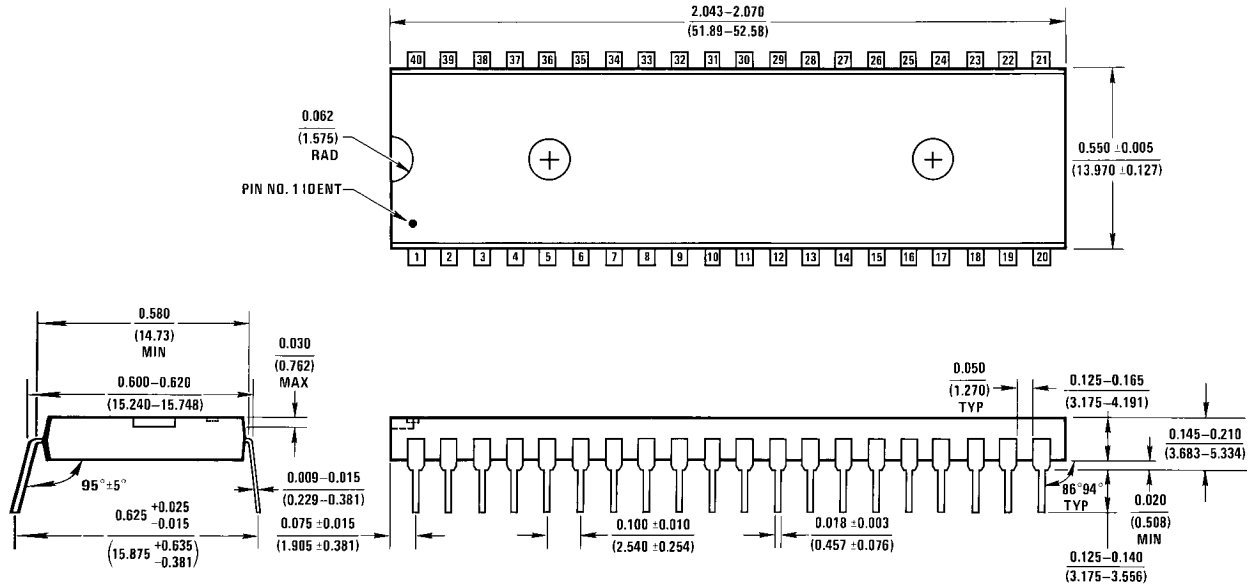


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Data is high until staircase > input

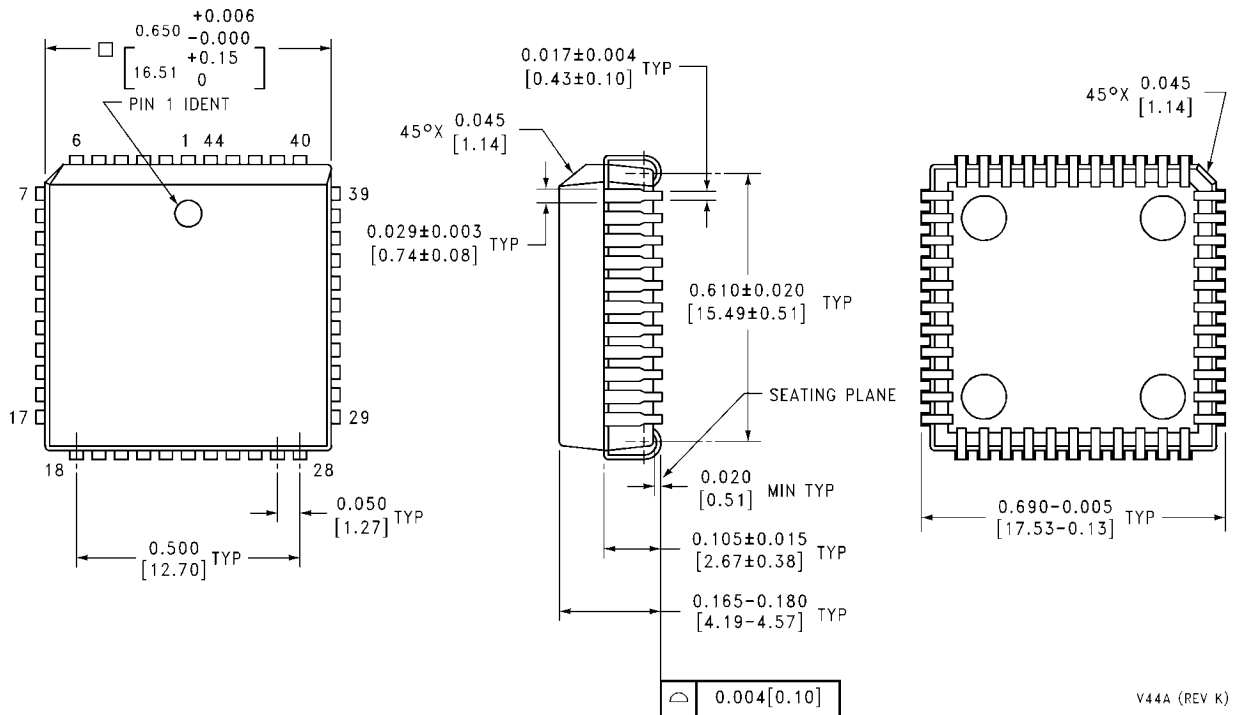
FIGURE 8. Analog Display

Physical Dimensions inches (millimeters) unless otherwise noted



N40A (REV E)

40-Pin Molded Dual-In-Line Package (N)
Order Number MM5452N or MM5453N
NS Package Number N40A



V44A (REV K)

44-Pin Plastic Chip Carrier (V)
Order Number MM5452V or MM5453V
NS Package Number V44A

Notes

Notes

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