16/20-BIT SINGLE-ENDED ANALOG INPUT/OUTPUT STEREO AUDIO CODECS

FEATURES

- **Monolithic 20-Bit ΔΣ ADC and DAC**
- **16/20-Bit Input/Output Data**
- **Software Control: PCM3002**
- **Hardware Control: PCM3003**
- **Stereo ADC:**
  - **Single-Ended Voltage Input**
  - **Antialiasing Filter**
  - **64× Oversampling**
  - **High Performance**
    - **THD+N: –86 dB**
    - **SNR: 90 dB**
    - **Dynamic Range: 90 dB**
- **Stereo DAC:**
  - **Single-Ended Voltage Output**
  - **Analog Low-Pass Filter**
  - **64× Oversampling**
  - **High Performance**
    - **THD+N: –86 dB**
    - **SNR: 94 dB**
    - **Dynamic Range: 94 dB**
- **Special Features (PCM3002, PCM3003)**
  - **Digital De-Emphasis: 32 kHz, 44.1 kHz, 48 kHz**
  - **Power Down: ADC/DAC Independent**
- **Special Features (PCM3002)**
  - **Digital Attenuation (256 Steps)**
  - **Soft Mute**
  - **Digital Loopback**
  - **Four Alternative Audio Data Formats**
- **Sampling Rate: 4 kHz to 48 kHz**
- **Single 3-V Power Supply**
- **Small Package: SSOP-24**

APPLICATIONS

- **DVC Applications**
- **DSC Applications**
- **Portable/Mobile Audio Applications**

DESCRIPTION

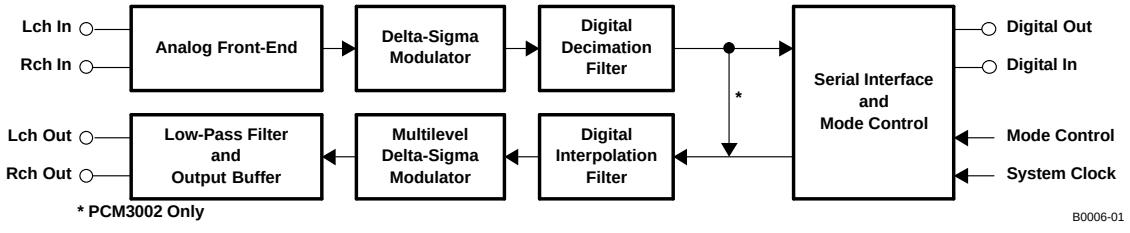
The PCM3002 and PCM3003 are low-cost, single-chip stereo audio codecs (analog-to-digital and digital-to-analog converters) with single-ended analog voltage input and output.

The ADCs and DACs employ delta-sigma modulation with 64-times oversampling. The ADCs include a digital decimation filter, and the DACs include an 8-times oversampling digital interpolation filter. The DACs also include digital attenuation, de-emphasis, infinite zero detection, and soft mute to form a complete subsystem. The PCM3002 and PCM3003 operate with left-justified (ADC) and right-justified (DAC) formats, while the PCM3002 also supports other formats, including the I^2S data format.

The PCM3002 and PCM3003 provide a power-down mode that operates on the ADCs and DACs independently.

The PCM3002 and PCM3003 are fabricated using a highly advanced CMOS process, and are available in a 24-pin SSOP package. The PCM3002 and PCM3003 are suitable for a wide variety of cost-sensitive consumer applications where good performance is required.

The PCM3002 programmable functions are controlled by software. The PCM3003 functions, which are controlled by hardware, include de-emphasis, power-down, and audio data format selections.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ELECTRICAL CHARACTERISTICS

All specifications at T_A = 25°C, V_{DD} = V_{CC} = 3 V, f_S = 44.1 kHz, SYSCLK = 384 f_S, and 16-bit data, unless otherwise noted

PARAMETER		CONDITIONS	PCM3002E/3003E			
			MIN	TYP	MAX	UNITS
DIGITAL INPUT/OUTPUT						
Input Logic						
V_{IH} (1)(2)(3)	Input logic level		0.7 V_{DD}			VDC
V_{IL} (1)(2)(3)					0.3 V_{DD}	
I_{IN} (2)	Input logic current				±1	µA
I_{IN} (1)(3)					100	
Output Logic						
V_{OH} (4)	Output logic level	I_{OUT} = –1 mA	V_{DD} – 0.3			VDC
V_{OL} (4)		I_{OUT} = 1 mA			0.3	
V_{OL} (5)		I_{OUT} = 1 mA			0.3	
CLOCK FREQUENCY						
f_s	Sampling frequency		4 (6)	44.1	48	kHz
	System clock frequency	256 f_S	1.024	11.2896	12.288	MHz
		384 f_S	1.536	16.9344	18.432	
		512 f_S	2.048	22.5792	24.576	
ADC CHARACTERISTICS						
Resolution				20		Bits
DC Accuracy						
	Gain mismatch, channel-to-channel			±1	±3	% of FSR
	Gain error			±2	±5	% of FSR
	Gain drift			±20		ppm of FSR/°C
	Bipolar zero error	High-pass filter bypassed (7)		±1.7		% of FSR
	Bipolar zero drift	High-pass filter bypassed (7)		±20		ppm of FSR/°C
Dynamic Performance (8)						
	THD+N	V_{IN} = –0.5 dB		–86	–80	dB
		V_{IN} = –60 dB		–28		
	Dynamic range	A-weighted	86	90		dB
	Signal-to-noise ratio	A-weighted	86	90		dB
	Channel separation		84	88		dB

(1) Pins 7, 8, 17 and 18: $\overline{RST}$, ML, MD, and MC for the PCM3002; $\overline{PDAD}$, $\overline{PDDA}$, DEM1, and DEM0 for PCM3003 (Schmitt-trigger input with 100-kΩ typical internal pulldown resistor)
(2) Pins 9, 10, 11, 15: SYSCLK, LRCIN, BCKIN, DIN (Schmitt-trigger input)
(3) Pin 16: 20BIT for PCM3003 (Schmitt-trigger input, 100-kΩ typical internal pulldown resistor)
(4) Pin 12: DOUT
(5) Pin 16: $\overline{ZFLG}$ for PCM3002 (open-drain output)
(6) See Application Bulletin SBAA033 for information relating to operation at lower sampling frequencies.
(7) High-pass filter for offset cancel
(8) f_{IN} = 1 kHz, using the System Two™ audio measurement system by Audio Precision™ in rms mode with 20-kHz LPF, 400-Hz HPF used for performance calculation.

ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, V_{DD} = V_{CC} = 3 V, f_S = 44.1 kHz, SYSCLK = 384 f_S, and 16-bit data, unless otherwise noted

PARAMETER	CONDITIONS	PCM3002E/3003E			
		MIN	TYP	MAX	UNITS
Digital Filter Performance					
Pass band				0.454 f_S	Hz
Stop band		0.583 f_S			Hz
Pass-band ripple				±0.05	dB
Stop-band attenuation		–65			dB
Delay time			17.4/f_S		s
HPF frequency response	–3 dB		0.019 f_S		mHz
Analog Input					
Voltage range			0.6 V_{CC}		Vp-p
Center voltage			0.5 V_{CC}		VDC
Input impedance			30		kΩ
Antialiasing filter frequency response	–3 dB		150		kHz
DAC CHARACTERISTICS					
Resolution			20		Bits
DC Accuracy					
Gain mismatch, channel-to-channel			±1	±3	% of FSR
Gain error			±1	±5	% of FSR
Gain drift			±20		ppm of FSR/°C
Bipolar zero error			±2.5		% of FSR
Bipolar zero drift			±20		ppm of FSR/°C
Dynamic Performance[9]					
THD+N	V_{OUT} = 0 dB (full scale)		–86	–80	dB
	V_{OUT} = –60 dB		–32		
Dynamic range	EIAJ, A-weighted	88	94		dB
Signal-to-noise ratio	EIAJ, A-weighted	88	94		dB
Channel separation		86	91		dB
Digital Filter Performance					
Pass band				0.445 f_S	Hz
Stop band		0.555 f_S			Hz
Pass-band ripple				±0.17	dB
Stop-band attenuation		–35			dB
Delay time			11.1/f_S		s
Analog Output					
Voltage range			0.6 V_{CC}		Vp-p
Center voltage			0.5 V_{CC}		VDC
Load impedance	AC coupling	10			kΩ
LPF frequency response	f = 20 kHz		–0.16		dB

(9) f_{OUT} = 1 kHz, using the System Two audio measurement system by Audio Precision in rms mode with 20-kHz LPF, 400-Hz HPF used for performance calculation.

ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, V_{DD} = V_{CC} = 3 V, f_S = 44.1 kHz, SYSCLK = 384 f_S, and 16-bit data, unless otherwise noted

PARAMETER		CONDITIONS	PCM3002E/3003E			
			MIN	TYP	MAX	UNITS
POWER SUPPLY REQUIREMENTS						
V_{CC}, V_{DD}	Supply voltage	–25°C to 85°C	2.7	3	3.6	VDC
		0° C to 70°C(10)	2.4	3	3.6	VDC
	Supply current	Operation, V_{CC} = V_{DD} = 3 V		18	24	mA
		Power down, V_{CC} = V_{DD} = 3 V		50		µA
	Power dissipation	Operation, V_{CC} = V_{DD} = 3 V		54	72	mW
		Power down(11), V_{CC} = V_{DD} = 3 V		150		µW
TEMPERATURE RANGE						
T_A	Operation		–25		85	°C
T_{stg}	Storage		–55		125	°C
θ_{JA}	Thermal resistance			100		°C/W

(10) Applies for voltages between 2.4 V and 2.7 V for 0°C to 70°C and 256 f_S/512 f_S operation (384 f_S not available)
(11) SYSCLK, BCKIN, and LRCIN are stopped.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE TYPE	PACKAGE CODE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA	QUANTITY
PCM3002E	24-pin SSOP	DB	PCM3002E	PCM3002E	Rails	58
				PCM3002E/2K	Tape and reel	2000
PCM3003E	24-pin SSOP	DB	PCM3003E	PCM3003E	Rails	58
				PCM3003E/2K	Tape and reel	2000

ABSOLUTE MAXIMUM RATINGS

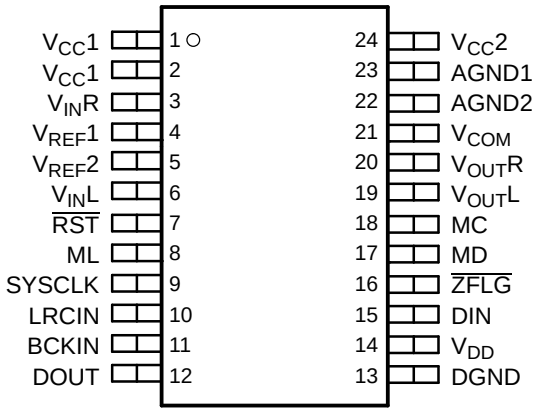
Supply voltage V_{DD}, $V_{CC}1$, $V_{CC}2$	–0.3 V to 6.5 V
Supply voltage differences	±0.1 V
GND voltage differences	±0.1 V
Digital input voltage	–0.3 V to V_{DD} + 0.3 V, < 6.5 V
Analog input voltage	–0.3 V to $V_{CC}1$, $V_{CC}2$ + 0.3 V, < 6.5 V
Power dissipation	300 mW
Input current (any pins except supplies)	±10 mA
Operating temperature	–25°C to 85°C
Storage temperature	–55°C to 125°C
Lead temperature, soldering	260°C, 5 s
Package temperature (IR reflow, peak)	235°C

RECOMMENDED OPERATING CONDITIONS

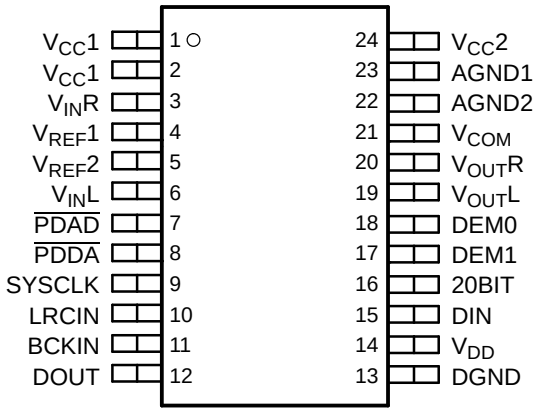
over operating free-air temperature range

		MIN	NOM	MAX	UNIT
Analog supply voltage, $V_{CC}1$, $V_{CC}2$		2.7	3	3.6	V
Digital supply voltage, V_{DD}		2.7	3	3.6	V
Analog input voltage, full scale (–0 dB)	V_{CC} = 3 V		1.8		Vp-p
Digital input logic family			CMOS		
Digital input clock frequency	System clock	8.192		24.576	MHz
	Sampling clock	32		48	kHz
Analog output load resistance		10			kΩ
Analog output load capacitance			30		pF
Digital output load capacitance			10		pF
Operating free-air temperature, T_A		–25		85	°C

PCM3002
(TOP VIEW)



PCM3003
(TOP VIEW)



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PIN ASSIGNMENTS—PCM3002

NAME	PIN	I/O	DESCRIPTION
AGND1	23	–	ADC analog ground
AGND2	22	–	DAC analog ground
BCKIN	11	I	Bit clock input(1)
DGND	13	–	Digital ground
DIN	15	I	Data input(1)
DOUT	12	O	Data output
LRCIN	10	I	Sample rate clock input (f_s)(1)
MC	18	I	Bit clock for mode control(1)(2)
MD	17	I	Serial data for mode control(1)(2)
ML	8	I	Strobe pulse for mode control(1)(2)
$\overline{RST}$	7	I	Reset, active LOW(1)(2)
SYSCLK	9	I	System clock input(1)
$V_{CC}1$	1, 2	–	ADC analog power supply
$V_{CC}2$	24	–	DAC analog power supply
V_{COM}	21	–	ADC/DAC common
V_{DD}	14	–	Digital power supply

(1) Schmitt-trigger input
(2) With 100-kΩ typical internal pulldown resistor

PIN ASSIGNMENTS—PCM3002 (continued)

NAME	PIN	I/O	DESCRIPTION
$V_{IN}L$	6	I	ADC analog input, Lch
$V_{IN}R$	3	I	ADC analog input, Rch
$V_{OUT}L$	19	O	DAC analog output, Lch
$V_{OUT}R$	20	O	DAC analog output, Rch
$V_{REF}1$	4	–	ADC reference 1
$V_{REF}2$	5	–	ADC reference 2
$\overline{ZFLG}$	16	O	Zero flag output, active LOW(3)

(3) Open-drain output

PIN ASSIGNMENTS—PCM3003

NAME	PIN	I/O	DESCRIPTION
AGND1	23	–	ADC analog ground
AGND2	22	–	DAC analog ground
BCKIN	11	I	Bit clock input(1)
DEM0	18	I	De-emphasis control 0(1)(2)
DEM1	17	I	De-emphasis control 1(1)(2)
DGND	13	–	Digital ground
DIN	15	I	Data input(1)
DOUT	12	O	Data output
LRCIN	10	I	Sample rate clock input (f_S)(1)
$\overline{PDAD}$	7	I	ADC power down, active LOW(1)(2)
$\overline{PDDA}$	8	I	DAC power down, active LOW(1)(2)
SYSCLK	9	I	System clock input(1)
$V_{CC}1$	1, 2	–	ADC analog power supply
$V_{CC}2$	24	–	DAC analog power supply
V_{COM}	21	–	ADC/DAC common
V_{DD}	14	–	Digital power supply
$V_{IN}L$	6	I	ADC analog input, Lch
$V_{IN}R$	3	I	ADC analog input, Rch
$V_{OUT}L$	19	O	DAC analog output, Lch
$V_{OUT}R$	20	O	DAC analog output, Rch
$V_{REF}1$	4	–	ADC reference 1
$V_{REF}2$	5	–	ADC reference 2
20BIT	16	I	20-bit format select(1)(2)

(1) Schmitt-trigger input
(2) With 100-kΩ typical internal pulldown resistor

TYPICAL PERFORMANCE CURVES

All specifications at T_A = 25°C, V_{CC} = V_{DD} = 3 V, f_S = 44.1 kHz, f_{SYSCLK} = 384 f_S, and f_{SIGNAL} = 1 kHz, unless otherwise noted

ADC SECTION

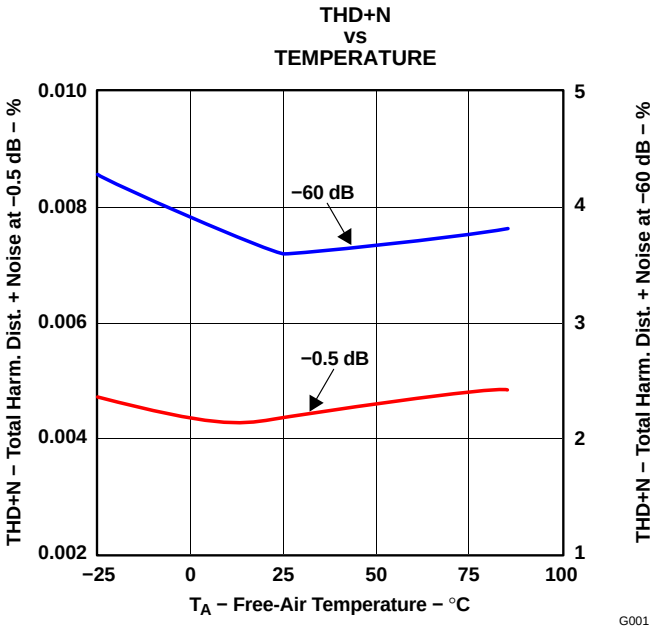


Figure 1.

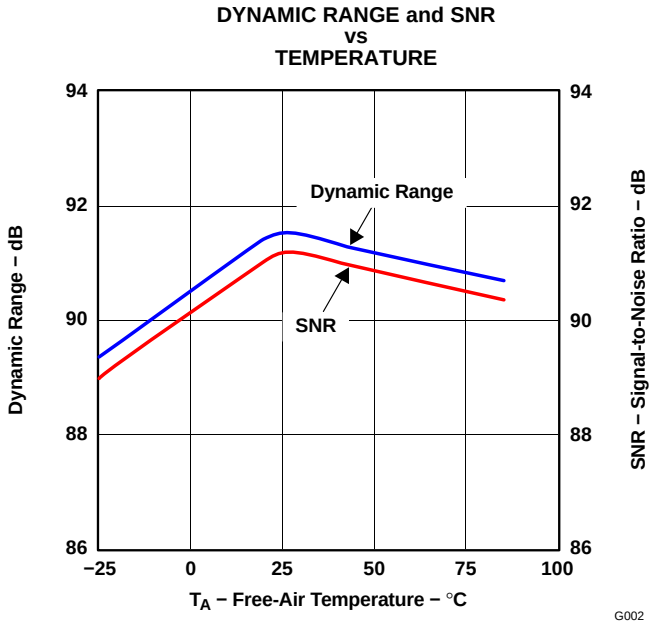


Figure 2.

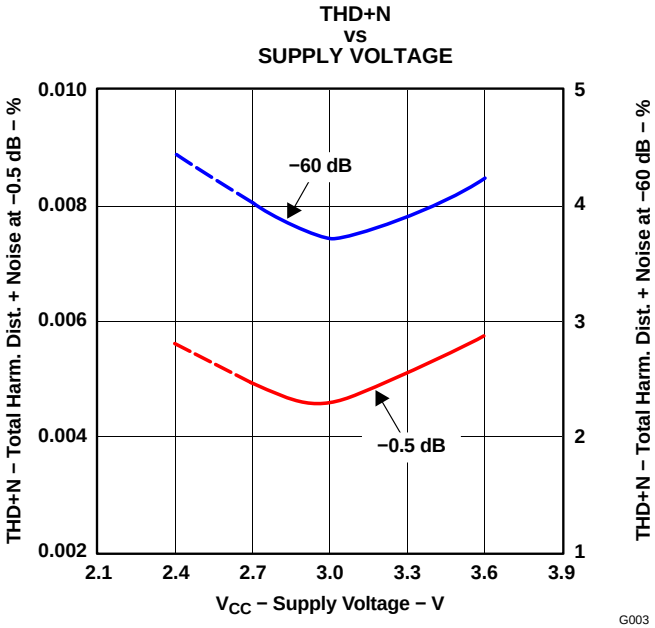


Figure 3.

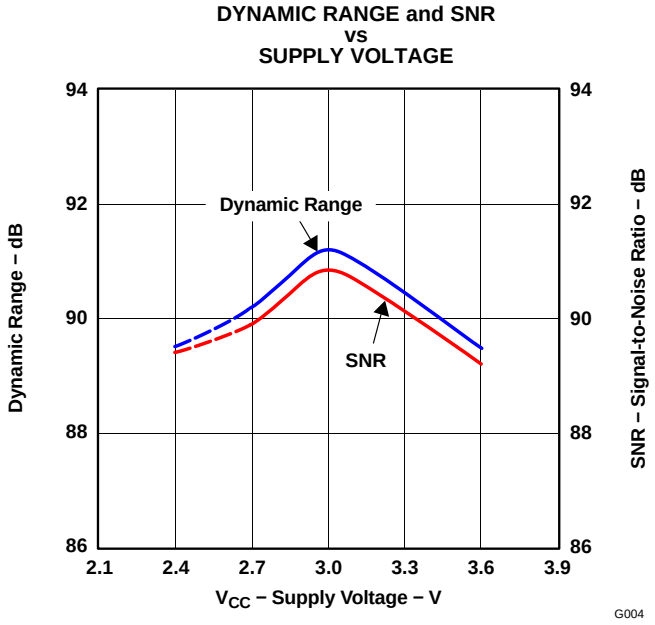


Figure 4.

NOTE: All characteristics at supply voltages from 2.4 V to 2.7 V are measured at SYSCLK = 256 f_S.

TYPICAL PERFORMANCE CURVES (continued)

All specifications at T_A = 25°C, V_{CC} = V_{DD} = 3 V, f_S = 44.1 kHz, f_{SYSCLK} = 384 f_S, and f_{SIGNAL} = 1 kHz, unless otherwise noted

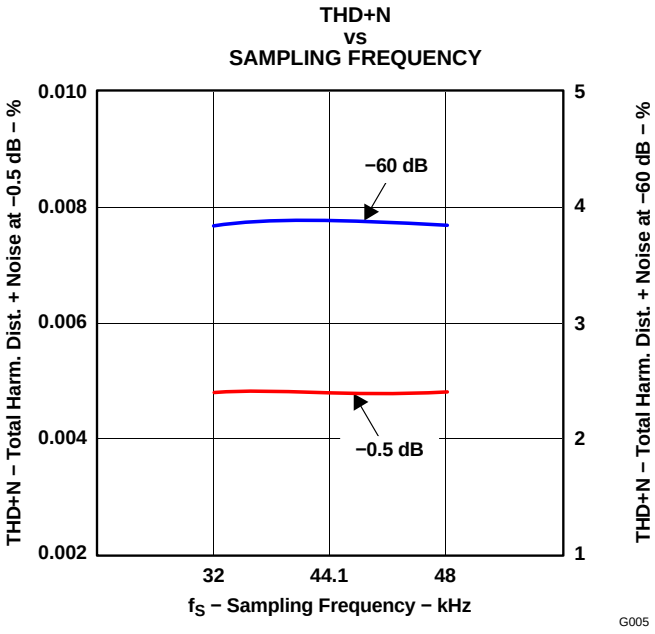


Figure 5.

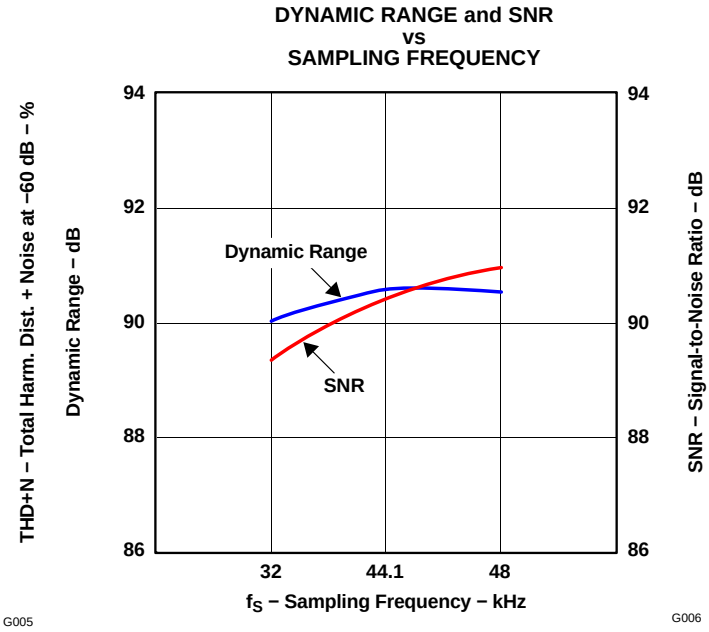


Figure 6.

DAC SECTION

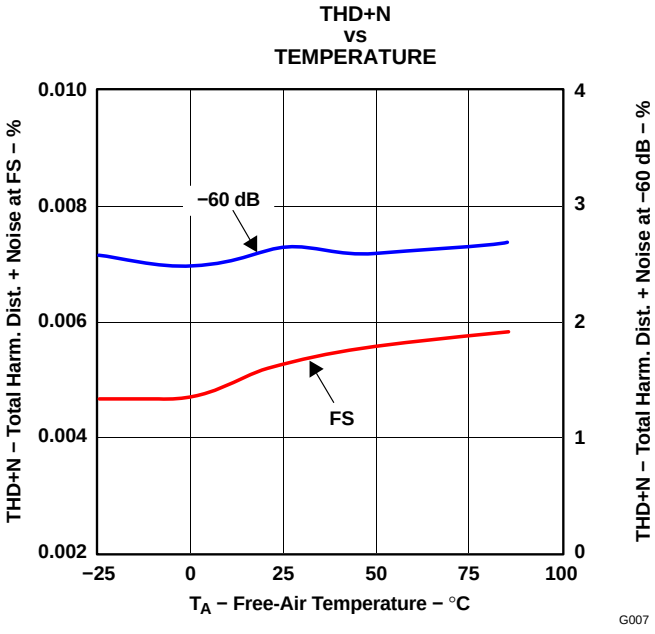


Figure 7.

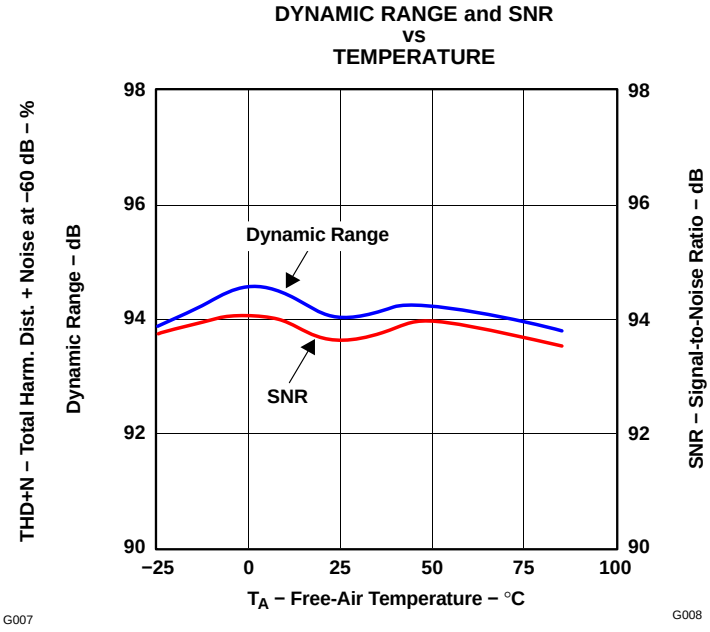


Figure 8.

TYPICAL PERFORMANCE CURVES (continued)

All specifications at T_A = 25°C, V_{CC} = V_{DD} = 3 V, f_S = 44.1 kHz, f_{SYSCLK} = 384 f_S, and f_{SIGNAL} = 1 kHz, unless otherwise noted

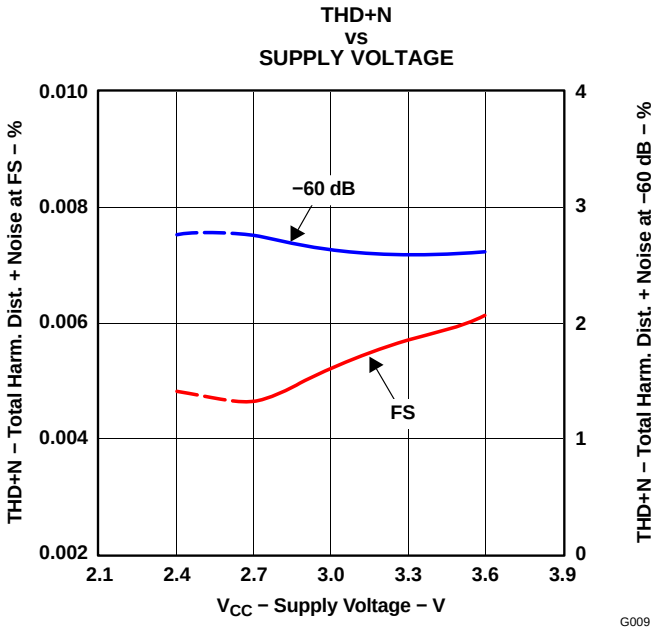


Figure 9.

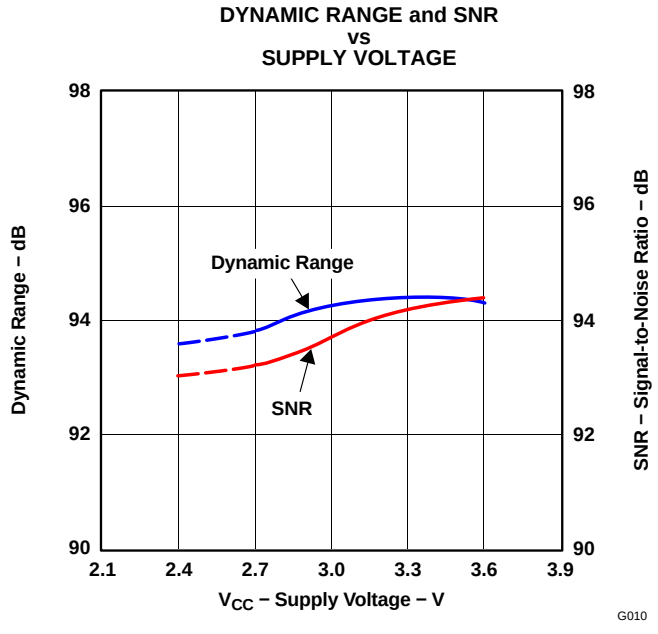


Figure 10.

NOTE: All characteristics at supply voltages from 2.4 V to 2.7 V are measured at SYSCLK = 256 f_S.

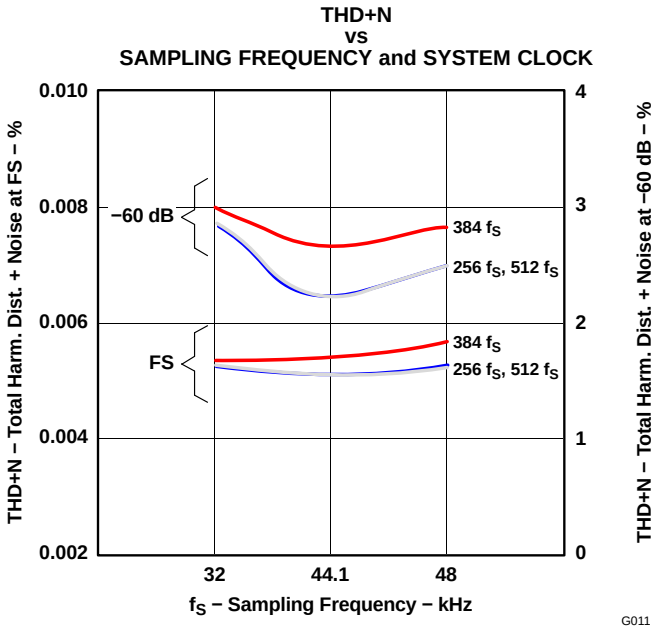


Figure 11.

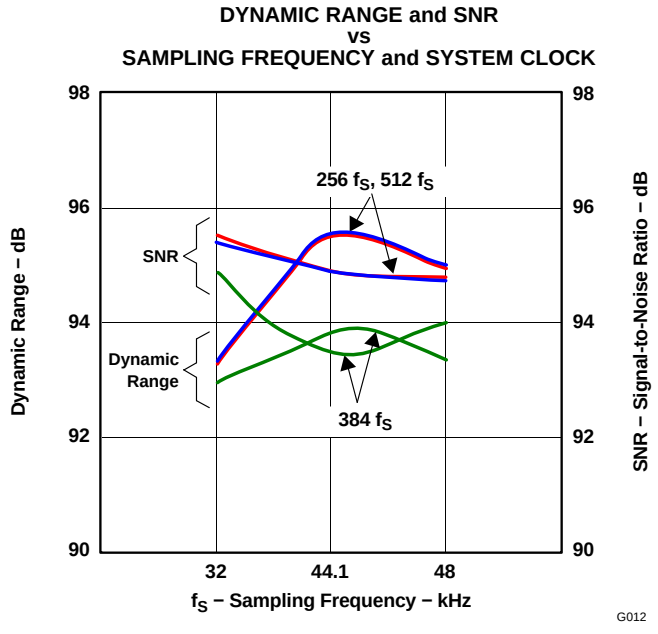


Figure 12.

TYPICAL PERFORMANCE CURVES (continued)

All specifications at T_A = 25°C, V_{CC} = V_{DD} = 3 V, f_S = 44.1 kHz, f_{SYSCLK} = 384 f_S, and f_{SIGNAL} = 1 kHz, unless otherwise noted

OUTPUT SPECTRUM

ADCs

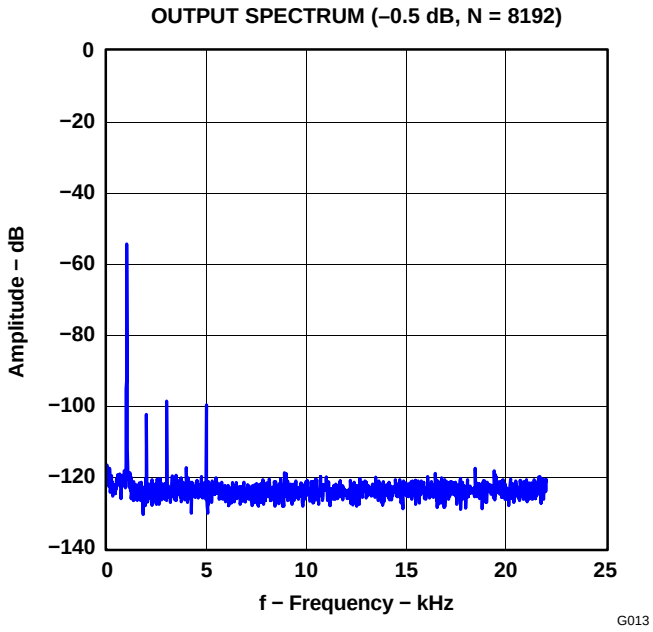


Figure 13.

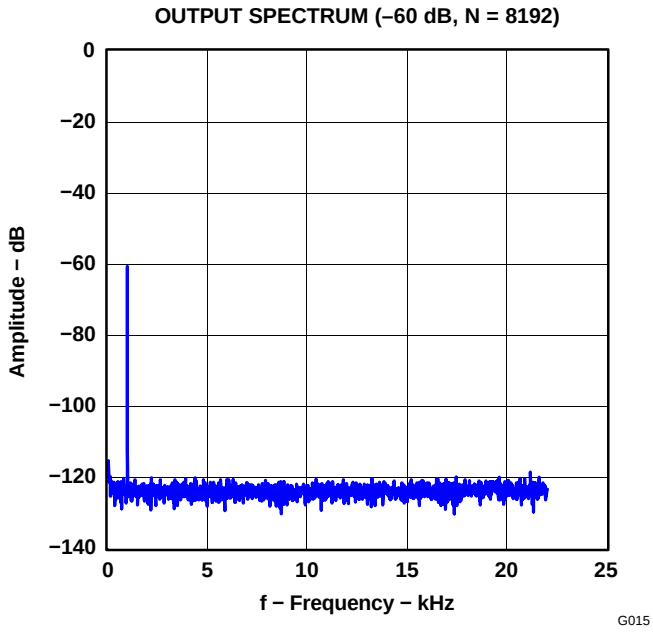


Figure 14.

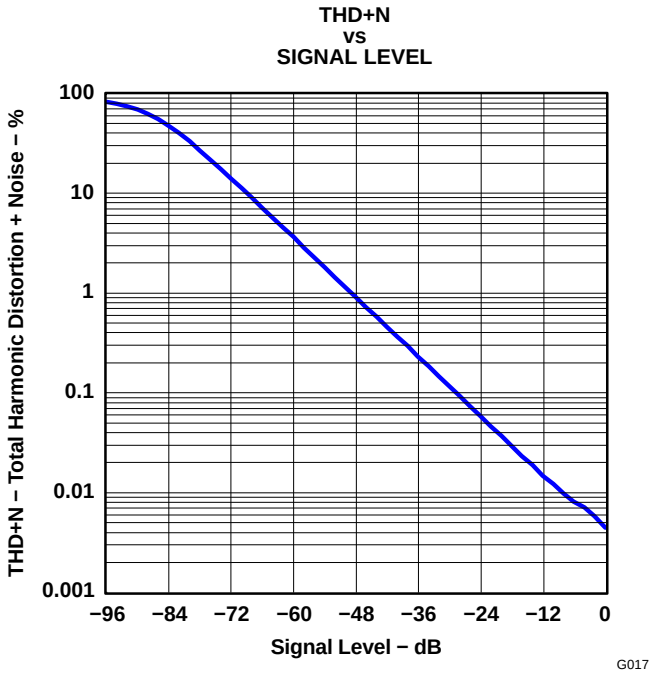


Figure 15.

TYPICAL PERFORMANCE CURVES (continued)

All specifications at T_A = 25°C, V_{CC} = V_{DD} = 3 V, f_S = 44.1 kHz, f_{SYSCLK} = 384 f_S, and f_{SIGNAL} = 1 kHz, unless otherwise noted

DACs

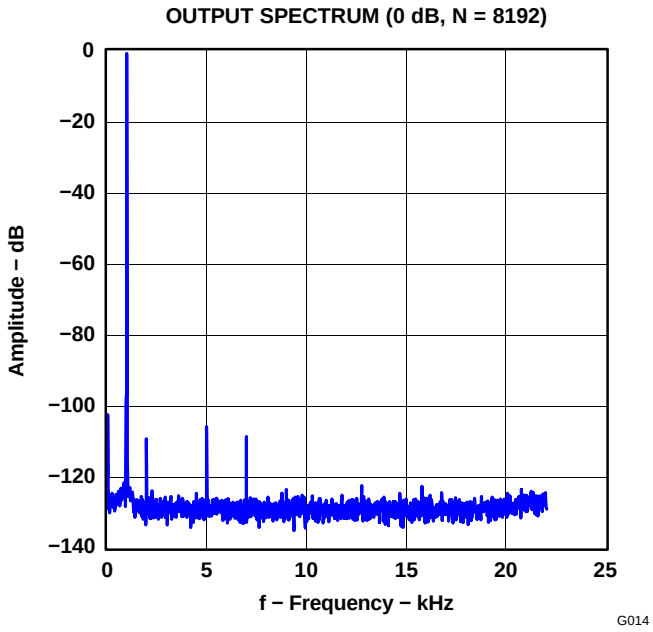


Figure 16.

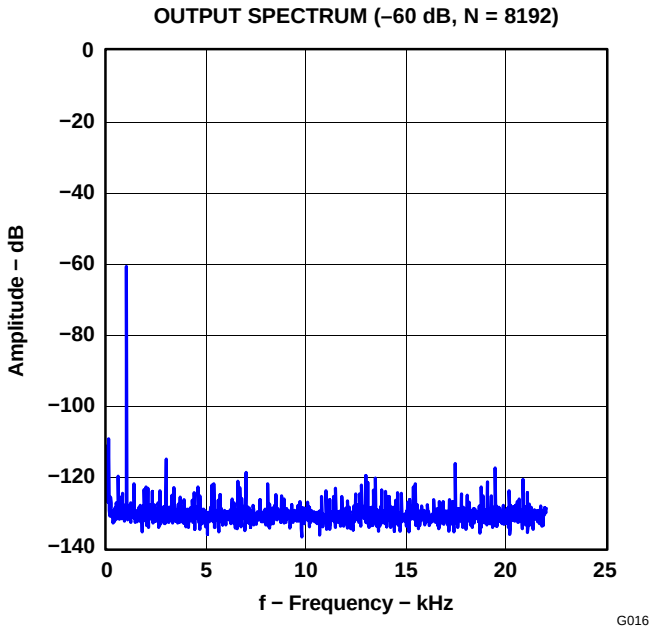


Figure 17.

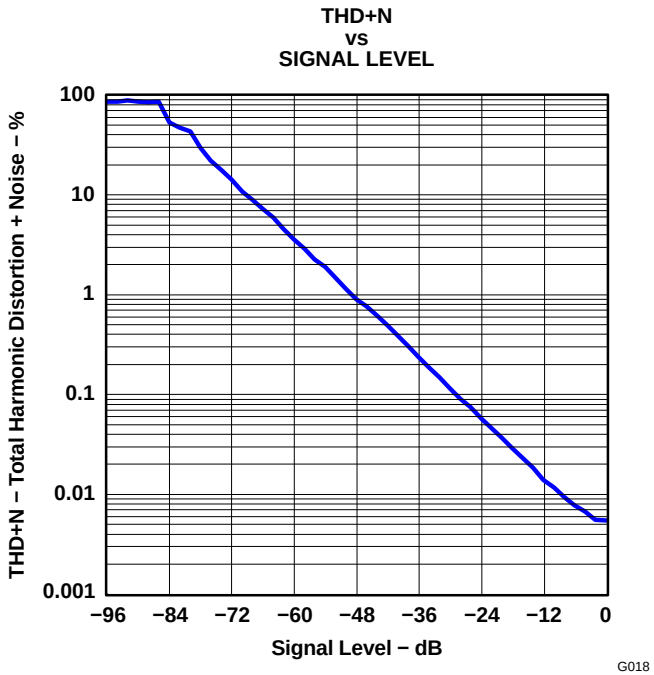


Figure 18.

TYPICAL PERFORMANCE CURVES

All specifications at T_A = 25°C, V_{CC} = V_{DD} = 3 V, f_S = 44.1 kHz, f_{SYSCLK} = 384 f_S, DIN = BPZ, and V_{IN} = BPZ, unless otherwise noted

SUPPLY CURRENT

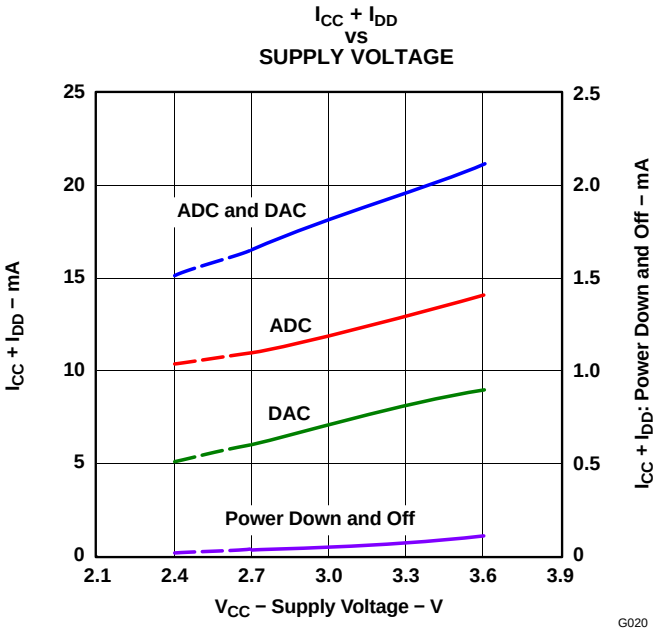


Figure 19.

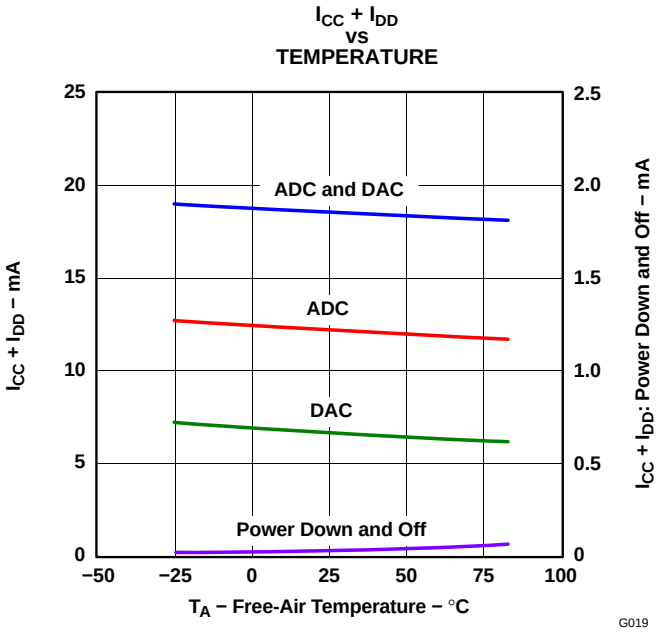


Figure 20.

All characteristics at supply voltages from 2.4 V to 2.7 V are measured at SYSCLK = 256 f_S.

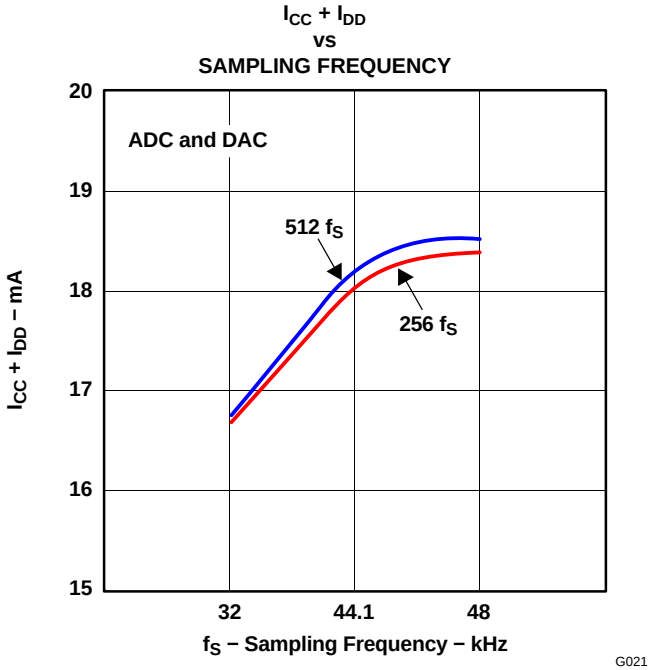


Figure 21.

TYPICAL PERFORMANCE CURVES OF INTERNAL FILTERS (ADCs)

All specifications at T_A = 25°C, V_{CC} = V_{DD} = 3 V, f_S = 44.1 kHz, and f_{SYSCLK} = 384 f_S, unless otherwise noted

DECIMATION FILTER

OVERALL CHARACTERISTICS

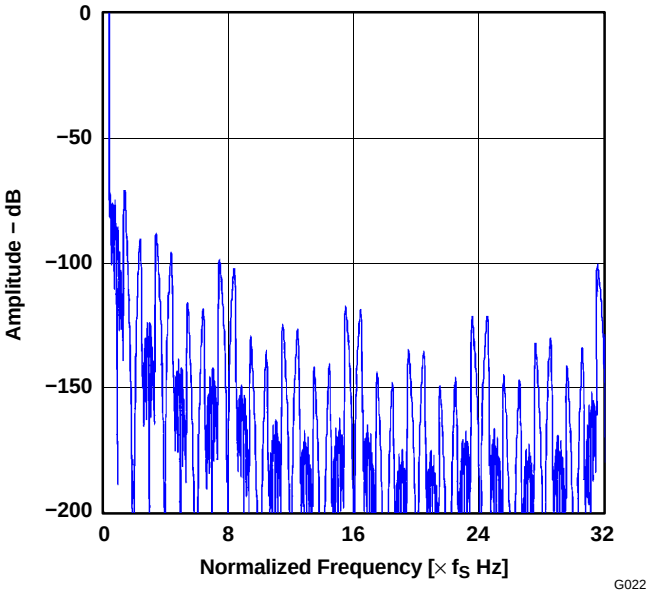


Figure 22.

STOP-BAND ATTENUATION CHARACTERISTICS

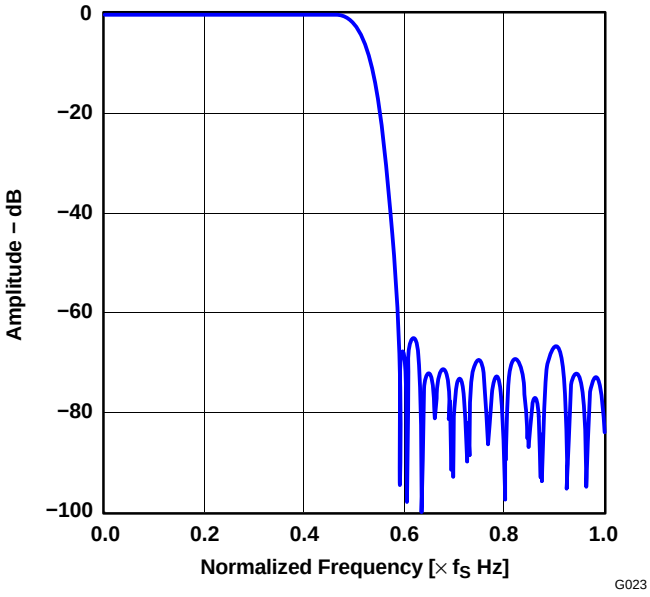


Figure 23.

PASS-BAND RIPPLE CHARACTERISTICS

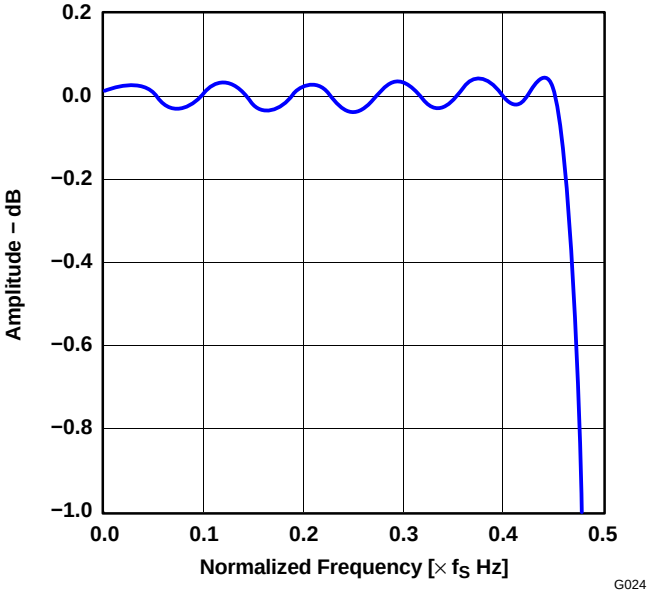


Figure 24.

TRANSITION BAND CHARACTERISTICS

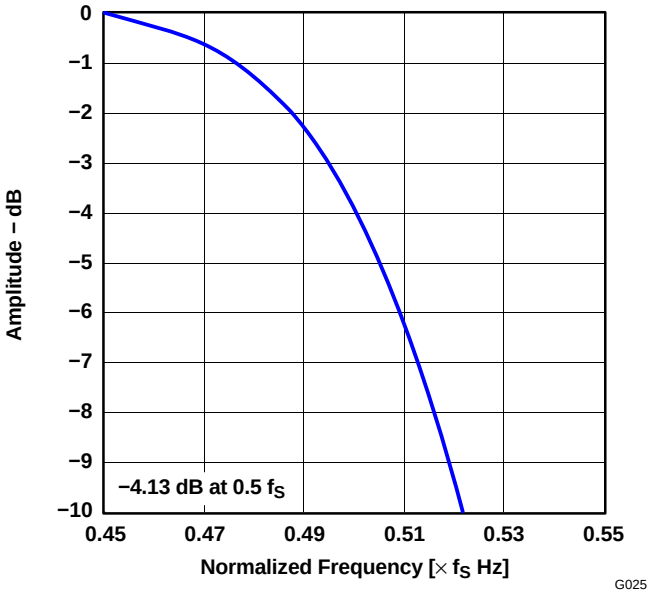


Figure 25.

TYPICAL PERFORMANCE CURVES OF INTERNAL FILTERS (ADCs) (continued)

All specifications at T_A = 25°C, V_{CC} = V_{DD} = 3 V, f_S = 44.1 kHz, and f_{SYSCLK} = 384 f_S, unless otherwise noted

HIGH-PASS FILTER

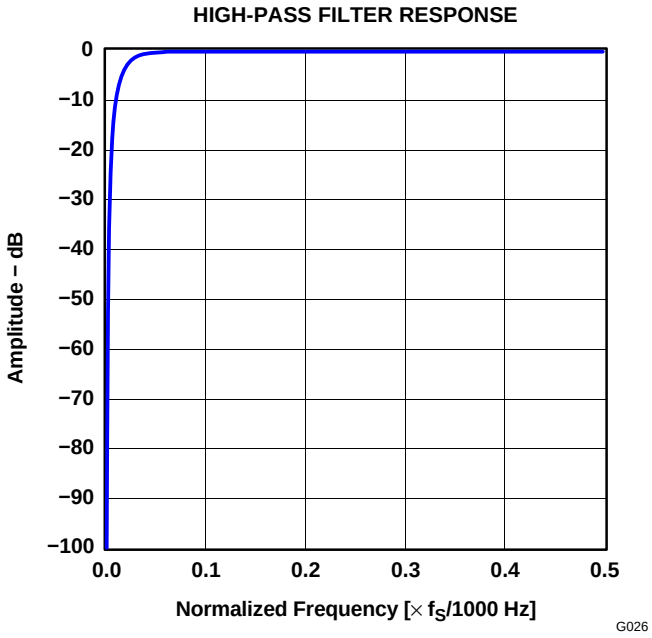


Figure 26.

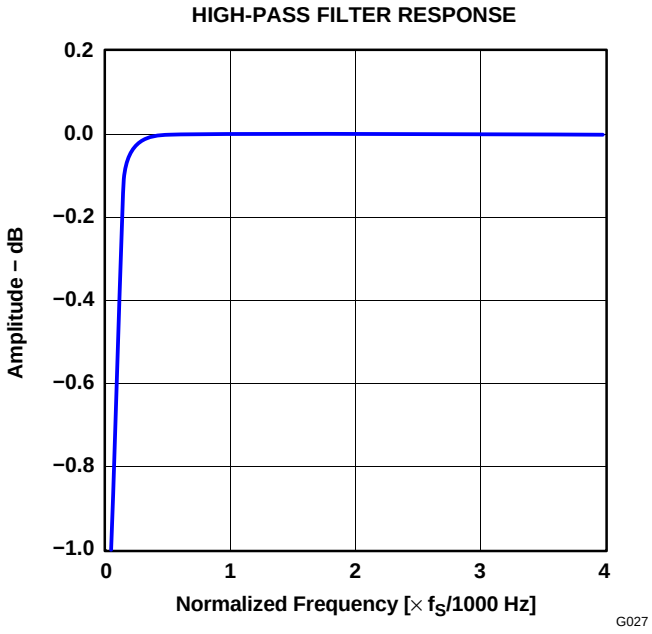


Figure 27.

ANTIALIASING FILTER

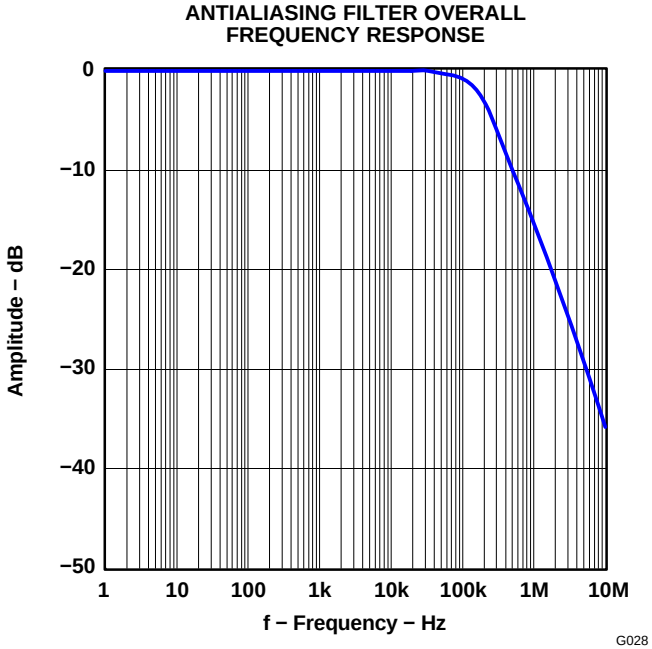


Figure 28.

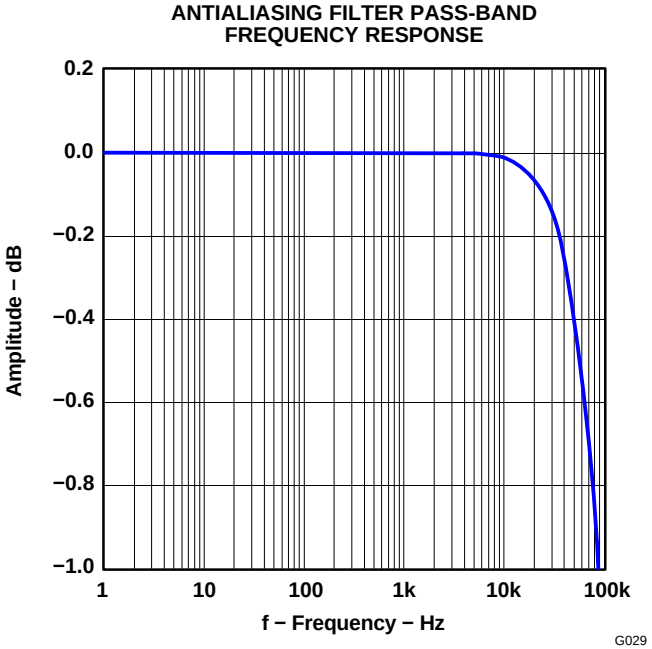


Figure 29.

TYPICAL PERFORMANCE CURVES OF INTERNAL FILTERS (DACs)

All specifications at T_A = 25°C, V_{CC} = V_{DD} = 3 V, f_S = 44.1 kHz, and f_{SYSCLK} = 384 f_S, unless otherwise noted

DIGITAL FILTER

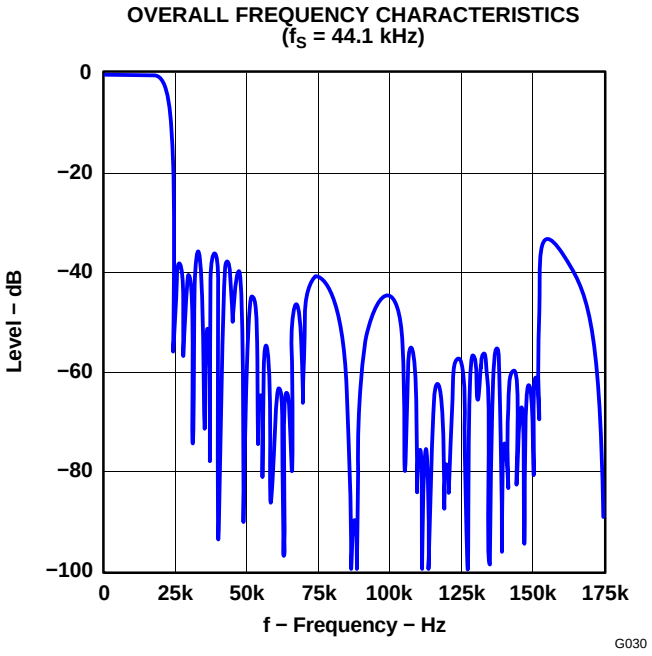


Figure 30.

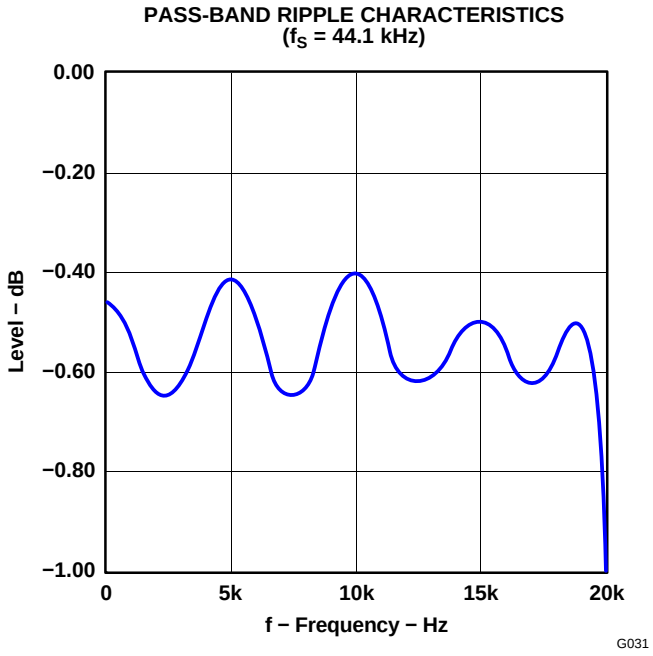


Figure 31.

DE-EMPHASIS FILTER

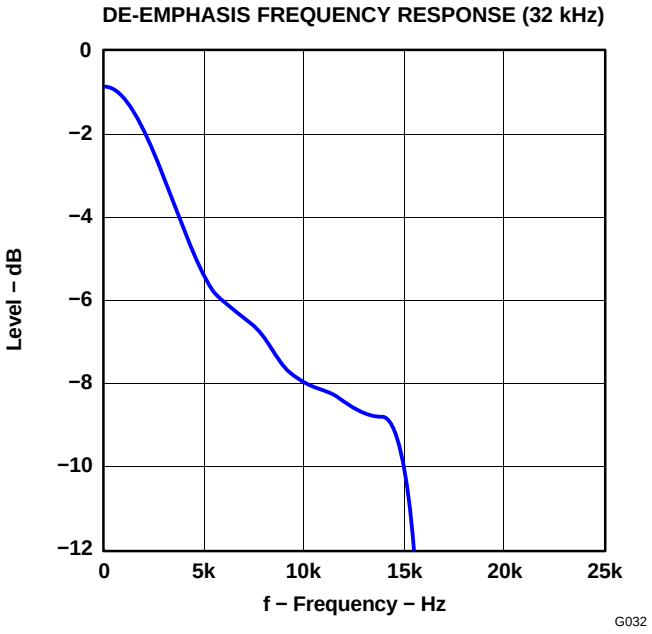


Figure 32.

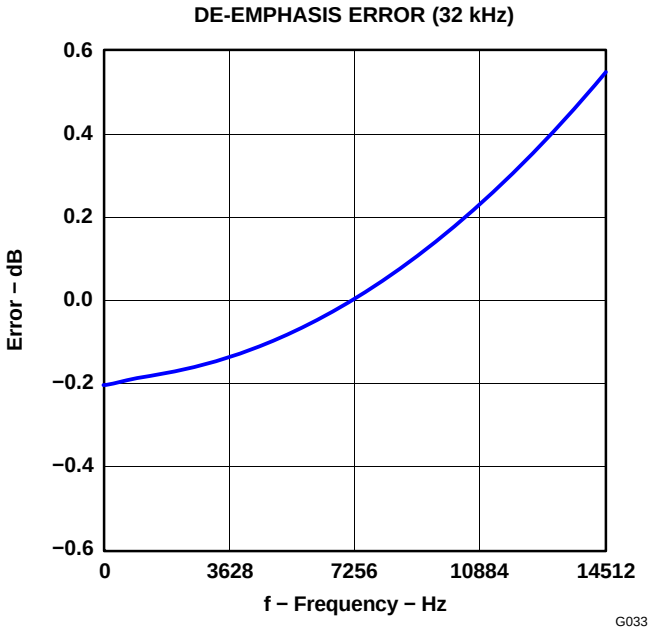


Figure 33.

TYPICAL PERFORMANCE CURVES OF INTERNAL FILTERS (DACs) (continued)

All specifications at T_A = 25°C, V_{CC} = V_{DD} = 3 V, f_S = 44.1 kHz, and f_{SYSCLK} = 384 f_S, unless otherwise noted

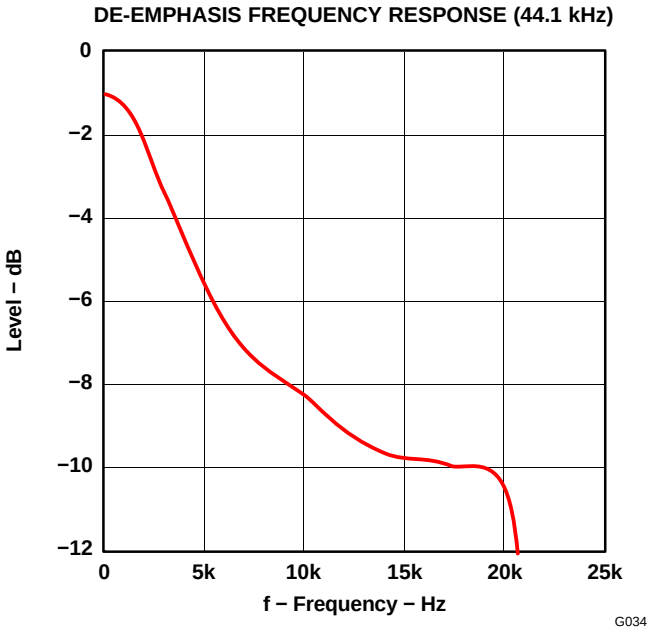


Figure 34.

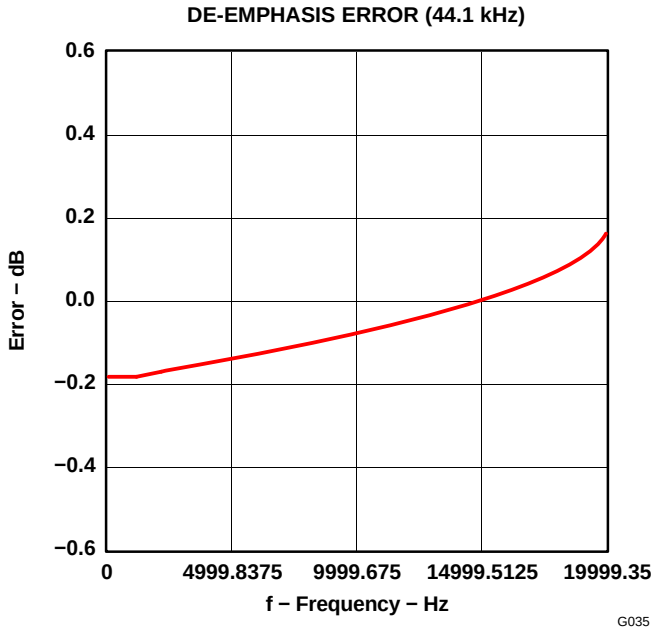


Figure 35.

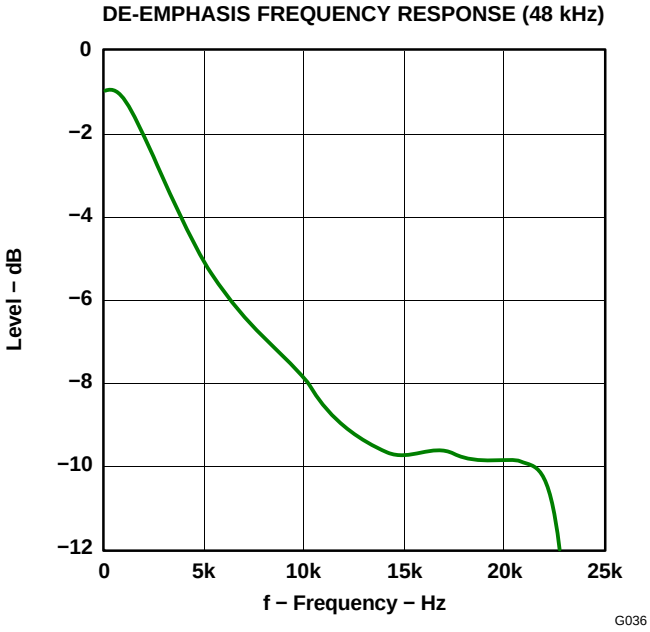


Figure 36.

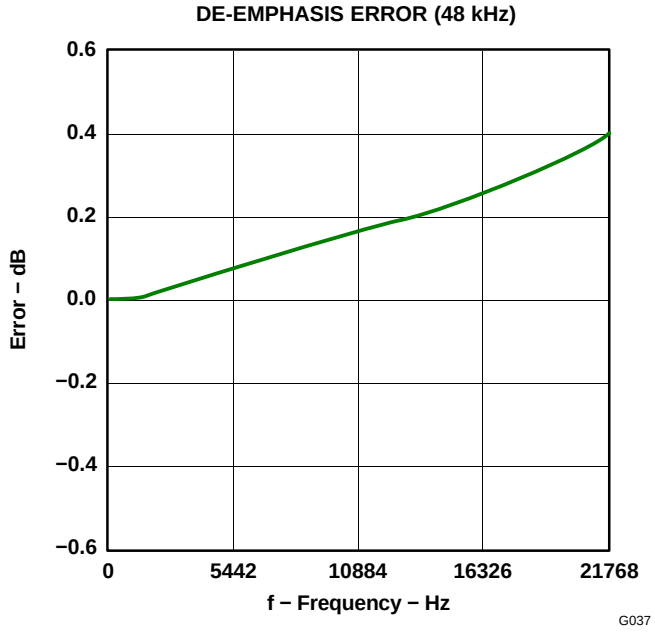


Figure 37.

TYPICAL PERFORMANCE CURVES OF INTERNAL FILTERS (DACs) (continued)

All specifications at T_A = 25°C, V_{CC} = V_{DD} = 3 V, f_S = 44.1 kHz, and f_{SYSCLK} = 384 f_S, unless otherwise noted

ANALOG LOW-PASS FILTER

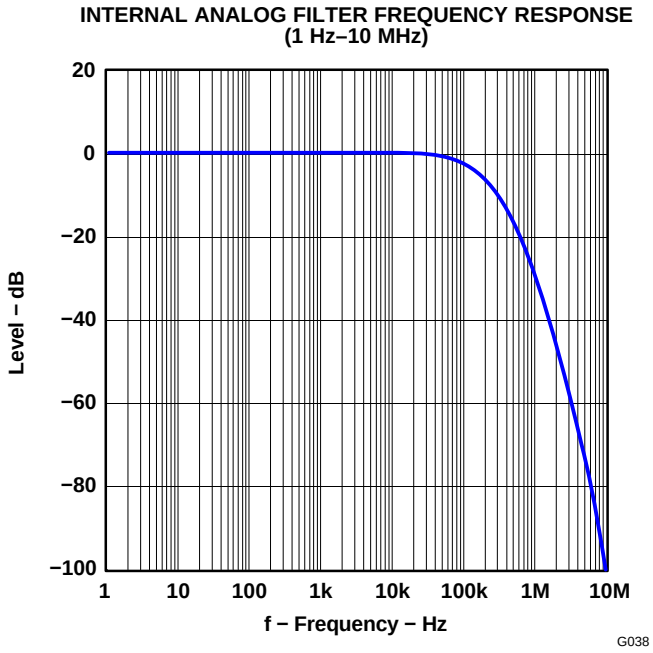


Figure 38.

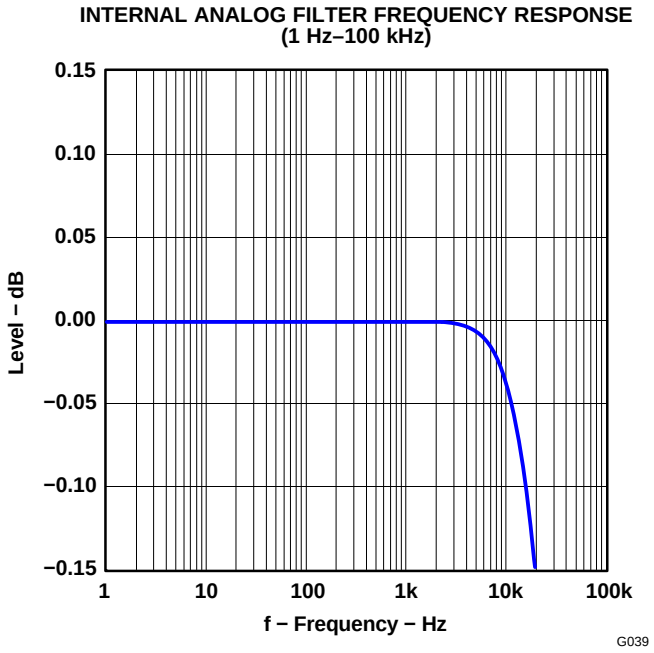
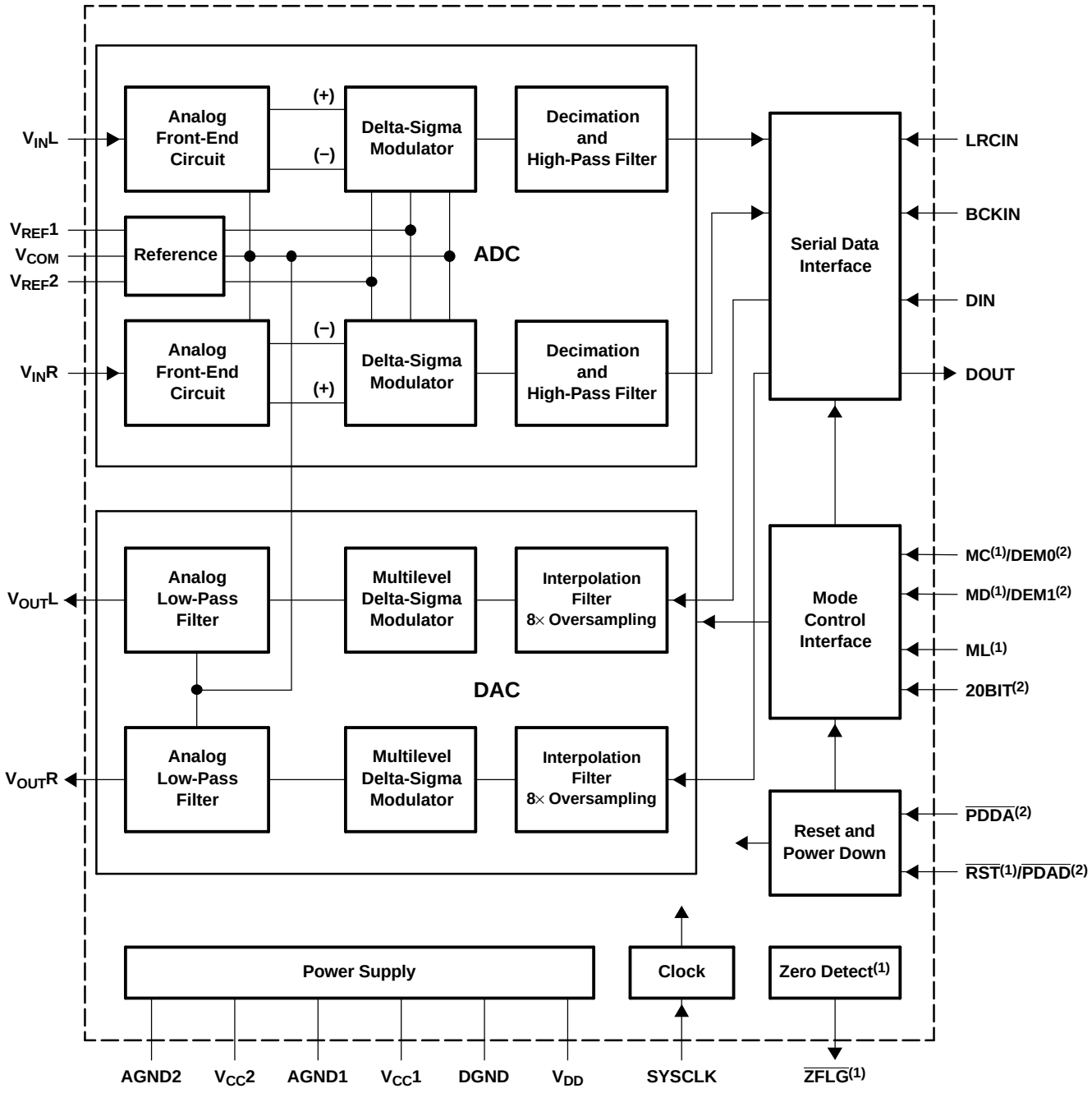


Figure 39.

BLOCK DIAGRAM



B0004-03

(1) MC, MD, ML, $\overline{\text{RST}}$, and $\overline{\text{ZFLG}}$ are for PCM3002 only.

(2) DEM0, DEM1, 20BIT, $\overline{\text{PDAD}}$, and $\overline{\text{PDDA}}$ are for PCM3003 only.

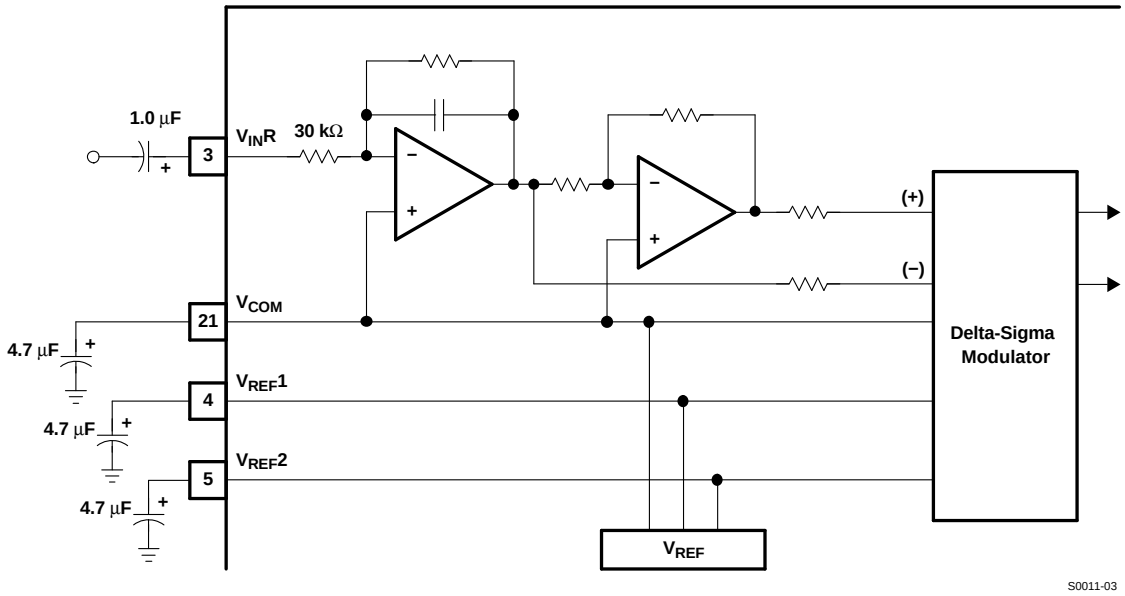


Figure 40. Analog Front-End (Single-Channel)

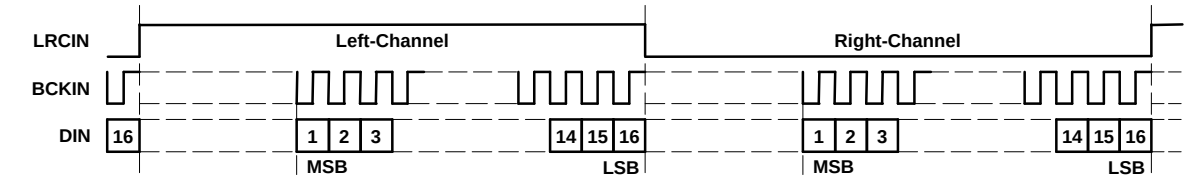
PCM AUDIO INTERFACE

The four-wire digital audio interface for the PCM3002/3003 comprises LRCIN (pin 10), BCKIN (pin 11), DIN (pin 15), and DOUT (pin 12). The PCM3002 can be used with any of the four input/output data formats (formats 0–3), while the PCM3003 can only be used with selected input/output formats (formats 0–1). For the PCM3002, these formats are selected through program register 3 in the software mode. For the PCM3003, data formats are selected by the 20BIT input (pin 16). Figure 41, Figure 42, and Figure 43 illustrate audio data input/output formats and timing.

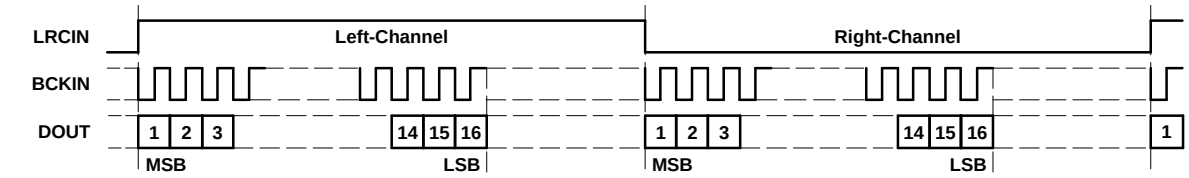
The PCM3002/3003 can accept 32, 48, or 64 bit clocks (BCKIN) in one clock of LRCIN. Only the 16-bit data format can be selected when 32-bit clocks/LRCIN are applied.

FORMAT 0: PCM3002/3003

DAC: 16-Bit, MSB-First, Right-Justified

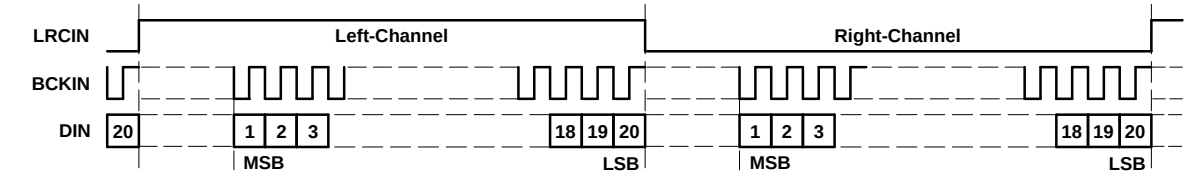


ADC: 16-Bit, MSB-First, Left-Justified

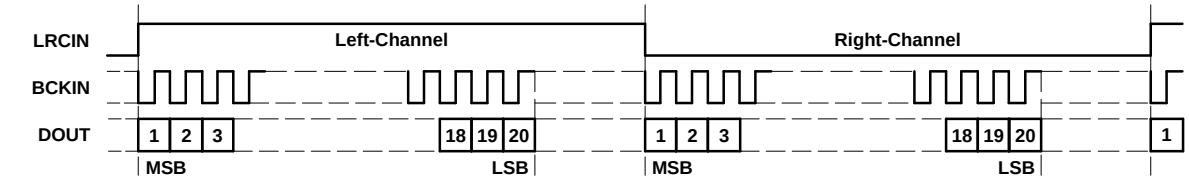


FORMAT 1: PCM3002/3003

DAC: 20-Bit, MSB-First, Right-Justified



ADC: 20-Bit, MSB-First, Left-Justified

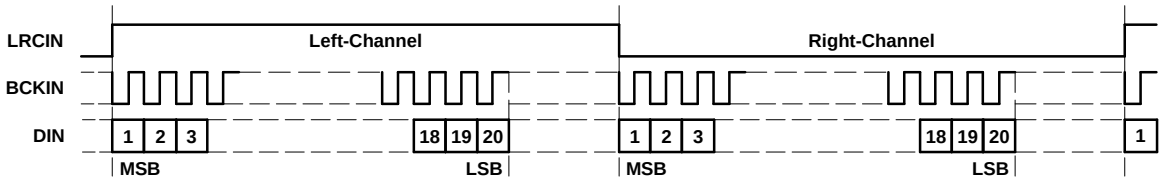


T0016-04

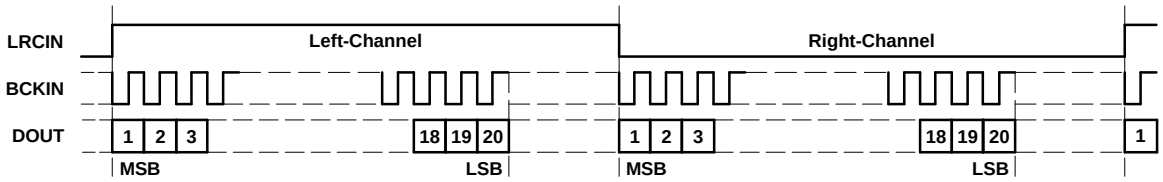
Figure 41. Audio Data Input/Output Format

FORMAT 2: PCM3002 Only

DAC: 20-Bit, MSB-First, Left-Justified

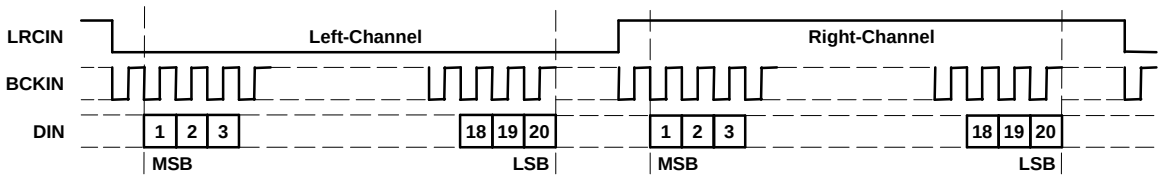


ADC: 20-Bit, MSB-First, Left-Justified

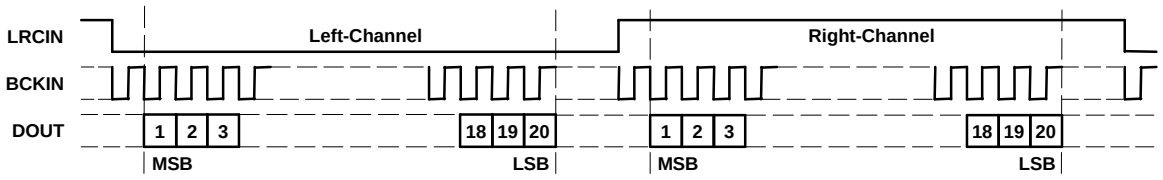


FORMAT 3: PCM3002 Only

DAC: 20-Bit, MSB-First, I^2S

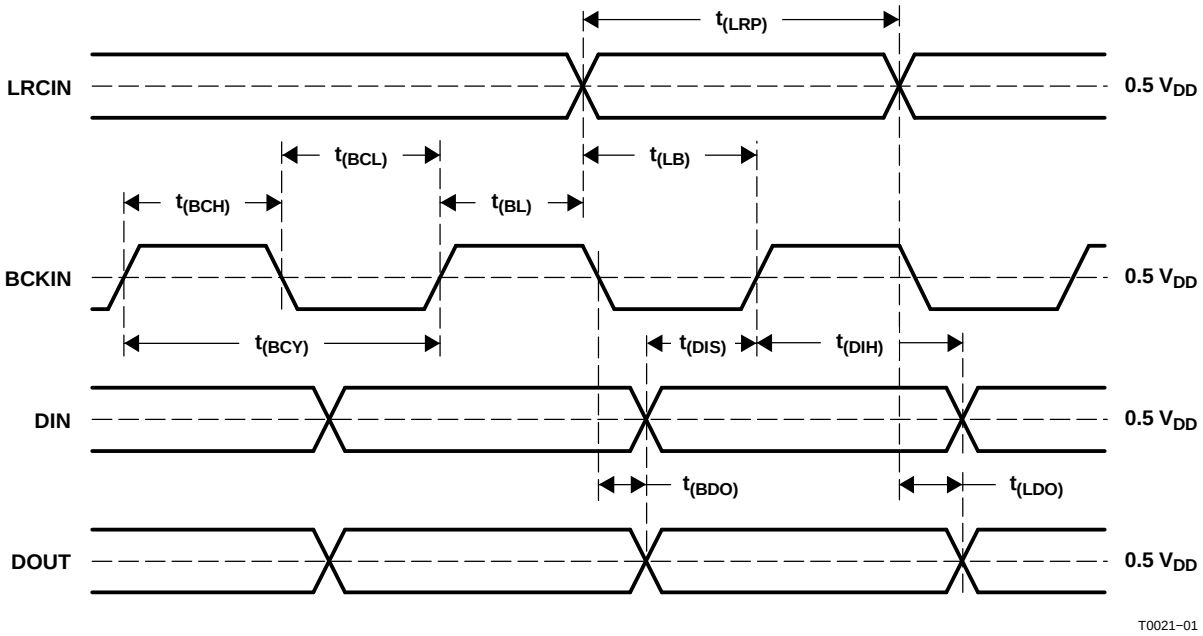


ADC: 20-Bit, MSB-First, I^2S



T0016-05

Figure 42. Audio Data Input/Output Format (PCM3002)



BCKIN pulse cycle time	$t_{(BCY)}$	300 ns (min)
BCKIN pulse duration, HIGH	$t_{(BCH)}$	120 ns (min)
BCKIN pulse duration, LOW	$t_{(BCL)}$	120 ns (min)
BCKIN rising edge to LRCIN edge	$t_{(BL)}$	40 ns (min)
LRCIN edge to BCKIN rising edge	$t_{(LB)}$	40 ns (min)
LRCIN pulse duration	$t_{(LRP)}$	$t_{(BCY)}$ (min)
DIN setup time	$t_{(DIS)}$	40 ns (min)
DIN hold time	$t_{(DIH)}$	40 ns (min)
DOUT delay time to BCKIN falling edge	$t_{(BDO)}$	40 ns (max)
DOUT delay time to LRCIN edge	$t_{(LDO)}$	40 ns (max)
Rising time of all signals	$t_{(RISE)}$	20 ns (max)
Falling time of all signals	$t_{(FALL)}$	20 ns (max)

Figure 43. Audio Data Input/Output Timing

SYSTEM CLOCK

The system clock for the PCM3002/3003 must be either 256 f_S, 384 f_S, or 512 f_S, where f_S is the audio sampling frequency. The system clock should be provided at the SYSCLK input (pin 9).

The PCM3002/3003 also has a system-clock detection circuit that automatically senses if the system clock is operating at 256 f_S, 384 f_S, or 512 f_S. When a 384-f_S or 512-f_S system clock is used, the clock is divided to 256 f_S automatically. The 256-f_S clock is used to operate the digital filters and the delta-sigma modulators.

Table 1 lists the relationship of typical sampling frequencies and system clock frequencies; Figure 44 illustrates the system clock timing.

Table 1. System Clock Frequencies

SAMPLING RATE FREQUENCY (kHz)	SYSTEM CLOCK FREQUENCY (MHz)		
	256 f_s	**384 f_s**	**512 f_s**
32	8.1920	12.2880	16.3840
44.1	11.2896	16.9344	22.5792
48	12.2880	18.4320	24.5760

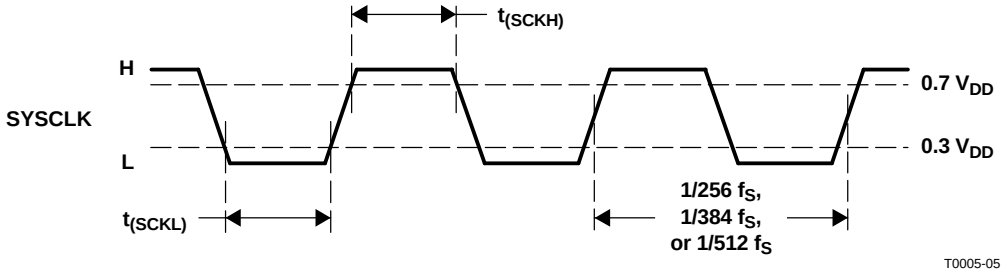


Figure 44. System Clock Timing

System clock pulse duration, HIGH	$t_{(SCKH)}$	12 ns (min)
System clock pulse duration, LOW	$t_{(SCKL)}$	12 ns (min)

POWER-ON RESET

Both the PCM3002 and PCM3003 have internal power-on reset circuitry. Power-on reset occurs when the system clock (SYSCLK) is active and V_{DD} > 2.2 V. For the PCM3003, the SYSCLK must complete a minimum of three complete cycles prior to V_{DD} > 2.2 V to ensure proper reset operation. The initialization sequence requires 1024 SYSCLK cycles for completion, as shown in Figure 45. Figure 46 shows the state of the DAC and ADC outputs during and after the reset sequence.

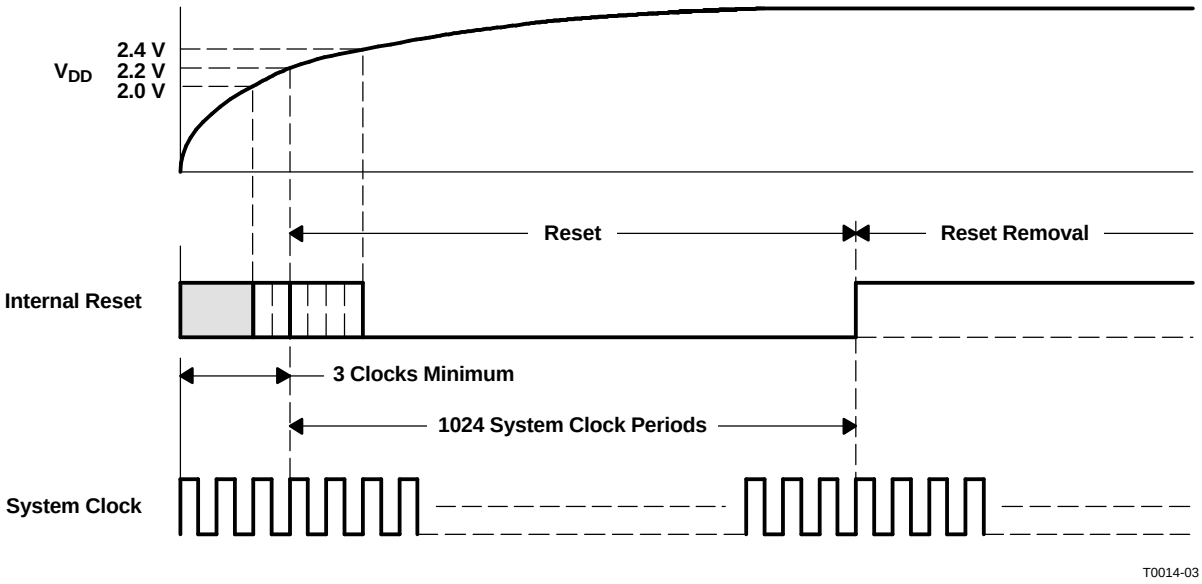
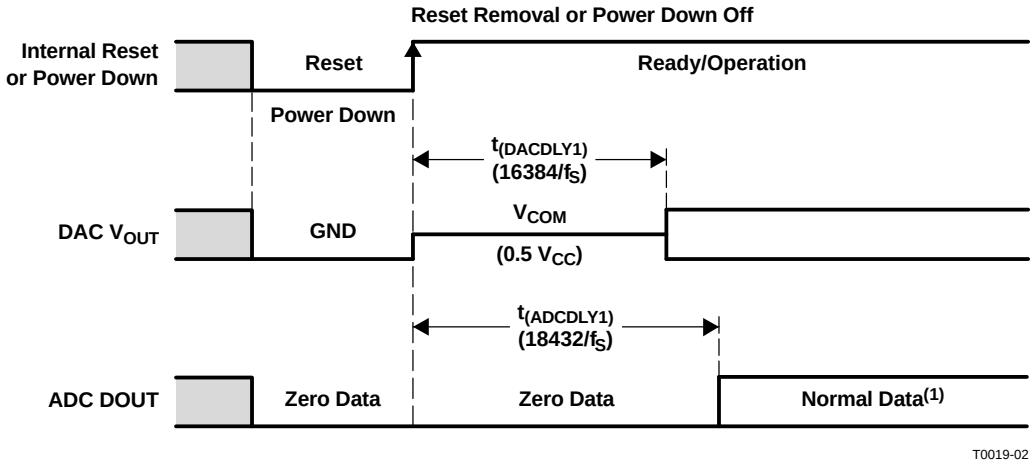


Figure 45. Internal Power-On Reset Timing



(1) The HPF transient response (exponentially attenuated signal from ±0.2% dc of FSR with 200-ms time constant) appears initially.

Figure 46. DAC Output and ADC Output for Reset and Power Down

EXTERNAL RESET

The PCM3002 includes a reset input, $\overline{RST}$ (pin 7), while the PCM3003 uses both $\overline{PDAD}$ (pin 7) and $\overline{PDDA}$ (pin 8) for external reset control. As shown in Figure 47, the external reset signal must drive $\overline{RST}$ or $\overline{PDAD}$ and $\overline{PDDA}$ low for a minimum of 40 nanoseconds while SYSCLK is active in order to initiate the reset sequence. Initialization starts on the rising edge of $\overline{RST}$ or $\overline{PDAD}$ and $\overline{PDDA}$, and requires 1024 SYSCLK cycles for completion. Figure 46 shows the state of the DAC and ADC outputs during and after the reset sequence.

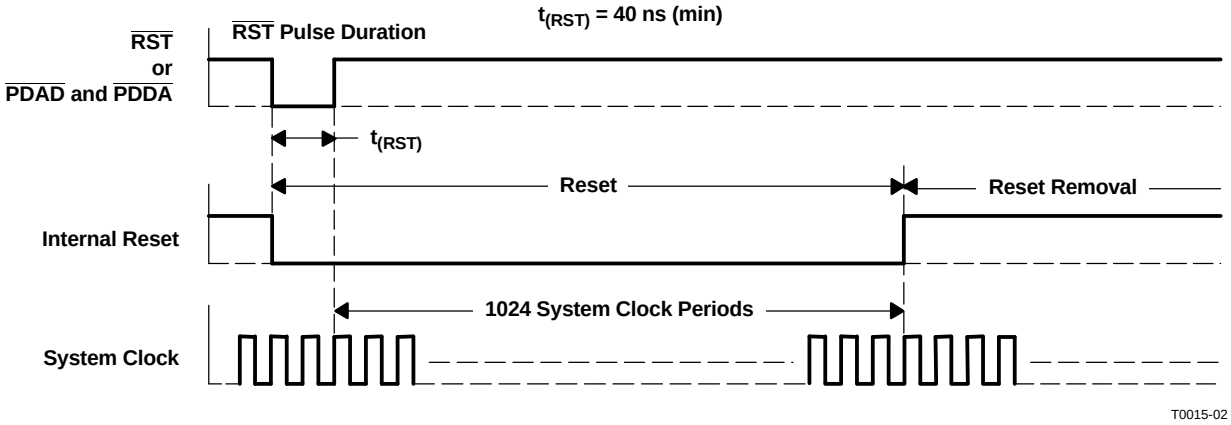
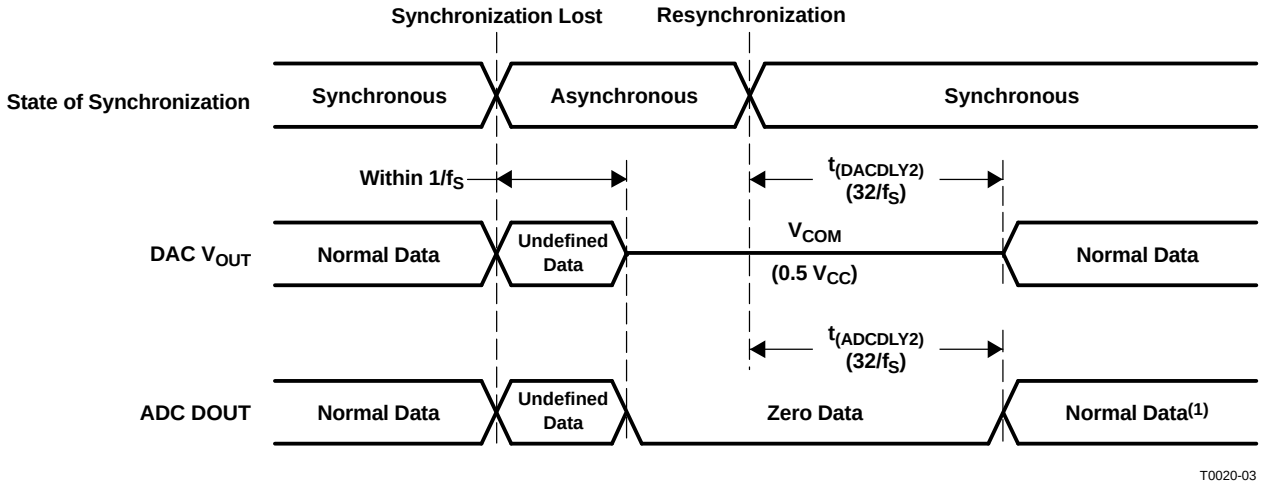


Figure 47. External Forced-Reset Timing

SYNCHRONIZATION WITH THE DIGITAL AUDIO SYSTEM

The PCM3002/3003 operates with LRCIN synchronized to the system clock. The PCM3002/3003 does not require any specific phase relationship between LRCIN and the system clock, but there must be synchronization of LRCIN and the system clock. If the synchronization between the system clock and LRCIN changes more than 6 bit clocks (BCKIN) during one sample (LRCIN) period because of phase jitter on LRCIN, internal operation of the DAC stops within $1/f_S$, and the analog output is forced to bipolar zero (0.5 V_{CC}) until the system clock is resynchronized to LRCIN followed by $t_{(DACDLY2)}$ delay time. Internal operation of the ADC also stops within $1/f_S$, and the digital output codes are set to bipolar zero until resynchronization occurs followed by $t_{(ADCDLY2)}$ delay time. If LRCIN is synchronized within 5 or fewer bit clocks to the system clock, operation is normal. Figure 48 illustrates the effects on the output when synchronization is lost. Before the outputs are forced to bipolar zero ($<1/f_S$ seconds), the outputs are not defined and some noise may occur. During the transitions between normal data and undefined states, the output has discontinuities, which cause output noise.



(1) The HPF transient response (exponentially attenuated signal from ±0.2% dc of FSR with 200-ms time constant) appears initially.

Figure 48. DAC Output and ADC Output for Loss of Synchronization

ZERO FLAG OUTPUT: PCM3002 ONLY

Pin 16 is an open-drain output, used as the infinite zero detection flag on the PCM3002 only. When input data is continuously zero for 65,536 BCKIN cycles, $\overline{\text{ZFLG}}$ is LOW; otherwise, $\overline{\text{ZFLG}}$ is in a high-impedance state.

OPERATIONAL CONTROL

The PCM3002 can be controlled in a software mode with a three-wire serial interface on MC (pin 18), MD (pin 17), and ML (pin 8). Table 2 indicates selectable functions, and Figure 49 and Figure 50 illustrate the control data input format and timing. The PCM3003 only allows for control of 16/20-bit data format, digital de-emphasis, and power-down control by hardware pins.

Table 2. Selectable Functions (O = User Selectable; X = Not Available)

FUNCTION	ADC/DAC	PCM3002	PCM3003
Audio data format	ADC/DAC	Four selectable formats	Two selectable formats
LRCIN polarity	ADC/DAC	O	X
Loopback control	ADC/DAC	O	X
Left-channel attenuation	DAC	O	X
Right-channel attenuation	DAC	O	X
Attenuation control	DAC	O	X
Infinite zero detection and mute	DAC	O	X
DAC output control	DAC	O	X
Soft mute control	DAC	O	X
De-emphasis (OFF, 32 kHz, 44.1 kHz, 48 kHz)	DAC	O	O
ADC power-down control	ADC	O	O
DAC power-down control	DAC	O	O
High-pass filter operation	ADC	O	X

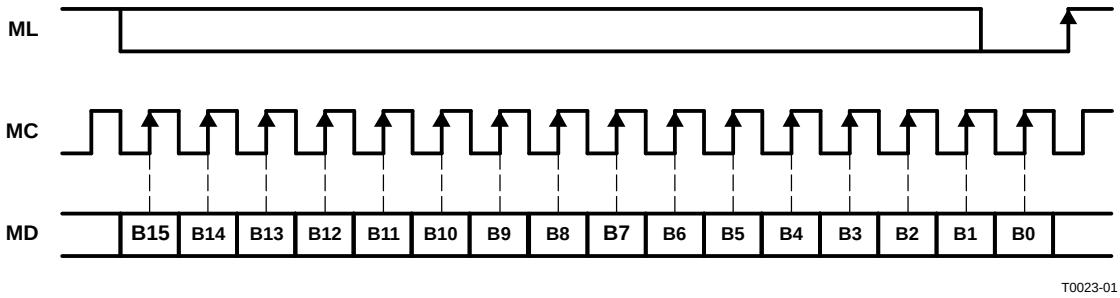
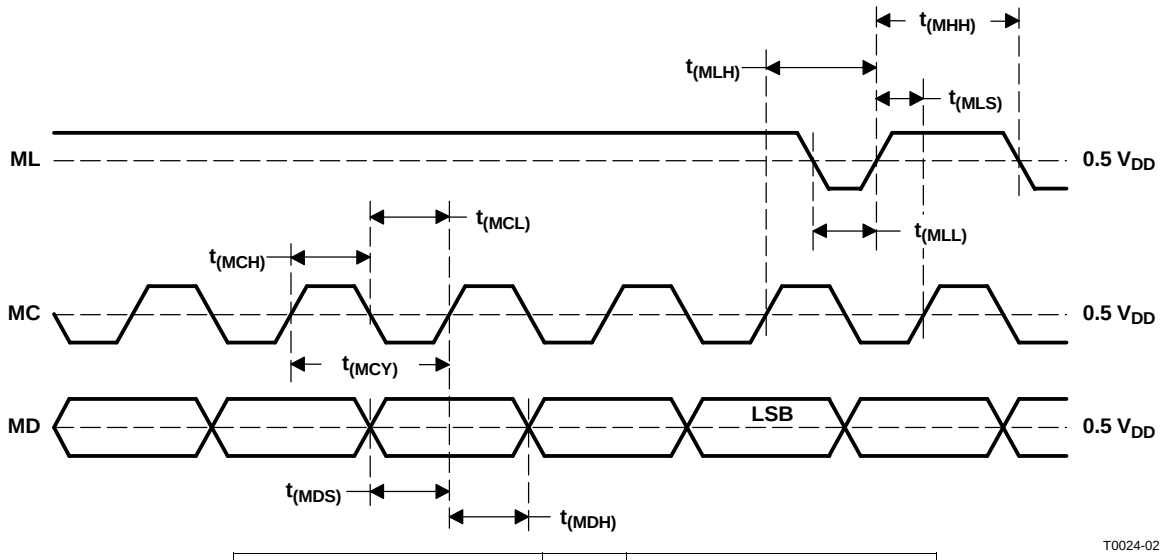


Figure 49. Control Data Input Format



MC pulse cycle time	$t_{(MCY)}$	100 ns (min)
MC pulse duration, LOW	$t_{(MCL)}$	40 ns (min)
MC pulse duration, HIGH	$t_{(MCH)}$	40 ns (min)
MD setup time	$t_{(MDS)}$	40 ns (min)
MD hold time	$t_{(MDH)}$	40 ns (min)
ML low-level time	$t_{(MLL)}$	40 ns + 1 SYSCLK(1) (min)
ML high-level time	$t_{(MHH)}$	40 ns + 1 SYSCLK(1) (min)
ML setup time(3)	$t_{(MLS)}$	40 ns (min)
ML hold time(2)	$t_{(MLH)}$	40 ns (min)
SYSCLK: 1/256 f_S or 1/384 f_S or 1/512 f_S		

(1) SYSCLK: System clock cycle

(2) MC rising edge of LSB to ML rising edge

(3) ML rising edge to the next MC rising edge

Figure 50. Control Data Input Timing

MAPPING OF PROGRAM REGISTERS

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 0	res	res	res	res	res	A1	A0	LDL	AL7	AL6	AL5	AL4	AL3	AL2	AL1	AL0
REGISTER 1	res	res	res	res	res	A1	A0	LDR	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0
REGISTER 2	res	res	res	res	res	A1	A0	PDAD	BYPS	PDDA	ATC	IZD	OUT	DEM1	DEM0	MUT
REGISTER 3	res	res	res	res	res	A1	A0	res	res	res	LOP	res	FMT1	FMT0	LRP	res

NOTE: res indicates a reserved bit that should be set to 0.

SOFTWARE CONTROL (PCM3002)

The PCM3002 special functions are controlled using four program registers which are each 16 bits long. There are four distinct registers, with bits 9 and 10 determining which register is in use. Table 3 describes the functions of the four registers.

Table 3. Functions of the Registers

REGISTER NAME	REGISTER BIT(S)	BIT NAME	DESCRIPTION
Register 0	15–11	res	Reserved, should be set to 0
	10–9	A[1:0]	Register address 00
	8	LDL	DAC attenuation data load control for Lch
	7–0	AL[7:0]	DAC attenuation data for Lch
Register 1	15–11	res	Reserved, should be set to 0
	10–9	A[1:0]	Register address 01
	8	LDR	DAC attenuation data load control for Rch
	7–0	AR[7:0]	DAC attenuation data for Rch
Register 2	15–11	res	Reserved, should be set to 0
	10–9	A[1:0]	Register address 10
	8	PDAD	ADC power-down control
	7	BYPS	ADC high-pass filter bypass control
	6	PDDA	DAC power-down control
	5	ATC	DAC attenuation data mode control
	4	IZD	DAC infinite zero detection and mute control
	3	OUT	DAC output enable control
	2–1	DEM[1:0]	DAC de-emphasis control
	0	MUT	DAC Lch and Rch soft mute control
Register 3	15–11	res	Reserved, should be set to 0
	10–9	A[1:0]	Register address 11
	8–6	res	Reserved, should be set to 0
	5	LOP	ADC/DAC digital loopback control
	4	res	Reserved, should be set to 0
	3–2	FMT[1:0]	ADC/DAC audio data format selection
	1	LRP	ADC/DAC polarity of LR-clock selection
	0	res	Reserved, should be set to 0

PROGRAM REGISTER 0

res: Bits 15–11: Reserved

These bits are reserved and should be set to 0.

A[1:0] Bits 10, 9: Register address

These bits define the address for register 0:

A1	A0	REGISTER
0	0	Register 0

LDL Bit 8: DAC attenuation data load control for left channel

This bit is used to set analog outputs of the left and right channels simultaneously. The output level is controlled by AL[7:0] attenuation data when this bit is set to 1. When set to 0, the new attenuation data is ignored, and the output level remains at the previous attenuation level. The LDR bit in register 1 has the equivalent function as LDL. When either LDL or LDR is set to 1, the output levels of the left and right channels are controlled simultaneously.

AL (7:0) Bits 7–0: DAC attenuation data for left channel

AL7 and AL0 are the MSB and LSB, respectively. The attenuation level (ATT) is given by:

ATT = $20 \times \log_{10}$ (AL[7:0]/256) [dB], except AL[7:0] = FFh

AL[7:0]	ATTENUATION LEVEL
00h	–∞dB (mute)
01h	–48.16 dB
:	:
FEh	–0.07 dB
FFh	0 dB (default)

PROGRAM REGISTER 1

res: Bits 15–11: Reserved

These bits are reserved and should be set to 0.

A[1:0] Bits 10, 9: Register address

These bits define the address for register 1:

A1	A0	REGISTER
0	1	Register 1

LDR Bit 8: DAC attenuation data load control for right channel

This bit is used to set analog outputs of the left and right channels simultaneously. The output level is controlled by AR[7:0] attenuation data when this bit is set to 1. When set to 0, the new attenuation data is ignored, and the output level remains at the previous attenuation level. The LDL bit in register 0 has the equivalent function as LDR. When either LDL or LDR is set to 1, the output levels of the left and right channels are controlled simultaneously.

AR[7:0] Bits 7–0: DAC attenuation data for right channel

AR7 and AR0 are the MSB and LSB, respectively.

ATT = $20 \times \log_{10}$ (AR[7:0]/256) [dB], except AR[7:0] = FFh

AR[7:0]	ATTENUATION LEVEL
00h	–∞dB (mute)
01h	–48.16 dB
:	:
FEh	–0.07 dB
FFh	0 dB (default)

PROGRAM REGISTER 2

res: Bits 15–11: Reserved

These bits are reserved and should be set to 0.

A[1:0] Bits 10, 9: Register address

These bits define the address for register 2:

A1	A0	REGISTER
1	0	Register 2

PDAD: Bit 8: ADC power-down control

This bit places the ADC section in the lowest power-consumption mode. The ADC operation is stopped by cutting the supply current to the ADC section, and DOUT is fixed to zero during ADC power-down mode enable. Figure 46 illustrates the ADC DOUT response for ADC power-down ON/OFF. This does not affect the DAC operation.

PDAD	DAC POWER-DOWN STATUS
0	Power-down mode disabled (default)
1	Power-down mode enabled

BYPS: Bit 7: ADC high-pass filter bypass control

This bit enables or disables the high-pass filter for the ADC.

BYPS	FILTER BYPASS STATUS
0	High-pass filter enabled (default)
1	High-pass filter disabled (bypassed)

PDDA: Bit 6: DAC power-down control

This bit places the DAC section in the lowest power-consumption mode. The DAC operation is stopped by cutting the supply current to the DAC section, and VOUT is fixed to GND during DAC power-down mode enable. Figure 46 illustrates the DAC VOUT response for DAC power-down ON/OFF. This does not affect the ADC operation.

PDDA	ADC POWER-DOWN STATUS
0	Power-down mode disabled (default)
1	Power-down mode enabled

ATC: Bit 5: DAC attenuation data mode control

When set to 1, the register 0 attenuation data can be used for both DAC channels. In this case, the register 1 attenuation data is ignored.

ATC	ATTENUATION CONTROL
0	Individual channel attenuation data control (default)
1	Common channel attenuation data control

IZD: Bit 4: DAC infinite zero detection and mute control

This bit enables the infinite zero detection circuit in the PCM3002. When enabled, this circuit disconnects the analog output amplifier from the delta-sigma DAC when the input is continuously zero for 65,536 consecutive cycles of BCKIN.

IZD	INFINITE ZERO DETECT STATUS
0	Infinite zero detection and mute control disabled (default)
1	Infinite zero detection and mute control enabled

OUT: Bit 3: DAC output enable control

When set to 1, the outputs are forced to $V_{CC}/2$ (bipolar zero). In this case, all registers in the PCM3002 hold the present data. Therefore, when set to 0, the outputs return to the previous programmed state.

OUT	DAC OUTPUT STATUS
0	DAC outputs enabled (default normal operation)
1	DAC outputs disabled (forced to BPZ)

DEM[1:0]: Bits 2, 1: DAC de-emphasis control

These bits select the de-emphasis mode as shown below:

DEM1	DEM0	DE-EMPHASIS STATUS
0	0	De-emphasis 44. 1 kHz ON
0	1	De-emphasis OFF (default)
1	0	De-emphasis 48 kHz ON
1	1	De-emphasis 32 kHz ON

MUT: Bit 0: DAC soft mute control

When set to 1, both left- and right-channel DAC outputs are muted at the same time. This muting is done by attenuating the data in the digital filter, so there is no audible click noise when soft mute is turned on.

MUT	MUTE STATUS
0	Mute disabled (default)
1	Mute enabled

PROGRAM REGISTER 3

res: Bits 15–11: Reserved

These bits are reserved and should be set to 0.

A[1:0] Bits 10, 9: Register address

These bits define the address for register 3:

A1	A0	REGISTER
1	1	Register 3

res: Bits 8–6: Reserved

These bits are reserved and should be set to 0.

LOP: Bit 5: ADC to DAC loopback control

When this bit is set to 1, the ADC audio data is sent directly to the DAC. The data format defaults to I^2S; DOUT is still available in loopback mode.

LOP	LOOPBACK STATUS
0	Loopback disabled (default)
1	Loopback enabled

res: Bit 4: Reserved

This bit is reserved and should be set to 0.

FMT[1:0] Bits 3–2: Audio data format select

These bits determine the input and output audio data formats.

FMT1	FMT0	DAC DATA FORMAT	ADC DATA FORMAT	NAME
0	0	16-bit, MSB-first, right-justified	16-bit, MSB-first, left-justified	Format 0 (default)
0	1	20-bit, MSB-first, right-justified	20-bit, MSB-first, left-justified	Format 1
1	0	20-bit, MSB-first, left-justified	20-bit, MSB-first, left-justified	Format 2
1	1	20-bit, MSB-first, I^2S	20-bit, MSB-first, I^2S	Format 3

LRP: Bit 1: ADC to DAC LRCIN polarity select

Polarity of LRCIN applies only to formats 0 through 2.

LRP	LEFT/RIGHT POLARITY
0	Left channel is H, right channel is L (default).
1	Left channel is L, right channel is H.

res: Bit 0: Reserved

This bit is reserved and should be set to 0.

PCM3003 DATA FORMAT CONTROL

The PCM3003 has hardware functional control using $\overline{\text{PDAD}}$ (pin 7) and $\overline{\text{PDDA}}$ (pin 8) for power-down control; DEM0 (pin 18) and DEM1 (pin 17) for de-emphasis; and 20BIT (pin 16) for 16/20-bit format selection.

Power-Down Control (Pin 7 and Pin 8)

Both the ADC and DAC power-down control pins place the ADC or DAC section in the lowest power-consumption mode. The ADC/DAC operation is stopped by cutting the supply current to the ADC/DAC section. DOUT is fixed to zero during ADC power-down mode enable and V_{OUT} is fixed to GND during DAC power-down mode enable. Figure 46 illustrates the ADC and DAC output response for power-down ON/OFF.

$\overline{\text{PDAD}}$	$\overline{\text{PDDA}}$	POWER DOWN
Low	Low	Reset (ADC/DAC power down enabled)
Low	High	ADC power-down/DAC operates
High	Low	ADC operates/DAC power down
High	High	ADC and DAC normal operation

De-Emphasis Control (Pin 17 and Pin 18)

DEM0 (pin 18) and DEM1 (pin 17) are used as de-emphasis control pins.

DEM1	DEMO	DE-EMPHASIS
Low	Low	De-emphasis enabled for 44.1 kHz
Low	High	De-emphasis disabled
High	Low	De-emphasis enabled for 48 kHz
High	High	De-emphasis enabled for 32 kHz

20BIT Audio Data Selection (Pin 16)

20BIT	FORMAT
Low	ADC: 16-bit MSB-first, left-justified
	DAC: 16-bit MSB-first, right-justified
High	ADC: 20-bit MSB-first, left-justified
	DAC: 20-bit MSB-first, right-justified

APPLICATION AND LAYOUT CONSIDERATIONS

POWER-SUPPLY BYPASSING

The digital and analog power supply lines to PCM3002/3003 should be bypassed to the corresponding ground pins with both 0.1-μF ceramic and 10-μF tantalum capacitors as close to the device pins as possible. Although the PCM3002/3003 has three power-supply lines to optimize dynamic performance, the use of one common power supply is generally recommended to avoid unexpected latch-up or pop noise due to power-supply sequencing problems. If separate power supplies are used, back-to-back diodes are recommended to avoid latch-up problems.

GROUNDING

In order to optimize the dynamic performance of the PCM3002/3003, the analog and digital grounds are not connected internally. The PCM3002/3003 performance is optimized with a single ground plane for all returns. It is recommended to tie all PCM3002/3003 ground pins to the analog ground plane using low-impedance connections. The PCM3002/3003 should reside entirely over this plane to avoid coupling high-frequency digital switching noise into the analog ground plane.

VOLTAGE INPUT

A tantalum or aluminum electrolytic capacitor, between 1 μF and 10 μF, is recommended as an ac-coupling capacitor at the inputs. Combined with the 30-kΩ characteristic input impedance, a 1-μF coupling capacitor establishes a 5.3-Hz cutoff frequency for blocking dc. The input voltage range can be increased by adding a series resistor on the analog input line. This series resistor, when combined with the 30-kΩ input impedance, creates a voltage divider and enables larger input ranges.

V_{REF} INPUTS

A 4.7-μF to 10-μF tantalum capacitor is recommended between $V_{REF}1$, $V_{REF}2$, and AGND1 to ensure low source impedance for the ADC references. These capacitors should be located as close as possible to the reference pins to reduce dynamic errors on the ADC reference.

V_{COM} INPUT

A 4.7-μF to 10-μF tantalum capacitor is recommended between V_{COM} and AGND1 to ensure low source impedance of the ADC and DAC common voltage. This capacitor should be located as close as possible to the V_{COM} pin to reduce dynamic errors on the dc common-mode voltage.

SYSTEM CLOCK

The quality of the system clock can influence dynamic performance of both the ADC and DAC in the PCM3002/3003. The duty cycle and jitter at the system-clock input pin should be carefully managed. When power is supplied to the part, the system clock, bit clock (BCKIN), and word clock (LCRIN) also must be supplied simultaneously. Failure to supply the audio clocks results in a power-dissipation increase of up to three times normal dissipation and can degrade long-term reliability if the maximum power-dissipation limit is exceeded.

RESET CONTROL

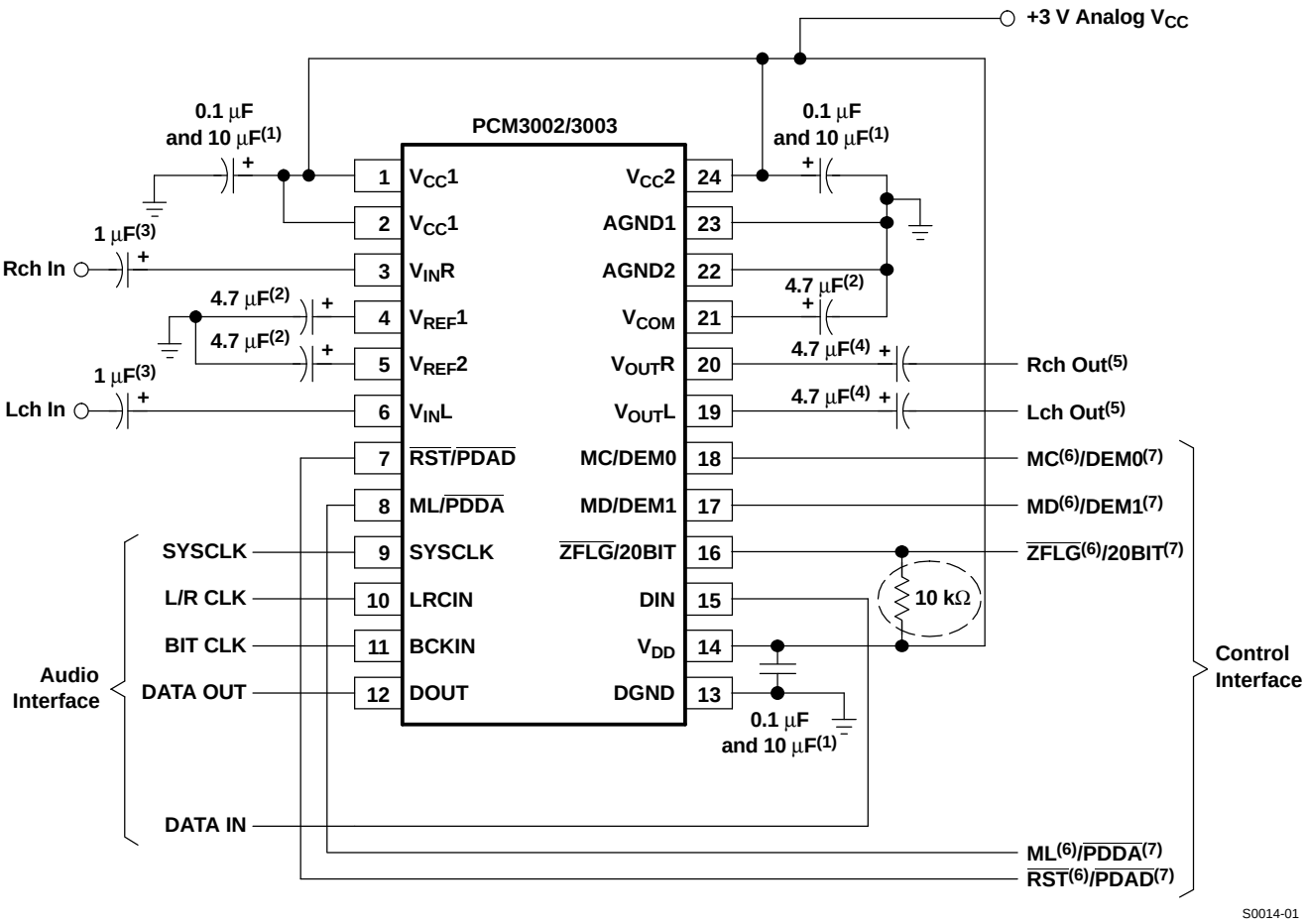
If capacitors larger than 22 μF are used on V_{REF} and V_{COM}, external reset control ($\overline{RST}$ = low for the PCM3002, $\overline{PDAD}$ = low and $\overline{PDDA}$ = low for the PCM3003) is required after the V_{REF}, V_{COM} transient response is settled.

EXTERNAL MUTE CONTROL

For power-down ON/OFF control without click noise, which is generated by a DC level change on the DAC output, use of the external mute control is recommended. The control sequence, which is external mute ON, codec power-down ON, SYSCLK stop and resume if necessary, codec power-down OFF, and external mute OFF is recommended.

TYPICAL CONNECTION DIAGRAM

A typical connection diagram for the PCM3002/3003 is shown in Figure 51.



(1) 0.1-μF ceramic and 10-μF tantalum, typical, depending on power supply quality and pattern layout

(2) 4.7-μF, typical, gives settling time with 30-ms (4.7 μF × 6.4 kΩ) time constant in the power ON and power-down OFF periods.

(3) 1-μF, typical, gives 5.3-Hz cutoff frequency for the input HPF in normal operation and gives settling time with 30-ms (1 μF × 30 kΩ) time constant in the power ON and power-down OFF periods.

(4) 4.7-μF, typical, gives 3.4-Hz cutoff frequency for the output HPF in normal operation and gives settling time with 47-ms (4.7 μF × 10 kΩ) time constant in the power ON and power-down OFF periods.

(5) Post low-pass filter with R_{IN} > 10 kΩ, depending on system performance requirements

(6) MC, MD, ML, $\overline{ZFLG}$, $\overline{RST}$, and 10-kΩ pullup resistor are for the PCM3002.

(7) DEM0, DEM1, 20BIT, $\overline{PDAD}$, $\overline{PDDA}$ are for the PCM3003.

Figure 51. Typical Connection Diagram for PCM3002/3003

THEORY OF OPERATION

ADC SECTION

The PCM3002/3003 ADC consists of two reference circuits, a stereo single-to-differential converter, a fully differential fifth-order delta-sigma modulator, a decimation filter (including digital high pass), and a serial interface circuit. The block diagram in this data sheet illustrates the architecture of the ADC section, Figure 40 shows the single-to-differential converter, and Figure 52 illustrates the architecture of the fifth-order delta-sigma modulator and transfer functions.

An internal reference circuit with three external capacitors provides all reference voltages required by the ADC, which defines the full-scale range for the converter. The internal single-to-differential voltage converter saves the space and extra parts needed for the external circuitry required by many delta-sigma converters. The internal full-differential signal processing architecture provides a wide dynamic range and excellent power supply rejection performance. The input signal is sampled at a 64× oversampling rate, eliminating the need for a sample-and-hold circuit, and simplifying antialias filtering requirements. The fifth-order delta-sigma noise shaper consists of five integrators which use a switched-capacitor topology, a comparator, and a feedback loop consisting of a one-bit DAC. The delta-sigma modulator shapes the quantization noise, shifting it out of the audio band in the frequency domain. The high order of the modulator enables it to randomize the modulator outputs, reducing idle tone levels.

The 64-f_S, one-bit data stream from the modulator is converted to 1-f_S, 16/20-bit data words by the decimation filter, which also acts as a low-pass filter to remove the shaped quantization noise. The dc components are removed by a high-pass filter function contained within the decimation filter.

DAC SECTION

The delta-sigma DAC section of the PCM3002/3003 is based on a 5-level amplitude quantizer and a third-order noise shaper. This section converts the oversampled input data to a 5-level delta-sigma format. A block diagram of the 5-level delta-sigma modulator is shown in Figure 53. This 5-level delta-sigma modulator has the advantage of improved stability and reduced clock-jitter sensitivity over the typical one-bit (2-level) delta-sigma modulator. The combined oversampling rate of the delta-sigma modulator and the internal 8× interpolation filter is 64 f_S for a 256-f_S system clock. The theoretical quantization noise performance of the 5-level delta-sigma modulator is shown in Figure 54.

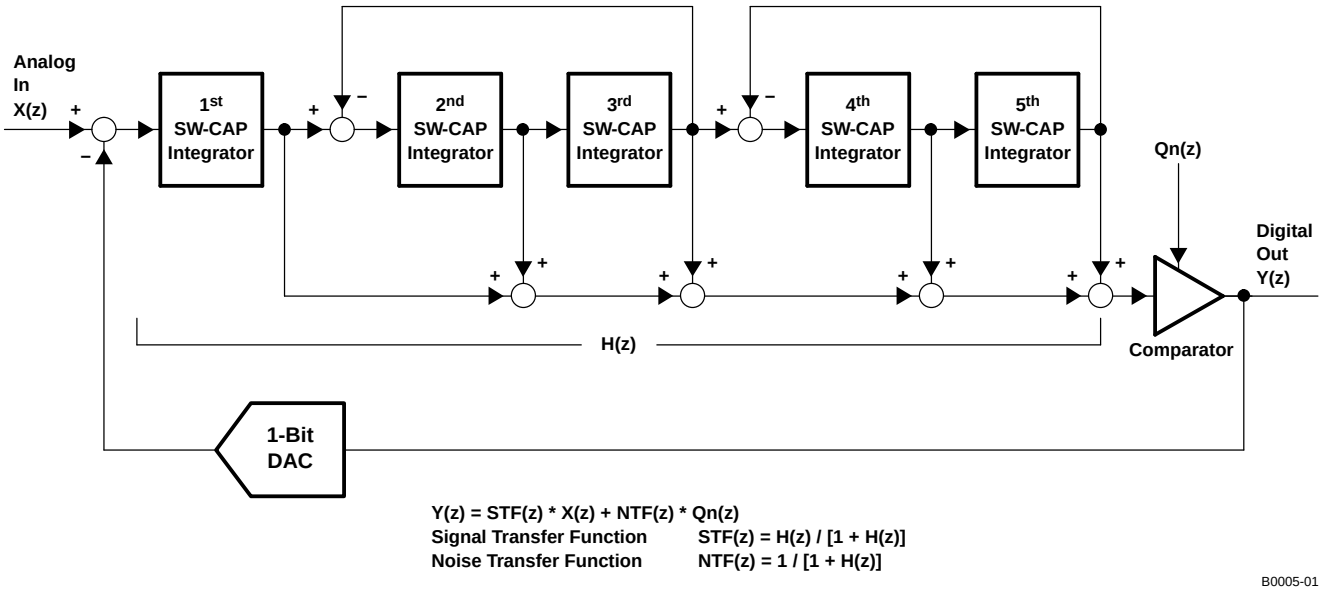


Figure 52. Simplified Fifth-Order Delta-Sigma Modulator

THEORY OF OPERATION (continued)

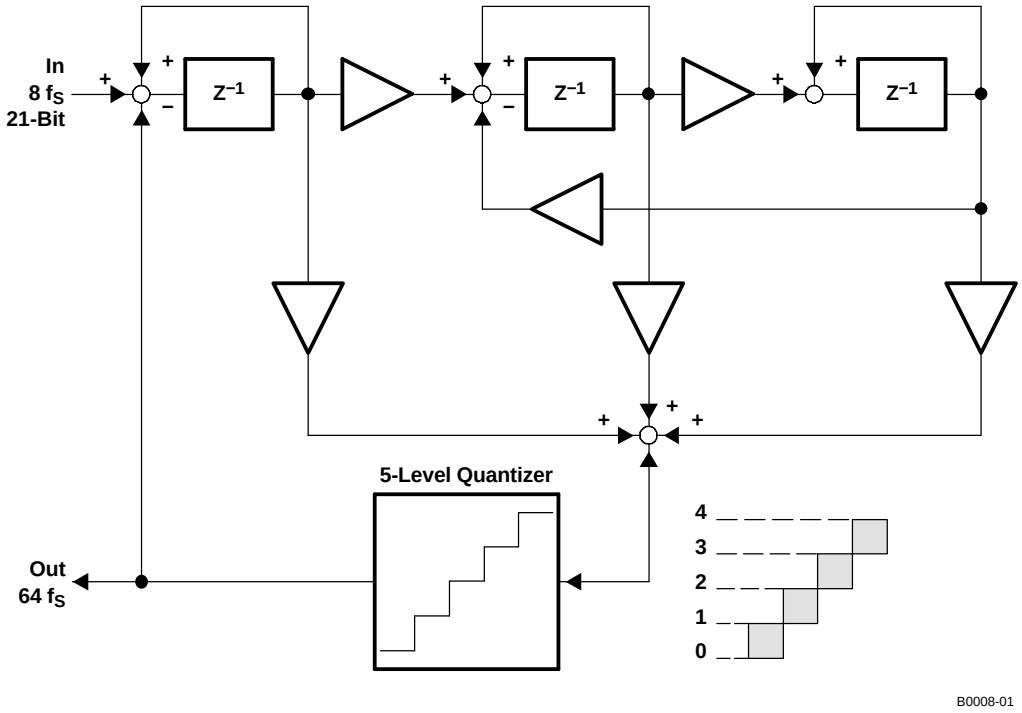


Figure 53. Five-Level Delta-Sigma Modulator Block Diagram

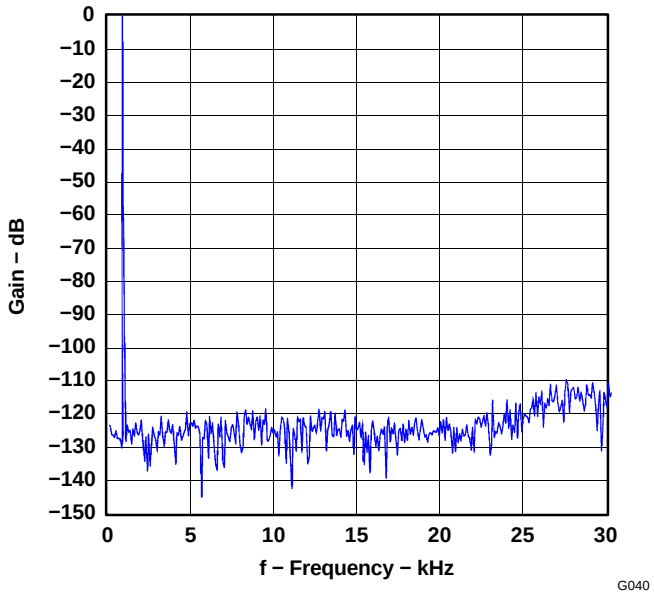


Figure 54. Quantization Noise Spectrum

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
PCM3002E	ACTIVE	SSOP	DB	24	58	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCM3002E/2K	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCM3002E/2KG4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCM3002EG	ACTIVE	SSOP	DB	24	58	Pb-Free (RoHS)	CU SNBI	Level-2-260C-1 YEAR
PCM3002EG/2K	ACTIVE	SSOP	DB	24	2000	Pb-Free (RoHS)	CU SNBI	Level-2-260C-1 YEAR
PCM3002EG/2KE6	ACTIVE	SSOP	DB	24	2000	Pb-Free (RoHS)	CU SNBI	Level-2-260C-1 YEAR
PCM3002EG4	ACTIVE	SSOP	DB	24	58	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCM3002EGE6	ACTIVE	SSOP	DB	24	58	Pb-Free (RoHS)	CU SNBI	Level-2-260C-1 YEAR
PCM3003E	ACTIVE	SSOP	DB	24	58	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCM3003E/2K	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCM3003E/2KG4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCM3003EG4	ACTIVE	SSOP	DB	24	58	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
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PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
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[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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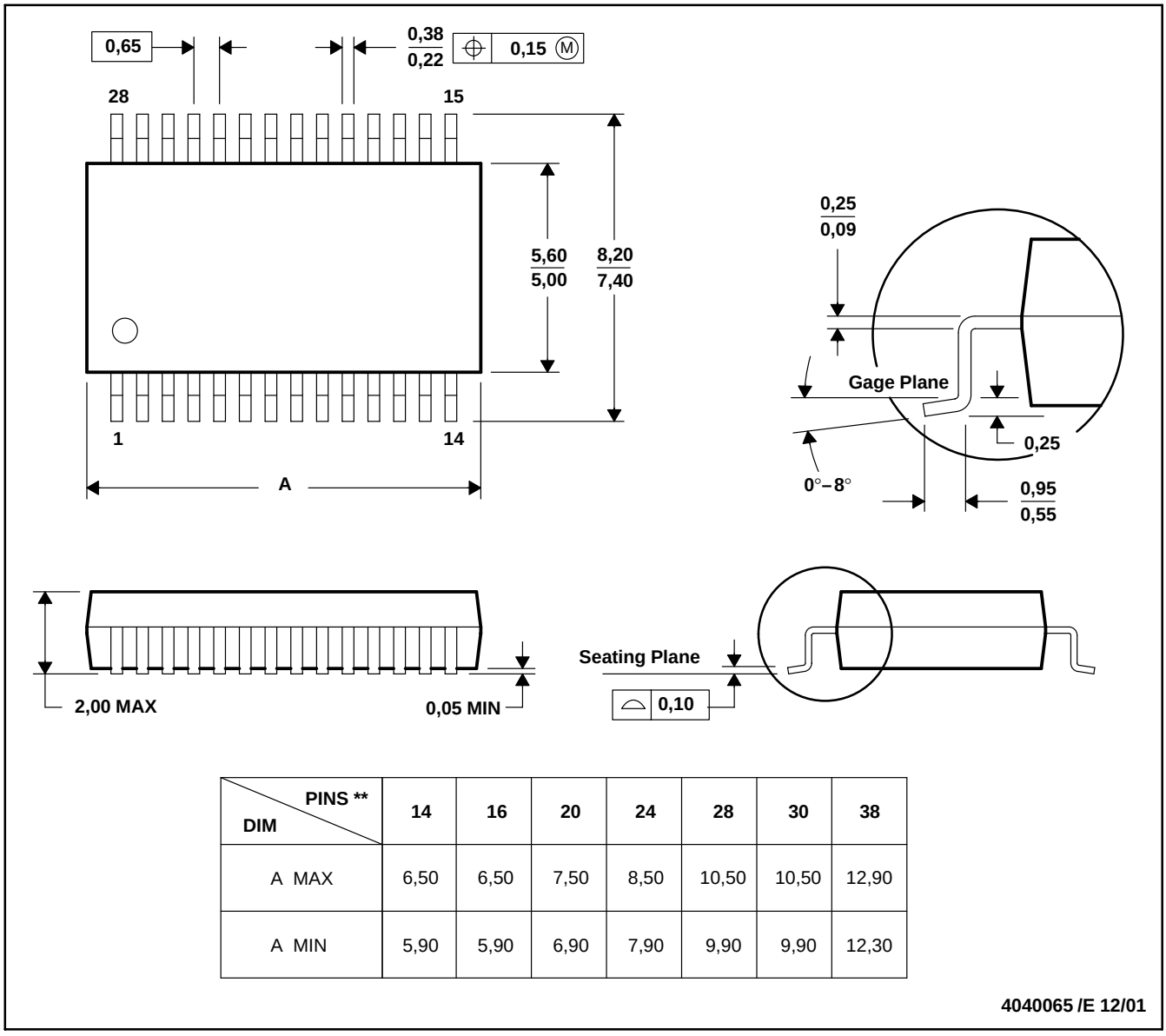
MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Telephony	www.ti.com/telephony
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

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