

8-Channel, High-Bandwidth, Analog Front-End

Check for Samples: [PGA5807](#)

FEATURES

- **8-Channel Complete AFE:**
 - LNA, PGA, and LPF
 - Full-Channel Gain: 12 dB to 30 dB
 - Input-Referred Noise: $2 \text{ nV}/\sqrt{\text{Hz}}$
- **LNA:**
 - Gain: 12 dB
 - Fully Differential
 - Wide Input Common-Mode Support: $2.1 \pm 200 \text{ mV}$
 - Maximum Linear Input Range: $500 \text{ mV}_{\text{PP}}$
- **18-dB PGA:**
 - With 3-dB Gain Steps
 - Programmable Via Either Serial Interface or External Pins
- **Programmable LPF:**
 - Corner Frequency: 75 MHz, 60 MHz
- **Power (Full-Chain):**
 - 60 mW per Channel
- **Fast and Consistent Overload Recovery**
- **Small Package: 9-mm x 9-mm QFN-64**

APPLICATIONS

- **Body Scan Imaging**
- **Data Acquisition Front Ends**
- **Ultrasound Imaging**

DESCRIPTION

The PGA5807 is an 8-channel, high-bandwidth, analog front end (AFE). The device functions on a single 3.3-V analog supply. The device supports input frequencies up to 25 MHz with a total power of 60 mW per channel. The PGA5807 consists of a low-noise amplifier (LNA), a programmable gain amplifier (PGA), and a programmable low-pass filter (LPF). The LNA has a fixed 12-dB gain (differential amplifier with dc input coupling) and supports a maximum linear input range of $500 \text{ mV}_{\text{PP}}$.

The device provides gain options from 0 dB to 18 dB, in 3-dB gain steps. This 18-dB PGA gain range can be programmed using either the serial interface or external pins. The PGA5807 integrates an antialiasing filter in the form of an LPF to reduce noise. The device is available in a very small, 9-mm x 9-mm QFN-16 package and is specified for operation over the -40°C to $+85^{\circ}\text{C}$ temperature range.

PRODUCT PREVIEW

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
PGA5807RGCR	PREVIEW	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	PGA5807	
PGA5807RGCT	PREVIEW	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	PGA5807	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

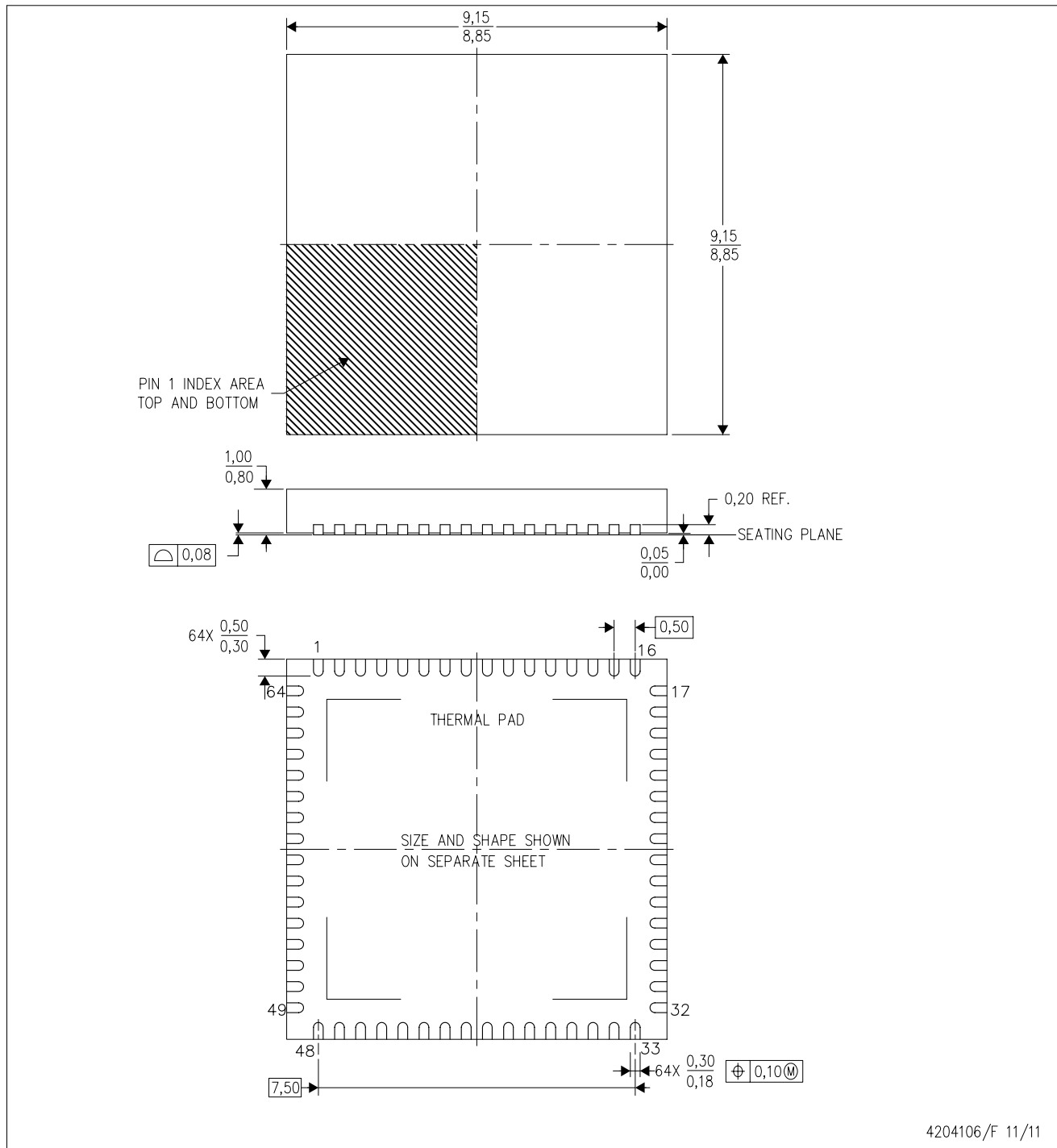
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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MECHANICAL DATA

RGC(S-PVQFN-N64) CUSTOM DEVICE PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
 - This drawing is subject to change without notice.
 - Quad Flatpack, No-leads (QFN) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

THERMAL PAD MECHANICAL DATA

RGC (S-PVQFN-N64)

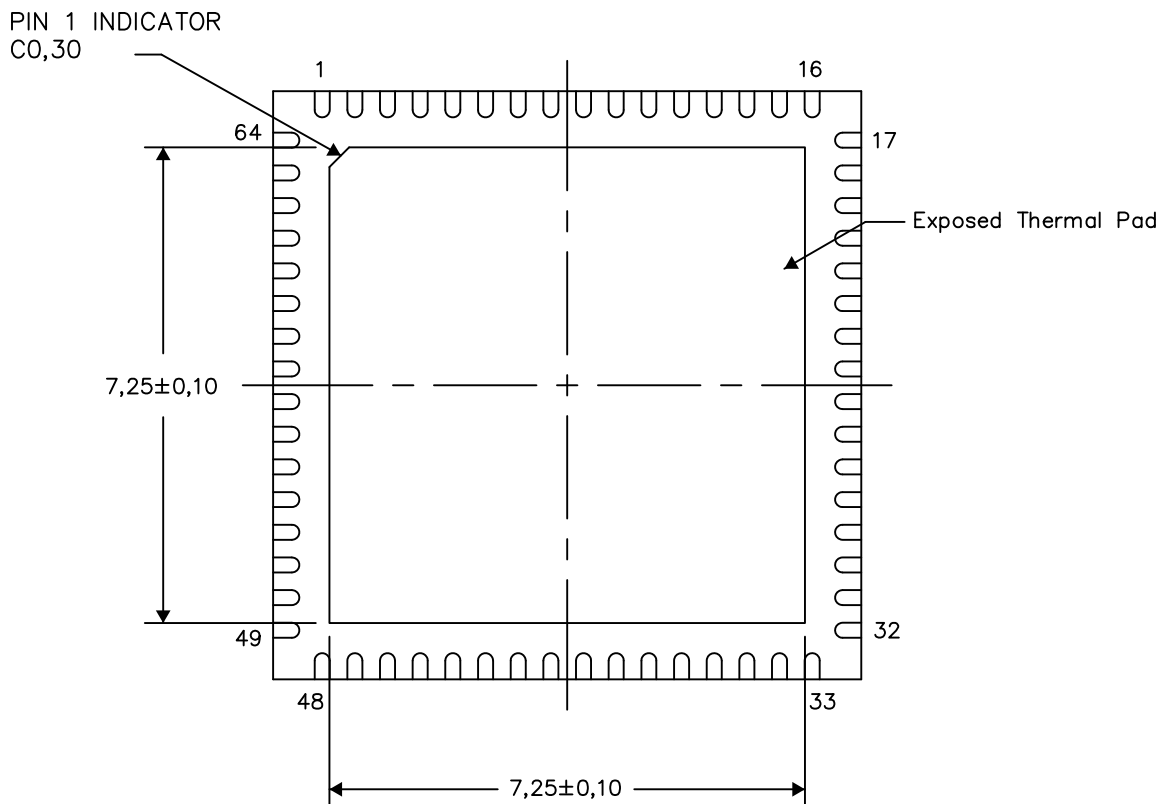
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

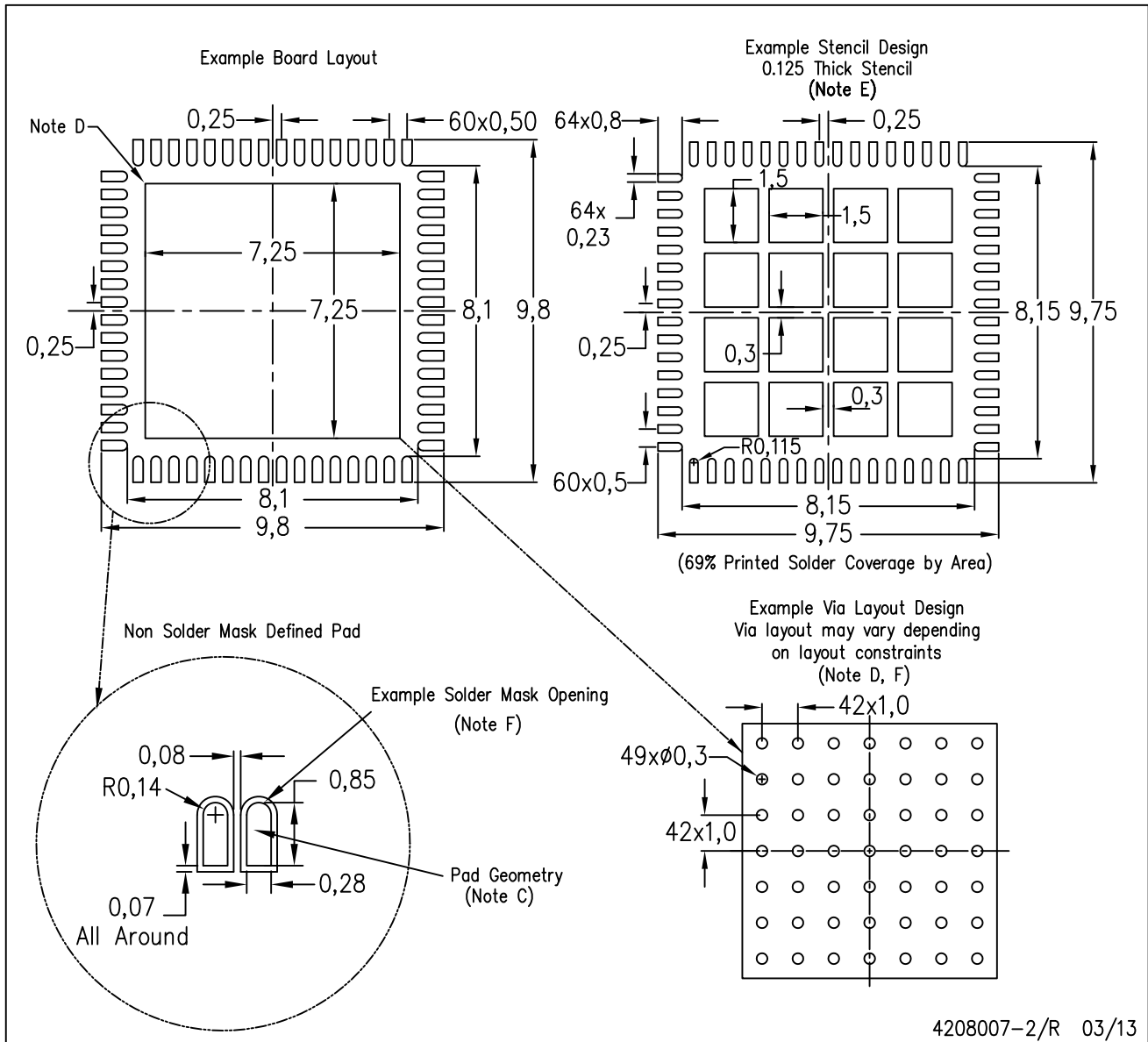
Exposed Thermal Pad Dimensions

4206192-2/Y 04/13

NOTE: A. All linear dimensions are in millimeters

RGC (S-PVQFN-N64)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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