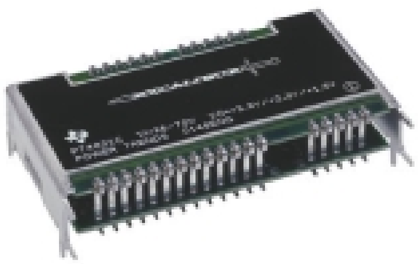
EXCALIBUR

35-W Triple Output Isolated DC/DC Converter for Logic Applications

SLTS165E - FEBRUARY 2002 - REVISED MARCH 2003



Features

- Triple Outputs (Independently Regulated)
- Input Voltage Range: 36V to 75V, 80V Surge
- 1500VDC Isolation
- Dual Logic On/Off Control
- Short-Circuit Protection (All Outputs)
- Fixed Frequency Operation
- Over-Temperature Shutdown
- Under-Voltage Lockout
- Space Saving Package: 1.3 sq. in. PCB Area (suffix N)
- Solderable Copper Case
- Safety Approvals:
  UL60950
  CSA 22.2 950
  VDE EN60950

Description

The PT4820 Excalibur™ power modules are a series of isolated triple-output DC/DC converters that operate from a standard (–48V) central office supply. Rated for up to 35W, these regulators are ideal for powering many mixed logic applications. The triple-output voltage combination allows for a compact multiple-output power supply in a single low-profile DC/DC module.

The available output voltage options include a low-voltage power bus for a DSP or ASIC core, and two additional standard logic supply voltages.

The PT4820 series incorporates many features to simplify system integration. These include a flexible On/Off enable control, an input under-voltage lock-out, and over-temperature protection. All outputs have short-circuit protection and are internally sequenced to meet the power-up and power-down requirements of popular DSP ICs.

The PT4820 series is housed in a space-saving solderable case. The module requires no external heat sink and can occupy as little as 1.3 in^2 of PCB area.

Ordering Information

PT4821❑ = +3.3/+2.5/+1.5V
PT4822❑ = +3.3/+1.8/+1.5V
PT4823❑ = +3.3/+2.5/+1.2V
PT4824❑ = +3.3/+1.8/+1.2V
PT4825❑ = +3.3/+1.5/+1.2V
PT4826❑ = +5.0/+3.3/+1.8V
PT4827❑ = +3.3/+2.5/+1.8V
PT4828❑ = +5.0/+2.5/+1.5V
PT4829❑ = +5.0/+1.8/+1.5V
PT4831❑ = +5.0/+3.3/+1.5V
PT4832❑ = +5.0/+3.3/+2.5V
* **PT4833❑** = +3.3/+2.0/+1.5V

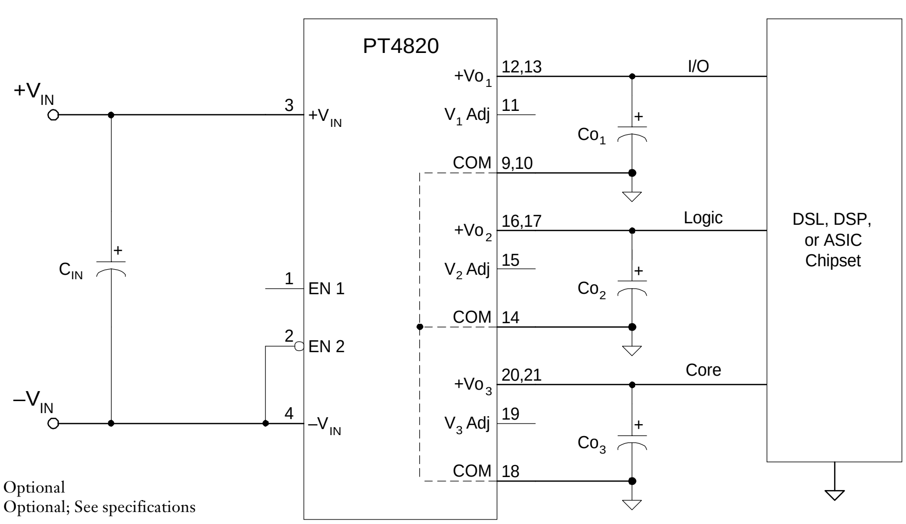
** The PT4833 is not included in the VDE safety certification.*

PT Series Suffix (PT1234x)

Case/Pin Configuration	Order Suffix	Package Code
Vertical	N	(ENM)
Horizontal	A	(ENN)
SMD	C	(ENP)

(Reference the applicable package code drawing for the dimensions and PC layout)

Typical Application



Cin = Optional
Co1, Co2, Co3 = Optional; See specifications
EN1 & EN2 pins: See On/Off Enable Logic

Environmental Specifications

Characteristics	Symbols	Conditions		Min	Typ	Max	Units
Ambient Temperature Range	T_a	Over V_{in} Range		–40	—	+85 (i)	°C
Case Temperature	T_c	Measured at center of case		—	—	+100	°C
Shutdown Temperature	OTP				115	125	°C
Solder Reflow Temperature	T_{reflow}	Surface temperature of module pins or case		—	—	215 (ii)	°C
Storage Temperature	T_s	—		–40	—	+125	°C
Mechanical Shock		Per Mil-STD-883D, Method 2002.3 1 msec, ½ Sine, mounted		—	500	—	G's
Mechanical Vibration		Mil-STD-883D, Method 2007.2 20-2000 Hz	Suffix A, C	—	20 (iii)	—	G's
Weight	—	Vertical/Horizontal		—	50	—	grams
Flammability	—	Meets UL 94V-O					

Notes: *(i) See SOA curves or consult factory for appropriate derating.*
(ii) During solder reflow of SMD package version, do not elevate the module case, pins, or internal component temperatures above a peak of 215°C. For further guidance refer to the application note, "Reflow Soldering Requirements for Plug-in Power Surface Mount Products," (SLTA051).
(iii) The case pins on through-hole pin configurations (N & A) must be soldered. For more information see the applicable package outline drawing.

Pin Configuration

Pin	Function
1	EN 1
2	EN 2
3	+Vin
4	–Vin
5	Do Not Connect
6	Pin Not Present
7	Pin Not Present
8	Pin Not Present
9	COM
10	COM
11	Vo_1 Adjust

Pin	Function
12	Vo_1
13	Vo_1
14	COM
15	Vo_2 adjust
16	$+Vo_2$
17	$+Vo_2$
18	COM
19	Vo_3 adjust
20	$+Vo_3$
21	$+Vo_3$

Note: Shaded functions indicates those pins that are at primary-side potential. All other pins are referenced to the secondary.

On/Off Enable Logic

Pin 1	Pin 2	Output Status
×	1	Off
1	0	On
0	×	Off

Notes:
Logic 1 =Open collector
Logic 0 = –Vin (pin 2) potential

For positive Enable function, connect pin 2 to pin 4 and use pin 1.

For negative Enable function, leave pin 1 open and use pin 2.

For automatice power-up connect pin 2 to pin 4 and leave pin 1 open.

Pin Descriptions

+Vin: The positive input supply for the module with respect to –Vin. When powering the module from a –48V telecom central office supply, this input is connected to the primary system ground.

–Vin: The negative input supply for the module, and the 0VDC reference for the EN 1, and EN 2 inputs. When powering the module from a +48V supply, this input is connected to the 48V(Return).

EN 1: The positive logic input that activates the module output. If not used, this pin should be left open circuit. Connecting this input to –Vin disables the module's outputs.

EN 2: The negative logic input that activates the module output. This pin must be connected to –Vin to enable the module's outputs. A high impedance disables the module's outputs.

Vo 1: The highest regulated output voltage, which is referenced to the COM node.

Vo 2: The regulated output that is designed to power logic circuitry. It is referenced to the COM node.

Vo 3: The low-voltage regulated output that provides power for a µ-processor or DSP core, and is referenced to the COM node.

COM: The secondary return reference for the module's three regulated output voltages. It is DC isolated from the input supply pins.

Vo_1 Adjust: Using a single resistor, this pin allows Vo_1 to be adjusted higher or lower than the preset value. If not used, this pin should be left open circuit.

Vo_2 Adjust: Using a single resistor, this pin allows Vo_2 to be adjusted higher or lower than the preset value. If not used, this pin should be left open circuit.

Vo_3 Adjust: Using a single resistor, this pin allows Vo_3 to be adjusted higher or lower than the preset value. If not used, this pin should be left open circuit.

PT4821 Electrical Specifications

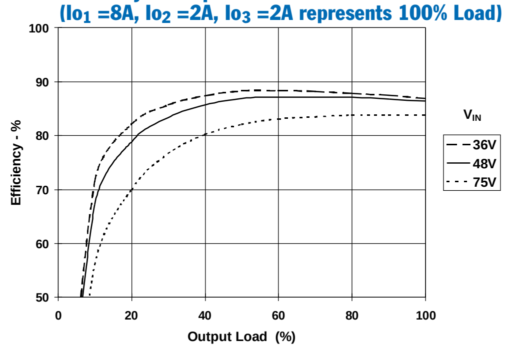
(Unless otherwise stated, the operating conditions are: T_a =25°C, V_{in} =48V, and I_o =0.5$I_o$max)

Characteristics	Symbols	Conditions		PT4821 Min	Typ	Max	Units
Output Current	I_o	Each output	Io_1 (3.3V) Io_2 (2.5V) Io_3 (1.5V)	0.25 (1) 0.1 (1) 0.1 (1)	— — —	8 (2) 6 (2) 6 (2)	A
		Total (Io_1 + Io_2 + Io_3)		—	—	12 (2)	A
Input Voltage Range	V_{in}	Continuous Surge (1 minute)		36 —	— —	75 80	V
Set-Point Voltage	V_o		Vo_1 Vo_2 Vo_3	3.24 2.45 1.47	3.3 2.5 1.5	3.36 2.55 1.53	V
Temperature Variation	Reg_{temp}	–40°C ≤T_a ≤+85°C, I_o =$I_o$min	Vo_1 Vo_2/Vo_3	— —	±0.5 ±0.5	— —	%V_o
Line Regulation	Reg_{line}	All outputs, Over V_{in} range		—	±0.1	±0.5	%V_o
Load Regulation	Reg_{load}	All outputs, 0≤I_o≤$I_o$max		—	±0.1	±0.5	%V_o
Total Output Voltage Variation	ΔV_o tol	Includes set-point, line, load, –40°C≤T_a≤+85°C	Vo_1 Vo_2/Vo_3	— —	— —	±3 (3) ±3 (3)	%V_o
Efficiency	η	Io_1 =6A, Io_2 =2A, Io_3 =2A		—	87	—	%
V_o Ripple/Noise (0 to 20MHz bandwidth)	V_n		Vo_1 Vo_2 Vo_3	— — —	40 35 25	— — —	mV_{pp}
Transient Response	t_{tr} V_{os}	0.1A/µs load step, 50% to 75% $I_o$max V_o over/undershoot		— —	200 3	— —	µSec %V_o
Output Adjust Range	$V_o$adj		Vo_1/Vo_2/Vo_3	—	±10	—	%V_o
Over-Current Threshold	I_{TRIP}	Total, all outputs. Reset with auto-recovery		—	14	—	A
Switching Frequency	f_s	Over V_{in} and I_o ranges		350	400	450	kHz
Under Voltage Lockout	V_{on} V_{off}	V_{in} increasing V_{in} decreasing		— —	35.5 34	— —	V
Turn-On Time	t_{on}	V_{in} =48V step		—	140 (4)	—	ms
Enable Control (pins 1 & 2) High-Level Input Voltage Low-Level Input Voltage	 V_{IH} V_{IL}	Referenced to $-V_{in}$ (pin 4)		 4 –0.2	 — —	 15 (5) 0.8	V
Low-Level Input Current	I_{IL}			—	1	2	mA
Standby Input Current	I_{in} standby	pins 1 & 2 open circuit		—	1	5	mA
Internal Input Capacitance	C_{int}			—	1.14	—	µF
External Output Capacitance	Co_1 Co_2 Co_3			0 0 0	220 220 220	1,000 (6) 1,000 (6) 1,000 (6)	µF
Primary/Secondary Isolation	V_{iso} C_{iso} R_{iso}			1500 — 10	— 2,200 —	— — —	V pF MΩ

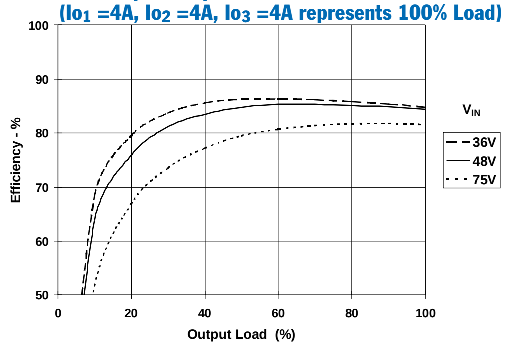
Notes: (1) *The converter will operate down to no load with reduced specifications.*
(2) *The sum-total current from outputs Vo_1, Vo_2, and Vo_3 not to exceed 12ADC.*
(3) *Limits are specified by design.*
(4) *Measured from the application of the input voltage to the instance that all outputs are in regulation.*
(5) *The Enable inputs (pins 1 & 2) have internal pull-ups. Leaving pin 1 open-circuit and connecting pin 2 to $-V_{in}$ allows the the converter to operate when input power is applied. The maximum open-circuit voltage is 4V.*
(6) *Ultra-low ESR capacitors, such as organic or polymer aluminum electrolytic types, may cause instability. Consult the factory before using.*

PT4821 Performance Characteristics (See Notes A, B)

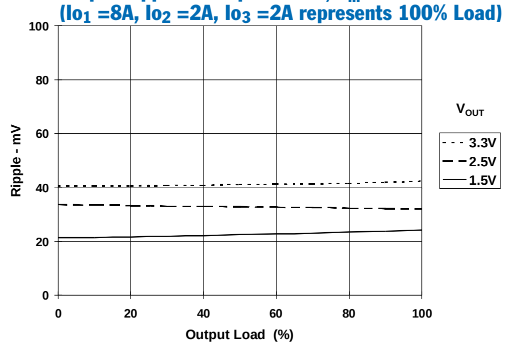
Efficiency vs Output Power
(Io_1 =8A, Io_2 =2A, Io_3 =2A represents 100% Load)



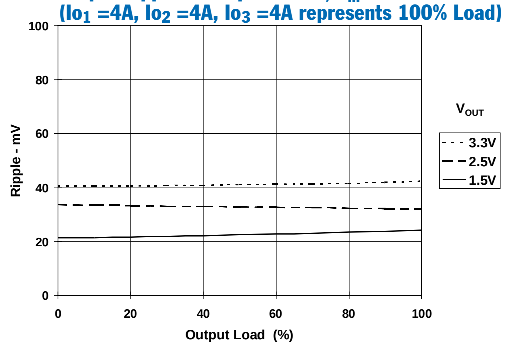
Efficiency vs Output Power
(Io_1 =4A, Io_2 =4A, Io_3 =4A represents 100% Load)



Output Ripple vs Output Power; V_{in} =48V
(Io_1 =8A, Io_2 =2A, Io_3 =2A represents 100% Load)



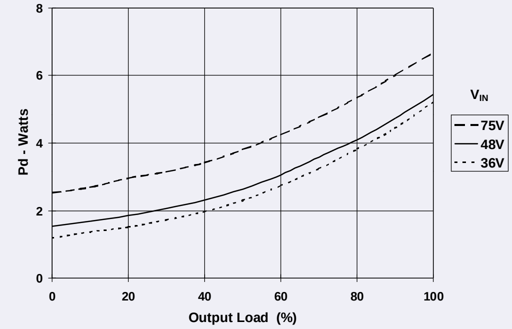
Output Ripple vs Output Power; V_{in} =48V
(Io_1 =4A, Io_2 =4A, Io_3 =4A represents 100% Load)



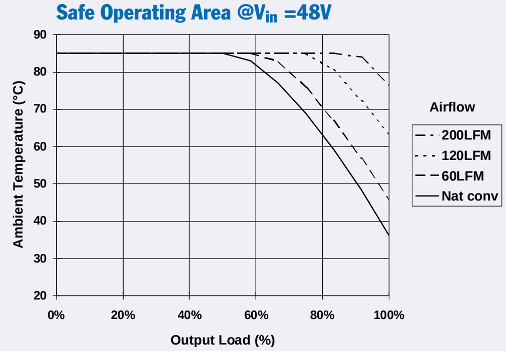
PT4821 Thermal Performance (See Note C)

(Io_1 + Io_2 + Io_3 =12A, represents 100% Load)

Power Dissipation vs Output Load



Safe Operating Area @V_{in} =48V



Note A: *All Characteristic data in the above graphs has been developed from actual products tested at 25°C. This data is considered typical data for the ISR.*
Note B: *Output Load (%) represents the percent drawn from each output of the stated 100% load condition.*
Note C: *SOA curves represent operating conditions at which the internal components are at or below the manufacturer's maximum rated operating temperatures.*

PT4822 Electrical Specifications

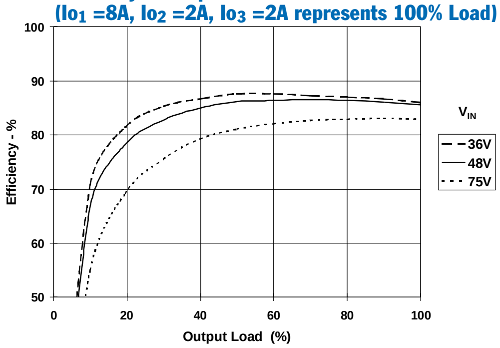
(Unless otherwise stated, the operating conditions are: T_a =25°C, V_{in} =48V, and I_o =0.5$I_o$max)

Characteristics	Symbols	Conditions		PT4822 Min	PT4822 Typ	PT4822 Max	Units
Output Current	I_o	Each output	Io_1 (3.3V) Io_2 (1.8V) Io_3 (1.5V)	0.25 (1) 0.1 (1) 0.1 (1)	— — —	8 (2) 6 (2) 6 (2)	A
		Total (Io_1 + Io_2 + Io_3)		—	—	12 (2)	A
Input Voltage Range	V_{in}	Continuous Surge (1 minute)		36 —	— —	75 80	V
Set-Point Voltage	V_o		Vo_1 Vo_2 Vo_3	3.24 1.76 1.47	3.3 1.8 1.5	3.36 1.84 1.53	V
Temperature Variation	Reg_{temp}	–40°C ≤T_a ≤+85°C, I_o =$I_o$min	Vo_1 Vo_2/Vo_3	— —	±0.5 ±0.5	— —	%V_o
Line Regulation	Reg_{line}	All outputs, Over V_{in} range		—	±0.1	±0.5	%V_o
Load Regulation	Reg_{load}	All outputs, 0≤I_o≤$I_o$max		—	±0.1	±0.5	%V_o
Total Output Voltage Variation	ΔV_o tol	Includes set-point, line, load, –40°C≤T_a≤+85°C	Vo_1 Vo_2/Vo_3	— —	— —	±3 (3) ±3 (3)	%V_o
Efficiency	η	Io_1 =6A, Io_2 =2A, Io_3 =2A		—	86	—	%
V_o Ripple/Noise (0 to 20MHz bandwidth)	V_n		Vo_1 Vo_2 Vo_3	— — —	40 25 25	— — —	mV$_{pp}$
Transient Response	t_{tr} V_{os}	0.1A/µs load step, 50% to 75% $I_o$max V_o over/undershoot		— —	200 3	— —	µSec %V_o
Output Adjust Range	$V_o$adj		Vo_1/Vo_2/Vo_3	—	±10	—	%V_o
Over-Current Threshold	I_{TRIP}	Total, all outputs. Reset with auto-recovery		—	14	—	A
Switching Frequency	f_s	Over V_{in} and I_o ranges		350	400	450	kHz
Under Voltage Lockout	V_{on} V_{off}	V_{in} increasing V_{in} decreasing		— —	35.5 34	— —	V
Turn-On Time	t_{on}	V_{in} =48V step		—	140 (4)	—	ms
Enable Control (pins 1 & 2) High-Level Input Voltage Low-Level Input Voltage	 V_{IH} V_{IL}	Referenced to $-V_{in}$ (pin 4)		 4 –0.2	 — —	 15 (5) 0.8	 V
Low-Level Input Current	I_{IL}			—	1	2	mA
Standby Input Current	I_{in} standby	pins 1 & 2 open circuit		—	1	5	mA
Internal Input Capacitance	C_{int}			—	1.14	—	µF
External Output Capacitance	Co_1 Co_2 Co_3			0 0 0	220 220 220	1,000 (6) 1,000 (6) 1,000 (6)	µF
Primary/Secondary Isolation	V_{iso} C_{iso} R_{iso}			1500 — 10	— 2,200 —	— — —	V pF MΩ

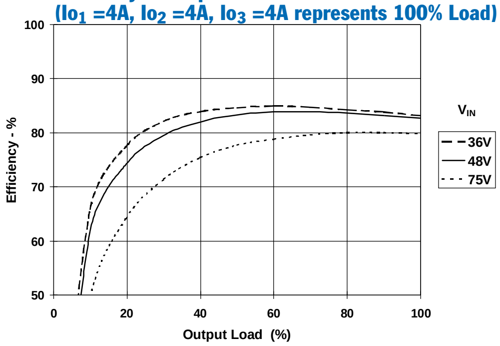
Notes: (1) *The converter will operate down to no load with reduced specifications.*
(2) *The sum-total current from outputs Vo_1, Vo_2, and Vo_3 cannot exceed 12ADC.*
(3) *Limits are specified by design.*
(4) *Measured from the application of the input voltage to the instance that all outputs are in regulation.*
(5) *The Enable inputs (pins 1 & 2) have internal pull-ups. Leaving pin 1 open-circuit and connecting pin 2 to $-V_{in}$ allows the the converter to operate when input power is applied. The maximum open-circuit voltage is 4V.*
(6) *Ultra-low ESR capacitors, such as organic or polymer aluminum electrolytic types, may cause instability. Consult the factory before using.*

PT4822 Performance Characteristics (See Note A, B)

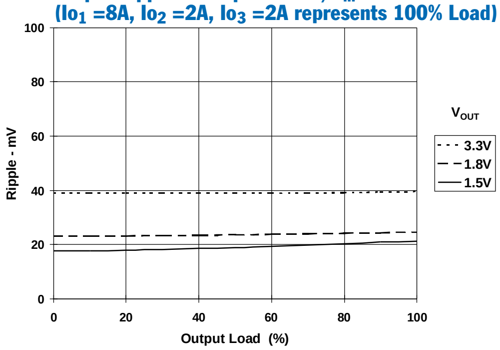
Efficiency vs Output Power
(Io_1 =8A, Io_2 =2A, Io_3 =2A represents 100% Load)



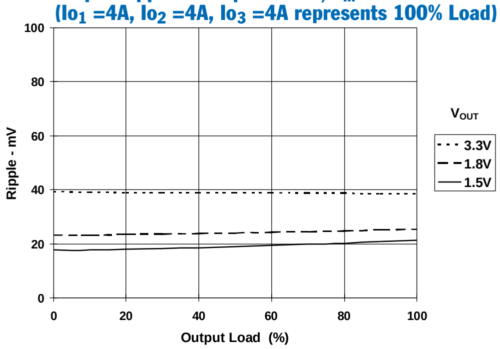
Efficiency vs Output Power
(Io_1 =4A, Io_2 =4A, Io_3 =4A represents 100% Load)



Output Ripple vs Output Power; V_{in} =48V
(Io_1 =8A, Io_2 =2A, Io_3 =2A represents 100% Load)

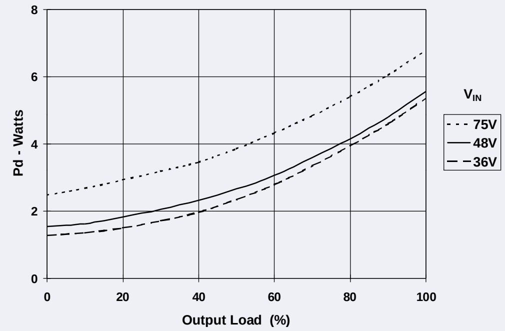


Output Ripple vs Output Power; V_{in} =48V
(Io_1 =4A, Io_2 =4A, Io_3 =4A represents 100% Load)

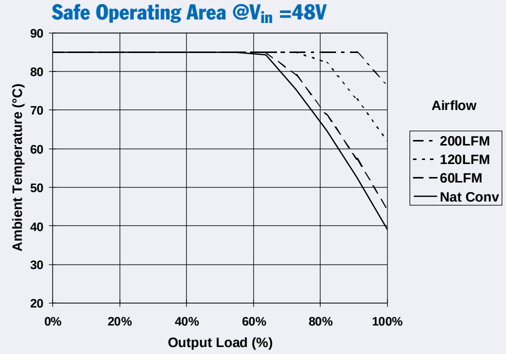


PT4822 Thermal Performance (See Note C)
(Io_1 + Io_2 + Io_3 =12A, represents 100% Load)

Power Dissipation vs Output Load



Safe Operating Area @V_{in} =48V



Note A: *All Characteristic data in the above graphs has been developed from actual products tested at 25°C. This data is considered typical data for the ISR.*
Note B: *Output Load (%) represents the percent drawn from each output of the stated 100% load condition.*
Note C: *SOA curves represent operating conditions at which the internal components are at or below the manufacturer's maximum rated operating temperatures.*

PT4823 Electrical Specifications

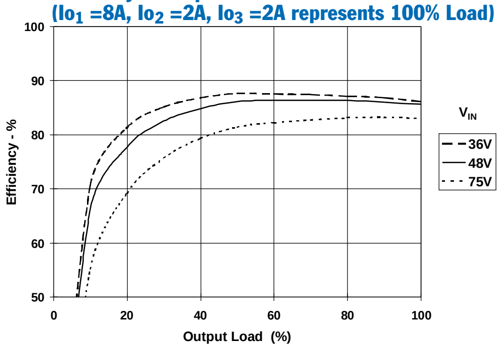
(Unless otherwise stated, the operating conditions are: T_a =25°C, V_{in} =48V, and I_o =0.5$I_o$max)

Characteristics	Symbols	Conditions		PT4823 Min	Typ	Max	Units
Output Current	I_o	Each output	Io_1 (3.3V) Io_2 (2.5V) Io_3 (1.2V)	0.25 (1) 0.1 (1) 0.1 (1)	— — —	8 (2) 6 (2) 6 (2)	A
		Total (Io_1 + Io_2 + Io_3)		—	—	12 (2)	A
Input Voltage Range	V_{in}	Continuous Surge (1 minute)		36 —	— —	75 80	V
Set-Point Voltage	V_o		Vo_1 Vo_2 Vo_3	3.24 2.45 1.17	3.3 2.5 1.2	3.36 2.55 1.23	V
Temperature Variation	Reg_{temp}	–40°C ≤T_a ≤+85°C, I_o =$I_o$min	Vo_1 Vo_2/Vo_3	— —	±0.5 ±0.5	— —	%V_o
Line Regulation	Reg_{line}	All outputs, Over V_{in} range		—	±0.1	±0.5	%V_o
Load Regulation	Reg_{load}	All outputs, 0≤I_o≤$I_o$max		—	±0.1	±0.5	%V_o
Total Output Voltage Variation	ΔV_o tol	Includes set-point, line, load, –40°C≤T_a ≤+85°C	Vo_1 Vo_2/Vo_3	— —	— —	±3 (3) ±3 (3)	%V_o
Efficiency	η	Io_1 =6A, Io_2 =2A, Io_3 =2A		—	85.6	—	%
V_o Ripple/Noise (0 to 20MHz bandwidth)	V_n		Vo_1 Vo_2 Vo_3	— — —	35 25 25	— — —	mV_{pp}
Transient Response	t_{tr} V_{os}	0.1A/µs load step, 50% to 75% $I_o$max V_o over/undershoot		— —	200 3	— —	µSec %V_o
Output Adjust Range	$V_o$adj		Vo_1/Vo_2/Vo_3	—	±10	—	%V_o
Over-Current Threshold	I_{TRIP}	Total, all outputs. Reset with auto-recovery		—	14	—	A
Switching Frequency	f_s	Over V_{in} and I_o ranges		350	400	450	kHz
Under Voltage Lockout	V_{on} V_{off}	V_{in} increasing V_{in} decreasing		— —	35.5 34	— —	V
Turn-On Time	t_{on}	V_{in} =48V step		—	140 (4)	—	ms
Enable Control (pins 1 & 2) High-Level Input Voltage Low-Level Input Voltage	 V_{IH} V_{IL}	Referenced to –V_{in} (pin 4)		 4 –0.2	 — —	 15 (5) 0.8	 V
Low-Level Input Current	I_{IL}			—	1	2	mA
Standby Input Current	I_{in} standby	pins 1 & 2 open circuit		—	1	5	mA
Internal Input Capacitance	C_{int}			—	1.14	—	µF
External Output Capacitance	Co_1 Co_2 Co_3			0 0 0	220 220 220	1,000 (6) 1,000 (6) 1,000 (6)	µF
Primary/Secondary Isolation	V_{iso} C_{iso} R_{iso}			1500 — 10	— 2,200 —	— — —	V pF MΩ

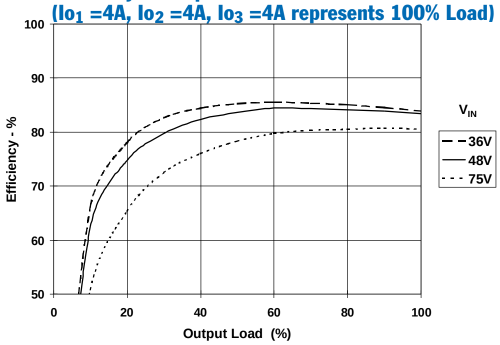
Notes: (1) *The converter will operate down to no load with reduced specifications.*
(2) *The sum-total current from outputs Vo_1, Vo_2, and Vo_3 cannot exceed 12ADC.*
(3) *Limits are specified by design.*
(4) *Measured from the application of the input voltage to the instance that all outputs are in regulation.*
(5) *The Enable inputs (pins 1 & 2) have internal pull-ups. Leaving pin 1 open-circuit and connecting pin 2 to –V_{in} allows the the converter to operate when input power is applied. The maximum open-circuit voltage is 4V.*
(6) *Ultra-low ESR capacitors, such as organic or polymer aluminum electrolytic types, may cause instability. Consult the factory before using.*

PT4823 Performance Characteristics (See Notes A, B)

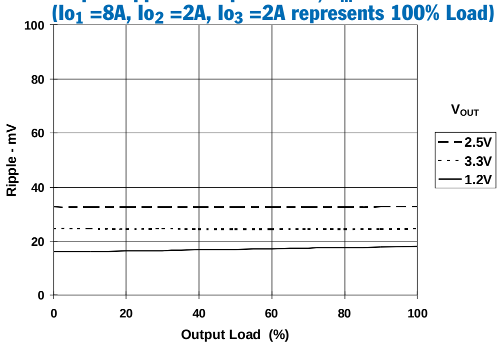
Efficiency vs Output Power
(Io_1 =8A, Io_2 =2A, Io_3 =2A represents 100% Load)



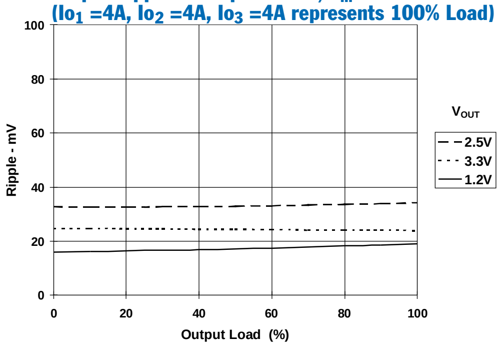
Efficiency vs Output Power
(Io_1 =4A, Io_2 =4A, Io_3 =4A represents 100% Load)



Output Ripple vs Output Power; V_{in} =48V
(Io_1 =8A, Io_2 =2A, Io_3 =2A represents 100% Load)



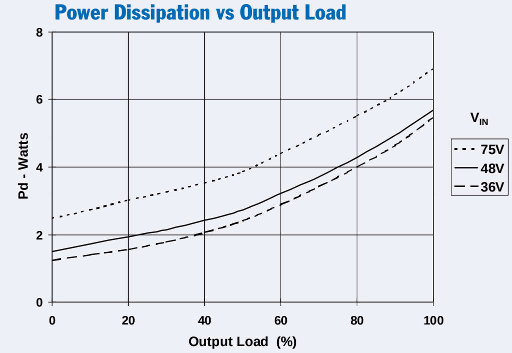
Output Ripple vs Output Power; V_{in} =48V
(Io_1 =4A, Io_2 =4A, Io_3 =4A represents 100% Load)



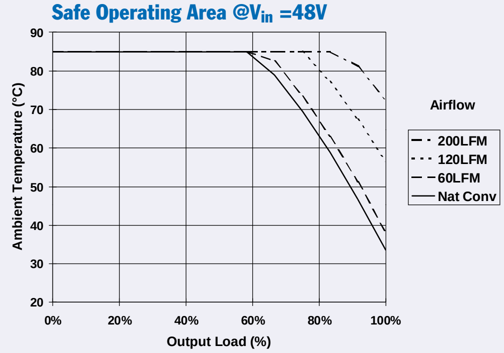
PT4823 Thermal Performance (See Note C)

(Io_1 + Io_2 + Io_3 =12A, represents 100% Load)

Power Dissipation vs Output Load



Safe Operating Area @V_{in} =48V



Note A: *All Characteristic data in the above graphs has been developed from actual products tested at 25°C. This data is considered typical data for the ISR.*
Note B: *Output Load (%) represents the percent drawn from each output of the stated 100% load condition.*
Note C: *SOA curves represent operating conditions at which the internal components are at or below the manufacturer's maximum rated operating temperatures.*

PT4824 Electrical Specifications

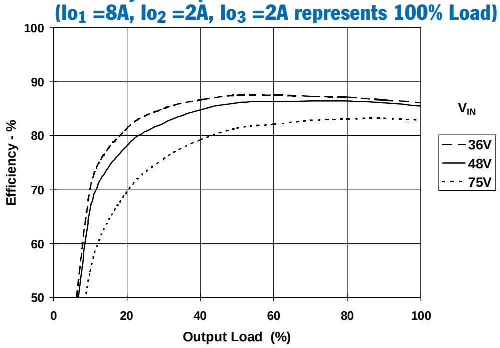
(Unless otherwise stated, the operating conditions are: T_a =25°C, V_{in} =48V, and I_o =0.5$I_o$max)

Characteristics	Symbols	Conditions		PT4824 Min	Typ	Max	Units
Output Current	I_o	Each output	I_{O1} (3.3V) I_{O2} (1.8V) I_{O3} (1.2V)	0.25 (1) 0.1 (1) 0.1 (1)	— — —	8 (2) 6 (2) 6 (2)	A
		Total (I_{O1} + I_{O2} + I_{O3})		—	—	12 (2)	A
Input Voltage Range	V_{in}	Continuous Surge (1 minute)		36 —	— —	75 80	V
Set-Point Voltage	V_o		V_{O1} V_{O2} V_{O3}	3.24 1.76 1.17	3.3 1.8 1.2	3.36 1.84 1.23	V
Temperature Variation	Reg_{temp}	–40°C ≤T_a ≤+85°C, I_o =$I_o$min	V_{O1} V_{O2}/V_{O3}	— —	±0.5 ±0.5	— —	%V_o
Line Regulation	Reg_{line}	All outputs, Over V_{in} range		—	±0.1	±0.5	%V_o
Load Regulation	Reg_{load}	All outputs, 0≤I_o≤$I_o$max		—	±0.1	±0.5	%V_o
Total Output Voltage Variation	ΔV_o tol	Includes set-point, line, load, –40°C≤T_a≤+85°C	V_{O1} V_{O2}/V_{O3}	— —	— —	±3 (3) ±3 (3)	%V_o
Efficiency	η	I_{O1} =6A, I_{O2} =2A, I_{O3} =2A		—	85	—	%
V_o Ripple/Noise (0 to 20MHz bandwidth)	V_n		V_{O1} V_{O2} V_{O3}	— — —	30 25 25	— — —	mV_{pp}
Transient Response	t_{tr} V_{os}	0.1A/µs load step, 50% to 75% $I_o$max V_o over/undershoot		— —	200 3	— —	µSec %V_o
Output Adjust Range	$V_o$adj		V_{O1}/V_{O2}/V_{O3}	—	±10	—	%V_o
Over-Current Threshold	I_{TRIP}	Total, all outputs. Reset with auto-recovery		—	14	—	A
Switching Frequency	f_s	Over V_{in} and I_o ranges		350	400	450	kHz
Under Voltage Lockout	V_{on} V_{off}	V_{in} increasing V_{in} decreasing		— —	35.5 34	— —	V
Turn-On Time	t_{on}	V_{in} =48V step		—	140 (4)	—	ms
Enable Control (pins 1 & 2) High-Level Input Voltage Low-Level Input Voltage	 V_{IH} V_{IL}	Referenced to $-V_{in}$ (pin 4)		 4 –0.2	 — —	 15 (5) 0.8	 V
Low-Level Input Current	I_{IL}			—	1	2	mA
Standby Input Current	I_{in} standby	pins 1 & 2 open circuit		—	1	5	mA
Internal Input Capacitance	C_{int}			—	1.14	—	µF
External Output Capacitance	C_{O1} C_{O2} C_{O3}			0 0 0	220 220 220	1,000 (6) 1,000 (6) 1,000 (6)	µF
Primary/Secondary Isolation	V_{iso} C_{iso} R_{iso}			1500 — 10	— 2,200 —	— — —	V pF MΩ

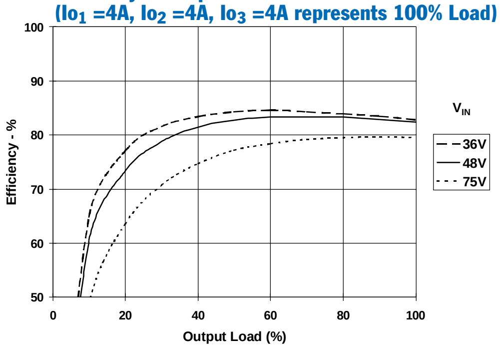
Notes: (1) *The converter will operate down to no load with reduced specifications.*
(2) *The sum-total current from outputs V_{O1}, V_{O2}, and V_{O3} cannot exceed 12ADC.*
(3) *Limits are specified by design.*
(4) *Measured from the application of the input voltage to the instance that all outputs are in regulation.*
(5) *The Enable inputs (pins 1 & 2) have internal pull-ups. Leaving pin 1 open-circuit and connecting pin 2 to $-V_{in}$ allows the the converter to operate when input power is applied. The maximum open-circuit voltage is 4V.*
(6) *Ultra-low ESR capacitors, such as organic or polymer aluminum electrolytic types, may cause instability. Consult the factory before using.*

PT4824 Performance Characteristics (See Notes A, B)

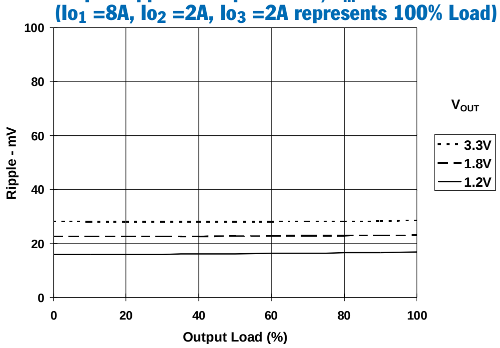
Efficiency vs Output Power (Io$_1$ =8A, Io$_2$ =2A, Io$_3$ =2A represents 100% Load)



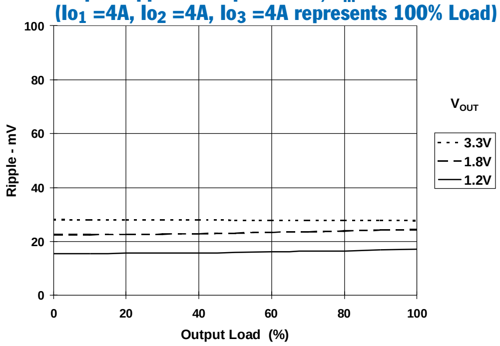
Efficiency vs Output Power (Io$_1$ =4A, Io$_2$ =4A, Io$_3$ =4A represents 100% Load)



Output Ripple vs Output Power; V_{in} =48V (Io$_1$ =8A, Io$_2$ =2A, Io$_3$ =2A represents 100% Load)



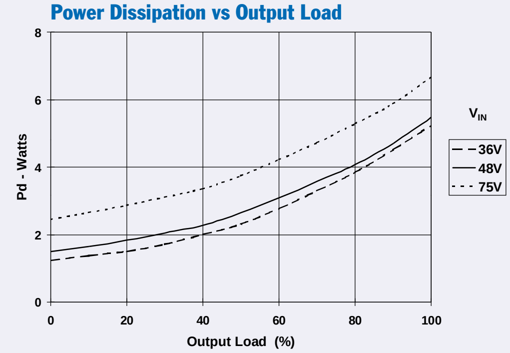
Output Ripple vs Output Power; V_{in} =48V (Io$_1$ =4A, Io$_2$ =4A, Io$_3$ =4A represents 100% Load)



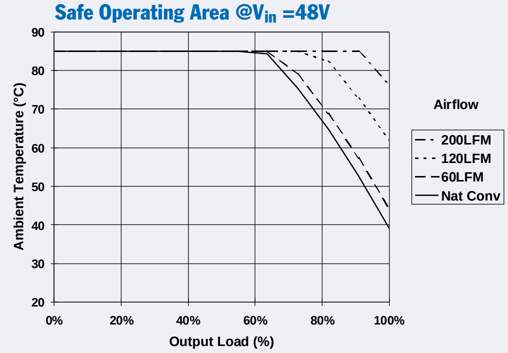
PT4824 Thermal Performance (See Note C)

(Io$_1$ + Io$_2$ + Io$_3$ =12A, represents 100% Load)

Power Dissipation vs Output Load



Safe Operating Area @V_{in} =48V



Note A: *All Characteristic data in the above graphs has been developed from actual products tested at 25°C. This data is considered typical data for the ISR.*
Note B: *Output Load (%) represents the percent drawn from each output of the stated 100% load condition.*
Note C: *SOA curves represent operating conditions at which the internal components are at or below the manufacturer's maximum rated operating temperatures.*

PT4825 Electrical Specifications

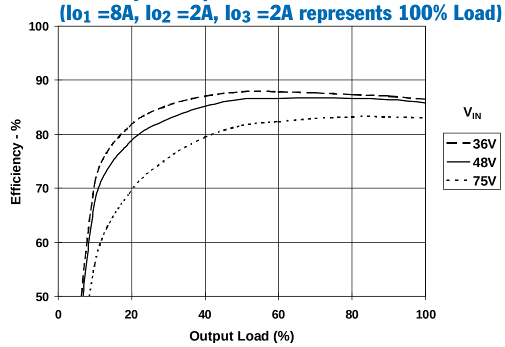
(Unless otherwise stated, the operating conditions are: T_a =25°C, V_{in} =48V, and I_o =0.5$I_o$max)

Characteristics	Symbols	Conditions		PT4825 Min	Typ	Max	Units
Output Current	I_o	Each output	Io_1 (3.3V) Io_2 (1.5V) Io_3 (1.2V)	0.25 (1) 0.1 (1) 0.1 (1)	— — —	8 (2) 6 (2) 6 (2)	A
		Total (Io_1 + Io_2 + Io_3)		—	—	12 (2)	A
Input Voltage Range	V_{in}	Continuous Surge (1 minute)		36 —	— —	75 80	V
Set-Point Voltage	V_o		Vo_1 Vo_2 Vo_3	3.24 1.47 1.17	3.3 1.5 1.2	3.36 1.53 1.23	V
Temperature Variation	Reg_{temp}	–40°C ≤T_a ≤+85°C, I_o =$I_o$min	Vo_1 Vo_2/Vo_3	— —	±0.5 ±0.5	— —	%V_o
Line Regulation	Reg_{line}	All outputs, Over V_{in} range		—	±0.1	±0.5	%V_o
Load Regulation	Reg_{load}	All outputs, 0≤I_o≤$I_o$max		—	±0.1	±0.5	%V_o
Total Output Voltage Variation	ΔV_o tol	Includes set-point, line, load, –40°C≤T_a≤+85°C	Vo_1 Vo_2/Vo_3	— —	— —	±3 (3) ±3 (3)	%V_o
Efficiency	η	Io_1 =6A, Io_2 =2A, Io_3 =2A		—	86	—	%
V_o Ripple/Noise (0 to 20MHz bandwidth)	V_n		Vo_1 Vo_2 Vo_3	— — —	35 25 25	— — —	mV_{pp}
Transient Response	t_{tr} V_{os}	0.1A/µs load step, 50% to 75% $I_o$max V_o over/undershoot		— —	200 3	— —	µSec %V_o
Output Adjust Range	$V_o$adj		Vo_1/Vo_2/Vo_3	—	±10	—	%V_o
Over-Current Threshold	I_{TRIP}	Total, all outputs. Reset with auto-recovery		—	14	—	A
Switching Frequency	f_s	Over V_{in} and I_o ranges		350	400	450	kHz
Under Voltage Lockout	V_{on} V_{off}	V_{in} increasing V_{in} decreasing		— —	35.5 34	— —	V
Turn-On Time	t_{on}	V_{in} =48V step		—	140 (4)	—	ms
Enable Control (pins 1 & 2) High-Level Input Voltage Low-Level Input Voltage	 V_{IH} V_{IL}	Referenced to –V_{in} (pin 4)		 4 –0.2	 — —	 15 (5) 0.8	 V
Low-Level Input Current	I_{IL}			—	1	2	mA
Standby Input Current	I_{in} standby	pins 1 & 2 open circuit		—	1	5	mA
Internal Input Capacitance	C_{int}			—	1.14	—	µF
External Output Capacitance	Co_1 Co_2 Co_3			0 0 0	220 220 220	1,000 (6) 1,000 (6) 1,000 (6)	µF
Primary/Secondary Isolation	V_{iso} C_{iso} R_{iso}			1500 — 10	— 2,200 —	— — —	V pF MΩ

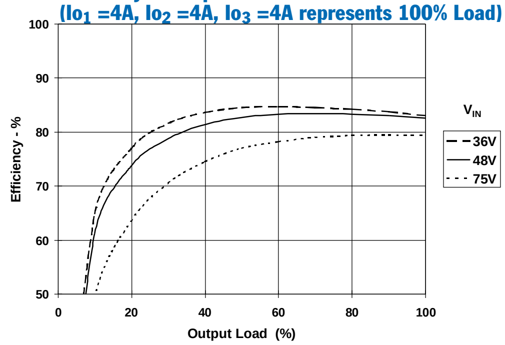
Notes: (1) *The converter will operate down to no load with reduced specifications.*
(2) *The sum-total current from outputs Vo_1, Vo_2, and Vo_3 not to exceed 12ADC.*
(3) *Limits are specified by design.*
(4) *Measured from the application of the input voltage to the instance that all outputs are in regulation.*
(5) *The Enable inputs (pins 1 & 2) have internal pull-ups. Leaving pin 1 open-circuit and connecting pin 2 to –V_{in} allows the the converter to operate when input power is applied. The maximum open-circuit voltage is 4V.*
(6) *Ultra-low ESR capacitors, such as organic or polymer aluminum electrolytic types, may cause instability. Consult the factory before using.*

PT4825 Performance Characteristics (See Notes A, B)

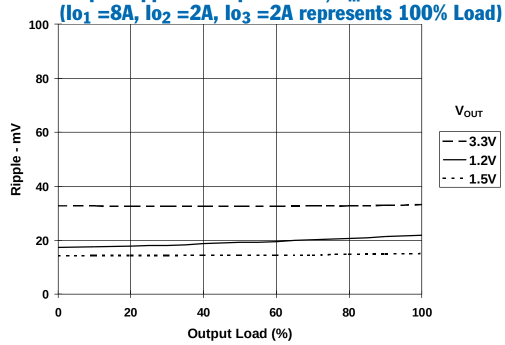
Efficiency vs Output Power
(Io_1 =8A, Io_2 =2A, Io_3 =2A represents 100% Load)



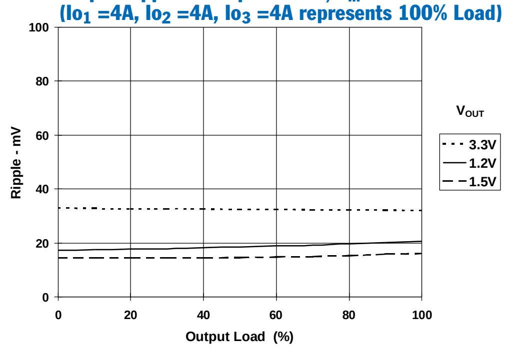
Efficiency vs Output Power
(Io_1 =4A, Io_2 =4A, Io_3 =4A represents 100% Load)



Output Ripple vs Output Power; V_{in} =48V
(Io_1 =8A, Io_2 =2A, Io_3 =2A represents 100% Load)



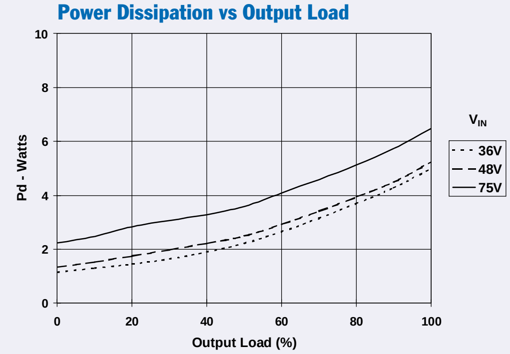
Output Ripple vs Output Power; V_{in} =48V
(Io_1 =4A, Io_2 =4A, Io_3 =4A represents 100% Load)



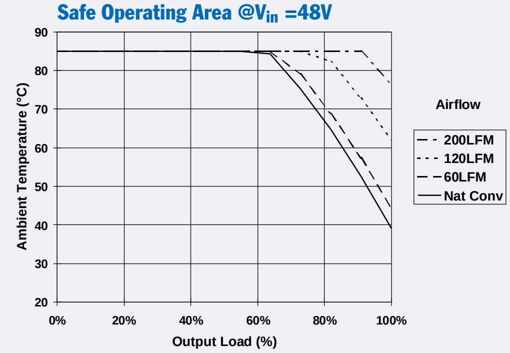
PT4825 Thermal Performance (See Note C)

(Io_1 + Io_2 + Io_3 =12A, represents 100% Load)

Power Dissipation vs Output Load



Safe Operating Area @V_{in} =48V



Note A: *All Characteristic data in the above graphs has been developed from actual products tested at 25°C. This data is considered typical data for the ISR.*
Note B: *Output Load (%) represents the percent drawn from each output of the stated 100% load condition.*
Note C: *SOA curves represent operating conditions at which the internal components are at or below the manufacturer's maximum rated operating temperatures.*

PT4826 Electrical Specifications

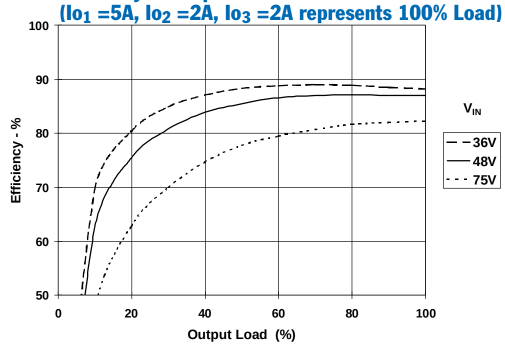
(Unless otherwise stated, the operating conditions are: T_a =25°C, V_{in} =48V, and I_o =0.5$I_o$max)

Characteristics	Symbols	Conditions		PT4826 Min	PT4826 Typ	PT4826 Max	Units
Output Current	I_o	Each output	Io_1 (5.0V) Io_2 (3.3V) Io_3 (1.8V)	0.25 (1) 0.1 (1) 0.1 (1)	— — —	5.0 (2) 5.5 (2) 5.5 (2)	A
		Total (Io_1 + Io_2 + Io_3)		—	—	9 (2)	A
Input Voltage Range	V_{in}	Continuous Surge (1 minute)		36 —	— —	75 80	V
Set-Point Voltage	V_o		Vo_1 Vo_2 Vo_3	4.9 3.24 1.76	5.0 3.3 1.8	5.1 3.36 1.84	V
Temperature Variation	Reg_{temp}	–40°C ≤T_a ≤+85°C, I_o =$I_o$min	Vo_1 Vo_2/Vo_3	— —	±0.5 ±0.5	— —	%V_o
Line Regulation	Reg_{line}	All outputs, Over V_{in} range		—	±0.1	±0.5	%V_o
Load Regulation	Reg_{load}	All outputs, 0≤I_o≤$I_o$max		—	±0.1	±0.5	%V_o
Total Output Voltage Variation	ΔV_o tol	Includes set-point, line, load, –40°C≤T_a ≤+85°C	Vo_1 Vo_2/Vo_3	— —	— —	±3 (3) ±3 (3)	%V_o
Efficiency	η	Io_1 =5A, Io_2 =2A, Io_3 =2A		—	87	—	%
V_o Ripple/Noise (0 to 20MHz bandwidth)	V_n		Vo_1 Vo_2 Vo_3	— — —	40 35 25	— — —	mV_{pp}
Transient Response	t_{tr} V_{os}	0.1A/µs load step, 50% to 75% $I_o$max V_o over/undershoot		— —	200 5	— —	µSec %V_o
Output Adjust Range	$V_o$adj		Vo_1/Vo_2/Vo_3	—	±10	—	%V_o
Over-Current Threshold	I_{TRIP}	Total, all outputs. Reset with auto-recovery		—	11	—	A
Switching Frequency	f_s	Over V_{in} and I_o ranges		350	400	450	kHz
Under Voltage Lockout	V_{on} V_{off}	V_{in} increasing V_{in} decreasing		— —	35.5 34	— —	V
Turn-On Time	t_{on}	V_{in} =48V step		—	140 (4)	—	ms
Enable Control (pins 1 & 2) High-Level Input Voltage Low-Level Input Voltage	 V_{IH} V_{IL}	Referenced to –V_{in} (pin 4)		 4 –0.2	 — —	 15 (5) 0.8	 V
Low-Level Input Current	I_{IL}			—	1	2	mA
Standby Input Current	I_{in} standby	pins 1 & 2 open circuit		—	1	5	mA
Internal Input Capacitance	C_{int}			—	1.14	—	µF
External Output Capacitance	Co_1 Co_2 Co_3			0 0 0	220 220 220	1,000 (6) 1,000 (6) 1,000 (6)	µF
Primary/Secondary Isolation	V_{iso} C_{iso} R_{iso}			1500 — 10	— 2,200 —	— — —	V pF MΩ

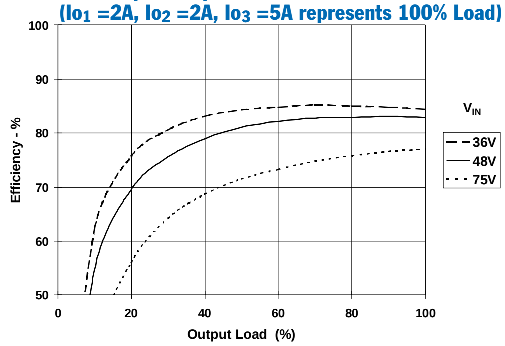
Notes: (1) *The converter will operate down to no load with reduced specifications.*
(2) *The sum-total current from outputs Vo_1, Vo_2, and Vo_3 cannot exceed 9ADC.*
(3) *Limits are specified by design.*
(4) *Measured from the application of the input voltage to the instance that all outputs are in regulation.*
(5) *The Enable inputs (pins 1 & 2) have internal pull-ups. Leaving pin 1 open-circuit and connecting pin 2 to –V_{in} allows the the converter to operate when input power is applied. The maximum open-circuit voltage is 4V.*
(6) *Ultra-low ESR capacitors, such as organic or polymer aluminum electrolytic types, may cause instability. Consult the factory before using.*

PT4826 Performance Characteristics (See Notes A, B)

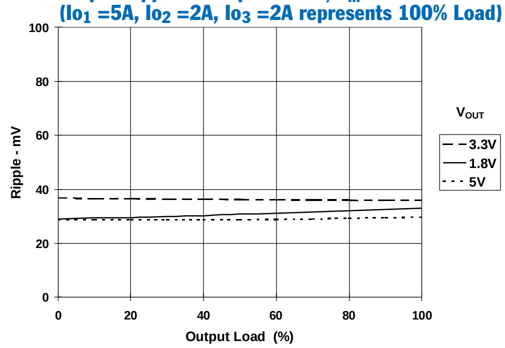
Efficiency vs Output Power
(Io_1 =5A, Io_2 =2A, Io_3 =2A represents 100% Load)



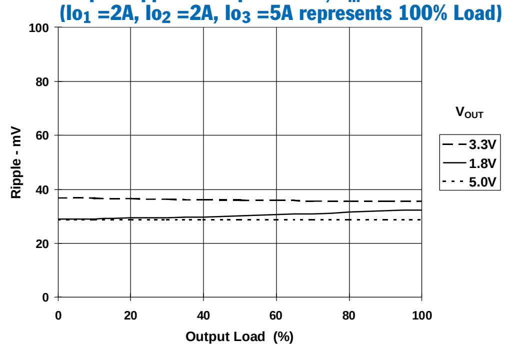
Efficiency vs Output Power
(Io_1 =2A, Io_2 =2A, Io_3 =5A represents 100% Load)



Output Ripple vs Output Power; V_{in} =48V
(Io_1 =5A, Io_2 =2A, Io_3 =2A represents 100% Load)



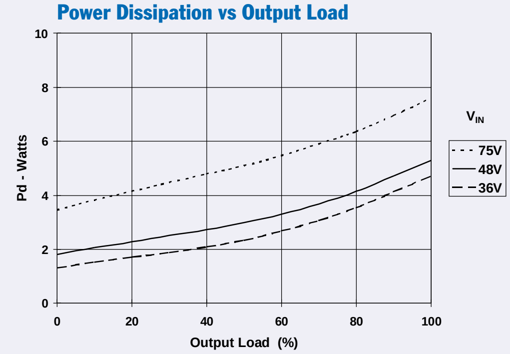
Output Ripple vs Output Power; V_{in} =48V
(Io_1 =2A, Io_2 =2A, Io_3 =5A represents 100% Load)



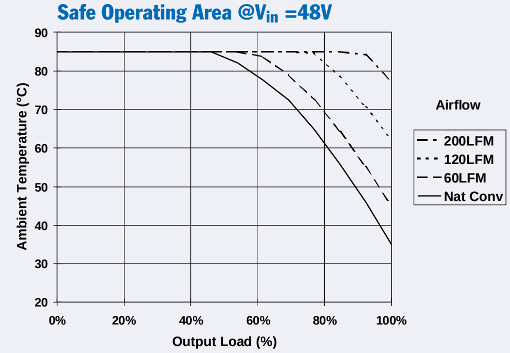
PT4826 Thermal Performance (See Note C)

(Io_1 + Io_2 + Io_3 =9A, represents 100% Load)

Power Dissipation vs Output Load



Safe Operating Area @V_{in} =48V



Note A: *All Characteristic data in the above graphs has been developed from actual products tested at 25°C. This data is considered typical data for the ISR.*
Note B: *Output Load (%) represents the percent drawn from each output of the stated 100% load condition.*
Note C: *SOA curves represent operating conditions at which the internal components are at or below the manufacturer's maximum rated operating temperatures.*

PT4827 Electrical Specifications

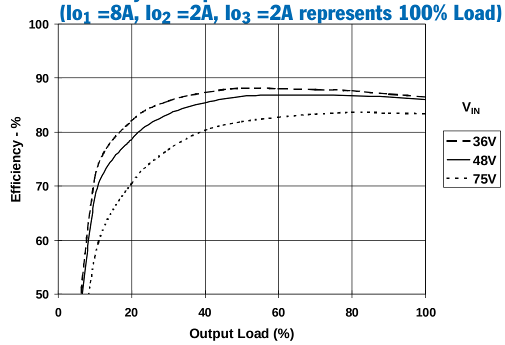
(Unless otherwise stated, the operating conditions are: T_a =25°C, V_{in} =48V, and I_o =0.5$I_o$max)

Characteristics	Symbols	Conditions		PT4827 Min	PT4827 Typ	PT4827 Max	Units
Output Current	I_o	Each output	Io_1 (3.3V) Io_2 (2.5V) Io_3 (1.8V)	0.25 (1) 0.1 (1) 0.1 (1)	— — —	8 (2) 6 (2) 6 (2)	A
		Total (Io_1 + Io_2 + Io_3)		—	—	12 (2)	A
Input Voltage Range	V_{in}	Continuous Surge (1 minute)		36 —	— —	75 80	V
Set-Point Voltage	V_o		Vo_1 Vo_2 Vo_3	3.24 2.45 1.76	3.3 2.5 1.8	3.36 2.55 1.84	V
Temperature Variation	Reg_{temp}	–40°C ≤T_a ≤+85°C, I_o =$I_o$min	Vo_1 Vo_2/Vo_3	— —	±0.5 ±0.5	— —	%V_o
Line Regulation	Reg_{line}	All outputs, Over V_{in} range		—	±0.1	±0.5	%V_o
Load Regulation	Reg_{load}	All outputs, 0≤I_o≤$I_o$max		—	±0.1	±0.5	%V_o
Total Output Voltage Variation	ΔV_o tol	Includes set-point, line, load, –40°C≤T_a≤+85°C	Vo_1 Vo_2/Vo_3	— —	— —	±3 (3) ±3 (3)	%V_o
Efficiency	η	Io_1 =6A, Io_2 =2A, Io_3 =2A		—	86	—	%
V_o Ripple/Noise (0 to 20MHz bandwidth)	V_n		Vo_1 Vo_2 Vo_3	— — —	40 35 25	— — —	mV_{pp}
Transient Response	t_{tr} V_{os}	0.1A/µs load step, 50% to 75% $I_o$max V_o over/undershoot		— —	200 3	— —	µSec %V_o
Output Adjust Range	$V_o$adj		Vo_1/Vo_2/Vo_3	—	±10	—	%V_o
Over-Current Threshold	I_{TRIP}	Total, all outputs. Reset with auto-recovery		—	14	—	A
Switching Frequency	f_s	Over V_{in} and I_o ranges		350	400	450	kHz
Under Voltage Lockout	V_{on} V_{off}	V_{in} increasing V_{in} decreasing		— —	35.5 34	— —	V
Turn-On Time	t_{on}	V_{in} =48V step		—	140 (4)	—	ms
Enable Control (pins 1 & 2) High-Level Input Voltage Low-Level Input Voltage	 V_{IH} V_{IL}	Referenced to $-V_{in}$ (pin 4)		 4 –0.2	 — —	 15 (5) 0.8	V
Low-Level Input Current	I_{IL}			—	1	2	mA
Standby Input Current	I_{in} standby	pins 1 & 2 open circuit		—	1	5	mA
Internal Input Capacitance	C_{int}			—	1.14	—	µF
External Output Capacitance	Co_1 Co_2 Co_3			0 0 0	220 220 220	1,000 (6) 1,000 (6) 1,000 (6)	µF
Primary/Secondary Isolation	V_{iso} C_{iso} R_{iso}			1500 — 10	— 2,200 —	— — —	V pF MΩ

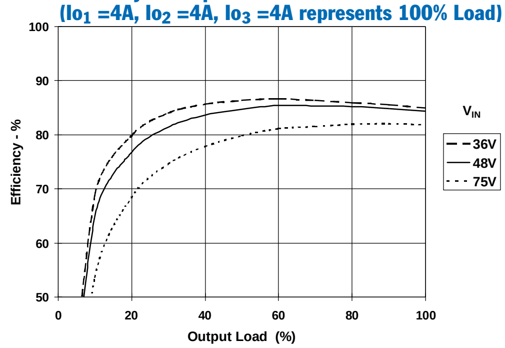
Notes: (1) *The converter will operate down to no load with reduced specifications.*
(2) *The sum-total current from outputs Vo_1, Vo_2, and Vo_3 cannot exceed 12ADC.*
(3) *Limits are specified by design.*
(4) *Measured from the application of the input voltage to the instance that all outputs are in regulation.*
(5) *The Enable inputs (pins 1 & 2) have internal pull-ups. Leaving pin 1 open-circuit and connecting pin 2 to $-V_{in}$ allows the the converter to operate when input power is applied. The maximum open-circuit voltage is 4V.*
(6) *Ultra-low ESR capacitors, such as organic or polymer aluminum electrolytic types, may cause instability. Consult the factory before using.*

PT4827 Performance Characteristics (See Notes A, B)

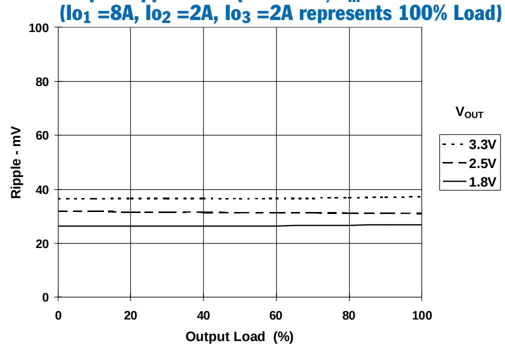
Efficiency vs Output Power
(Io_1 =8A, Io_2 =2A, Io_3 =2A represents 100% Load)



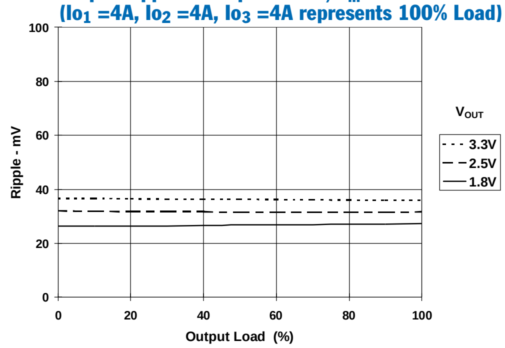
Efficiency vs Output Power
(Io_1 =4A, Io_2 =4A, Io_3 =4A represents 100% Load)



Output Ripple vs Output Power; V_{in} =48V
(Io_1 =8A, Io_2 =2A, Io_3 =2A represents 100% Load)



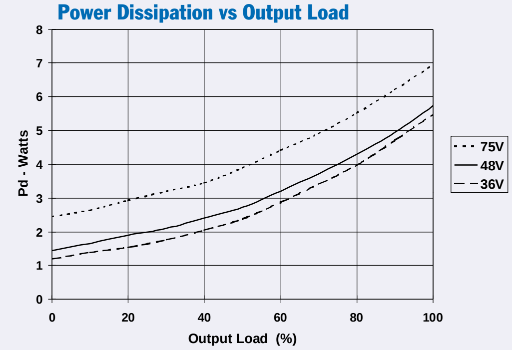
Output Ripple vs Output Power; V_{in} =48V
(Io_1 =4A, Io_2 =4A, Io_3 =4A represents 100% Load)



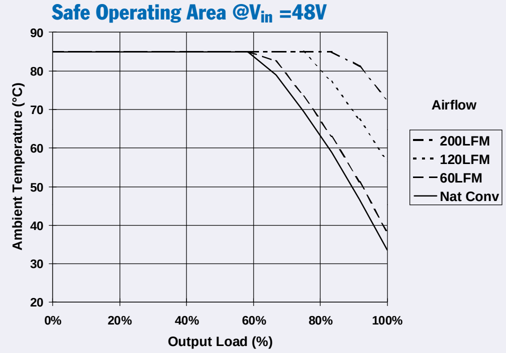
PT4827 Thermal Performance (See Note C)

($Io_1 + Io_2 + Io_3$ =12A, represents 100% Load)

Power Dissipation vs Output Load



Safe Operating Area @V_{in} =48V



Note A: *All Characteristic data in the above graphs has been developed from actual products tested at 25°C. This data is considered typical data for the ISR.*
Note B: *Output Load (%) represents the percent drawn from each output of the stated 100% load condition.*
Note C: *SOA curves represent operating conditions at which the internal components are at or below the manufacturer's maximum rated operating temperatures.*

PT4828 Electrical Specifications

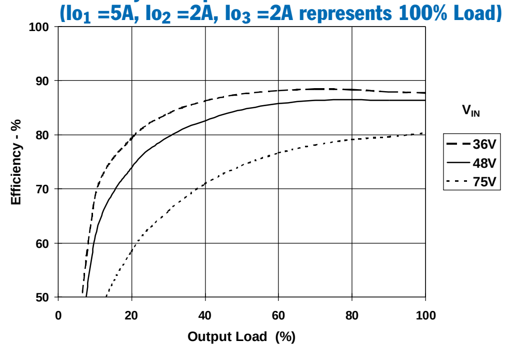
(Unless otherwise stated, the operating conditions are: T_a =25°C, V_{in} =48V, and I_o =0.5$I_o$max)

Characteristics	Symbols	Conditions		PT4828 Min	Typ	Max	Units
Output Current	I_o	Each output	Io_1 (5.0V) Io_2 (2.5V) Io_3 (1.5V)	0.25 (1) 0.1 (1) 0.1 (1)	— — —	5.0 (2) 5.5 (2) 5.5 (2)	A
		Total (Io_1 + Io_2 + Io_3)		—	—	9 (2)	A
Input Voltage Range	V_{in}	Continuous Surge (1 minute)		36 —	— —	75 80	V
Set-Point Voltage	V_o		Vo_1 Vo_2 Vo_3	4.9 2.45 1.47	5.0 2.5 1.5	5.1 2.55 1.53	V
Temperature Variation	Reg_{temp}	–40°C ≤T_a ≤+85°C, I_o =$I_o$min	Vo_1 Vo_2/Vo_3	— —	±0.5 ±0.5	— —	%V_o
Line Regulation	Reg_{line}	All outputs, Over V_{in} range		—	±0.1	±0.5	%V_o
Load Regulation	Reg_{load}	All outputs, 0≤I_o≤$I_o$max		—	±0.1	±0.5	%V_o
Total Output Voltage Variation	ΔV_o tol	Includes set-point, line, load, –40°C≤T_a≤+85°C	Vo_1 Vo_2/Vo_3	— —	— —	±3 (3) ±3 (3)	%V_o
Efficiency	η	Io_1 =5A, Io_2 =2A, Io_3 =2A		—	86.5	—	%
V_o Ripple/Noise (0 to 20MHz bandwidth)	V_n		Vo_1 Vo_2 Vo_3	— — —	30 30 25	— — —	mV_{pp}
Transient Response	t_{tr} V_{os}	0.1A/µs load step, 50% to 75% $I_o$max V_o over/undershoot		— —	200 5	— —	µSec %V_o
Output Adjust Range	$V_o$adj		Vo_1/Vo_2/Vo_3	—	±10	—	%V_o
Over-Current Threshold	I_{TRIP}	Total, all outputs. Reset with auto-recovery		—	11	—	A
Switching Frequency	f_s	Over V_{in} and I_o ranges		350	400	450	kHz
Under Voltage Lockout	V_{on} V_{off}	V_{in} increasing V_{in} decreasing		— —	35.5 34	— —	V
Turn-On Time	t_{on}	V_{in} =48V step		—	140 (4)	—	ms
Enable Control (pins 1 & 2) High-Level Input Voltage Low-Level Input Voltage	 V_{IH} V_{IL}	Referenced to $-V_{in}$ (pin 4)		 4 –0.2	 — —	 15 (5) 0.8	 V
Low-Level Input Current	I_{IL}			—	1	2	mA
Standby Input Current	I_{in} standby	pins 1 & 2 open circuit		—	1	5	mA
Internal Input Capacitance	C_{int}			—	1.14	—	µF
External Output Capacitance	Co_1 Co_2 Co_3			0 0 0	220 220 220	1,000 (6) 1,000 (6) 1,000 (6)	µF
Primary/Secondary Isolation	V_{iso} C_{iso} R_{iso}			1500 — 10	— 2,200 —	— — —	V pF MΩ

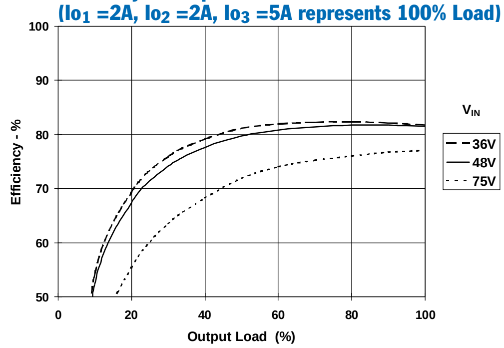
Notes: (1) *The converter will operate down to no load with reduced specifications.*
(2) *The sum-total current from outputs Vo_2, and Vo_3 cannot exceed 9ADC.*
(3) *Limits are specified by design.*
(4) *Measured from the application of the input voltage to the instance that all outputs are in regulation.*
(5) *The Enable inputs (pins 1 & 2) have internal pull-ups. Leaving pin 1 open-circuit and connecting pin 2 to $-V_{in}$ allows the the converter to operate when input power is applied. The maximum open-circuit voltage is 4V.*
(6) *Ultra-low ESR capacitors, such as organic or polymer aluminum electrolytic types, may cause instability. Consult the factory before using.*

PT4828 Performance Characteristics (See Notes A, B)

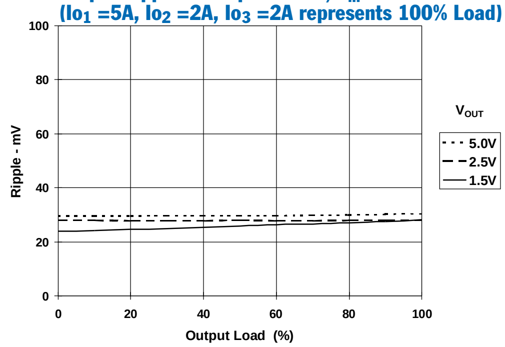
Efficiency vs Output Power (Io$_1$ =5A, Io$_2$ =2A, Io$_3$ =2A represents 100% Load)



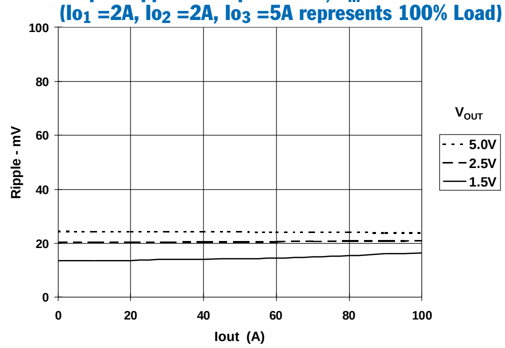
Efficiency vs Output Power (Io$_1$ =2A, Io$_2$ =2A, Io$_3$ =5A represents 100% Load)



Output Ripple vs Output Power; V$_{in}$ =48V (Io$_1$ =5A, Io$_2$ =2A, Io$_3$ =2A represents 100% Load)



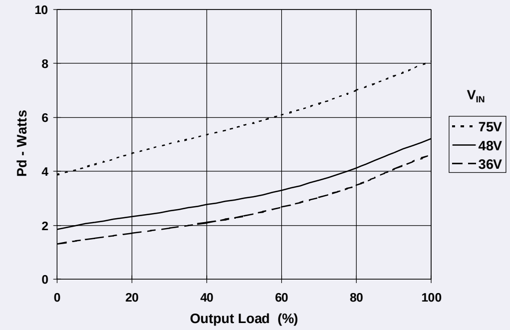
Output Ripple vs Output Power; V$_{in}$ =48V (Io$_1$ =2A, Io$_2$ =2A, Io$_3$ =5A represents 100% Load)



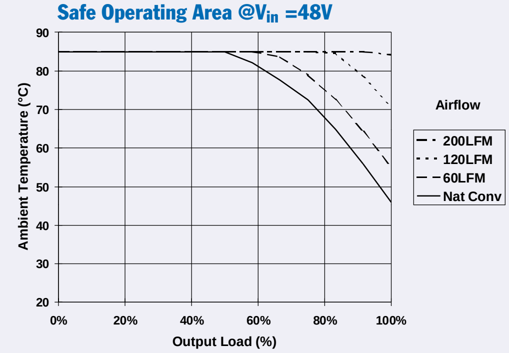
PT4828 Thermal Performance (See Note C)

(Io$_1$ + Io$_2$ + Io$_3$ =9A ,represents 100% Load)

Power Dissipation vs Output Load



Safe Operating Area @V$_{in}$ =48V



Note A: *All Characteristic data in the above graphs has been developed from actual products tested at 25°C. This data is considered typical data for the ISR.*
Note B: *Output Load (%) represents the percent drawn from each output of the stated 100% load condition.*
Note C: *SOA curves represent operating conditions at which the internal components are at or below the manufacturer's maximum rated operating temperatures.*

PT4829 Electrical Specifications

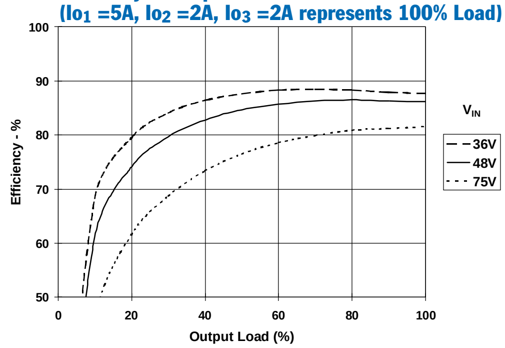
(Unless otherwise stated, the operating conditions are: T_a =25°C, V_{in} =48V, and I_o =0.5$I_o$max)

Characteristics	Symbols	Conditions	PT4829 Min	Typ	Max	Units
Output Current	I_o	Each output Io_1 (5.0V) Io_2 (1.8V) Io_3 (1.5V)	0.25 (1) 0.1 (1) 0.1 (1)	— — —	5.0 (2) 5.5 (2) 5.5 (2)	A
		Total (Io_1 + Io_2 + Io_3)	—	—	9 (2)	A
Input Voltage Range	V_{in}	Continuous Surge (1 minute)	36 —	— —	75 80	V
Set-Point Voltage	V_o	Vo_1 Vo_2 Vo_3	4.9 1.76 1.47	5.0 1.8 1.5	5.1 1.84 1.53	V
Temperature Variation	Reg_{temp}	–40°C ≤T_a ≤+85°C, I_o =$I_o$min Vo_1 Vo_2/Vo_3	— —	±0.5 ±0.5	— —	%V_o
Line Regulation	Reg_{line}	All outputs, Over V_{in} range	—	±0.1	±0.5	%V_o
Load Regulation	Reg_{load}	All outputs, 0≤I_o≤$I_o$max	—	±0.1	±0.5	%V_o
Total Output Voltage Variation	ΔV_o tol	Includes set-point, line, load, Vo_1 –40°C≤T_a≤+85°C Vo_2/Vo_3	— —	— —	±3 (3) ±3 (3)	%V_o
Efficiency	η	Io_1 =5A, Io_2 =2A, Io_3 =2A	—	86.2	—	%
V_o Ripple/Noise (0 to 20MHz bandwidth)	V_n	Vo_1 Vo_2 Vo_3	— — —	35 25 25	— — —	mV_{pp}
Transient Response	t_{tr} V_{os}	0.1A/µs load step, 50% to 75% $I_o$max V_o over/undershoot	— —	200 5	— —	µSec %V_o
Output Adjust Range	$V_o$adj	Vo_1/Vo_2/Vo_3	—	±10	—	%V_o
Over-Current Threshold	I_{TRIP}	Total, all outputs. Reset with auto-recovery	—	11	—	A
Switching Frequency	f_s	Over V_{in} and I_o ranges	350	400	450	kHz
Under Voltage Lockout	V_{on} V_{off}	V_{in} increasing V_{in} decreasing	— —	35.5 34	— —	V
Turn-On Time	t_{on}	V_{in} =48V step	—	140 (4)	—	ms
Enable Control (pins 1 & 2) High-Level Input Voltage Low-Level Input Voltage	 V_{IH} V_{IL}	Referenced to $-V_{in}$ (pin 4)	 4 –0.2	 — —	 15 (5) 0.8	 V
Low-Level Input Current	I_{IL}		—	1	2	mA
Standby Input Current	I_{in} standby	pins 1 & 2 open circuit	—	1	5	mA
Internal Input Capacitance	C_{int}		—	1.14	—	µF
External Output Capacitance	Co_1 Co_2 Co_3		0 0 0	220 220 220	1,000 (6) 1,000 (6) 1,000 (6)	µF
Primary/Secondary Isolation	V_{iso} C_{iso} R_{iso}		1500 — 10	— 2,200 —	— — —	V pF MΩ

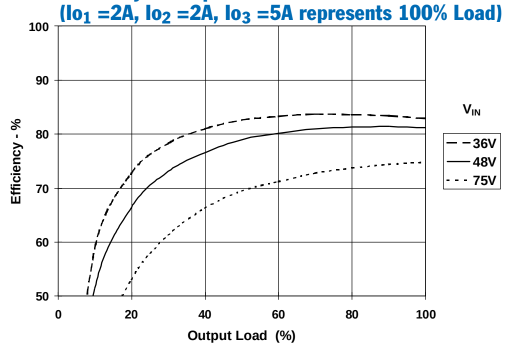
Notes: (1) *The converter will operate down to no load with reduced specifications.*
(2) *The sum-total current from outputs Vo_2, and Vo_3 cannot exceed 9ADC.*
(3) *Limits are specified by design.*
(4) *Measured from the application of the input voltage to the instance that all outputs are in regulation.*
(5) *The Enable inputs (pins 1 & 2) have internal pull-ups. Leaving pin 1 open-circuit and connecting pin 2 to $-V_{in}$ allows the the converter to operate when input power is applied. The maximum open-circuit voltage is 4V.*
(6) *Ultra-low ESR capacitors, such as organic or polymer aluminum electrolytic types, may cause instability. Consult the factory before using.*

PT4829 Performance Characteristics (See Notes A, B)

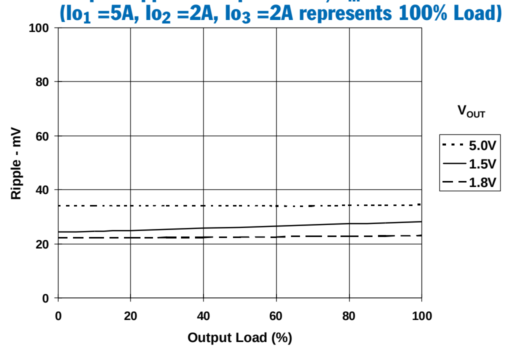
Efficiency vs Output Power
(Io_1 =5A, Io_2 =2A, Io_3 =2A represents 100% Load)



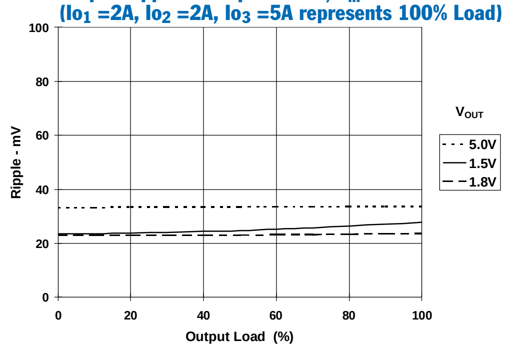
Efficiency vs Output Power
(Io_1 =2A, Io_2 =2A, Io_3 =5A represents 100% Load)



Output Ripple vs Output Power; V_{in} =48V
(Io_1 =5A, Io_2 =2A, Io_3 =2A represents 100% Load)



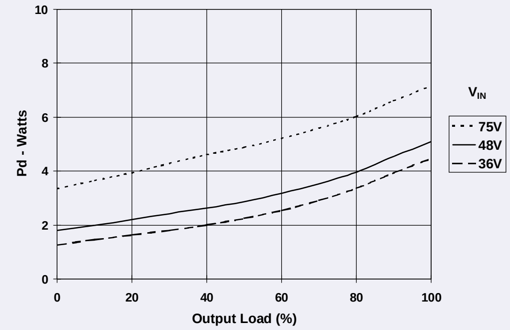
Output Ripple vs Output Power; V_{in} =48V
(Io_1 =2A, Io_2 =2A, Io_3 =5A represents 100% Load)



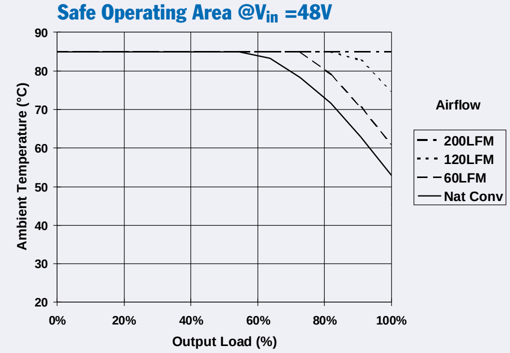
PT4829 Thermal Performance (See Note C)

(Io_1 + Io_2 + Io_3 =9A, represents 100% Load)

Power Dissipation vs Output Power



Safe Operating Area @V_{in} =48V



Note A: *All Characteristic data in the above graphs has been developed from actual products tested at 25°C. This data is considered typical data for the ISR.*
Note B: *Output Load (%) represents the percent drawn from each output of the stated 100% load condition.*
Note C: *SOA curves represent operating conditions at which the internal components are at or below the manufacturer's maximum rated operating temperatures.*

PT4831 Electrical Specifications

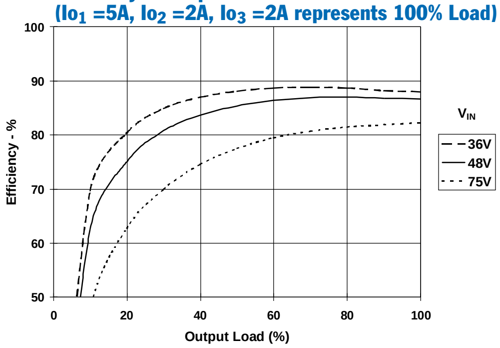
(Unless otherwise stated, the operating conditions are: T_a =25°C, V_{in} =48V, and I_o =0.5$I_o$max)

Characteristics	Symbols	Conditions		PT4831 Min	Typ	Max	Units
Output Current	I_o	Each output	Io_1 (5.0V) Io_2 (3.3V) Io_3 (1.5V)	0.25 (1) 0.1 (1) 0.1 (1)	— — —	5.0 (2) 5.5 (2) 5.5 (2)	A
		Total (Io_1 + Io_2 + Io_3)		—	—	9 (2)	A
Input Voltage Range	V_{in}	Continuous Surge (1 minute)		36 —	— —	75 80	V
Set-Point Voltage	V_o		Vo_1 Vo_2 Vo_3	4.9 3.24 1.47	5.0 3.3 1.5	5.1 3.36 1.53	V
Temperature Variation	Reg_{temp}	–40°C ≤T_a ≤+85°C, I_o =$I_o$min	Vo_1 Vo_2/Vo_3	— —	±0.5 ±0.5	— —	%V_o
Line Regulation	Reg_{line}	All outputs, Over V_{in} range		—	±0.1	±0.5	%V_o
Load Regulation	Reg_{load}	All outputs, 0≤I_o≤$I_o$max		—	±0.1	±0.5	%V_o
Total Output Voltage Variation	ΔV_o tol	Includes set-point, line, load, –40°C≤T_a≤+85°C	Vo_1 Vo_2/Vo_3	— —	— —	±3 (3) ±3 (3)	%V_o
Efficiency	η	Io_1 =5A, Io_2 =2A, Io_3 =2A		—	87	—	%
V_o Ripple/Noise (0 to 20MHz bandwidth)	V_n		Vo_1 Vo_2 Vo_3	— — —	40 35 25	— — —	mV_{pp}
Transient Response	t_{tr} V_{os}	0.1A/µs load step, 50% to 75% $I_o$max V_o over/undershoot		— —	200 5	— —	µSec %V_o
Output Adjust Range	$V_o$adj		Vo_1/Vo_2/Vo_3	—	±10	—	%V_o
Over-Current Threshold	I_{TRIP}	Total, all outputs. Reset with auto-recovery		—	11	—	A
Switching Frequency	f_s	Over V_{in} and I_o ranges		350	400	450	kHz
Under Voltage Lockout	V_{on} V_{off}	V_{in} increasing V_{in} decreasing		— —	35.5 34	— —	V
Turn-On Time	t_{on}	V_{in} =48V step		—	140 (4)	—	ms
Enable Control (pins 1 & 2) High-Level Input Voltage Low-Level Input Voltage	 V_{IH} V_{IL}	Referenced to $-V_{in}$ (pin 4)		 4 –0.2	 — —	 15 (5) 0.8	 V
Low-Level Input Current	I_{IL}			—	1	2	mA
Standby Input Current	I_{in} standby	pins 1 & 2 open circuit		—	1	5	mA
Internal Input Capacitance	C_{int}			—	1.14	—	µF
External Output Capacitance	Co_1 Co_2 Co_3			0 0 0	220 220 220	1,000 (6) 1,000 (6) 1,000 (6)	µF
Primary/Secondary Isolation	V_{iso} C_{iso} R_{iso}			1500 — 10	— 2,200 —	— — —	V pF MΩ

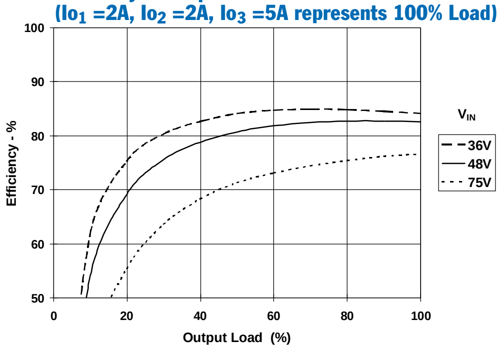
Notes: (1) *The converter will operate down to no load with reduced specifications.*
(2) *The sum-total current from outputs Vo_1, Vo_2, and Vo_3 cannot exceed 9ADC.*
(3) *Limits are specified by design.*
(4) *Measured from the application of the input voltage to the instance that all outputs are in regulation.*
(5) *The Enable inputs (pins 1 & 2) have internal pull-ups. Leaving pin 1 open-circuit and connecting pin 2 to $-V_{in}$ allows the the converter to operate when input power is applied. The maximum open-circuit voltage is 4V.*
(6) *Ultra-low ESR capacitors, such as organic or polymer aluminum electrolytic types, may cause instability. Consult the factory before using.*

PT4831 Performance Characteristics (See Notes A, B)

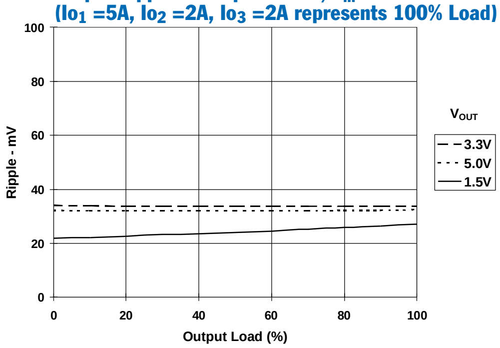
Efficiency vs Output Power
(Io_1 =5A, Io_2 =2A, Io_3 =2A represents 100% Load)



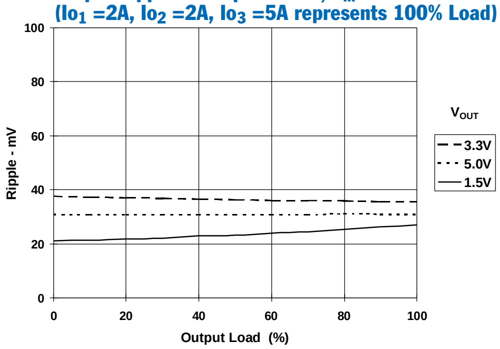
Efficiency vs Output Power
(Io_1 =2A, Io_2 =2A, Io_3 =5A represents 100% Load)



Output Ripple vs Output Power; V_{in} =48V
(Io_1 =5A, Io_2 =2A, Io_3 =2A represents 100% Load)



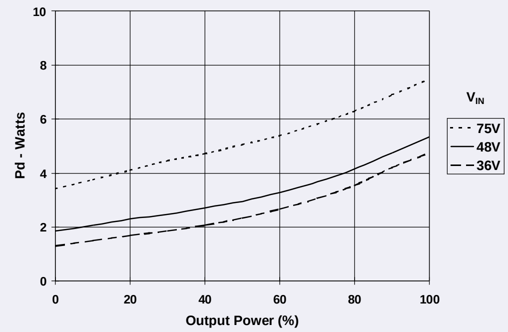
Output Ripple vs Output Power; V_{in} =48V
(Io_1 =2A, Io_2 =2A, Io_3 =5A represents 100% Load)



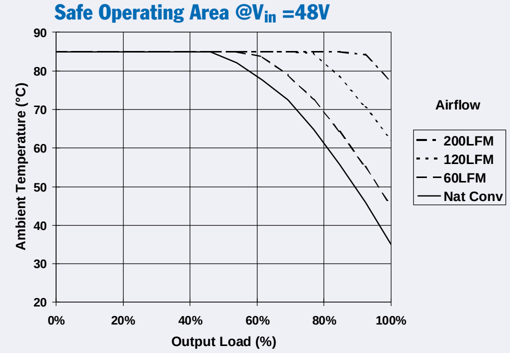
PT4831 Thermal Performance (See Note C)

(Io_1 + Io_2 + Io_3 =9A, represents 100% Load)

Power Dissipation vs Output Power



Safe Operating Area @V_{in} =48V



Note A: *All Characteristic data in the above graphs has been developed from actual products tested at 25°C. This data is considered typical data for the ISR.*
Note B: *Output Load (%) represents the percent drawn from each output of the stated 100% load condition.*
Note C: *SOA curves represent operating conditions at which the internal components are at or below the manufacturer's maximum rated operating temperatures.*

PT4832 Electrical Specifications

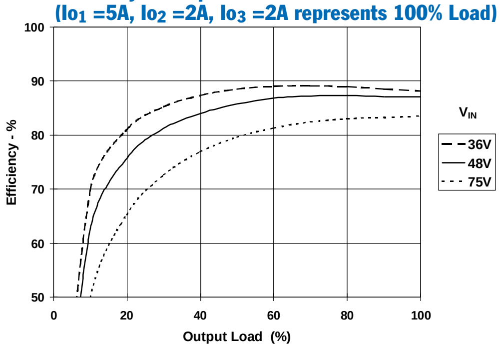
(Unless otherwise stated, the operating conditions are: T_a =25°C, V_{in} =48V, and I_o =0.5$I_o$max)

				PT4832		
Characteristics	**Symbols**	**Conditions**	**Min**	**Typ**	**Max**	**Units**
Output Current	I_o	Each output — Io_1 (5.0V) Io_2 (3.3V) Io_3 (2.5V)	0.25 (1) 0.1 (1) 0.1 (1)	— — —	5.0 (2) 5.5 (2) 5.5 (2)	A
		Total (Io_1 + Io_2 + Io_3)	—	—	9 (2)	A
Input Voltage Range	V_{in}	Continuous Surge (1 minute)	36 —	— —	75 80	V
Set-Point Voltage	V_o	Vo_1 Vo_2 Vo_3	4.9 3.24 2.45	5.0 3.3 2.5	5.1 3.36 2.55	V
Temperature Variation	Reg_{temp}	–40°C ≤T_a ≤+85°C, I_o =$I_o$min — Vo_1 Vo_2/Vo_3	— —	±0.5 ±0.5	— —	%V_o
Line Regulation	Reg_{line}	All outputs, Over V_{in} range	—	±0.1	±0.5	%V_o
Load Regulation	Reg_{load}	All outputs, 0≤I_o≤$I_o$max	—	±0.1	±0.5	%V_o
Total Output Voltage Variation	ΔV_o tol	Includes set-point, line, load, — Vo_1 –40°C≤T_a≤+85°C — Vo_2/Vo_3	— —	— —	±3 (3) ±3 (3)	%V_o
Efficiency	η	Io_1 =5A, Io_2 =2A, Io_3 =2A	—	86.7	—	%
V_o Ripple/Noise (0 to 20MHz bandwidth)	V_n	Vo_1 Vo_2 Vo_3	— — —	30 25 25	— — —	mV_{pp}
Transient Response	t_{tr} V_{os}	0.1A/µs load step, 50% to 75% $I_o$max V_o over/undershoot	— —	200 5	— —	µSec %V_o
Output Adjust Range	$V_o$adj	Vo_1/Vo_2/Vo_3	—	±10	—	%V_o
Over-Current Threshold	I_{TRIP}	Total, all outputs. Reset with auto-recovery	—	11	—	A
Switching Frequency	f_s	Over V_{in} and I_o ranges	350	400	450	kHz
Under Voltage Lockout	V_{on} V_{off}	V_{in} increasing V_{in} decreasing	— —	35.5 34	— —	V
Turn-On Time	t_{on}	V_{in} =48V step	—	140 (4)	—	ms
Enable Control (pins 1 & 2) High-Level Input Voltage Low-Level Input Voltage	 V_{IH} V_{IL}	Referenced to –V_{in} (pin 4)	 4 –0.2	 — —	 15 (5) 0.8	 V
Low-Level Input Current	I_{IL}		—	1	2	mA
Standby Input Current	I_{in} standby	pins 1 & 2 open circuit	—	1	5	mA
Internal Input Capacitance	C_{int}		—	1.14	—	µF
External Output Capacitance	Co_1 Co_2 Co_3		0 0 0	220 220 220	1,000 (6) 1,000 (6) 1,000 (6)	µF
Primary/Secondary Isolation	V_{iso} C_{iso} R_{iso}		1500 — 10	— 2,200 —	— — —	V pF MΩ

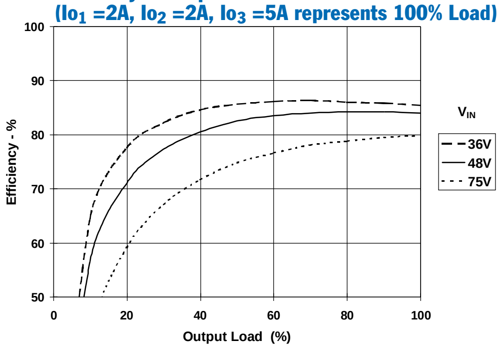
Notes: (1) *The converter will operate down to no load with reduced specifications.*
(2) *The sum-total current from outputs Vo_2, and Vo_3 cannot exceed 9ADC.*
(3) *Limits are specified by design.*
(4) *Measured from the application of the input voltage to the instance that all outputs are in regulation.*
(5) *The Enable inputs (pins 1 & 2) have internal pull-ups. Leaving pin 1 open-circuit and connecting pin 2 to –V_{in} allows the the converter to operate when input power is applied. The maximum open-circuit voltage is 4V.*
(6) *Ultra-low ESR capacitors, such as organic or polymer aluminum electrolytic types, may cause instability. Consult the factory before using.*

PT4832 Performance Characteristics (See Notes A, B)

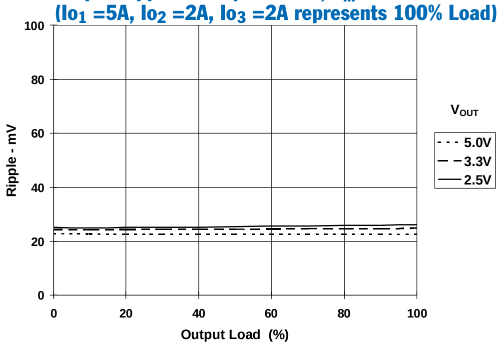
Efficiency vs Output Power
(Io_1 =5A, Io_2 =2A, Io_3 =2A represents 100% Load)



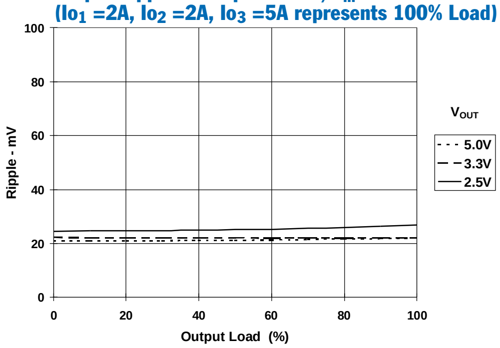
Efficiency vs Output Power
(Io_1 =2A, Io_2 =2A, Io_3 =5A represents 100% Load)



Output Ripple vs Output Power; V_{in} =48V
(Io_1 =5A, Io_2 =2A, Io_3 =2A represents 100% Load)



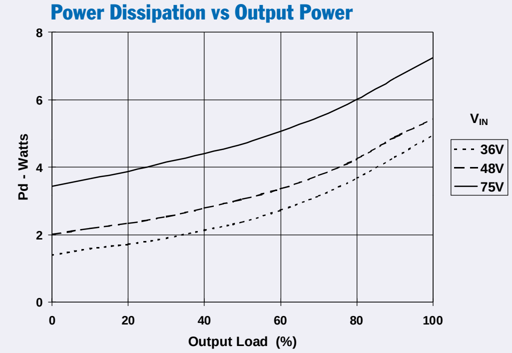
Output Ripple vs Output Power; V_{in} =48V
(Io_1 =2A, Io_2 =2A, Io_3 =5A represents 100% Load)



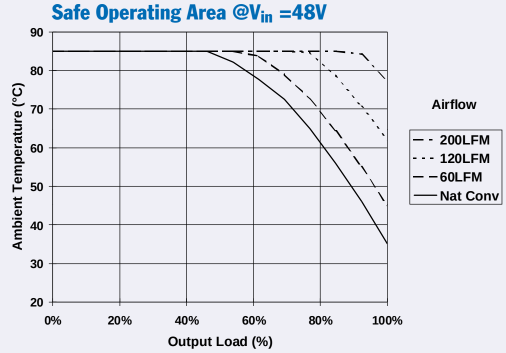
PT4832 Thermal Performance (See Note C)

(Io_1 + Io_2 + Io_3 =9A, represents 100% Load)

Power Dissipation vs Output Power



Safe Operating Area @V_{in} =48V



Note A: *All Characteristic data in the above graphs has been developed from actual products tested at 25°C. This data is considered typical data for the ISR.*
Note B: *Output Load (%) represents the percent drawn from each output of the stated 100% load condition.*
Note C: *SOA curves represent operating conditions at which the internal components are at or below the manufacturer's maximum rated operating temperatures.*

PT4833 Electrical Specifications

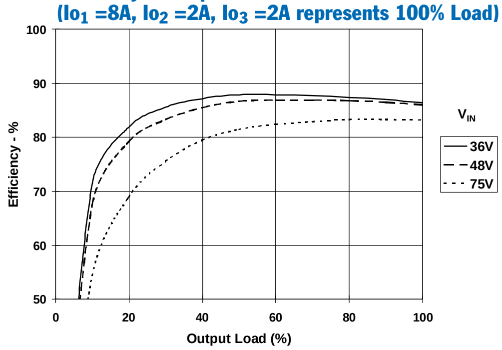
(Unless otherwise stated, the operating conditions are: T_a =25°C, V_{in} =48V, and I_o =0.5$I_o$max)

Characteristics	Symbols	Conditions		PT4833 Min	Typ	Max	Units
Output Current	I_o	Each output	Io_1 (3.3V)	0.25 (1)	—	8 (2)	A
			Io_2 (2.0V)	0.1 (1)	—	6 (2)	
			Io_3 (1.5V)	0.1 (1)	—	6 (2)	
		Total (Io_1 + Io_2 + Io_3)		—	—	12 (2)	A
Input Voltage Range	V_{in}	Continuous		36	—	75	V
		Surge (1 minute)		—	—	80	
Set-Point Voltage	V_o		Vo_1	3.24	3.3	3.36	V
			Vo_2	1.96	2.0	2.04	
			Vo_3	1.47	1.5	1.53	
Temperature Variation	Reg_{temp}	–40°C ≤T_a ≤+85°C, I_o =$I_o$min	Vo_1	—	±0.5	—	%V_o
			Vo_2/Vo_3	—	±0.5	—	
Line Regulation	Reg_{line}	All outputs, Over V_{in} range		—	±0.1	±0.5	%V_o
Load Regulation	Reg_{load}	All outputs, 0≤I_o≤$I_o$max		—	±0.1	±0.5	%V_o
Total Output Voltage Variation	ΔV_o tol	Includes set-point, line, load,	Vo_1	—	—	±3 (3)	%V_o
		–40°C≤T_a≤+85°C	Vo_2/Vo_3	—	—	±3 (3)	
Efficiency	η	Io_1 =6A, Io_2 =2A, Io_3 =2A		—	86	—	%
V_o Ripple/Noise (0 to 20MHz bandwidth)	V_n		Vo_1	—	40	—	mV_{pp}
			Vo_2	—	25	—	
			Vo_3	—	25	—	
Transient Response	t_{tr}	0.1A/µs load step, 50% to 75% $I_o$max		—	200	—	µSec
	V_{os}	V_o over/undershoot		—	3	—	%V_o
Output Adjust Range	$V_o$adj		Vo_1/Vo_2/Vo_3	—	±10	—	%V_o
Over-Current Threshold	I_{TRIP}	Total, all outputs. Reset with auto-recovery		—	14	—	A
Switching Frequency	f_s	Over V_{in} and I_o ranges		350	400	450	kHz
Under Voltage Lockout	V_{on}	V_{in} increasing		—	35.5	—	V
	V_{off}	V_{in} decreasing		—	34	—	
Turn-On Time	t_{on}	V_{in} =48V step		—	140 (4)	—	ms
Enable Control (pins 1 & 2)		Referenced to $-V_{in}$ (pin 4)					
High-Level Input Voltage	V_{IH}			4	—	15 (5)	V
Low-Level Input Voltage	V_{IL}			–0.2	—	0.8	
Low-Level Input Current	I_{IL}			—	1	2	mA
Standby Input Current	I_{in} standby	pins 1 & 2 open circuit		—	1	5	mA
Internal Input Capacitance	C_{int}			—	1.14	—	µF
External Output Capacitance	Co_1			0	220	1,000 (6)	µF
	Co_2			0	220	1,000 (6)	
	Co_3			0	220	1,000 (6)	
Primary/Secondary Isolation	V_{iso}			1500	—	—	V
	C_{iso}			—	2,200	—	pF
	R_{iso}			10	—	—	MΩ

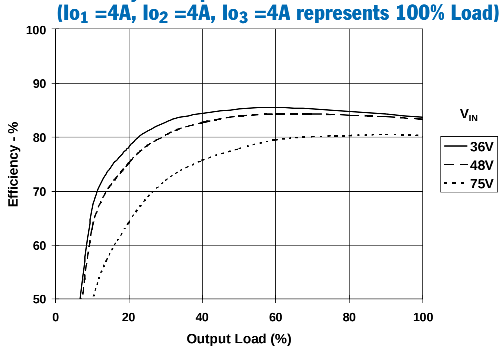
Notes: (1) *The converter will operate down to no load with reduced specifications.*
(2) *The sum-total current from outputs Vo_1, Vo_2, and Vo_3 cannot exceed 12ADC.*
(3) *Limits are specified by design.*
(4) *Measured from the application of the input voltage to the instance that all outputs are in regulation.*
(5) *The Enable inputs (pins 1 & 2) have internal pull-ups. Leaving pin 1 open-circuit and connecting pin 2 to $-V_{in}$ allows the the converter to operate when input power is applied. The maximum open-circuit voltage is 4V.*
(6) *Ultra-low ESR capacitors, such as organic or polymer aluminum electrolytic types, may cause instability. Consult the factory before using.*

PT4833 Performance Characteristics (See Note A, B)

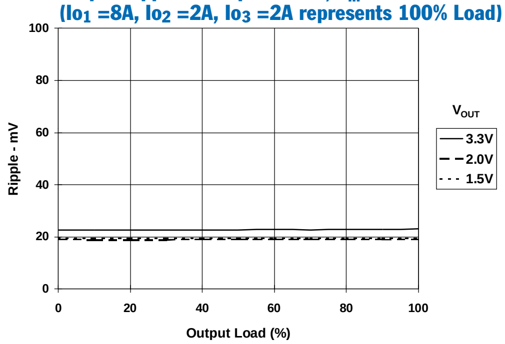
Efficiency vs Output Power (Io$_1$ =8A, Io$_2$ =2A, Io$_3$ =2A represents 100% Load)



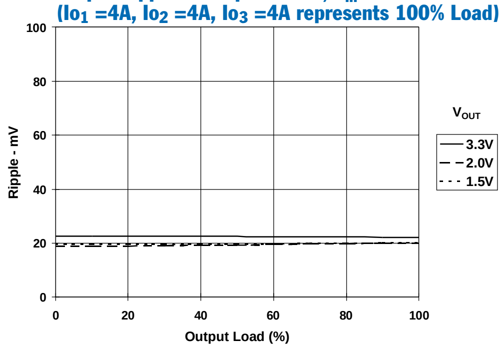
Efficiency vs Output Power (Io$_1$ =4A, Io$_2$ =4A, Io$_3$ =4A represents 100% Load)



Output Ripple vs Output Power; V$_{in}$ =48V (Io$_1$ =8A, Io$_2$ =2A, Io$_3$ =2A represents 100% Load)



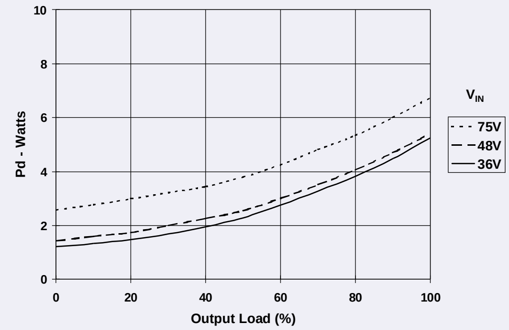
Output Ripple vs Output Power; V$_{in}$ =48V (Io$_1$ =4A, Io$_2$ =4A, Io$_3$ =4A represents 100% Load)



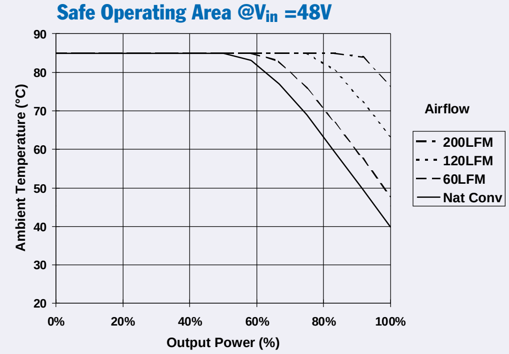
PT4833 Thermal Performance (See Note C)

(Io$_1$ + Io$_2$ + Io$_3$ =12A, represents 100% Load)

Power Dissipation vs Output Load



Safe Operating Area @V$_{in}$ =48V



Note A: *All Characteristic data in the above graphs has been developed from actual products tested at 25°C. This data is considered typical data for the ISR.*
Note B: *Output Load (%) represents the percent drawn from each output of the stated 100% load condition.*
Note C: *SOA curves represent operating conditions at which the internal components are at or below the manufacturer's maximum rated operating temperatures.*

Operating Features of the PT4820 Triple-Output DC/DC Converters

Short-Circuit Protection

To protect against load faults the PT4820 series of triple-output DC/DC converters incorporate output short-circuit protection. When the combined output current from all three outputs exceeds the over-current threshold (see data sheet specifications), the PT4820 shuts down after a short period of typically 15ms. This forces the output voltage at all three regulated outputs to simultaneously fall to zero. Following shutdown, the module automatically attempts to recover by executing a soft-start power-up. This occurs at intervals of approximately 65ms. If the load fault persists, the module will continually cycle through successive over-current trips and restarts.

Over-Temperature Protection

The PT4820 DC/DC converter series have an internal temperature sensor, which monitors the temperature of the module's metal case. If the case temperature exceeds a nominal 110°C the converter will shut down. The converter will automatically restart when the sensed temperature returns to about 100°C.

Under-Voltage Lock-Out

The Under-Voltage Lock-Out (UVLO) circuit prevents operation of the converter whenever the input voltage to the module is insufficient to maintain output regulation. The UVLO has approximately 2V of hysterisis. This is to prevent oscillation with a slowly changing input voltage. Below the UVLO threshold the module is off and the enable control inputs, EN1 and EN2 are inoperative.

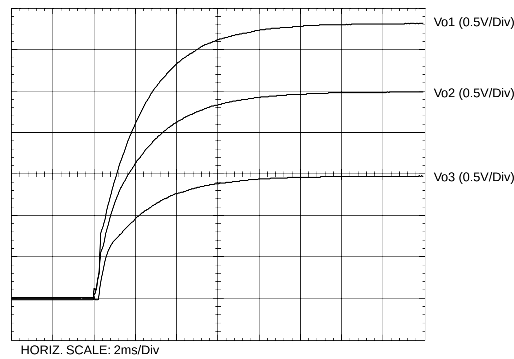
On/Off Output Voltage Sequencing

The power-up characteristic of the PT4820 series of DC/DC converters meets the requirements of microprocessor and DSP chipsets. All three outputs are internally sequenced to power-up in unison. Figure 1-1 shows the PT4820 output voltage rise times and characteristic shapes after either power is applied to the input of the converter, or the converter is enabled using one of the enable control inputs. All three output voltages rise simultaneously and monotonically until each reaches its respective output voltage. There is no turn-on overshoot and the output voltages are proportional to each other during power on.

Turn-On Time

The turn-on on time varies with the input voltage. The typical turn-on time (measured from the application of a valid input voltage to instance all outputs are in regulation) is typically 140 milliseconds at V_{in} =48V. The rise time of the output voltage is between 10 and 15 milliseconds.

Figure 1-1; Vo_1, Vo_2, Vo_3 Power-Up Sequence



Primary-Secondary Isolation

The PT4820 series of DC/DC converters incorporate electrical isolation between the input terminals (primary) and the output terminals (secondary). All converters are production tested to a withstand voltage of 1500VDC. The isolation complies with UL60950 and EN60950, and the requirements for operational isolation. This allows the converter to be configured for either a positive or negative input voltage source.

The regulation control circuitry for these modules is located on the secondary (output) side of the isolation barrier. Control signals are passed between the primary and secondary sides of the converter. The data sheet 'Pin Descriptions' and 'Pin-Out Information' provides guidance as to which reference, primary or secondary, each pin is associated.

Input Current Limiting

The converter is not internally fused. For safety and overall system protection, the maximum input current to the converter must be limited. Active or passive current limiting can be used. Passive current limiting can be a fast acting fuse. A 125-V fuse, rated no more than 5A, is recommended. Active current limiting can be implemented with a current limited "Hot-Swap" controller.

Using the On/Off Enable Controls on the PT4820 Series of Triple Output DC/DC Converters

The PT4820 (48V input) series of triple-output DC/DC converters incorporate two output enable controls. EN1 (pin 1) is the *Positive Enable* input, and EN2 (pin 2) is the *Negative Enable* input. Both inputs are electrically referenced to -V_{in} (pin 4) on the primary or input side of the converter. The *Enable* pins are ideally controlled with an open-collector (or open-drain) discrete transistor. A pull-up resistor is not required. If a pull-up resistor is added, the pull-up voltage must be limited to 15V.

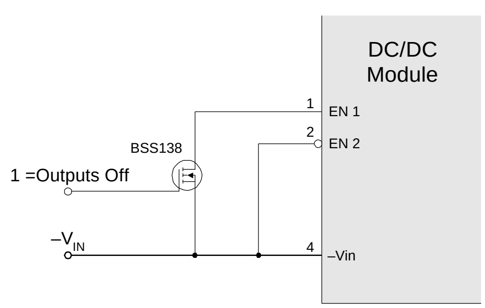
Automatic (UVLO) Power-Up

Connecting EN2 (pin 2) to -V_{in} (pin 4) and leaving EN1 (pin 1) open-circuit configures the converter for automatic power up. (See data sheet "Typical Application"). The converter control circuitry incorporates an "Under Voltage Lockout" (UVLO) function, which disables the converter until the minimum specified input voltage is present at ±V_{in}. (See data sheet Specifications). The UVLO circuitry ensures a clean transition during power-up and power-down, allowing the converter to tolerate a slow-rising input voltage. For most applications EN1 and EN2, can be configured for automatic power-up.

Positive Output Enable (Negative Inhibit)

To configure the converter for a positive enable function, connect EN2 (pin 2) to -V_{in} (pin 4), and apply the system On/Off control signal to EN1 (pin 1). In this configuration, applying less than 0.8V (with respect to -V_{in} potential) to pin 1 disables the converter outputs. Figure 2-1 is an example of this implemention using a buffer transistor.

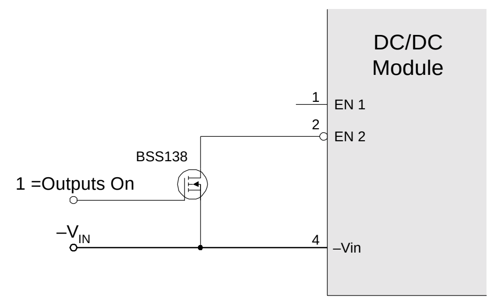
Figure 2-1; Positive Enable Configuration



Negative Output Enable (Positive Inhibit)

To configure the converter for a negative enable function, EN1 (pin 1) is left open circuit, and the system On/Off control signal is applied to EN2 (pin 2). Applying less than 0.8V (with respect to -V_{in} potential) to pin 2, enables the converter outputs. An example using a buffer transistor is again detailed in Figure 2-2. *Note: The converter will only produce and output voltage if a valid input voltage is applied to ±V_{in}.*

Figure 2-2; Negative Enable Configuration



On/Off Enable Turn-On Time

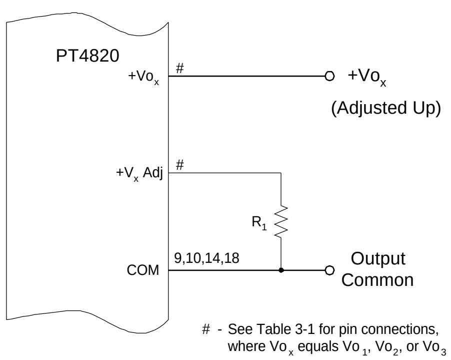
When the On/Off enable inputs, EN1 or EN2 are used to enable the PT4820's output voltages, the turn-on delay time (measured from the transition of the enable signal to the instance the outputs begin to rise) will vary with the input voltage and the module's internal timing. At an input voltage of 48V, the total turn-on time is between 20 and 60 milliseconds. This turn-on time reduces as the input voltage is increased. The rise time of the output voltages is between 10 and 15 milliseconds.

Adjusting the Output Voltages of the PT4820 Triple-Output DC/DC Converters

The output voltages of the PT4820 series of triple-output DC/DC converters, Vo_1, Vo_2 and Vo_3 are independently adjustable. The adjustment method uses a single external resistor, [1] which may be used to adjust a selected output by up to a nominal ±10% from the factory preset value. The value of the resistor determines the magnitude of adjustment, and the placement of the resistor determines the direction of adjustment (up or down). Resistor values can be calculated using the appropriate formula (see below) and the constants provided in Table 3-2. Alternatively the value may be selected directly from Table 3-3. The placement of each resistor is detailed as follows.

Adjust Up: To increase a specific output, add a resistor R_1 between the appropriate Vo_x Adj (Vo_1 Adj, Vo_2 Adj, or Vo_3 Adj) and the output common (COM). See Figure 3-1(a) and Table 3-1 for the resistor placement and pin connections.

Figure 3-1a



Adjust Down: Add a resistor (R_2), between the appropriate Vo_x Adj (Vo_1, Vo_2, or Vo_3) and the output being adjusted. See Figure 3-1(b) and Table 1 for the resistor placement and pin connections.

Figure 3-1b

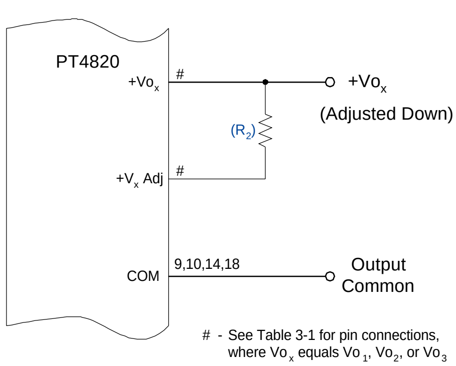


Table 3-1; Adjust Resistor Pin Connections

	To Adjust Up Connect R_1		To Adjust Down Connect (R_2)	
	from Vo_x Adj	to COM	from Vo_x Adj	to Vo_x
Vo_1	11	10	11	12
Vo_2	15	14	15	16
Vo_3	19	18	19	20

Calculation of Adjust Values

The adjust resistor values may be calculated. Use the applicable formula and select the appropriate constants from Table 2 for the output and model being adjusted.

$$R_1 \text{ [Adjust Up]}^3 = \frac{R_o \cdot V_r}{V_a - V_o} - R_s \quad k\Omega$$

$$(R_2) \text{ [Adjust Down]}^3 = \frac{R_o (V_a - V_r)}{V_o - V_a} - R_s \quad k\Omega$$

Where: V_o = Original output voltage
V_a = Adjusted output voltage
V_r = The reference voltage from Table 3-2
R_o = The resistance value in Table 3-2
R_s = The series resistance from Table 3-2

Notes:

1. Use only a single 1% (or better) tolerance resistor in either the R_1 or (R_2) location to adjust a specific output. Place the resistor as close to the ISR as possible.
2. Never connect capacitors to any of the 'Vo_x Adj' pins. Any capacitance added to these control pins will affect the stability of the respective regulated output.
3. Adjustments made to any output must also comply with the following limitations.

   $Vo_1 \geq (Vo_2 + 0.5V)$, and
   $Vo_1 \geq (Vo_3 + 0.5V)$

Table 3-2

V_{o1}, V_{o2}, & V_{o3} OUTPUT VOLTAGE ADJUSTMENT RANGE AND FORMULA PARAMETERS

V_o (nom)	5.0V	3.3V	2.5V	2.0V	1.8V	1.5V	1.2V
V_a (min)	4.5V	2.97V	2.25V	1.8V	1.62V	1.35V	1.08V
V_a (max)	5.5V	3.63V	2.75V	2.2V	1.98V	1.65V	1.32V
V_r	1.225V	1.225V	1.225V	1.225	1.225V	1.225V	1.003V
R_o (kΩ)	15.4	11.0	10.2	10.2	12.1	7.5	9.76
R_s (kΩ)	33.2	40.2	40.2	24.9	22.1	5.36	3.65

Table 3-3

V_{o1}, V_{o2}, & V_{o3} OUTPUT VOLTAGE ADJUST RESISTOR VALUES *(See Note 3 for adjustment limitations)*

V_o (nom)	5.0V	3.3V	2.5	V_o (nom)	2.0V	1.8V	1.5V	1.2V
V_a (req'd)				V_a (req'd)				
2.25			(1.6)kΩ	1.080				(2.6)kΩ
2.3			(14.6)kΩ	1.100				(5.8)kΩ
2.35			(36.3)kΩ	1.120				(10.6)kΩ
2.4			(79.6)kΩ	1.140				(18.6)kΩ
2.45			(210.0)kΩ	1.160				(34.7)kΩ
2.5				1.180				(82.7)kΩ
2.55			210.0kΩ	1.200				
2.6			84.7kΩ	1.220				486.0kΩ
2.65			43.1kΩ	1.240				241.0kΩ
2.7			22.3kΩ	1.260				160.0kΩ
2.75			9.8kΩ	1.280				119.0kΩ
2.97		(18.0)kΩ		1.300				94.2kΩ
3.0		(24.9)kΩ		1.320				77.9kΩ
3.05		(40.1)kΩ		1.350			(0.9)kΩ	
3.1		(62.9)kΩ		1.375			(3.6)kΩ	
3.15		(101.0)kΩ		1.400			(7.8)kΩ	
3.2		(177.0)kΩ		1.425			(14.6)kΩ	
3.25		(405.0)kΩ		1.450			(28.4)kΩ	
3.3				1.475			(69.6)kΩ	
3.35		229.0kΩ		1.500				
3.4		94.5kΩ		1.525			362.0kΩ	
3.45		49.6kΩ		1.550			178.0kΩ	
3.5		27.2kΩ		1.575			117.0kΩ	
3.55		13.7kΩ		1.600			86.5kΩ	
3.6		4.7kΩ		1.620		(4.5)kΩ	71.2kΩ	
3.63		0.6kΩ		1.650		(12.2)kΩ	55.9kΩ	
•				1.700		(35.4)kΩ		
4.5	(67.7)kΩ			1.750		(105.0)kΩ		
4.6	(96.7)kΩ			1.800	(4.4)kΩ			
4.7	(145.0)kΩ			1.850	(17.6)kΩ	274.0kΩ		
4.8	(242.0)kΩ			1.900	(43.9)kΩ	126.0kΩ		
4.9	(533.0)kΩ			1.950	(123.0)kΩ	76.7kΩ		
5.0				2.000				
5.1	155.0kΩ			2.050	225.0kΩ			
5.2	61.1kΩ			2.100	100.0kΩ			
5.3	29.7kΩ			2.150	58.4kΩ			
5.4	14.0kΩ			2.200	37.6kΩ			
5.5	4.5kΩ							

R1 = (Blue) R2 = Black

VDE Approved Installation Instructions (Installationsanleitung)

Nennspannnug (Rated Voltage):	PT4820 36 to 72 Vdc, Transient to 80Vdc
Nennaufnahme (Rated Input):	PT4820 1.5 Adc
Nennleistung (Rated Power):	40 Watts Maximum
Ausgangsspannung (Sec. Voltage):	PT4820 Series
	PT4821, +3.3/ +2.5/ +1.5 Vdc; 8.0/ 6.0/ 6.0 Adc; Max total is 12Adc
	PT4822, +3.3/ +1.8/ +1.5 Vdc; 8.0/ 6.0/ 6.0 Adc; Max total is 12Adc
Ausgangsstrom (Sec. Current):	PT4823, +3.3/ +2.5/ +1.2 Vdc; 8.0/ 6.0/ 6.0 Adc; Max total is 12Adc
oder (or)	PT4824, +3.3/ +1.8/ +1.2 Vdc; 8.0/ 6.0/ 6.0 Adc; Max total is 12Adc
Ausgangsleistung (Sec. Power):	PT4825, +3.3/ +1.5/ +1.2 Vdc; 8.0/ 6.0/ 6.0 Adc; Max total is 12Adc
	PT4826, +5.0/ +3.3/ +1.8 Vdc; 5.0/ 5.5 /5.5 Adc; Max total is 9Adc
	PT4827, +3.3/ +2.5/ +1.8 Vdc; 8.0/ 6.0 /6.0 Adc; Max total is 12Adc
	PT4828, +5.0/ +2.5/ +1.5 Vdc; 5.0/ 5.5 /5.5 Adc; Max total is 9Adc
	PT4829, +5.0/ +1.8/ +1.5 Vdc; 5.0/ 5.5 /5.5 Adc; Max total is 9Adc
	PT4831, +5.0/ +3.3/ +1.5 Vdc; 5.0/ 5.5 /5.5 Adc; Max total is 9Adc
	PT4832, +5.0/ +3.3/ +2.5 Vdc; 5.0/ 5.5 /5.5 Adc; Max total is 9Adc

Angabe der Umgebungstemperatur

(Information on ambient temperature): +85 °C maximum as tested

Besondere Hinweise (Special Instructions):

Es ist vorzusehen, daß die Spannungsversorgung in einer Endanwendung über eine isolierte Sekundaerschaltung bereit gestellt wird. Die Eingangspannung der Spannungsversorgungsmodule muss eine verstaerkte Isolierung von der Wechselstromquelle aufweisen.

Die Spannungsversorgung muss gemaess den Gehaeuse-, Montage-, Kriech- und Luftstrecken-, Markierungs- und Trennanforderungen der Endanwendung installiert werden.

(The power supply is intended to be supplied by isolated secondary circuitry in an end use application. The input power to these power supplies shall have reinforced insulation from the AC mains.

The power supply shall be installed in compliance with the enclosure, mounting, creepage, clearance, casualty, markings, and segregation requirements of the end-use application.

Offenbach,

VDE Prüf- und Zertifizierungsinstitut
Abteilung / *Department TD*

(Jürgen Bärwinkel)

Ort / *Place*: Datum / *Date*: Nov 6, 2002

(Stempel und Unterschrift des Herstellers / Stamp and signature of the manufacturer)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
PT4821C	NRND	SIP MODULE	ENP	21	8	TBD	Call TI	Level-3-215C-168HRS	
PT4822A	OBSOLETE	SIP MODULE	ENN	21		TBD	Call TI	Call TI	
PT4822C	OBSOLETE	SIP MODULE	ENP	21		TBD	Call TI	Call TI	
PT4822N	OBSOLETE	SIP MODULE	ENM	21		TBD	Call TI	Call TI	
PT4823C	NRND	SIP MODULE	ENP	21	8	TBD	Call TI	Level-3-215C-168HRS	
PT4823N	OBSOLETE	SIP MODULE	ENM	21		TBD	Call TI	Call TI	
PT4824A	OBSOLETE	SIP MODULE	ENN	21		TBD	Call TI	Call TI	
PT4824N	OBSOLETE	SIP MODULE	ENM	21		TBD	Call TI	Call TI	
PT4825A	OBSOLETE	SIP MODULE	ENN	21		TBD	Call TI	Call TI	
PT4825C	OBSOLETE	SIP MODULE	ENP	21		TBD	Call TI	Call TI	
PT4825N	OBSOLETE	SIP MODULE	ENM	21		TBD	Call TI	Call TI	
PT4826A	NRND	SIP MODULE	ENN	21	8	TBD	Call TI	Level-1-215C-UNLIM	
PT4826C	NRND	SIP MODULE	ENP	21	8	TBD	Call TI	Level-3-215C-168HRS	
PT4828A	OBSOLETE	SIP MODULE	ENN	21		TBD	Call TI	Call TI	
PT4828C	NRND	SIP MODULE	ENP	21	8	TBD	Call TI	Level-3-215C-168HRS	
PT4829A	OBSOLETE	SIP MODULE	ENN	21		TBD	Call TI	Call TI	
PT4829C	NRND	SIP MODULE	ENP	21	8	TBD	Call TI	Level-3-215C-168HRS	
PT4829N	OBSOLETE	SIP MODULE	ENM	21		TBD	Call TI	Call TI	
PT4831C	NRND	SIP MODULE	ENP	21	8	TBD	Call TI	Level-3-215C-168HRS	
PT4831N	OBSOLETE	SIP MODULE	ENM	21		TBD	Call TI	Call TI	
PT4833A	OBSOLETE	SIP MODULE	ENN	21		TBD	Call TI	Call TI	
PT4833C	NRND	SIP MODULE	ENP	21	8	TBD	Call TI	Level-3-215C-168HRS	
PT4833N	OBSOLETE	SIP MODULE	ENM	21		TBD	Call TI	Call TI	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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