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Jameco Part Number 2062310

2.25-A, WIDE-INPUT ADJUSTABLE SWITCHING REGULATOR

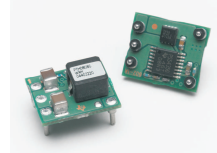
FEATURES

- Up to 2.25-A Output Current at 85°C
- 4.5-V to 18-V Input Voltage Range
- Wide-Output Voltage Adjust (0.9 V to 5.5 V)
- Efficiencies Up To 93%
- On/Off Inhibit
- Undervoltage Lockout (UVLO)
- Output Overcurrent Protection (Nonlatching, Auto-Reset)
- Overtemperature Protection
- Ambient Temperature Range: -40°C to 85°C
- Surface-Mount Package

- Safety Agency Approvals:
UL/CUL 60950, EN60950

APPLICATIONS

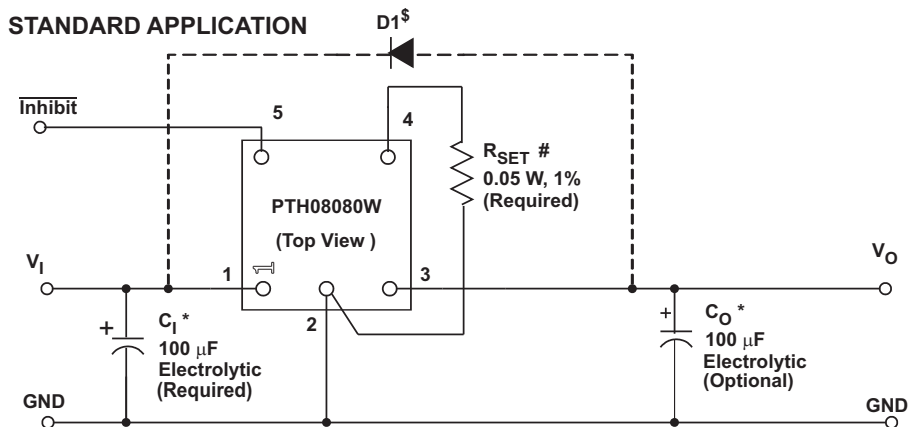
- Telecommunications, Instrumentation, and General-Purpose Circuits



DESCRIPTION

The PTH08080W is a highly integrated, low-cost switching regulator module that delivers up to 2.25 A of output current. The PTH08080W sources output current at a much higher efficiency than a TO-220 linear regulator IC, thereby eliminating the need for a heat sink. Its small size (0.5 × 0.6 in) and flexible operation creates value for a variety of applications.

The input voltage range of the PTH08080W is from 4.5 V to 18 V, allowing operation from either a 5-V or 12-V input bus. Using state-of-the-art switched-mode power-conversion technology, the PTH08080W can step down to voltages as low as 0.9 V from a 5-V input bus, with less than 1 W of power dissipation. The output voltage can be adjusted to any voltage over the range, 0.9 V to 5.5 V, using a single external resistor. Operating features include an undervoltage lockout (UVLO), on/off inhibit, overcurrent protection, and overtemperature protection. Target applications include telecommunications, test and measurement applications, and high-end consumer products. This product is available in both through-hole and surface-mount package options, including tape and reel.



- * See The Capacitor Application Information
- # See the Specification Table for the R_{SET} value.
- § Diode is Required When $V_O \geq 5.25$ V and $V_I \geq 16$ V.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this datasheet, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted⁽¹⁾

| | | PTH08080W | UNIT |
|------------------|---|------------|------|
| T _A | Operating free-air temperature Over V _I range | −40 to 85 | °C |
| T _S | Surface temperature of module body or pins | Suffix AH | 235 |
| | | Suffix AD | 260 |
| | | Suffix AS | 235 |
| | | Suffix AZ | 260 |
| T _{stg} | Storage temperature | −55 to 125 | °C |

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

| | | MIN | MAX | UNIT |
|----------------|--------------------------------|-----|-----|------|
| V _I | Input voltage | 4.5 | 18 | V |
| T _A | Operating free-air temperature | −40 | 85 | °C |

PACKAGE SPECIFICATIONS

| PTH08080W (Suffix AH and AS) | | |
|------------------------------|--|----------------------|
| Weight | | 1.5 grams |
| Flammability | Meets UL 94 V-O | |
| Mechanical shock | Per Mil-STD-883D, Method 2002.3, 1 ms, 1/2 sine, mounted | 500 G ⁽¹⁾ |
| Mechanical vibration | Mil-STD-883D, Method 2007.2, 20-2000 Hz | 20 G ⁽¹⁾ |

(1) Qualification limit.

ELECTRICAL CHARACTERISTICS

at 25°C free-air temperature, $V_I = 12\text{ V}$, $V_O = 3.3\text{ V}$, $I_O = I_{Omax}$, $C_I = 100\text{ }\mu\text{F}$, $C_O = 100\text{ }\mu\text{F}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------|--------------------------------|---|--|--------------------|-----------------------|------------------|
| I_O | Output current | $T_A = 85^\circ\text{C}$, natural convection airflow | 0 | | 2.25 | A |
| P_O | Output power | $T_A = 85^\circ\text{C}$, natural convection airflow | | | 10 | W |
| V_O | Set-point voltage tolerance | $T_A = 25^\circ\text{C}$ | | | 2 ⁽¹⁾ | % |
| | Temperature variation | $-40 \leq T_A \leq +85^\circ\text{C}$ | | 0.5 | | % V_O |
| | Line regulation | Over V_I range | | 7 | | mV |
| | Load regulation | Over I_O range | | 0.13 | | % V_O |
| | Total output voltage variation | Includes set-point, line, load, $-40 \leq T_A \leq +85^\circ\text{C}$ | | | | 3 ⁽¹⁾ |
| V_{ADJ} | Output Voltage Adjust Range | Over I_O range | 0.9 | | 5.5 | V |
| V_I | Input Voltage Range | Over V_O range | | | | |
| | | $0.9\text{ V} \leq V_O \leq 1.8\text{ V}$ | 4.5 | | $V_O \times 10^{(2)}$ | |
| | | $1.8\text{ V} < V_O \leq 3.4\text{ V}$ | 4.5 | | 18 | |
| | | $3.4\text{ V} < V_O \leq 5.5\text{ V}$ | $V_O + 1.1^{(2)}$ | | 18 ⁽²⁾ | |
| η | Efficiency | $T_A = 25^\circ\text{C}$, $I_O = 2\text{ A}$ | $R_{SET} = 348\text{ }\Omega$, $V_O = 5\text{ V}$ | | 93.5% | |
| | | | $R_{SET} = 1.87\text{ k}\Omega$, $V_O = 3.3\text{ V}$ | | 92% | |
| | | | $R_{SET} = 3.74\text{ k}\Omega$, $V_O = 2.5\text{ V}$ | | 91% | |
| | | | $R_{SET} = 6.19\text{ k}\Omega$, $V_O = 2\text{ V}$ | | 90% | |
| | | | $R_{SET} = 8.06\text{ k}\Omega$, $V_O = 1.8\text{ V}$ | | 89% | |
| | | | $R_{SET} = 13\text{ k}\Omega$, $V_O = 1.5\text{ V}$ | | 87.5% | |
| | | | $R_{SET} = 27.4\text{ k}\Omega$, $V_O = 1.2\text{ V}$ | | 86.5% | |
| | Output voltage ripple | 20 MHz bandwidth | | 30 | | mV _{PP} |
| I_O (trip) | Overcurrent threshold | Reset, followed by autorecovery | | 3.5 | | A |
| | Transient response | $C_O = 100\text{ }\mu\text{F}$, 1 A/ μs load step from 50% to 100% I_{Omax} | Recovery time | | 50 | μs |
| | | | V_O over/undershoot | | 70 | mV |
| UVLO | Undervoltage lockout | $V_I = \text{increasing}$ | | 4.35 | 4.5 | |
| | | $V_I = \text{decreasing}$ | 3.6 | 4 | | V |
| | Inhibit control (pin 5) | Input high voltage (V_{IH}) | | | Open ⁽³⁾ | |
| | | Input low voltage (V_{IL}) | -0.2 | | 0.5 | V |
| | | Input low current (I_{IL}) | | 5 | | μA |
| I_I (stby) | Input standby current | Pins 5 and 2 connected | | 1 | | mA |
| f_S | Switching frequency | Over V_I and I_O ranges | | 300 | | kHz |
| | External input capacitance | Electrolytic type (C_I) | 100 ⁽⁴⁾ | | | μF |
| | External output capacitance | Ceramic type (C_O) | | | 220 | |
| | | Nonceramic type (C_O) | | 100 ⁽⁵⁾ | 330 ⁽⁶⁾ | μF |
| | | Equivalent series resistance (nonceramic) | 10 ⁽⁷⁾ | | | m Ω |
| MTBF | Calculated reliability | Per Telcordia SR-332, 50% stress, $T_A = 40^\circ\text{C}$, ground benign | 48 | | | 10^6 Hr |

- The set-point voltage tolerance is affected by the tolerance and stability of R_{SET} . The stated limit is unconditionally met if R_{SET} has a tolerance of 1% with 100 ppm/°C or better temperature stability.
- The minimum input voltage is 4.5 V or $(V_O + 1.1)$ V, whichever is greater. The maximum input voltage is 18 V or $V_O \times 10$, whichever is less.
- This control pin has an internal pull-up to 3 V (TYP). Do not place an internal pull-up on this pin. If it is left open-circuit, the module operates when input power is applied. A small low-leakage (< 100 nA) MOSFET is recommended for control. See the application information for further guidance.
- An external 100- μF electrolytic capacitor is required across the input (V_I and GND) for proper operation. Locate the capacitor close to the module.
- An external 100- μF electrolytic capacitor is optional across the output (V_O and GND). Locate the capacitor close to the module. Additional capacitance close to the load improves the response of the regulator to load transients.
- This is the calculated maximum capacitance. The minimum ESR limitation often results in a lower value. See the capacitor application information for further guidance.
- This is the typical ESR for all the electrolytic (nonceramic) capacitance. Use 14 m Ω as the minimum when calculating the total equivalent series resistance (ESR) using the maximum ESR values specified by the capacitor manufacturer.

PIN ASSIGNMENT
TERMINAL FUNCTIONS

| TERMINAL | | I/O | DESCRIPTION |
|-----------------------|-----|-----|---|
| NAME | NO. | | |
| V _I | 1 | I | The positive input voltage power node to the module, which is referenced to common GND. |
| GND | 2 | | This is the common ground connection for the V _I and V _O power connections. It is also the 0-Vdc reference for the <i>Inhibit</i> and V _O <i>Adjust</i> control inputs. |
| V _O | 3 | O | The regulated positive power output with respect to the GND node. |
| V _O Adjust | 4 | I | A 1% resistor must be connected between this pin and GND (pin 1) to set the output voltage of the module higher than 0.9 V. If left open-circuit, the output voltage defaults to this value. The temperature stability of the resistor should be 100 ppm/°C (or better). The set-point range is from 0.9 V to 5.5 V. The electrical specification table gives the standard resistor value for a number of common output voltages. See the application information for further guidance. |
| <u>Inhibit</u> | 5 | I | The Inhibit pin is an open-collector/drain-negative logic input that is referenced to GND. Applying a low-level ground signal to this input disables the module's output. When the Inhibit control is active, the input current drawn by the regulator is significantly reduced. If the Inhibit pin is left open-circuit, the module produces an output voltage whenever a valid input source is applied. Do not place an external pull-up on this pin. |

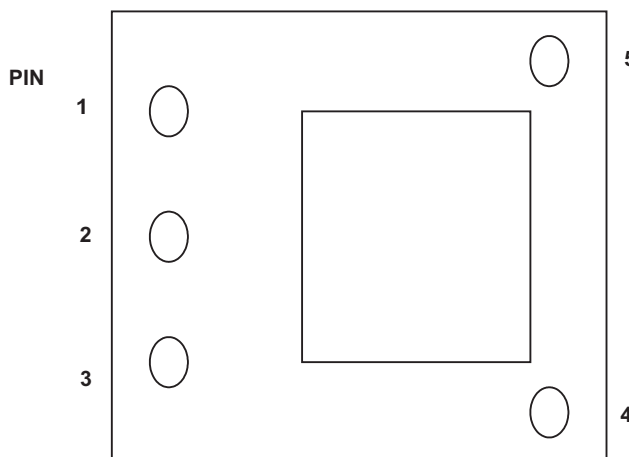


Figure 1. Terminal Location

TYPICAL CHARACTERISTICS (5-V INPUT)⁽¹⁾⁽²⁾

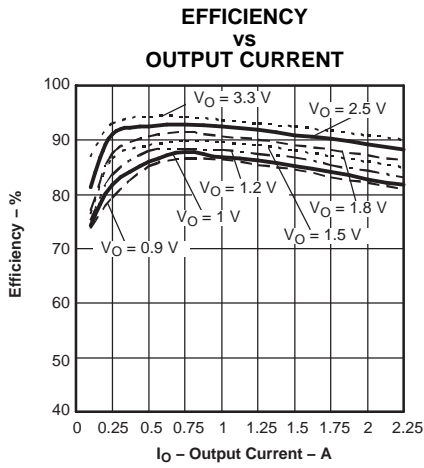


Figure 2.

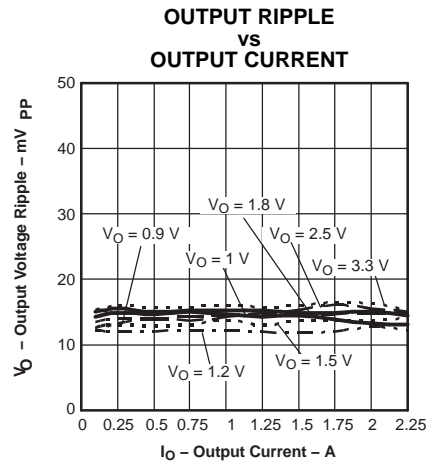


Figure 3.

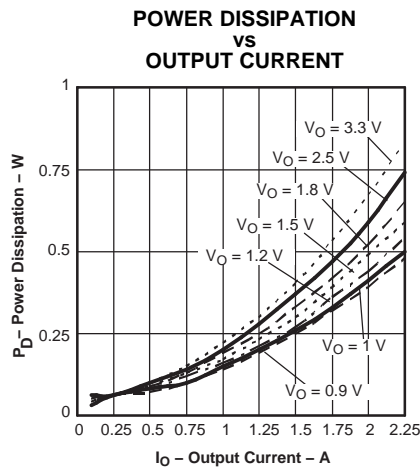


Figure 4.

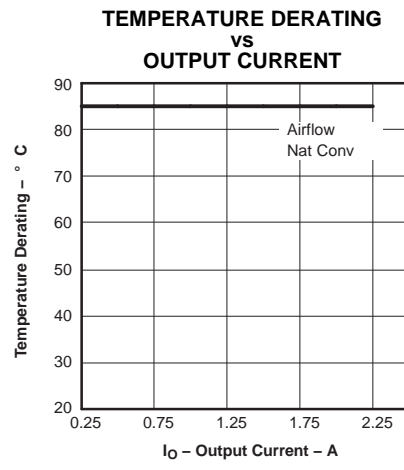


Figure 5.

- (1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to [Figure 2](#), [Figure 3](#), and [Figure 4](#).
- (2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100-mm × 100-mm, double-sided PCB with 2-oz. copper. Applies to [Figure 5](#).

TYPICAL CHARACTERISTICS (12-V INPUT)⁽¹⁾⁽²⁾

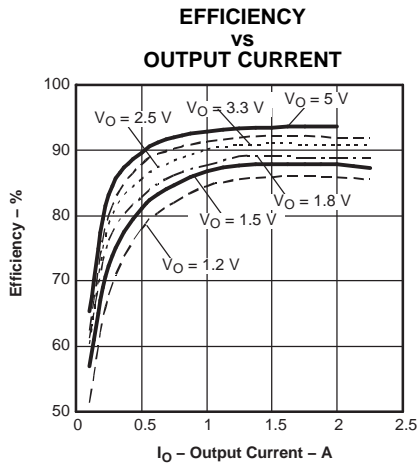


Figure 6.

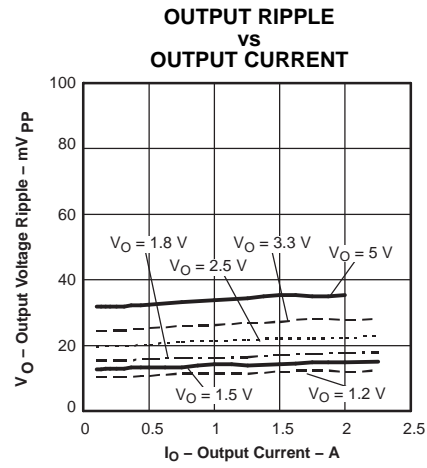


Figure 7.

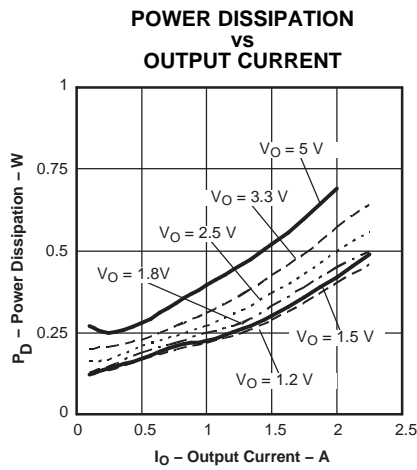


Figure 8.

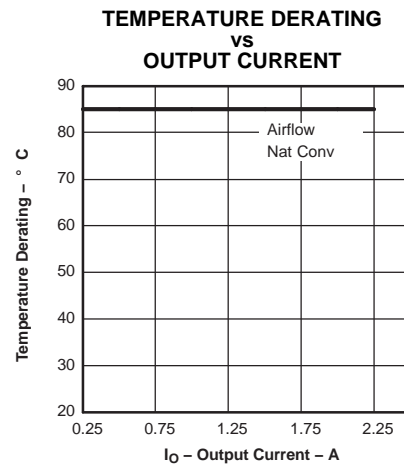


Figure 9.

- (1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to [Figure 6](#), [Figure 7](#), and [Figure 8](#).
- (2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100-mm × 100-mm, double-sided PCB with 2-oz. copper. Applies to [Figure 9](#).

APPLICATION INFORMATION

Adjusting the Output Voltage of the PTH08080W Wide-Output Adjust Power Modules

The V_O Adjust control (pin 4) sets the output voltage of the PTH08080W product. The adjustment range is from 0.9 V to 5.5 V. The adjustment method requires the addition of a single external resistor, R_{SET} , that must be connected directly between the V_O Adjust and GND (pin 2). Table 1 gives the standard external resistor for a number of common bus voltages, along with the actual voltage the resistance produces.

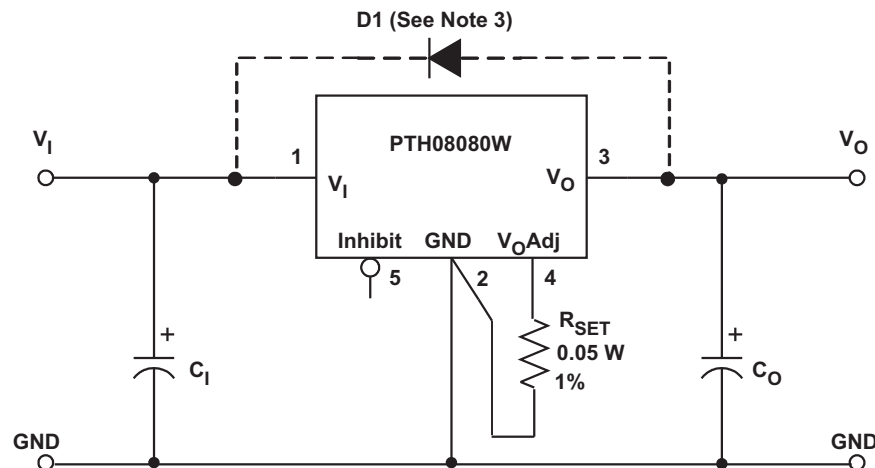
For other output voltages, the value of the required resistor can either be calculated using the following formula, or simply selected from the range of values given in Table 2. Figure 10 shows the placement of the required resistor.

$$R_{SET} = 10 \text{ k}\Omega \times \frac{0.891 \text{ V}}{V_{out} - 0.9 \text{ V}} - 1.82 \text{ k}\Omega$$

Table 1. Standard Values of R_{SET} for Common Output Voltages

| V_O (Required) | R_{set} (Standard Value) | V_O (Actual) |
|----------------------|-------------------------------|-------------------|
| 5 V ⁽¹⁾ | 348 Ω | 5.010 V |
| 3.3 V | 1.87 k Ω | 3.315 V |
| 2.5 V | 3.74 k Ω | 2.503 V |
| 2 V | 6.19 k Ω | 2.012 V |
| 1.8 V | 8.06 k Ω | 1.802 V |
| 1.5 V ⁽²⁾ | 13.0 k Ω | 1.501 V |
| 1.2 V ⁽²⁾ | 27.4 k Ω | 1.205 V |
| 1 V ⁽²⁾ | 86.6 k Ω | 1.001 V |
| 0.9 V ⁽²⁾ | Open | 0.9 V |

- (1) The minimum input voltage is 4.5 V or ($V_O + 1.1$) V, whichever is greater.
- (2) The maximum input voltage is 18 V or ($V_O \times 10$) V, whichever is lesser.



- (1) A 0.05-W rated resistor may be used. The tolerance should be 1%, with a temperature stability of 100 ppm/ $^{\circ}$ C (or better). Place the resistor as close to the regulator as possible. Connect the resistor directly between pins 4 and 2 using dedicated PCB traces.
- (2) Never connect capacitors from V_O Adjust to either GND or V_O . Any capacitance added to the V_O Adjust pin affects the stability of the regulator.
- (3) The protection diode, D1, is required whenever the output voltage setpoint is adjusted to 5.25 V (or higher) and V_I is 16 V or greater.

Figure 10. V_O Adjust Resistor Placement

Table 2. Calculated Set-Point Resistor Values

| V _a Required | R _{set} | V _a Required | R _{set} | V _a Required | R _{set} |
|-------------------------|------------------|-------------------------|------------------|-------------------------|------------------|
| 0.900 | Open | 1.800 | 8.08 kΩ | 3.700 | 1.36 kΩ |
| 0.925 | 355 kΩ | 1.850 | 7.56 kΩ | 3.750 | 1.32 kΩ |
| 0.950 | 176 kΩ | 1.900 | 7.09 kΩ | 3.800 | 1.25 kΩ |
| 0.975 | 117 kΩ | 1.950 | 6.67 kΩ | 3.850 | 1.20 kΩ |
| 1.000 | 87.2 kΩ | 2.000 | 6.28 kΩ | 3.900 | 1.15 kΩ |
| 1.025 | 69.5 kΩ | 2.050 | 5.92 kΩ | 3.950 | 1.10 kΩ |
| 1.050 | 57.6 kΩ | 2.100 | 5.61 kΩ | 4.000 | 1.05 kΩ |
| 1.075 | 49.1 kΩ | 2.150 | 5.31 kΩ | 4.050 | 1.01 kΩ |
| 1.100 | 42.7 kΩ | 2.200 | 5.03 kΩ | 4.100 | 964 Ω |
| 1.125 | 37.8 kΩ | 2.250 | 4.78 kΩ | 4.150 | 922 Ω |
| 1.150 | 33.8 kΩ | 2.300 | 4.54 kΩ | 4.200 | 880 Ω |
| 1.175 | 30.6 kΩ | 2.350 | 4.33 kΩ | 4.250 | 840 Ω |
| 1.200 | 27.9 kΩ | 2.400 | 4.12 kΩ | 4.300 | 801 Ω |
| 1.225 | 25.6 kΩ | 2.450 | 3.93 kΩ | 4.350 | 763 Ω |
| 1.250 | 23.6 kΩ | 2.500 | 3.75 kΩ | 4.400 | 726 Ω |
| 1.275 | 21.9 kΩ | 2.550 | 3.58 kΩ | 4.450 | 690 Ω |
| 1.300 | 20.5 kΩ | 2.600 | 3.42 kΩ | 4.500 | 655 Ω |
| 1.325 | 19.1 kΩ | 2.650 | 3.27 kΩ | 4.550 | 621 Ω |
| 1.350 | 17.9 kΩ | 2.700 | 3.13 kΩ | 4.600 | 588 Ω |
| 1.375 | 16.9 kΩ | 2.750 | 2.99 kΩ | 4.650 | 556 Ω |
| 1.400 | 14.6 kΩ | 2.800 | 2.87 kΩ | 4.700 | 525 Ω |
| 1.425 | 13.7 kΩ | 2.850 | 2.75 kΩ | 4.750 | 494 Ω |
| 1.450 | 13.0 kΩ | 2.900 | 2.64 kΩ | 4.800 | 465 Ω |
| 1.475 | 13.7 kΩ | 2.950 | 2.53 kΩ | 4.850 | 436 Ω |
| 1.500 | 13.0 kΩ | 3.000 | 2.42 kΩ | 4.900 | 408 Ω |
| 1.525 | 12.4 kΩ | 3.050 | 2.32 kΩ | 4.950 | 380 Ω |
| 1.550 | 11.9 kΩ | 3.100 | 2.23 kΩ | 5.000 | 353 Ω |
| 1.575 | 11.4 kΩ | 3.150 | 2.14 kΩ | 5.050 | 327 Ω |
| 1.600 | 10.9 kΩ | 3.200 | 2.05 kΩ | 5.100 | 301 Ω |
| 1.625 | 10.5 kΩ | 3.250 | 1.97 kΩ | 5.150 | 276 Ω |
| 1.650 | 10.0 kΩ | 3.300 | 1.89 kΩ | 5.200 | 252 Ω |
| 1.675 | 9.68 kΩ | 3.350 | 1.82 kΩ | 5.250 | 228 Ω |
| 1.700 | 9.32 kΩ | 3.400 | 1.74 kΩ | 5.300 | 205 Ω |
| 1.725 | 8.98 kΩ | 3.450 | 1.67 kΩ | 5.350 | 182 Ω |
| 1.750 | 8.66 kΩ | 3.500 | 1.61 kΩ | 5.400 | 160 Ω |
| 1.775 | 8.36 kΩ | 3.550 | 1.54 kΩ | 5.450 | 138 Ω |
| 1.800 | 8.08 kΩ | 3.600 | 1.48 kΩ | 5.500 | 117 Ω |
| 1.825 | 7.81 kΩ | 3.650 | 1.42 kΩ | | |

CAPACITOR RECOMMENDATIONS FOR THE PTH08080W WIDE-OUTPUT ADJUST POWER MODULES

Input Capacitor

The minimum recommended input capacitor is 100 μF of capacitance. When $V_O > 3.4\text{ V}$, the 100- μF electrolytic capacitance must be rated for 650-mArms ripple current. For $V_O < 3.4\text{ V}$, the ripple current rating must be at least 500 mArms. The ripple current rating of electrolytic capacitors is a major consideration when they are used at the input.

When specifying regular tantalum capacitors for use at the input, a minimum voltage rating of $2 \times$ (maximum dc voltage + ac ripple) is highly recommended. This is standard practice to ensure reliability. Polymer-tantalum capacitors are not affected by this requirement.

For improved ripple reduction on the input bus, ceramic capacitors can also be added to complement the required electrolytic capacitance.

Output Capacitors (Optional)

No output capacitance is required for normal operation. However, applications with load transients (sudden changes in load current) can benefit by adding external output capacitance. A 100- μF electrolytic or ceramic capacitor can be used to improve transient response. Adding a 100- μF nonceramic capacitor allows the module to meet its transient response specification. A high-quality computer-grade electrolytic capacitor should be adequate.

Electrolytic capacitors should be located close to the load circuit. These capacitors provide decoupling over the frequency range, 2 kHz to 150 kHz. Aluminum electrolytic capacitors are suitable for ambient temperatures above 0°C . For operation below 0°C , tantalum or Os-Con-type capacitors are recommended. When using one or more nonceramic capacitors, the calculated equivalent ESR should be no lower than 10 m Ω (14 m Ω using the manufacturer's maximum ESR for a single capacitor). A list of preferred low-ESR-type capacitors are identified in [Table 3](#), the recommended capacitor table.

Ceramic Capacitors

Above 150 kHz, the performance of aluminum electrolytic capacitors becomes less effective. To further improve the reflected input ripple current, or the output transient response, multilayer ceramic capacitors must be added. Ceramic capacitors have low ESR and their resonant frequency is higher than the bandwidth of the regulator. When placed at the output their combined ESR is not critical as long as the total value of ceramic capacitance does not exceed 200 μF . Also, to prevent the formation of local resonances, do not exceed the maximum number of capacitors specified in the capacitor table.

Tantalum Capacitors

Additional tantalum-type capacitors can be used at both the input and output, and are recommended for applications where the ambient operating temperature can be less than 0°C . The AVX TPS, Sprague 593D/594/595, and Kemet T495/T510/T520 capacitors series are suggested over many other tantalum types due to their rated surge, power dissipation, and ripple current capability. As a caution, many general-purpose tantalum capacitors have considerably higher ESR, reduced power dissipation, and lower ripple current capability. These capacitors are also less reliable as they have lower power dissipation and surge current ratings. Tantalum capacitors that do not have a stated ESR or surge current rating are not recommended for power applications. When specifying Os-Con and polymer tantalum capacitors for the output, the minimum ESR limit is encountered well before the maximum capacitance value is reached.

Capacitor Table

The capacitor table, [Table 3](#), identifies the characteristics of capacitors from a number of vendors with acceptable ESR and ripple current (rms) ratings. The recommended number of capacitors required at both the input and output buses is identified for each capacitor type. This is not an extensive capacitor list. Capacitors from other vendors are available with comparable specifications. Those listed are for guidance. The rms rating and ESR (at 100 kHz) are critical parameters necessary to ensure both optimum regulator performance and long capacitor life.

Designing for Load Transients

The transient response of the dc/dc converter has been characterized using a load transient with a di/dt of 1 A/ μ s. The typical voltage deviation for this load transient is given in the data-sheet specification table using the optional value of output capacitance. As the di/dt of a transient is increased, the response of a converter's regulation circuit ultimately depends on its output capacitor decoupling network. This is an inherent limitation with any dc/dc converter once the speed of the transient exceeds its bandwidth capability. If the target application specifies a higher di/dt or lower voltage deviation, the requirement can only be met with additional output capacitor decoupling. In these cases, special attention must be paid to the type, value, and ESR of the capacitors selected.

If the transient performance requirements exceed those specified in the data sheet, the selection of output capacitors becomes more important. Review the minimum ESR in the characteristic data sheet for details on the capacitance maximum.

Table 3. Recommended Input/Output Capacitors

| CAPACITOR VENDOR/ COMPONENT SERIES | CAPACITOR CHARACTERISTICS | | | | | QUANTITY | | VENDOR NUMBER |
|--|---------------------------|---------------------|--|--|--|--|-----------------------------|--|
| | WORKING VOLTAGE (V) | VALUE (μ F) | EQUIVALENT SERIES RESISTANCE (ESR) (Ω) | 85°C MAXIMUM RIPPLE CURRENT (I_{rms}) (mA) | PHYSICAL SIZE (mm) | INPUT BUS ⁽¹⁾ | OUTPUT BUS (Optional) | |
| Panasonic WA (SMT) | 20 | 150 | 0.026 | 3700 | 10 × 10,2 | 1 | ≤ 2 | EEFWA1D151P |
| FC (SMT) | 25 | 220 | 0.150 | 670 | 10 × 10,2 | 1 | 1 | EEVFC1E221P |
| Panasonic SL SP-cap(SMT) | 6.3 6.3 | 47 120 | 0.018 0.007 | 2500 3500 | 7,3 × 4,3 7,3 × 4,3 | N/R ⁽²⁾ N/R ⁽²⁾ | ≤ 3 ≤ 1 | EEFCD0J470R EEFSD0J121R |
| United Chemi-con PXA (SMT) | 16 | 150 | 0.026 | 3400 | 10 × 7,7 | 1 | ≤ 2 | PXA16VC151MJ80TP $V_i < 14$ V |
| PS | 25 | 100 | 0.020 | 4300 | 10 × 12,5 | 1 | ≤ 2 | 25PS100MJ12 |
| LXZ | 35 | 220 | 0.180 | 760 | 10 × 12,5 | 1 | 1 | LXZ35VB221M10X12LL |
| MVZ (SMT) | 25 | 470 | 0.090 | 670 | 10 × 10 | 1 | 1 | MVZ25VC471MJ10TP |
| Nichicon UWG (SMT) | 35 | 100 | 0.150 | 670 | 10 × 10 | 1 | 1 | UWG1V101MNR1GS |
| F559(Tantalum) | 10 | 100 | 0.055 | 2000 | 7,7 × 4,3 | N/R ⁽³⁾ | ≤ 3 | F551A107MN |
| HD | 25 | 220 | 0.072 | 760 | 8 × 11,5 | 1 | 1 | UHD1E221MPR |
| Sanyo Os-con\ POS-Cap SVP (SMT) | 10 20 | 68 150 | 0.025 0.020 | 2400 4320 | 7,3 × 4,3 10 × 12,7 | N/R ⁽²⁾ 1 | ≤ 2 ≤ 1 | 10TPE68M 20SVP150M |
| SP | 20 | 120 | 0.024 | 3110 | 8 × 10,5 | 1 | ≤ 2 | 20SP120M |
| AVX Tantalum TPS (SMD) | 35 25 | 47 47 | 0.100 0.100 | 1430 1150 | 7,3 × 4,3 × 4,1 7,3 × 4,3 × 4,1 | 2 2 | ≤ 4 ≤ 4 | TPSV476M035R0100 TPSE476M025R0100 $V_i < 13$ V |
| Kemet T520 (SMD) | 10 | 100 | 0.025 | > 2000 | 7,3 × 5,7 × 4 | N/R ⁽²⁾ | ≤ 1 | T520V107M010ASE025 |
| AO-CAP | 6.3 | 100 | 0.018 | > 2900 | 7,3 × 5,7 × 4 | N/R ⁽²⁾ | ≤ 1 | A700V107M006AT |
| Vishay/Sprague 594D/SVP(SMD) | 35 20 | 47 100 | 0.280 0.025 | > 1000 3200 | 7,3 × 6 × 4,1 8 × 12 | 2 1 | ≤ 5 ≤ 2 | 595D476X0035R2T 94SVP107X0020E12 |
| 94SS | 20 | 150 | 0.030 | 3200 | 10 × 10,5 | 1 | ≤ 2 | 94SS157X0020FBP |
| Murata Ceramic X5R | 16 | 47 | 0.002 | > 1400 | 3225 | 1 ⁽⁴⁾ | ≤ 3 | GRM32ER61C476M $V_i < 14$ V |
| TDK ceramic X5R | 6.3 | 47 | 0.002 | > 1400 | 3225 | N/R ⁽²⁾ | ≤ 3 | C3225X5R0J476MT $V_o < 5.5$ V |
| Kemet Ceramic X5R | 6.3 | 47 | 0.002 | > 1400 | 3225 | N/R ⁽²⁾ | ≤ 3 | C1210C476K9PAC $V_o < 5.5$ V |
| TDK Ceramic X7R | 25 | 10 | 0.002 | > 1400 | 3225 | 1 ⁽⁴⁾ | ≤ 4 | C3225X7R1E106K |
| Murata Ceramic X5R | 25 | 10 | 0.002 | > 1400 | 3225 | 1 ⁽⁴⁾ | ≤ 4 | GRM32DR61E106KA12 |
| Kemet | 16 | 10 | 0.002 | > 1400 | 3225 | 1 ⁽⁴⁾ | ≤ 4 | C1210C106M4PAC $V_i < 14$ V |
| TDK Ceramic X7R | 25 | 2.2 | 0.002 | > 1400 | 3225 | 1 | 1 | C3225X7R1E225KT/MT |
| Murata Ceramic X7R | 25 | 2.2 | 0.002 | > 1400 | 3225 | 1 | 1 | GRM32RR71J225KC01L |
| Kemet | 25 | 2.2 | 0.002 | > 1400 | 3225 | 1 | 1 | C1210C225K3RAC |

- (1) The voltage rating of the input capacitor must be selected for the desired operating input voltage range of the regulator. To operate the regulator at a higher input voltage, select a capacitor with a higher voltage rating.
- (2) Not recommended (N/R). The voltage rating of this capacitor only allows it to be used for output voltages bus and voltage of < 5.5 V.
- (3) The voltage rating of the input capacitor must be selected for the desired operating input voltage range of the regulator. To operate the regulator at a higher input voltage, select a capacitor with a higher voltage rating.
- (4) Ceramic capacitors can be used to complement electrolytic types at the input bus by reducing high-frequency ripple current.

Power-Up Characteristics

When configured per the standard application, the PTH08080 power module produces a regulated output voltage following the application of a valid input source voltage. During power up, internal soft-start circuitry slows the rate that the output voltage rises, thereby limiting the amount of in-rush current that can be drawn from the input source. Figure 11 shows the power-up waveforms for a PTH08080W, operating from a 12-V input and with the output voltage adjusted to 1.8 V. The waveforms were measured with a 2-A resistive load.

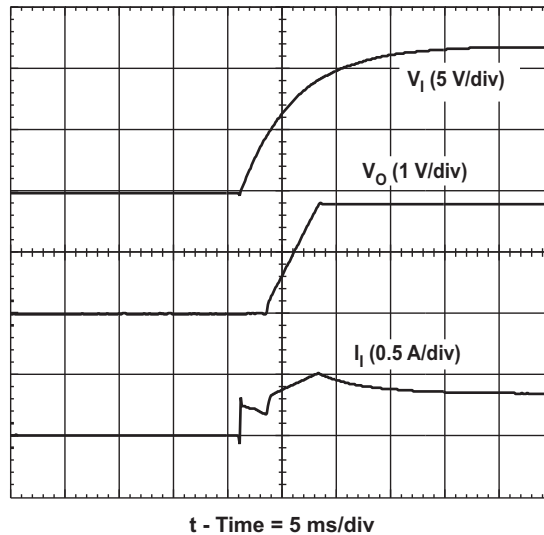


Figure 11. Power-Up Waveforms

Current Limit Protection

The PTH08080 modules protect against load faults with an output overcurrent trip. Under a load fault condition, the output current cannot exceed the current limit value. Attempting to draw current that exceeds the current limit value causes the output voltage to enter into a *hiccup* mode of operation, whereby the module continues in a cycle of successive shutdown and power up until the load fault is removed. On removal of the fault, the output voltage promptly recovers.

Thermal Shutdown

Thermal shutdown protects the module internal circuitry against excessively high temperatures. A rise in temperature may be the result of a drop in airflow, a high ambient temperature, or a higher than normal output current. If the junction temperature of the internal components exceeds 165°C, the module shuts down. This reduces the output voltage to zero. The module starts up automatically, by initiating a soft-start power up when the sensed temperature decreases 10°C below the thermal shutdown trip-point.

Output On/Off Inhibit

For applications requiring output voltage on/off control, the PTH08080 power module incorporates an output on/off Inhibit control (pin 5). The inhibit feature can be used wherever there is a requirement for the output voltage from the regulator to be turned off.

The power module functions normally when the Inhibit pin is left open-circuit, providing a regulated output whenever a valid source voltage is connected to V_1 with respect to GND.

Figure 12 shows the typical application of the inhibit function. Note the discrete transistor (Q1). The Inhibit control has its own internal pull-up to 3 volts. An open-collector or open-drain device is recommended to control this input. **Do not place an external pull-up on this pin.**

Turning Q1 on applies a low voltage to the *Inhibit* control pin and disables the output of the module. If Q1 is then turned off, the module executes a soft-start power-up sequence. A regulated output voltage is produced within 20 ms. Figure 13 shows the typical rise in the output voltage, following the turn off of Q1. The turn off of Q1 corresponds to the rise in the waveform, Q1 V_{DS} . The waveforms were measured with a 2-A resistive load.

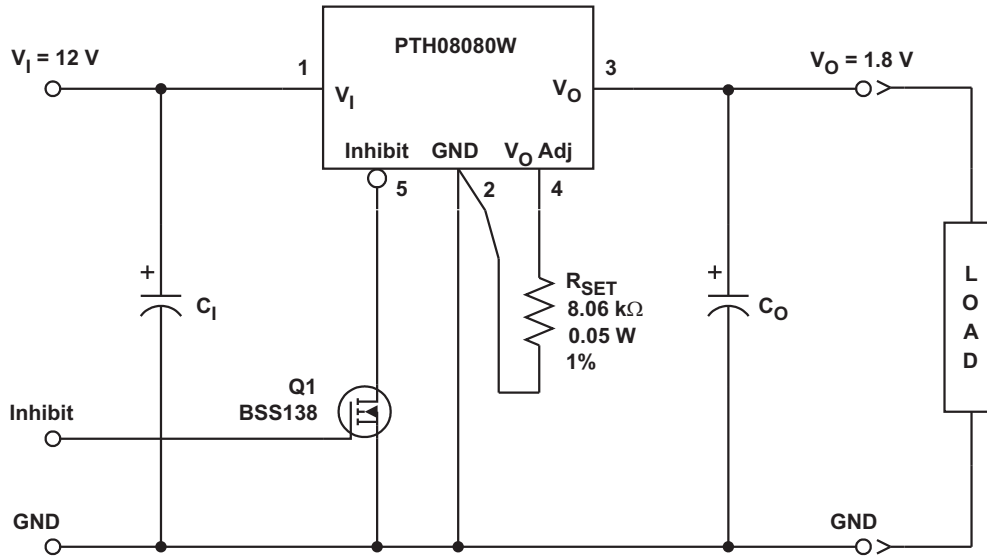


Figure 12. On/Off Inhibit Control Circuit

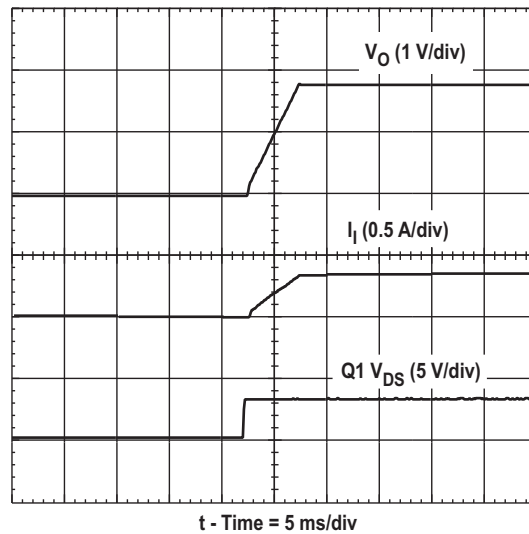


Figure 13. Power-Up Response From Inhibit Control

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| PTH08080WAD | ACTIVE | DIP MOD ULE | EUJ | 5 | 90 | Pb-Free (RoHS) | Call TI | N / A for Pkg Type |
| PTH08080WAH | ACTIVE | DIP MOD ULE | EUJ | 5 | 90 | Pb-Free (RoHS) | Call TI | N / A for Pkg Type |
| PTH08080WAS | ACTIVE | DIP MOD ULE | EUG | 5 | 90 | TBD | Call TI | Call TI |
| PTH08080WAST | ACTIVE | DIP MOD ULE | EUG | 5 | 250 | TBD | Call TI | Call TI |
| PTH08080WAZ | ACTIVE | DIP MOD ULE | EUG | 5 | 90 | Pb-Free (RoHS) | Call TI | Level-3-260C-168 HR |
| PTH08080WAZT | ACTIVE | DIP MOD ULE | EUG | 5 | 250 | Pb-Free (RoHS) | Call TI | Level-3-260C-168 HR |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

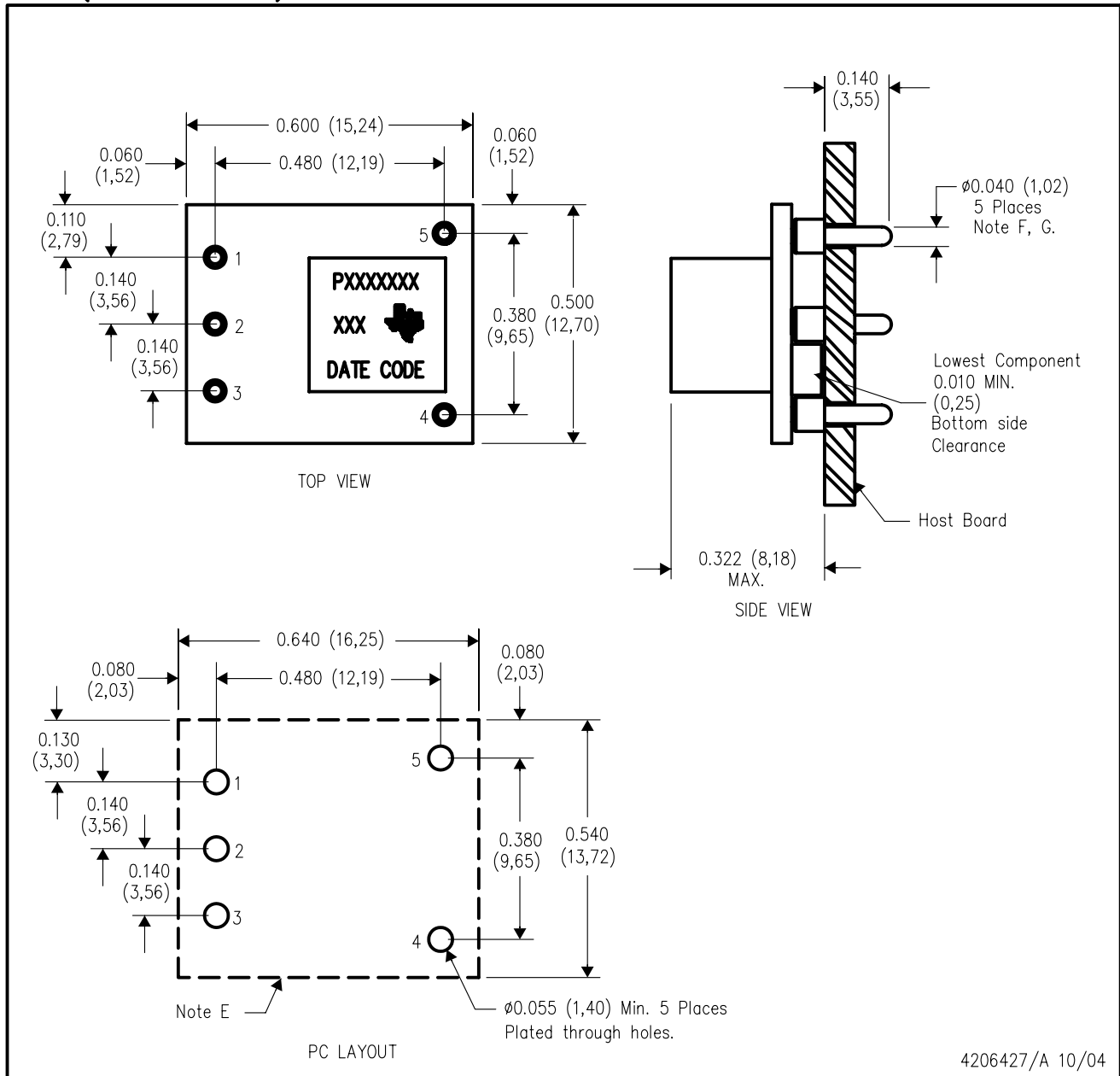
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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EUF (R-PDSS-T5)

DOUBLE SIDED MODULE



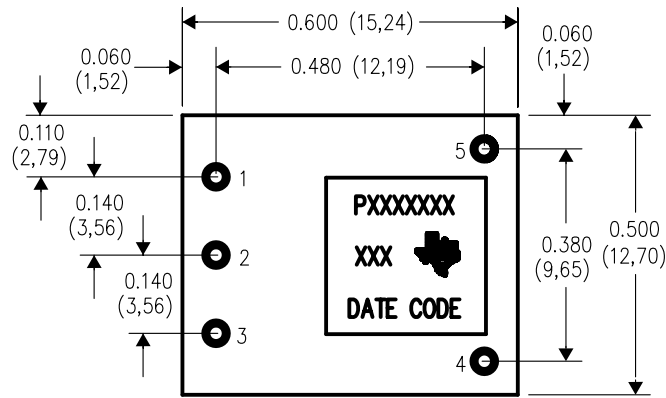
4206427/A 10/04

- NOTES:
- A. All linear dimensions are in inches (mm).
 - B. This drawing is subject to change without notice.
 - C. 2 place decimals are ± 0.030 ($\pm 0,76$ mm).
 - D. 3 place decimals are ± 0.010 ($\pm 0,25$ mm).
 - E. Recommended keep out area for user components.

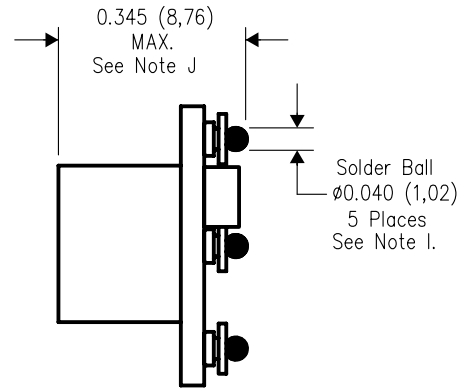
- F. Pins are 0.040" (1,02) diameter with 0.070" (1,78) diameter standoff shoulder.
- G. All pins: Material - Copper Alloy
Finish - Tin (100%) over Nickel plate

EUG (R-PDSS-B5)

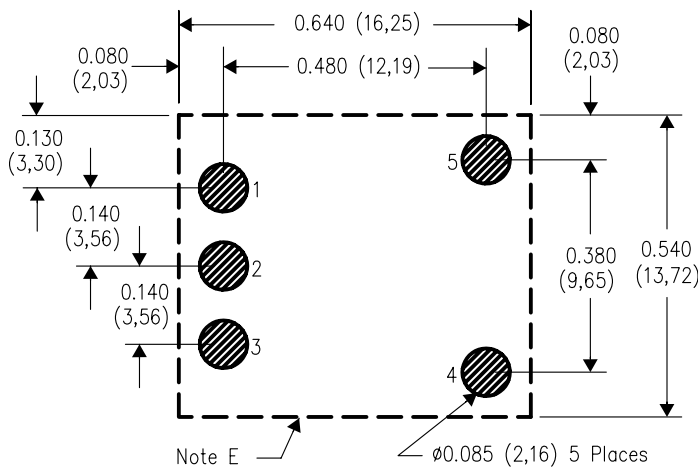
DOUBLE SIDED MODULE



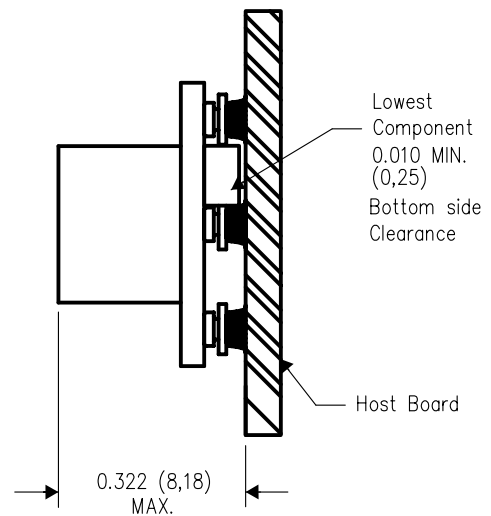
TOP VIEW



SIDE VIEW



PC LAYOUT



4206428/A 10/04

- NOTES:
- A. All linear dimensions are in inches (mm).
 - B. This drawing is subject to change without notice.
 - C. 2 place decimals are ± 0.030 ($\pm 0,76$ mm).
 - D. 3 place decimals are ± 0.010 ($\pm 0,25$ mm).
 - E. Recommended keep out area for user components.
 - F. Power pin connection should utilize two or more vias to the interior power plane of 0.025 (0,63) I.D. per input, ground and output pin (or the electrical equivalent).

- G. Paste screen opening: 0.080 (2,03) to 0.085 (2,16).
Paste screen thickness: 0.006 (0,15).
- H. Pad type: Solder mask defined.
- I. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate
Solder Ball – See product data sheet.
- J. Dimension prior to reflow solder.

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