

DUAL AUDIO OPERATIONAL AMPLIFIER

FEATURES

- Operating Voltage . . . ± 2 V to ± 18 V
- Low Noise Voltage . . . $1.2 \mu\text{V}_{\text{rms}}$ (Typ)
- Wide GBW . . . 15 MHz (Typ)
- Low THD . . . 0.05% (Typ)
- Slew Rate . . . $5.5 \text{ V}/\mu\text{sec}$ (Typ)
- Suitable for Applications Such as Audio Preamplifier, Active Filter, Headphone Amplifier, Industrial Measurement Equipment

DESCRIPTION/ORDERING INFORMATION

The RC4560 is a high-gain, wide-bandwidth, dual operational amplifier capable of driving 20 V peak-to-peak into 400- Ω loads. The RC4560 combines many of the features of the RC4558, but with wider bandwidth and higher slew rate, making this device ideal for active filters, data and telecommunications, and many instrumentation applications.

ORDERING INFORMATION⁽¹⁾

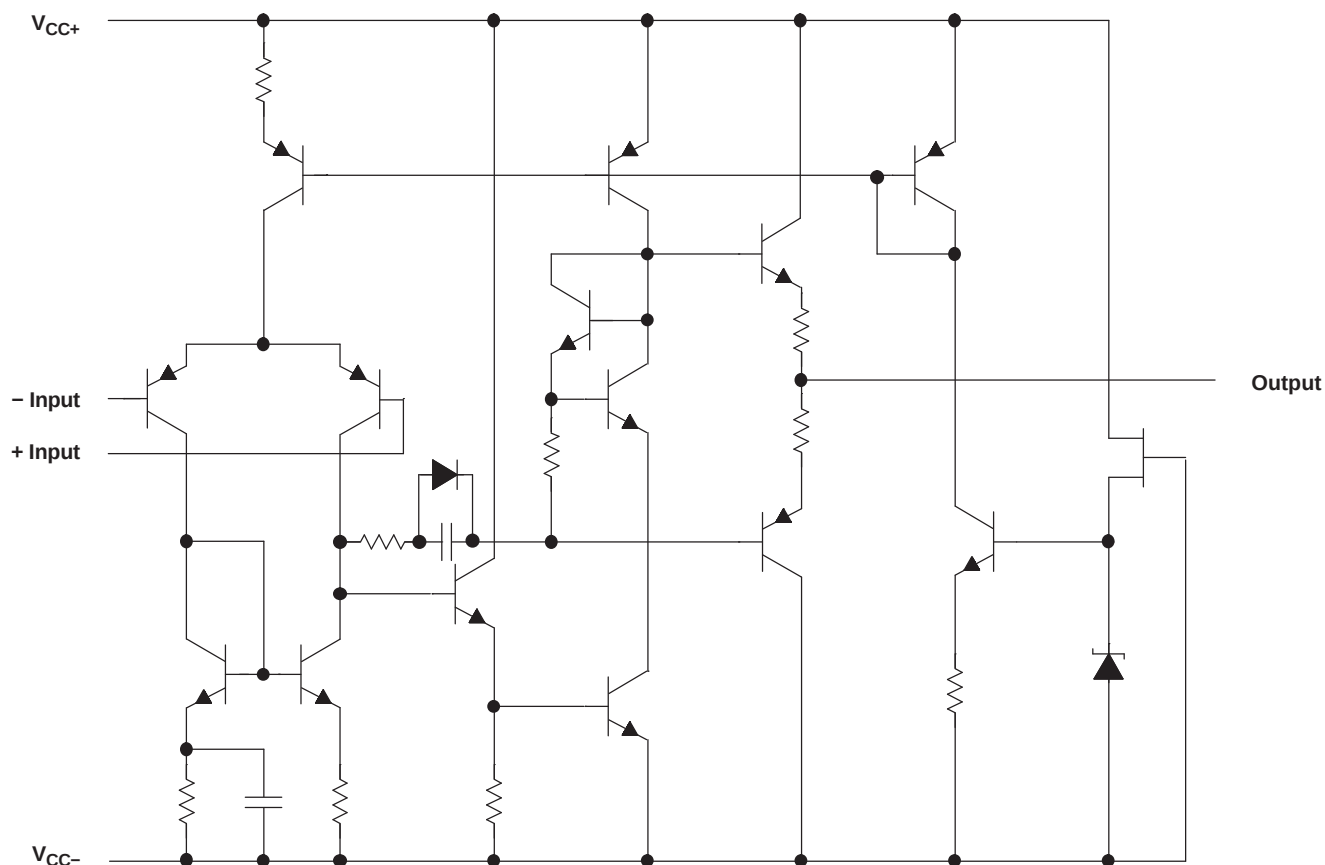
T_A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – P	Tube of 50	RC4560IP	RC4560IP
	SOIC – D	Tube of 75	RC4560ID	R4560I
		Reel of 2500	RC4560IDR	
	TSSOP – PW	Tube of 150	RC4560IPW	R4560I
		Reel of 2000	RC4560IPWR	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EQUIVALENT CIRCUIT**ABSOLUTE MAXIMUM RATINGS⁽¹⁾**

over operating free-air temperature range (unless otherwise noted)

$V_{CC\pm}$	Supply voltage		± 18 V
	Input voltage (any input)		± 15 V
	Output current		± 50 mA
θ_{JA}	Package thermal impedance ⁽²⁾⁽³⁾	D package	97°C/W
		P package	85°C/W
		PW package	149°C/W
T_J	Operating virtual junction temperature		150°C
T_{stg}	Storage temperature range		-60°C to 125°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Maximum power dissipation is a function of $T_J(\text{max})$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC+}	Supply voltage	2	16	V
V_{CC-}		–2	–16	
V_{ID}	Differential input voltage		±30	V
V_{ICR}	Input common mode range	–14	14	V
T_A	Operating free-air temperature range	–40	85	°C

ELECTRICAL CHARACTERISTICS

$V_{CC\pm} = \pm 15$ V, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO} Input offset voltage	$R_S \leq 10\text{ k}\Omega$		0.5	6	mV
I_{IO} Input offset current			5	200	nA
I_{IB} Input bias current			40	500	nA
A_{VD} Large-signal differential voltage amplification	$R_L \geq 2\text{ k}\Omega$, $V_O = \pm 10\text{ V}$	86	100		dB
r_i Input resistance		0.3	5		M Ω
V_O Output voltage swing	$R_L \geq 2\text{ k}\Omega$	±12	±14		V
	$I_O = 25\text{ mA}$	±10	±12.5		
V_{ICR} Common-mode input voltage range		±12	±14		V
CMRR Common-mode rejection ratio	$R_S \leq 10\text{ k}\Omega$	70	90		dB
k_{SVR} Supply-voltage rejection ratio ⁽¹⁾	$R_S \leq 10\text{ k}\Omega$	76.5	90		dB
I_{CC} Supply current (all amplifiers)			4.3	5.7	mA

(1) Measured with $V_{CC\pm}$ differentially varied simultaneously from ± 4 V to ± 15 V

OPERATING CHARACTERISTICS

$V_{CC\pm} = \pm 15$ V, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYP	UNIT
SR Slew rate at unity gain		5.5	V/ μs
GBW Gain bandwidth product		15	MHz
THD Total harmonic distortion	$V_O = 5\text{ V}$, $R_L = 2\text{ k}\Omega$, $f = 1\text{ kHz}$, $A_{VD} = 20\text{ dB}$	0.05	%
V_n Equivalent input noise voltage	RIAA, $R_S \leq 2\text{ k}\Omega$, 30-kHz LPF	1.2	μVrms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
RC4560ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R4560I	Samples
RC4560IDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R4560I	Samples
RC4560IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R4560I	Samples
RC4560IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R4560I	Samples
RC4560IDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R4560I	Samples
RC4560IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R4560I	Samples
RC4560IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	RC4560IP	Samples
RC4560IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	RC4560IP	Samples
RC4560IPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R4560I	Samples
RC4560IPWE4	ACTIVE	TSSOP	PW	8		TBD	Call TI	Call TI	-40 to 85		Samples
RC4560IPWG4	ACTIVE	TSSOP	PW	8		TBD	Call TI	Call TI	-40 to 85		Samples
RC4560IPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R4560I	Samples
RC4560IPWRE4	ACTIVE	TSSOP	PW	8		TBD	Call TI	Call TI	-40 to 85		Samples
RC4560IPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R4560I	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

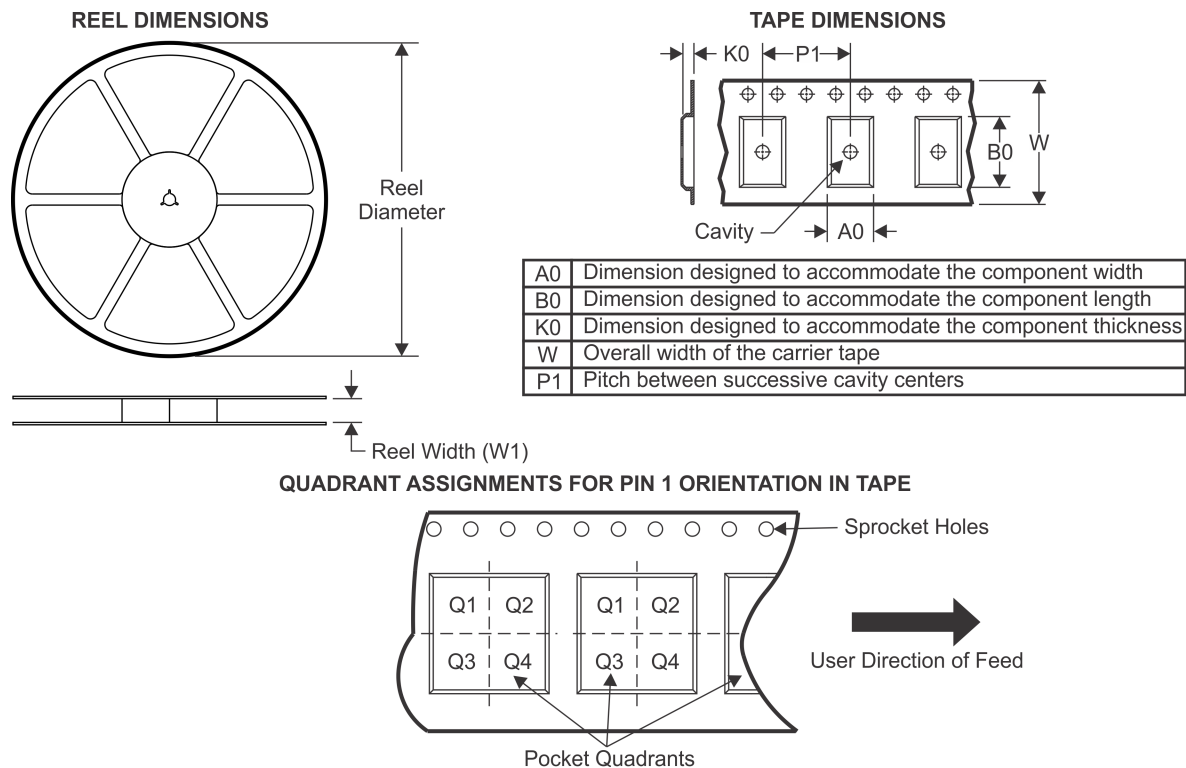
⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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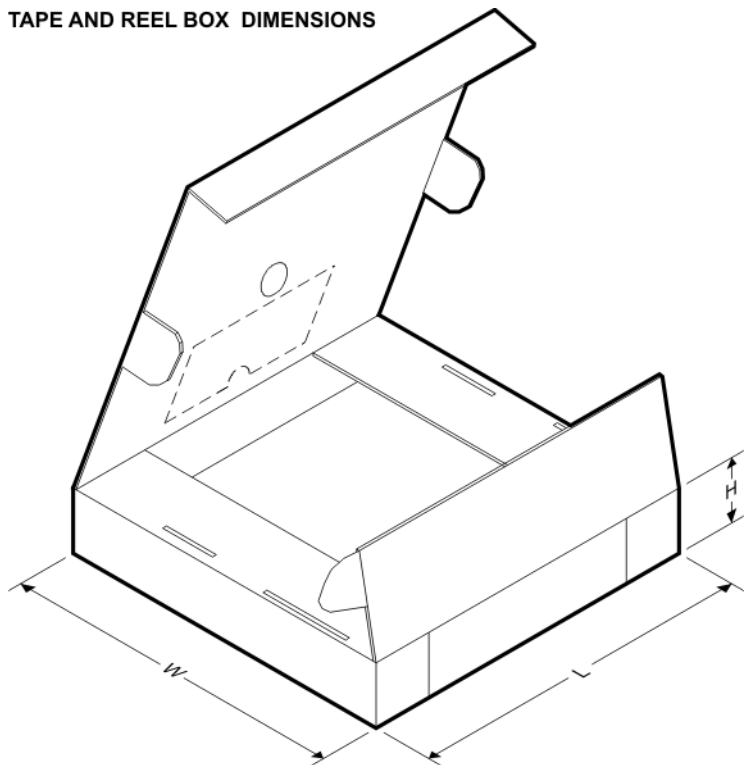
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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
RC4560IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
RC4560IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

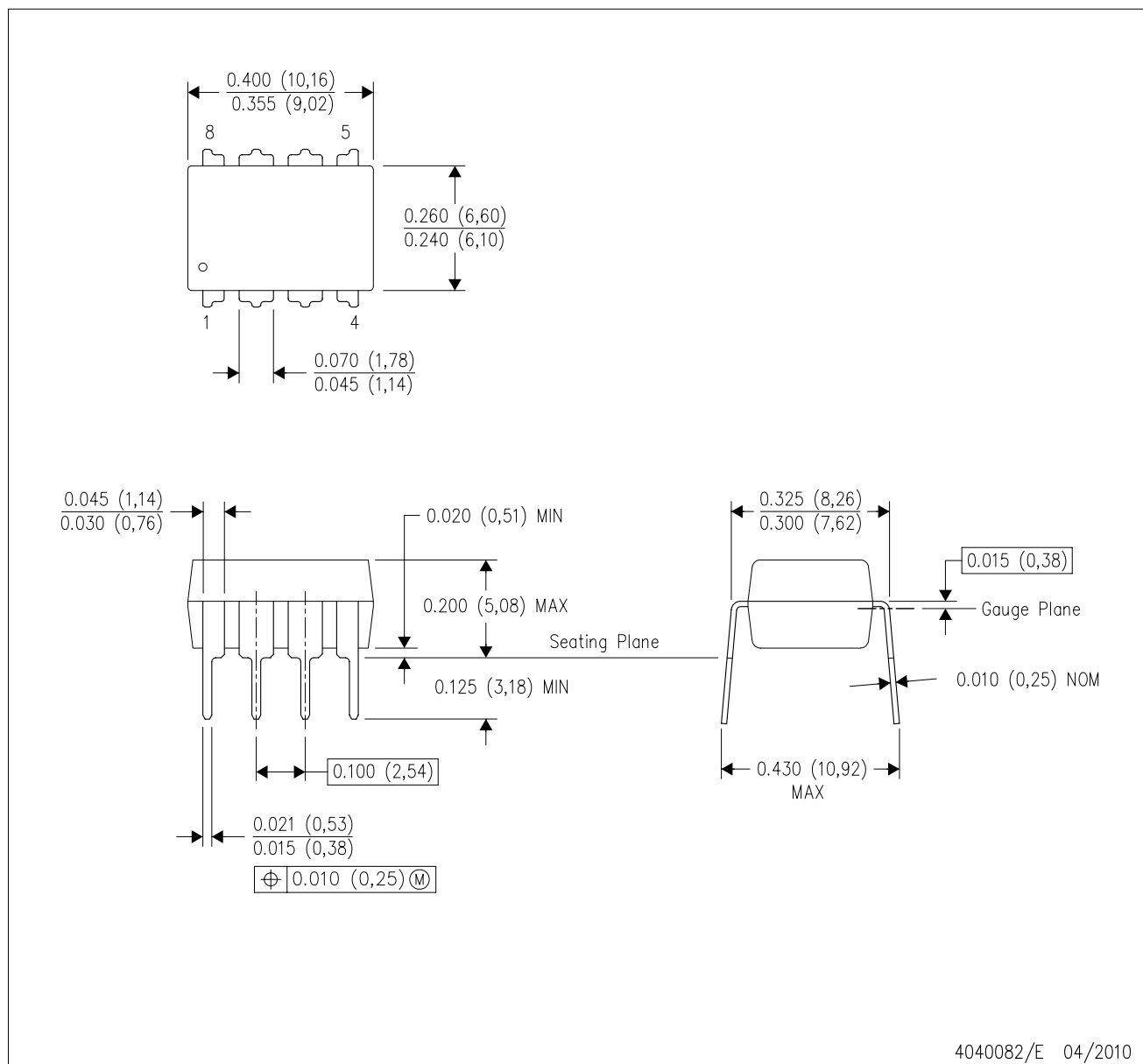


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
RC4560IDR	SOIC	D	8	2500	340.5	338.1	20.6
RC4560IPWR	TSSOP	PW	8	2000	367.0	367.0	35.0

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



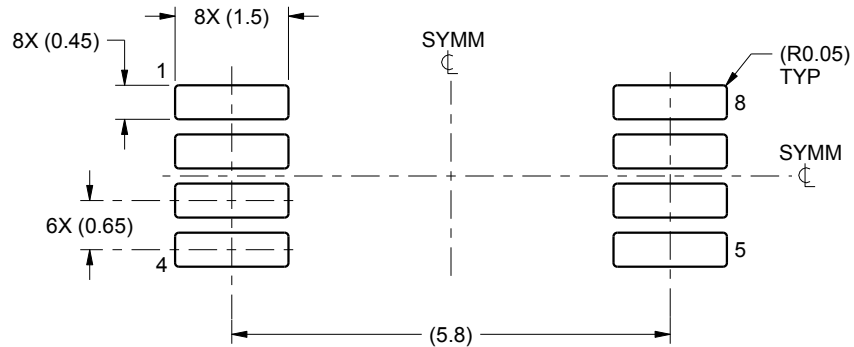
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

EXAMPLE BOARD LAYOUT

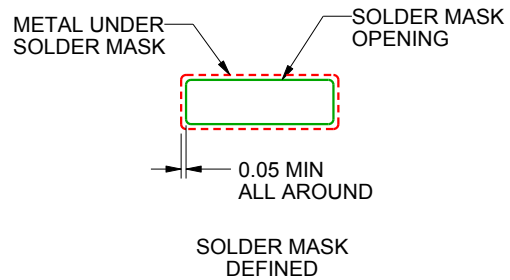
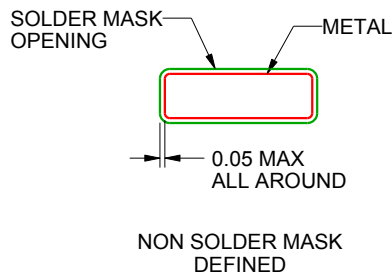
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

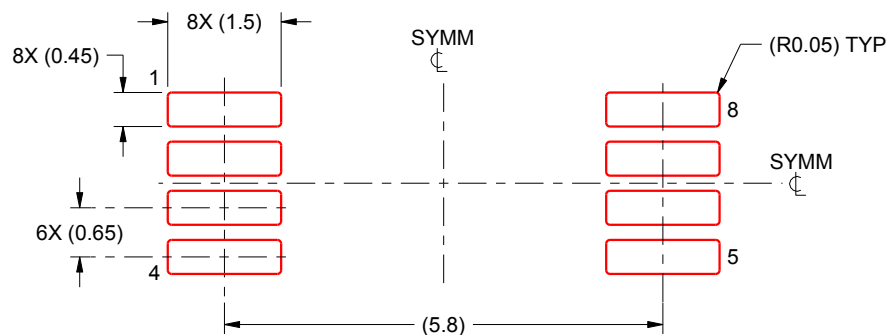
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

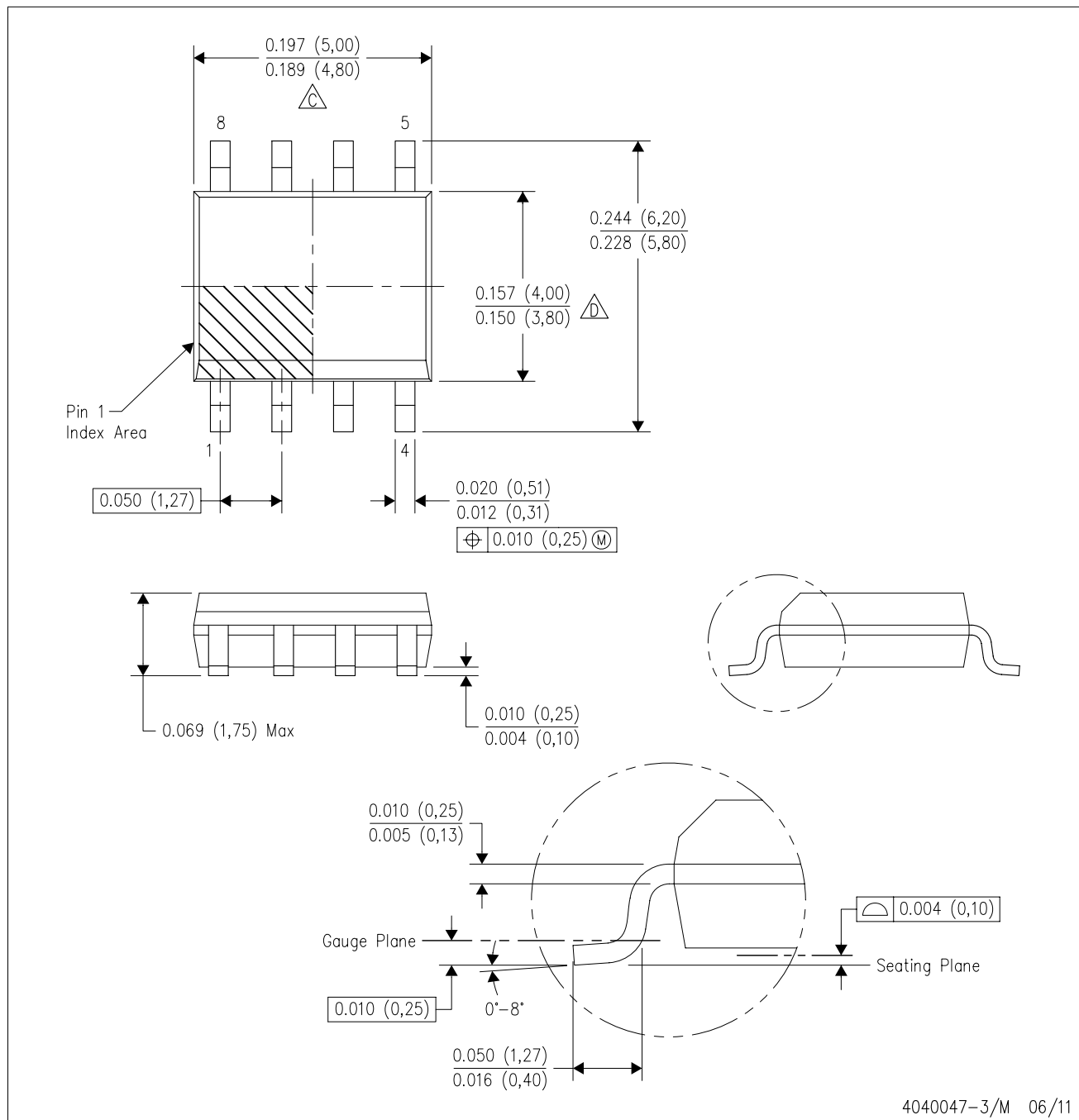
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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE

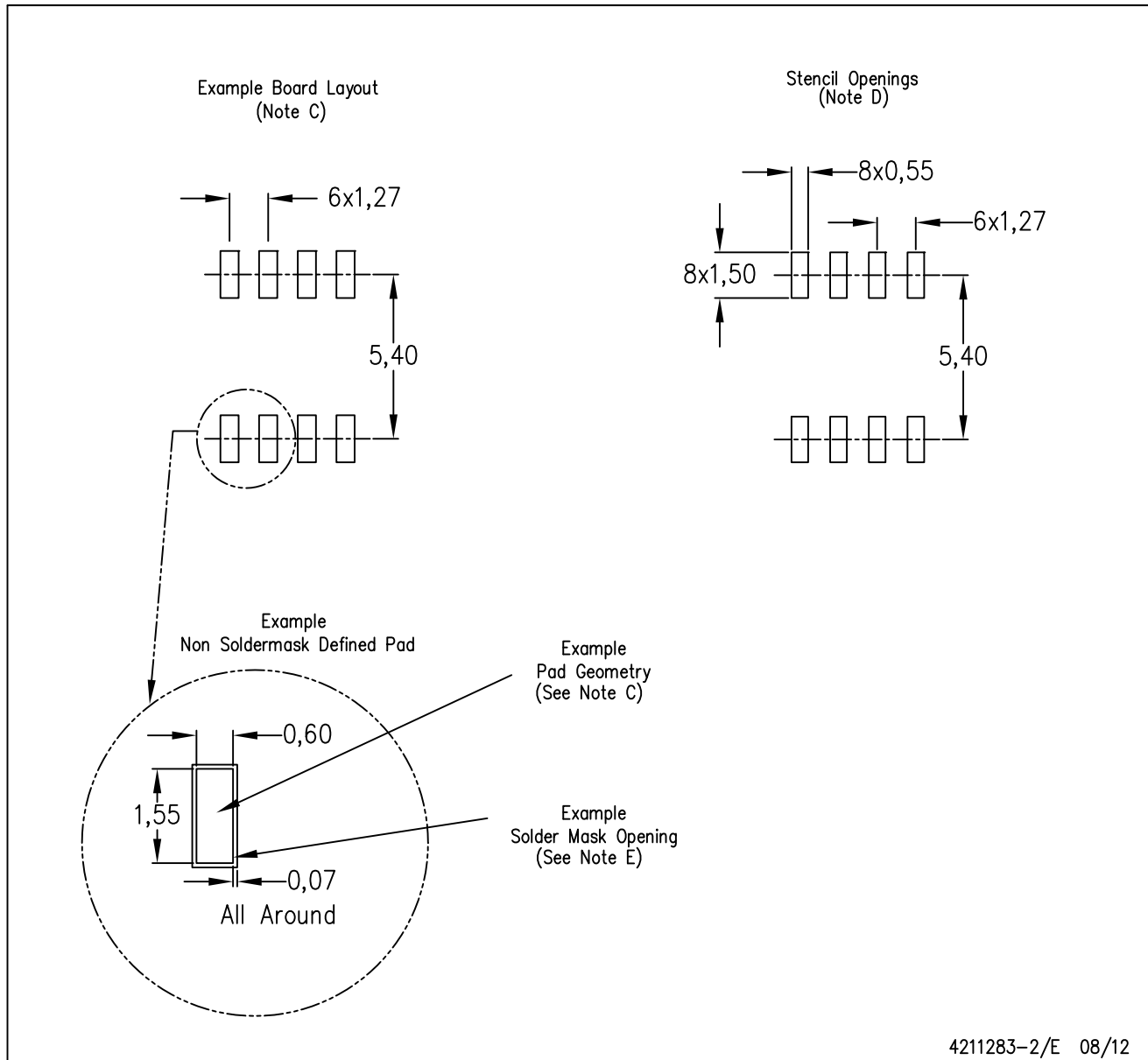


NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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