DC TO 4-GBPS DUAL 1:2 MULTIPLEXER/REPEATER/EQUALIZER

FEATURES

- **Receiver Equalization and Selectable Driver Preemphasis to Counteract High-Frequency Transmission Line Losses**
- **Integration of Two-Serial Port**
- **Selectable Loopback**
- **Typical Power Consumption 650 mW**
- **30-ps Deterministic Jitter**
- **On-Chip 100-Ω Receiver and Driver Differential Termination Resistors Eliminate External Components and Reflection from Stubs**
- **3.3-V Nominal Power Supply**
- **48-Terminal QFN (Quad Flatpack No-lead) 7 mm × 7 mm × 1 mm, 0.5-mm Terminal Pitch**

APPLICATIONS

- **Bidirectional Link Replicator**
- **Signal Conditioner**
- **XAUI 802.3ae Protocol Backplane Redundancy**
- **Host Adapter (Applications With Internal and External Connection to SERDES)**
- **Signaling Rates DC to 4 Gbps Including XAUI, GbE, FC, HDTV**

DESCRIPTION

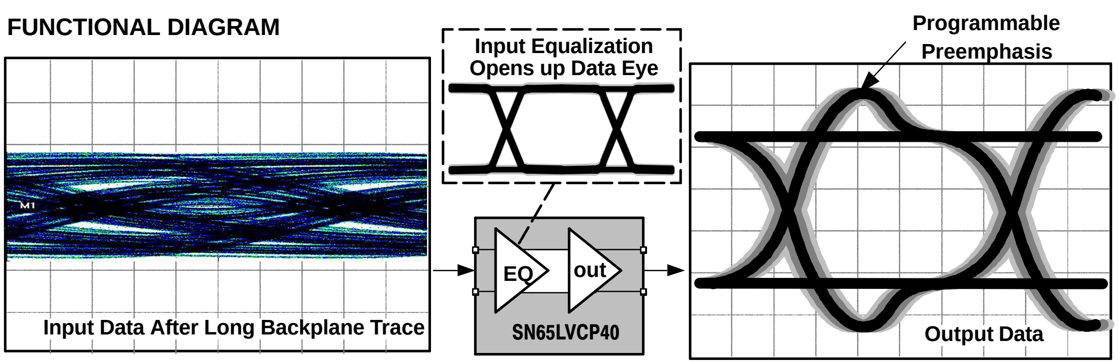
The SN65LVCP40 is a signal conditioner and data multiplexer optimized for backplanes. Input equalization and programmable output preemphasis support data rates up to 4 Gbps. Common applications are redundancy switching, signal buffering, or performance improvements on legacy backplane hardware.

The SN65LVCP40 combines a pair of 1:2 buffers with a pair of 2:1 multiplexers (mux). Selectable switch-side loopback supports system testing. System interconnects and serial backplane applications of up to 4 Gbps are supported. Each of the two independent channels consists of a transmitter with a fan-out of two, and a receiver with a 2:1 input multiplexer.

The drivers provide four selectable levels of preemphasis to compensate for transmission line losses. The receivers incorporates receive equalization and compensates for input transmission line loss. This minimizes deterministic jitter in the link. The equalization is optimized to compensate for a FR-4 backplane trace with 5-dB, high-frequency loss between 375 MHz and 1.875 MHz. This corresponds to a 24-inch long FR-4 trace with 6-mil trace width.

This device operates from a single 3.3-V supply. The device has integrated 100-Ω line termination and provides self-biasing. The input tolerates most differential signaling levels such as LVDS, LVPECL or CML. The output impedance matches 100-Ω line impedance. The inputs and outputs may be ac coupled for best interconnectivity with other devices such as SERDES I/O or additional XAUI multiplexer buffer. With ac coupling, jitter is the lowest.

FUNCTIONAL DIAGRAM



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

The SN65LVCP40 is packaged in a 7 mm × 7 mm × 1 mm QFN (quad flatpack no-lead) lead-free package, and is characterized for operation from 0°C to 85°C.

AVAILABLE OPTIONS

T_A	DESCRIPTION	PACKAGED DEVICE(1)
		RGZ (48 pin)
0°C to 85°C	Serial multiplexer	SN65LVCP40

(1) The package is available taped and reeled. Add an R suffix to device types (e.g., SN65LVCP40RGZR).

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

				UNIT
V_{CC}	Supply voltage range(2)			–0.5 V to 6 V
	Voltage range		Control inputs, all outputs	–0.5 V to (V_{CC} + 0.5 V)
			Receiver inputs	–0.5 V to 4 V
	ESD	Human Body Model(3)	All pins	4 kV
		Charged-Device Model(4)	All pins	500 V
	Continuous power dissipation			See Dissipation Rating Table
	Moisture sensitivity level			2
	Reflow temperature package soldering, 4 seconds			260°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

POWER DISSIPATION RATINGS

PACKAGE THERMAL CHARACTERISTICS(1)		NOM	UNIT
θ_{JA} (junction-to-ambient)	4-layer JEDEC Board (JESD51-7) using eight GND-vias Ø-0.2 on the center pad as shown in the section: *Recommended pcb footprint* with boundary and environment conditions of JEDEC Board (JESD51-2)	33.0	°C/W
θ_{JB} (junction-to-board)		20.0	°C/W
θ_{JC} (junction-to-case)		23.6	°C/W
PSI-jt (junction-to-top pseudo)		0.6	°C/W
PSI-jb (junction-to-board pseudo)		19.4	°C/W
θ_{JP} (junction-to-pad)		5.4	°C/W

(1) See application note SPRA953 for a detailed explanation of thermal parameters (http://www-s.ti.com/sc/psheets/spra953/spra953.pdf).

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
dR	Operating data rate				4.0	Gbps
V_{CC}	Supply voltage		3.135	3.3	3.465	V
$V_{CC(N)}$	Supply voltage noise amplitude	10 Hz to 2 GHz			20	mV
T_J	Junction temperature				125	°C
T_A	Operating free-air temperature (1)		0		85	°C
DIFFERENTIAL INPUTS						
V_{ID}	Receiver peak-to-peak differential input voltage (2)	$dR_{(in)} \leq$ 1.25 Gbps	100		1750	mVpp
		1.25 Gbps < $dR_{(in)} \leq$ 2.125 Gbps	100		1560	mVpp
		$dR_{(in)}$ > 3.125 Gbps	100		1000	mVpp
V_{ICM}	Receiver common-mode input voltage	Note: for best jitter performance ac coupling is recommended.	1.5	1.6	$V_{CC} - \frac{\lvert V_{ID}\rvert}{2}$	V
CONTROL INPUTS						
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
DIFFERENTIAL OUTPUTS						
R_L	Differential load resistance		80	100	120	Ω

(1) Maximum free-air temperature operation is allowed as long as the device maximum junction temperature is not exceeded.
(2) Differential input voltage V_{ID} is defined as | IN+ – IN– |.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
DIFFERENTIAL INPUTS						
V_{IT+}	Positive going differential input high threshold				50	mV
V_{IT-}	Negative going differential input low threshold		–50			mV
$A_{(EQ)}$	Equalizer gain	From 375 MHz to 1.875 GHz		5		dB
$R_{T(D)}$	Termination resistance, differential		80	100	120	Ω
V_{BB}	Open-circuit Input voltage (input self-bias voltage)	AC-coupled inputs		1.6		V
$R_{(BBDC)}$	Biasing network dc impedance			30		kΩ
$R_{(BBAC)}$	Biasing network ac impedance	375 MHz		42		Ω
		1.875 GHz		8.4		
DIFFERENTIAL OUTPUTS						
V_{OH}	High-level output voltage	R_L = 100 Ω±1%, PRES_1 = PRES_0=0; PREL_1 = PREL_0=0; 4.0 Gbps alternating 1010-pattern; Figure 1		650		mVpp
V_{OL}	Low-level output voltage			–650		mVpp
$V_{ODB(PP)}$	Output differential voltage without preemphasis (2)		1000	1300	1500	mVpp
V_{OCM}	Output common mode voltage	See Figure 6		1.65		V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states			1		mV

(1) All typical values are at T_A = 25°C and V_{CC} = 3.3 V supply unless otherwise noted. They are for reference purposes and are not production tested.
(2) Differential output voltage $V_{(ODB)}$ is defined as | OUT+ – OUT– |.

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
$V_{(PE)}$	Output preemphasis voltage ratio, $\frac{V_{ODB(PP)}}{V_{ODPE(PP)}}$	RL = 100 Ω± 1%; x = L or S; See Figure 1	PREx_1:PREx_0 = 00		0		dB
			PREx_1:PREx_0 = 01		3		
			PREx_1:PREx_0 = 10		6		
			PREx_1:PREx_0 = 11		9		
$t_{(PRE)}$	Preemphasis duration measurement	Output preemphasis is set to 9 dB during test PREx_x = 1; Measured with a 100-MHz clock signal; R_L = 100 Ω, ±1%, See Figure 2			175		ps
r_o	Output resistance	Differential on-chip termination between OUT+ and OUT–			100		Ω
CONTROL INPUTS							
I_{IH}	High-level Input current	VIN = VCC				5	µA
I_{IL}	Low-level Input currentn	VIN = GND			90	125	µA
$R_{(PU)}$	Pullup resistance				35		kΩ
POWER CONSUMPTION							
P_D	Device power dissipation	All outputs terminated 100 Ω			650	880	mW
I_{CC}	Device current consumption	All outputs terminated 100 Ω	PRBS 2^{7-1} pattern at 4 Gbps			254	mA

SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
MULTIPLEXER						
$t_{(SM)}$	Multiplexer switch time	Multiplexer or loopback control to valid output		3	6	ns
DIFFERENTIAL OUTPUTS						
t_{PLH}	Low-to-high propagation delay	Propagation delay input to output See Figure 4		0.5	1	ns
t_{PHL}	High-to-low propagation delay			0.5	1	ns
t_r	Rise time	20% to 80% of $V_{O(DB)}$; Test Pattern: 100-MHz clock signal; See Figure 3 and Figure 7		80		ps
t_f	Fall time			80		ps
$t_{sk(p)}$	Pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$(2)				20	ps
$t_{sk(o)}$	Output skew(3)	All outputs terminated with 100 Ω		25	200	ps
$t_{sk(pp)}$	Part-to-part skew(4)				500	ps
RJ	Device random jitter, rms	See Figure 7for test circuit. BERT setting 10^{-15} Alternating 10-pattern.		0.8	2	ps-rms

(1) All typical values are at 25°C and with 3.3 V supply unless otherwise noted.
(2) $t_{sk(p)}$ is the magnitude of the time difference between the t_{PLH} and t_{PHL} of any output of a single device.
(3) $t_{sk(o)}$ is the magnitude of the time difference between the t_{PLH} and t_{PHL} of any two outputs of a single device.
(4) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

PARAMETER		TEST CONDITIONS			MIN	TYP[1]	MAX	UNIT
DJ	Intrinsic deterministic device jitter [5][6], peak-to-peak	0 dB preemphasis (PREx_x = 0); See Figure 7 for the test circuit.	PRBS 2^{7-1} pattern	4 Gbps			30	ps
	Absolute deterministic output jitter[7], peak-to-peak	0 dB preemphasis (PREx_x = 0); See Figure 7 for the test circuit.	PRBS 2^{7-1} pattern	1.25 Gbps Over 20-inch FR4 trace		7		ps
				4 Gbps Over FR4 trace 2-inch to 20 inches long		20		

(5) Intrinsic deterministic device jitter is a measurement of the deterministic jitter contribution from the device. It is derived by the equation ($DJ_{(OUT)}$– $DJ_{(IN)}$), where $DJ_{(OUT)}$ is the total peak-to-peak deterministic jitter measured at the output of the device in pspp. $DJ_{(IN)}$ is the peak-to-peak deterministic jitter of the pattern generator driving the device.
(6) The SN65LVCP40 built-in passive input equalizer compensates for ISI. For a 20-inch FR4 transmission line with 8-mil trace width, the LVCP40 typically reduces jitter by 60 ps from the device input to the device output.
(7) Absolute deterministic output jitter reflects the deterministic jitter measured at the SN65LVCP40 output. The value is a real measured value with a Bit error tester as described in Figure 7. The absolute DJ reflects the sum of all deterministic jitter components accumulated over the link: $DJ_{(absolute)} = DJ_{(Signal\ generator)} + DJ_{(transmission\ line)} + DJ_{(intrinsic(LVCP40))}$.

PIN ASSIGNMENTS

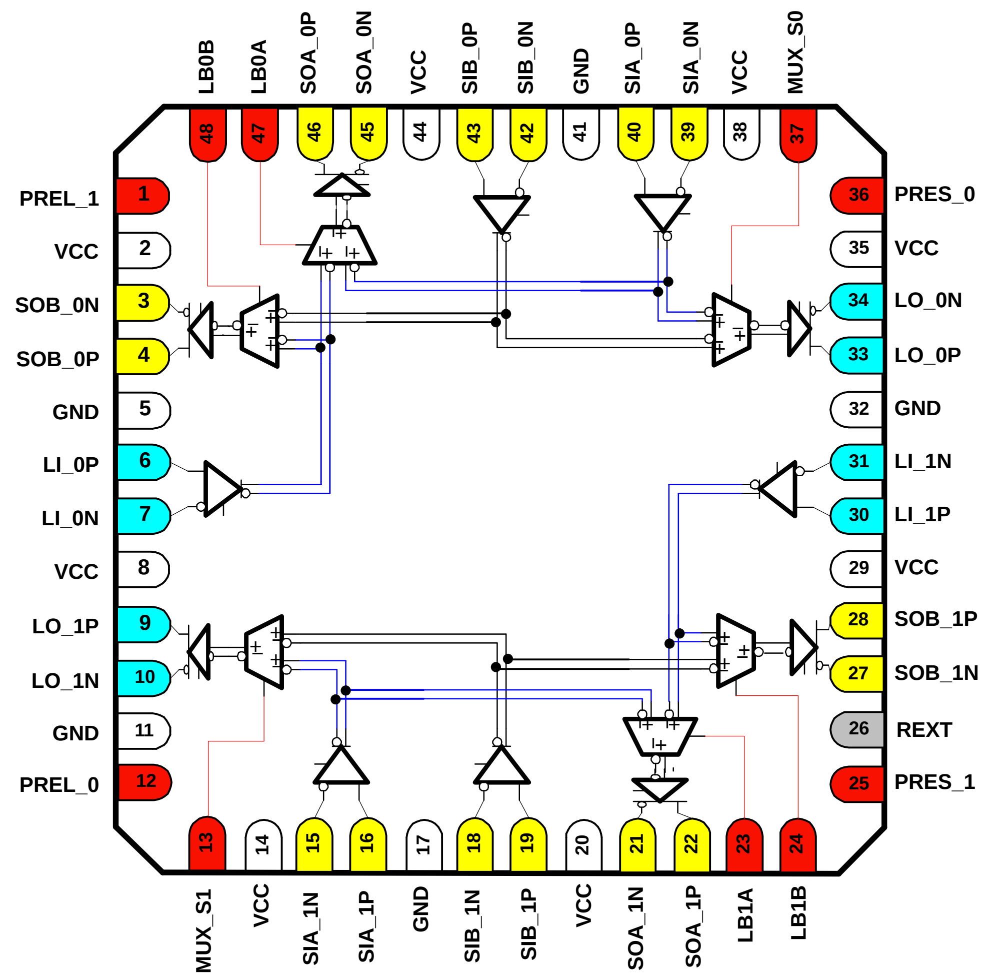
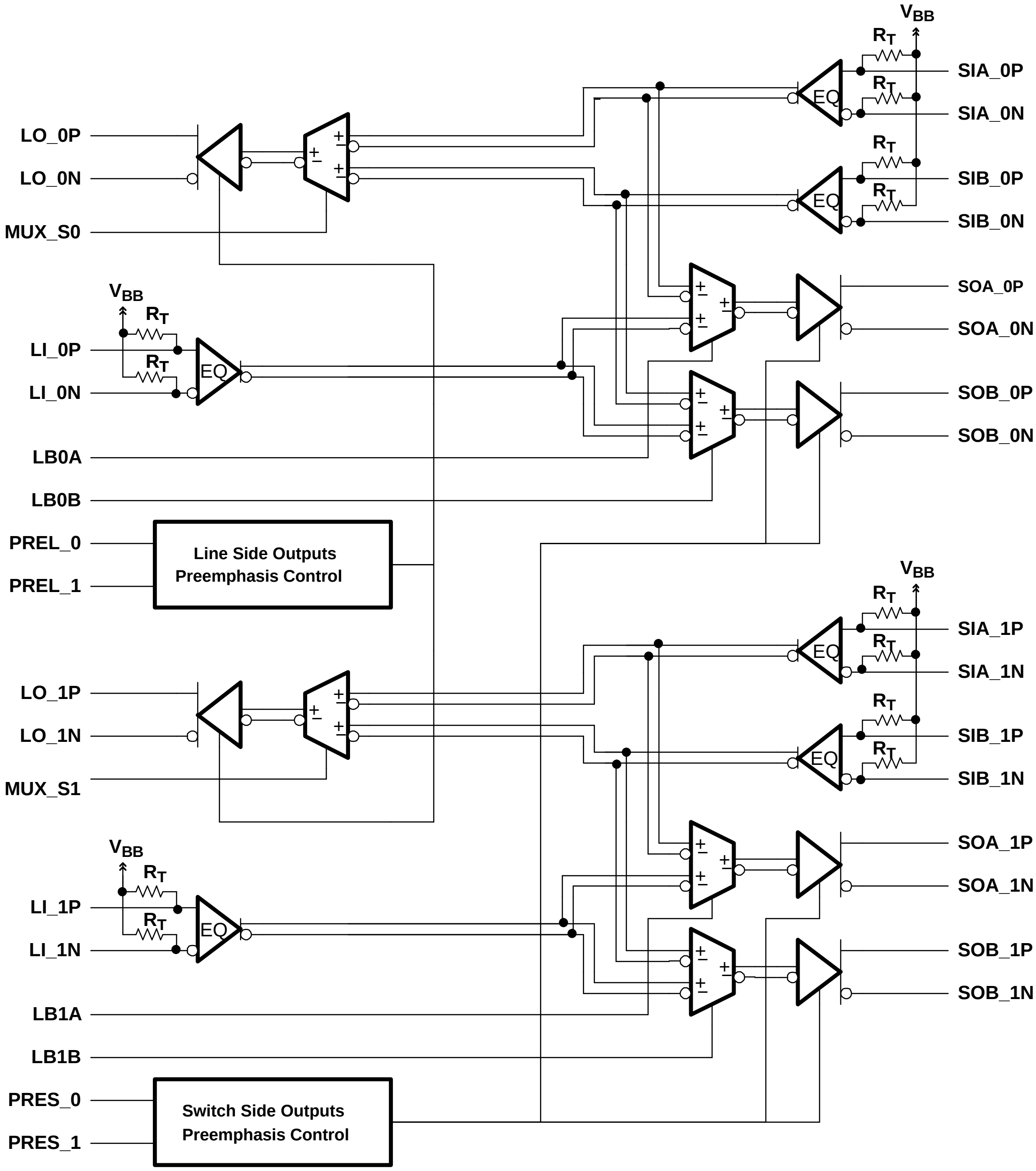


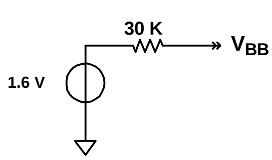
Table 1. Signal Descriptions

SIGNAL	PIN(S)	TYPE	SIGNAL TYPE	DESCRIPTION
LINE SIDE HIGH-SPEED I/O				
LI_0P LI_0N	6 7	I (w/ 50-Ω termination to VBB)	PECL/CML compatible	Differential input, port_0 line side
LI_1P LI_1N	30 31	I (w/ 50-Ω termination to VBB)	PECL/CML compatible	Differential input, port_1 line side
LO_0P LO_0N	33 34	O	VML(1)	Differential output, port_0 line side
LO_1P LO_1N	9 10	O	VML(1)	Differential output, port_1 line side
SWITCH SIDE HIGH-SPEED I/O				
SIA_0P SIA_0N	40 39	I (w/ 50-Ω termination to VBB)	CML/PECL compatible	Differential input, mux_0 switch_A_side
SIB_0P SIB_0N	43 42	I (w/ 50-Ω termination to VBB)	CML/PECL compatible	Differential input, mux_0 switch_B_side
SIA_1P SIA_1N	16 15	I (w/ 50-Ω termination to VBB)	CML/PECL compatible	Differential input, mux_1 switch_A_side
SIB_1P SIB_1N	19 18	I (w/ 50-Ω termination to VBB)	CML/PECL compatible	Differential input, mux_1 switch_B_side
SOA_0P SOA_0N	46 45	O	VML(1)	Differential output, mux_0 switch_A_side
SOB_0P SOB_0N	4 3	O	VML(1)	Differential output, mux_0 switch_B_side
SOA_1P SOA_1N	22 21	O	VML(1)	Differential output, mux_1 switch_A_side
SOB_1P SOB_1N	28 27	O	VML(1)	Differential output, mux_1 switch_B_side
CONTROL SIGNALS				
PREL_0 PREL_1	12 1	I (w/ 35-kΩ pullup)	LVTTL	Output preemphasis control, line side port_0 and port_1. Has internal pull-up. See **Preemphasis Controls PREL_0, PREL_1, PRES_0 and PRES** for function definition.
PRES_0 PRES_1	36 25	I (w/ 35-kΩ pullup)	LVTTL	Output preemphasis control, switch side port_0 and port_1. See **Preemphasis Controls PREL_0, PREL_1, PRES_0 and PRES** for function definition.
LB0A LB0B	47 48	I (w/ 35-kΩ pullup)	LVTTL	Loopback control for mux_0 switch side. See **Loopback Controls LB0A, LB0B, LB1A and LB1B** for function definition.n
LB1A LB1B	23 24	I (w/ 35-kΩ pullup)	LVTTL	Loopback control for mux_1 switch side. See **Loopback Controls LB0A, LB0B, LB1A and LB1B** for function definition.n
MUX_S0 MUX_S1	37 13	I (w/ 35-kΩ pullup)	LVTTL	Port A and B multiplex control of mux_0 and mux_1. See **Multiplex Controls MUX_S0 and MUX_S1** for function definition.
REXT	26		N/A	No connect. This pin is unused and can be left open or tied to GND with any resistor.
POWER SUPPLY				
VCC	2, 8, 14, 20, 29, 35	PWR		Power supply 3.3 V ±5%
GND	5, 11, 17, 32, 41	PWR		Power supply return
GND Center Pad		PWR		The ground center pad is the metal contact at the bottom of the 48-pin package. It must be connected to the GND plane. At least 4 vias are recommended to minimize inductance and provide a solid ground. See the package drawing for the via placement.

(1) VML stands for Voltage Mode logic; VML provides a differential output impedance of 100-Ω. VML offers the benefits of CML and consumes less power.

FUNCTIONAL BLOCK DIAGRAM





Note:

V_{BB}: Receiver input internal biasing voltage (allows ac coupling)
EQ: Input Equalizer (compensates for frequency dependent transmission line loss of backplanes)
R_T: Internal 50−Ohm receiver termination (100−Ohm differential)
Preemphasis: Output precompensation for transmission line losses

FUNCTIONAL DEFINITIONS

Table 2. Multiplex Controls MUX_S0 and MUX_S1

MUX_Sn(1)	MUX FUNCTION
0	MUX_n select input B
1	MUX_n select input A

(1) n = 0 or 1

Table 3. Loopback Controls LB0A, LB0B, LB1A and LB1B

LBnx(1)	LOOPBACK FUNCTION
0	Enable loopback of six input to SOx output
1	Disable loopback of six input to SOx output

(1) n = 0 or 1, x = A or B

Table 4. Multiplexer and Loopback Controls

INPUTS / OUTPUTS	SOA_0	SOB_0	SOA_1	SOB_1	LO_0	LO_1
SIA_0	LB0A = 1	x	x	x	MUX_S0 = 1	x
SIB_0	x	LB0B = 1	x	x	MUX_S0 = 0	x
SIA_1	x	x	LB1A = 1	x	x	MUX_S1 = 1
SIB_1	x	x	x	LB1B =1	x	MUX_S1 =01
LI_0	LB0A = 0	LB0B = 0	x	x	x	x
LI_1	x	x	LB1A = 0	LB1B = 0	x	x

Table 5. Preemphasis Controls PREL_0, PREL_1, PRES_0, and PRES_1

PREx_1(1)	PREx_0(1)	OUTPUT PREEMPHASIS LEVEL IN dB	OUTPUT LEVEL IN mVpp		TYPICAL FR4 TRACE LENGTH
			DEEMPHASIZED	PREEMPHASIZED	
0	0	0 dB	1200	1200	10 inches of FR4 trace
0	1	3 dB	850	1200	20 inches of FR4 trace
1	0	6 dB	600	1200	30 inches of FR4 trace
1	1	9 dB	425	1200	40 inches of FR4 trace

(1) x = L or S

Preemphasis is the primary signal conditioning mechanism. See Figure 1 and Figure 2 for further definition.

Equalization is secondary signal conditioning mechanism. The input stage provides 5-dB of fixed equalization gain from 375 MHz to 1.875 GHz (optimized for 3.75-Gbps 8B10B coded data).

PARAMETER MEASUREMENT INFORMATION

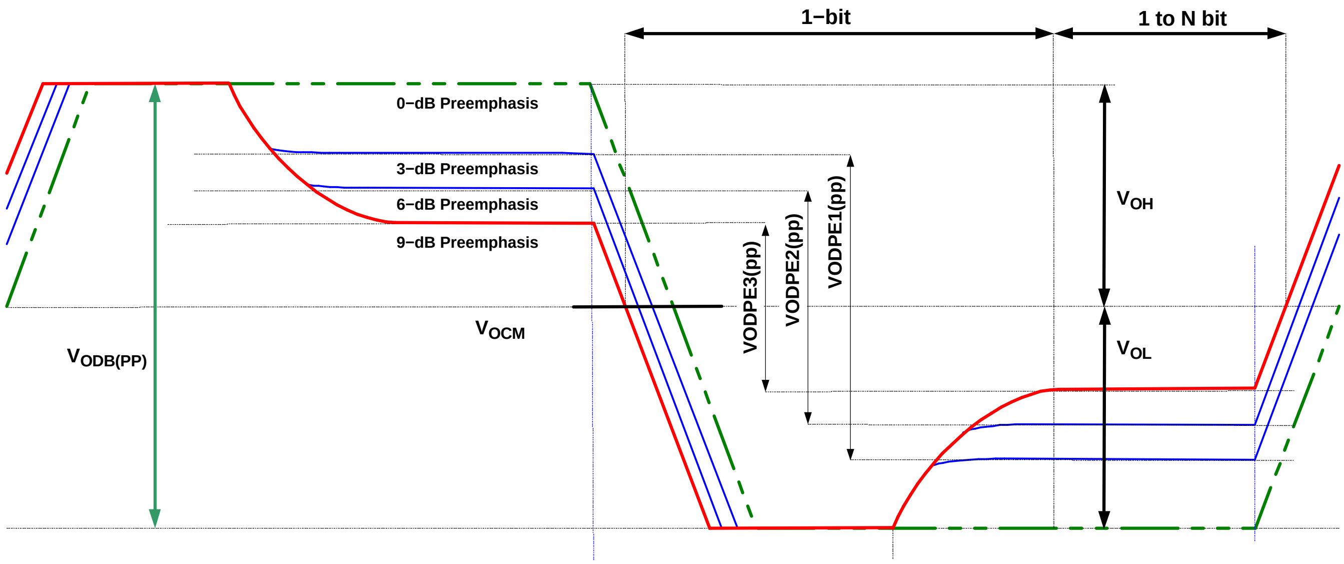


Figure 1. Preemphasis and Output Voltage Waveforms and Definitions

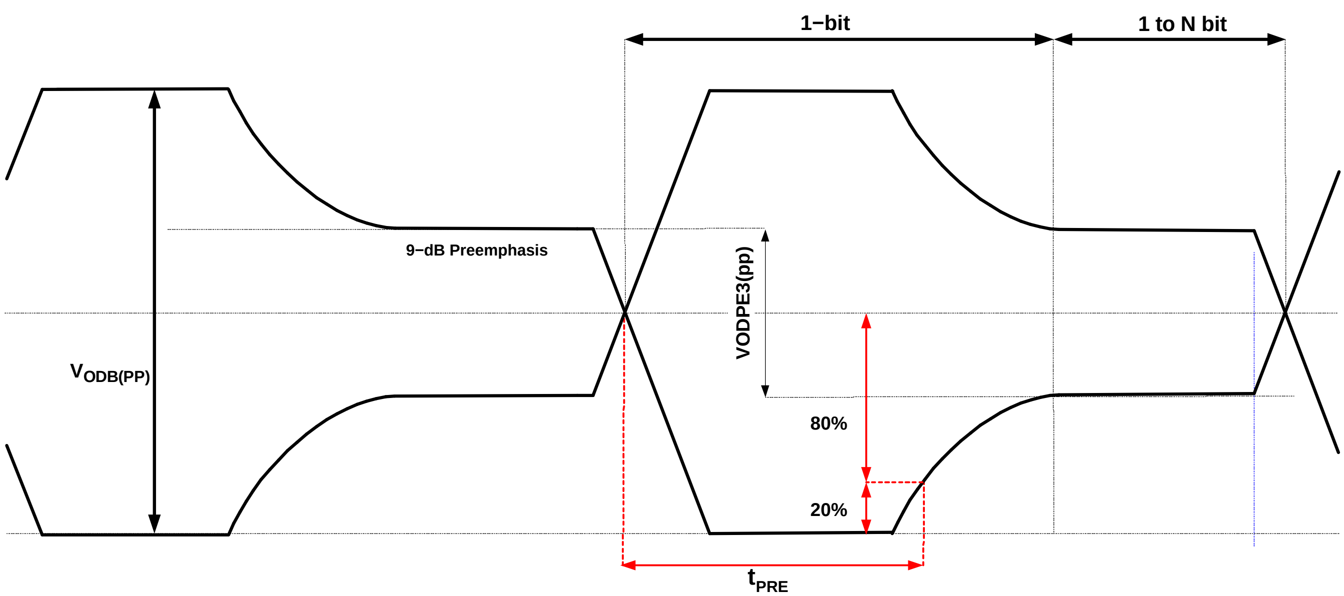


Figure 2. $t_{(PRE)}$) Preemphasis Duration Measurement

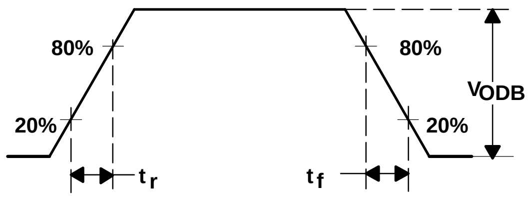


Figure 3. Driver Output Transition Time

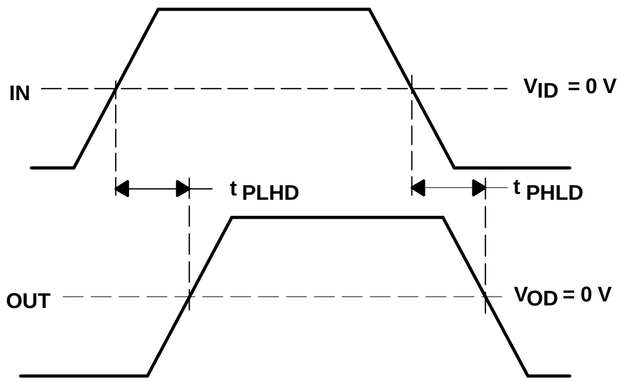


Figure 4. Propagation Delay Input to Output

CIRCUIT DIAGRAMS

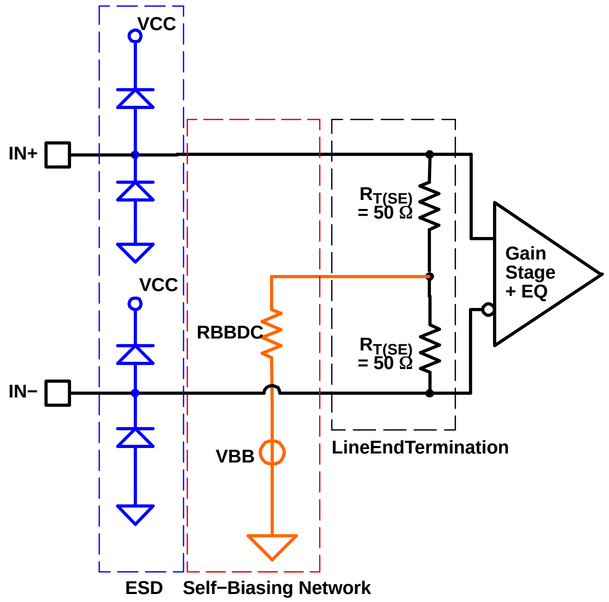


Figure 5. Equivalent Input Circuit Design

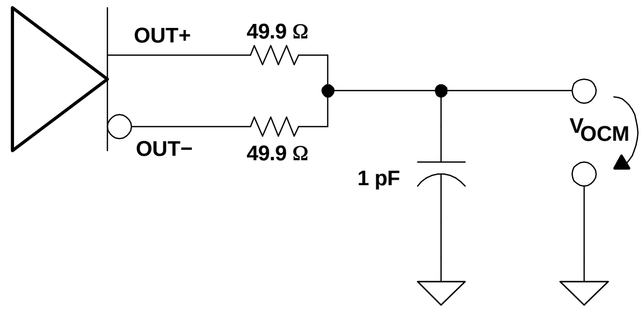
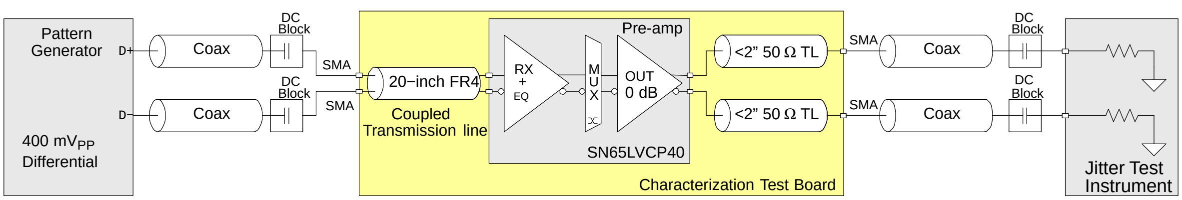


Figure 6. Common-Mode Output Voltage Test Circuit

JITTER TEST CIRCUIT

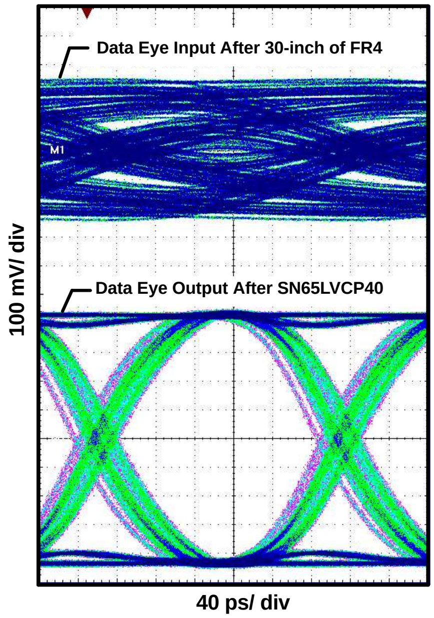


NOTE: For the Jitter Test, the preemphasis level of the output is set to 0 dB (PREx_x=0)

Figure 7. AC Test Circuit – Jitter and Output Rise Time Test Circuit

The SN65LVCP40 input equalizer provides 5-dB frequency gain to compensate for frequency loss of a shorter backplane transmission line. For characterization purposes, a 24-inch FR-4 coupled transmission line is used in place of the backplane trace. The 24-inch trace provides roughly 5 dB of attenuation between 375 MHz and 1.875 GHz, representing closely the characteristics of a short backplane trace. The loss tangent of the FR4 in the test board is 0.018 with an effective ε(r) of 3.1.

TYPICAL DEVICE BEHAVIOR



NOTE: 30 Inch Input Trace, dR = 4 Gbps; 2^{7-1} PRBS

Figure 8. Data Input and Output Pattern

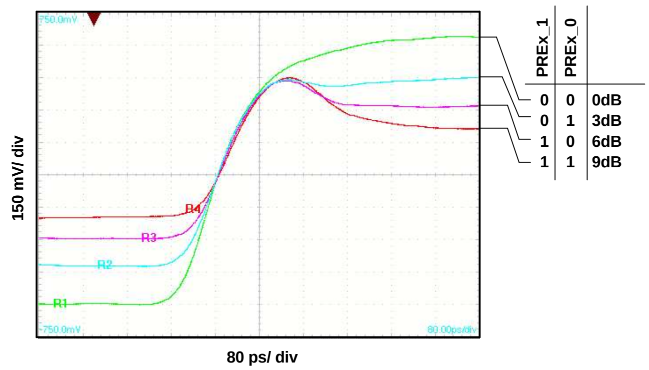


Figure 9. Preemphasis Signal Shape

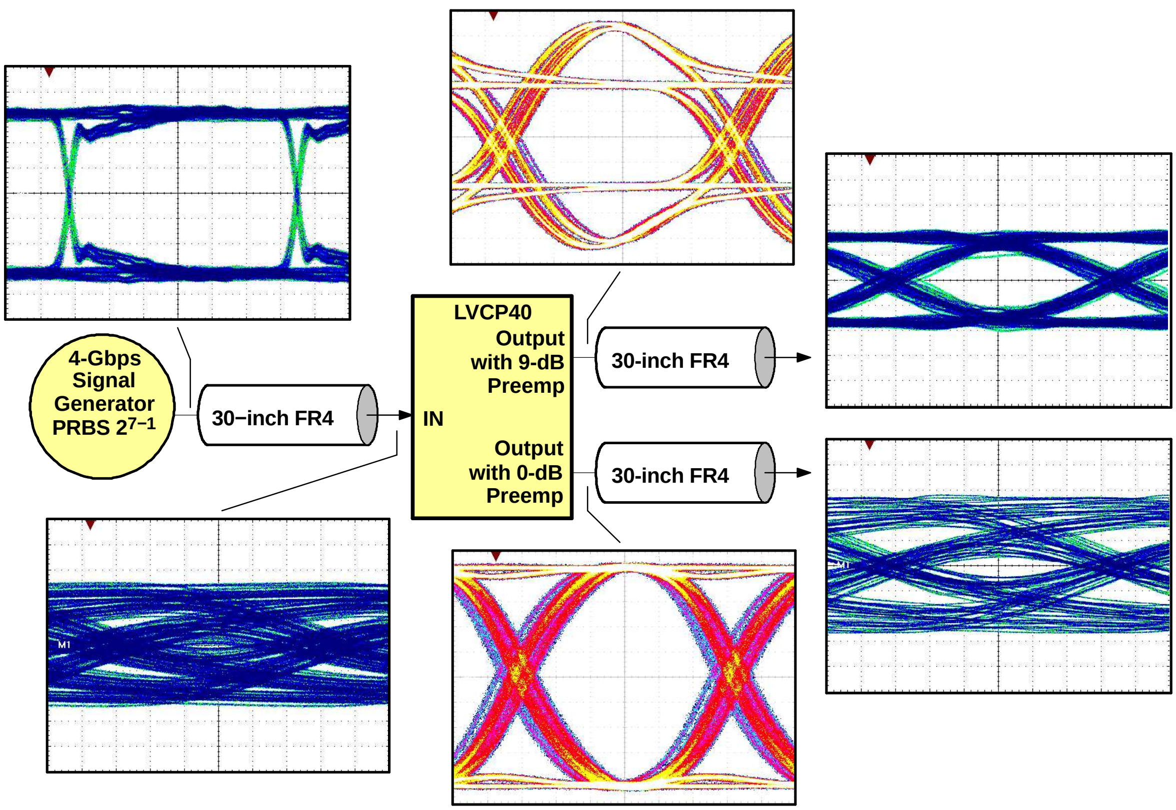


Figure 10. Data Output Pattern

TYPICAL CHARACTERISTICS

DETERMINISTIC OUTPUT JITTER vs DATA RATE

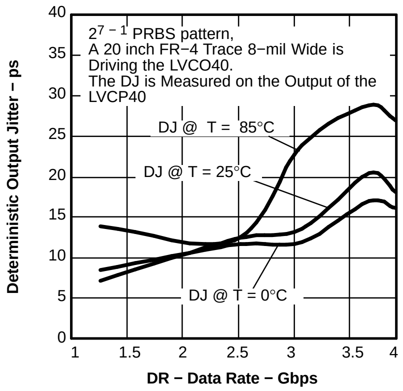


Figure 11.

DETERMINISTIC OUTPUT JITTER vs DIFFERENTIAL INPUT AMPLITUDE

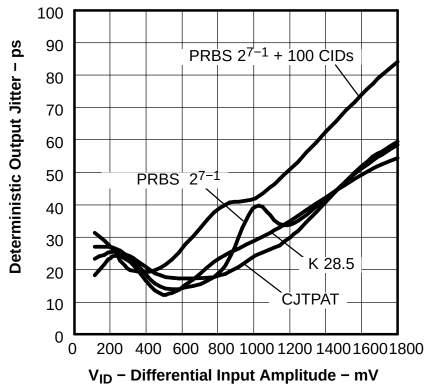


Figure 12.

DETERMINISTIC OUTPUT JITTER vs DIFFERENTIAL INPUT AMPLITUDE

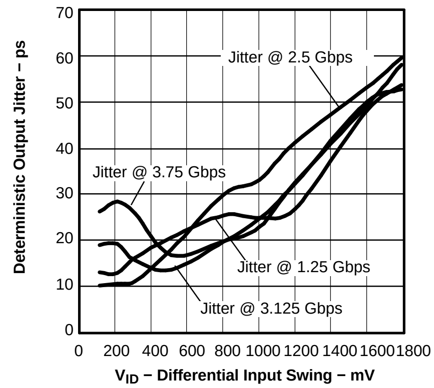


Figure 13.

DETERMINISTIC OUTPUT JITTER vs INPUT TRACE LENGTH

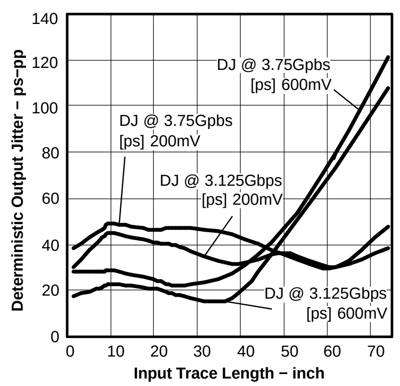


Figure 14.

RANDOM OUTPUT JITTER vs DATA RATE

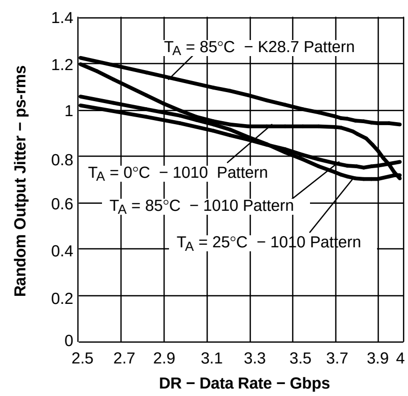


Figure 15.

RANDOM OUTPUT JITTER vs DIFFERENTIAL INPUT SWING

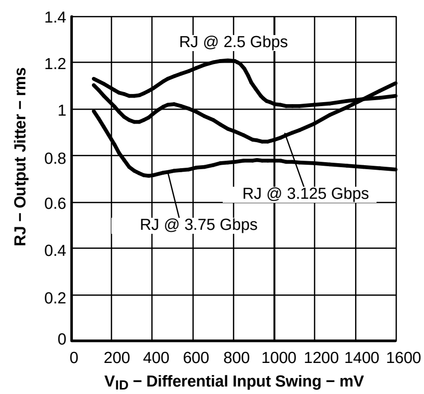


Figure 16.

RANDOM OUTPUT JITTER vs INPUT TRACE LENGTH

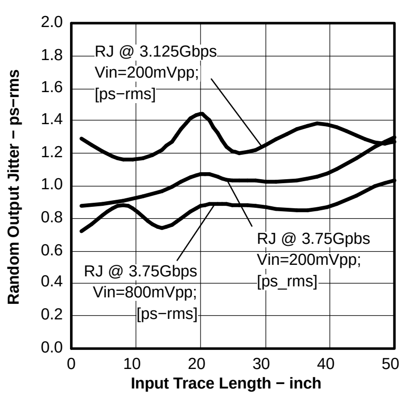


Figure 17.

TOTAL OUTPUT JITTER vs POWER SUPPLY NOISE

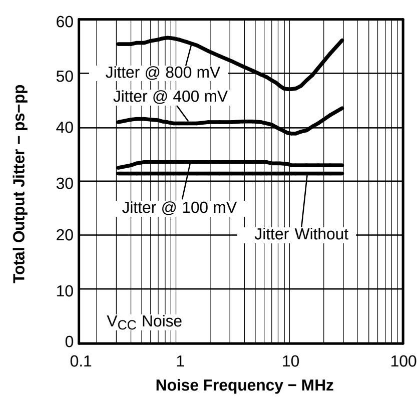


Figure 18.

DJ/RJ OUTPUT JITTER vs COMMON-MODE INPUT VOLTAGE

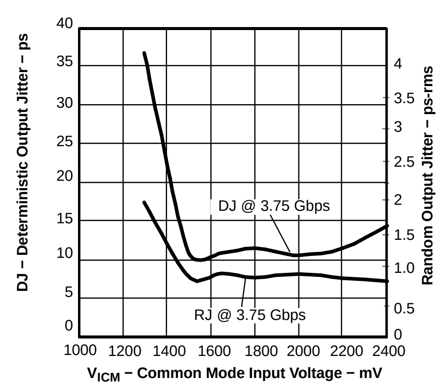


Figure 19.

TYPICAL CHARACTERISTICS (continued)

TOTAL OUTPUT JITTER vs FREE-AIR TEMPERATURE

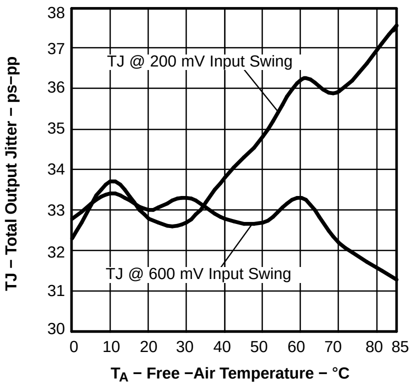


Figure 20.

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

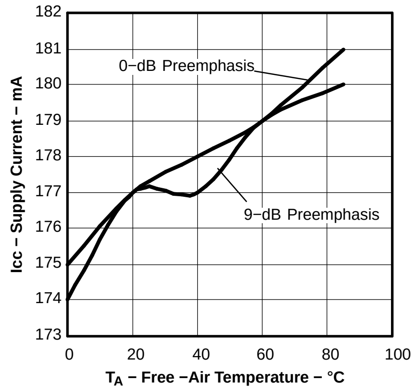


Figure 21.

DIFFERENTIAL OUTPUT SWING vs INPUT SIGNAL FREQUENCY

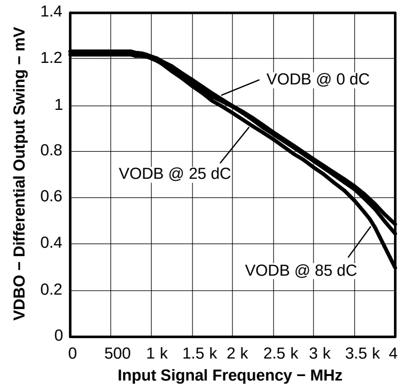


Figure 22.

RECEIVER INPUT RETURN LOSS vs FREQUENCY

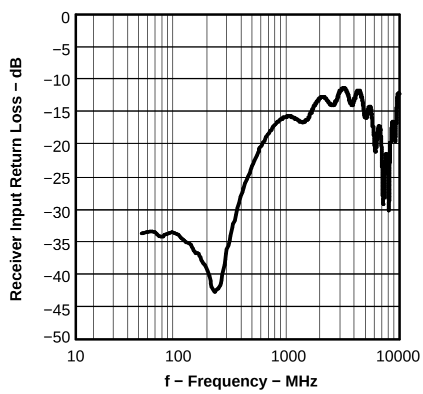


Figure 23.

APPLICATION INFORMATION

BANDWIDTH REQUIREMENTS

Error free transmission of data over a transmission line has specific bandwidth demands. It is helpful to analyze the frequency spectrum of the transmit data first. For an 8B10B coded data stream at 3.75 Gbps of random data, the highest bit transition density occurs with a 1010 pattern (1.875 GHz). The least transition density in 8B10B allows for five consecutive ones or zeros. Hence, the lowest frequency of interest is 1.875 GHz/5 = 375 MHz. Real data signals consist of higher frequency components than sine waves due to the fast rise time. The faster the rise time, the more bandwidth becomes required. For 80-ps rise time, the highest important frequency component is at least $0.6/(\pi \times 80\ \text{ps}) = 2.4$ GHz. Figure 24shows the Fourier transformation of the 375-MHz and 1.875-GHz trapezoidal signal.

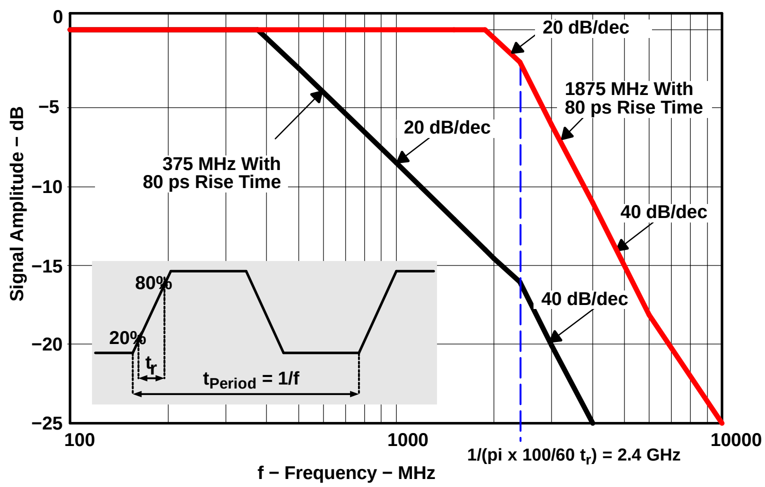


Figure 24. Approximate Frequency Spectrum of the Transmit Output Signal With 80 ps Rise Time

The spectrum analysis of the data signal suggests building a backplane with little frequency attenuation up to 2 GHz. Practically, this is achievable only with expensive, specialized PCB material. To support material like FR4, a compensation technique is necessary to compensate for backplane imperfections.

EXPLANATION OF EQUALIZATION

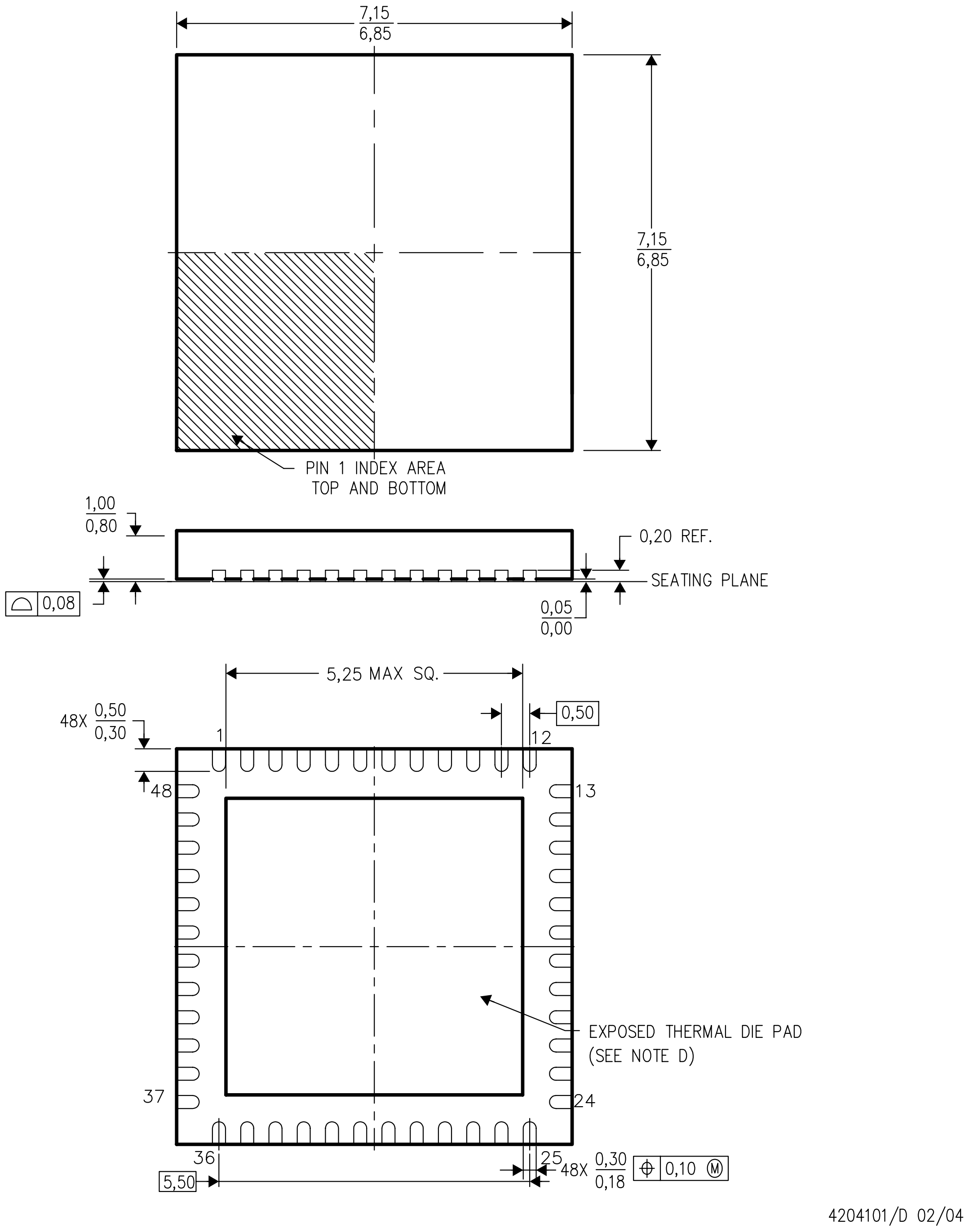
Backplane designs differ widely in size, layer stack-up, and connector placement. In addition, the performance is impacted by trace architecture (trace width, coupling method) and isolation from adjacent signals. Common to most commercial backplanes is the use of FR4 as board material and its related high-frequency signal attenuation. Within a backplane, the shortest to longest trace lengths differ substantially – often ranging from 8 inches up to 40 inches. Increased loss is associated with longer signal traces. In addition, the backplane connector often contributes a good amount of signal attenuation. As a result, the frequency signal attenuation for a 300-MHz signal might range from 1 dB to 4 dB while the corresponding attenuation for a 2-GHz signal might span 6 dB to 24 dB. This frequency dependent loss causes distortion jitter on the transmitted signal. Each LVCP40 receiver input incorporates an equalizer and compensates for such frequency loss. The SN65LVCP40 equalizer provides 5 dB of frequency gain between 375 MHz and 1.875 GHz, compensating roughly for 20 inches of FR4 material with 8-mil trace width. Distortion jitter improvement is substantial, often providing more than 30-ps jitter reduction. The 5-dB compensation is sufficient for most short backplane traces. For longer trace lengths, it is recommended to enable transmit preemphasis in addition.

SETTING THE PREEMPHASIS LEVEL

The receive equalization compensates for ISI. This reduces jitter and opens the data eye. In order to find the best preemphasis setting for each link, calibration of every link is recommended. Assuming each link consists of a transmitter (with adjustable pre-emphasis such as LVCP40) and the LVCP40 receiver, the following steps are necessary:

1. Set the transmitter and receiver to 0-dB preemphasis; record the data eye on the LVCP40 receiver output.
2. Increase the transmitter preemphasis until the data eye on the LVCP40 receiver output looks the cleanest.

RGZ (S-PQFP-N48) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No-leads (QFN) package configuration.
D. The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane.
E. Falls within JEDEC MO-220.

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