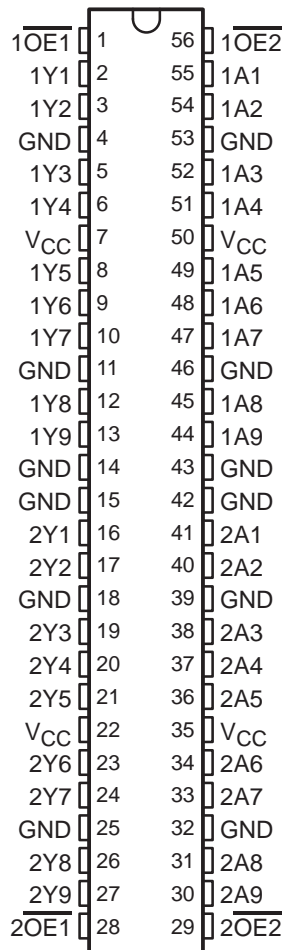


SN54ABT162825, SN74ABT162825 18-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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- Members of the Texas Instruments Widebus™ Family
- Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required
- Typical V_{OLP} (Output Ground Bounce) <1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Impedance State During Power Up and Power Down
- I_{off} and Power-Up 3-State Support Hot Insertion
- Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout

SN54ABT162825 . . . WD PACKAGE
SN74ABT162825 . . . DL PACKAGE
(TOP VIEW)



description/ordering information

The 'ABT162825 devices are 18-bit buffers and line drivers designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. These devices provide true data and can be used as two 9-bit buffers or one 18-bit buffer.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all nine affected outputs are in the high-impedance state.

The outputs, which are designed to source or sink up to 12 mA, include equivalent 25-Ω series resistors to reduce overshoot and undershoot.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

ORDERING INFORMATION

| T_A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|-----------|---------------|-----------------------|------------------|
| -40°C to 85°C | SSOP – DL | Tube | SN74ABT1628251DL | ABT162825 |
| | | Tape and reel | SN74ABT162825DLR | |
| -55°C to 125°C | CFP – WD | Tube | SNJ54ABT162825WD | SNJ54ABT162825WD |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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 **TEXAS
INSTRUMENTS**

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SN54ABT162825, SN74ABT162825
18-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

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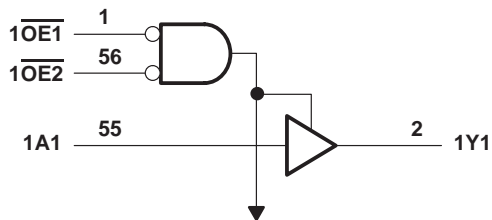
description/ordering information (continued)

To ensure the high-impedance state during power up or power down, \overline{OE} shall be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

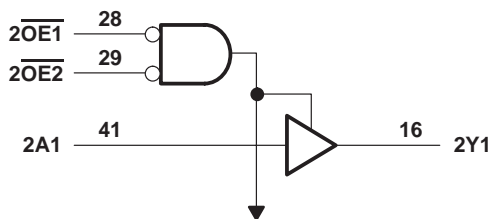
FUNCTION TABLE
 (each 9-bit buffer)

| INPUTS | | | OUTPUT |
|------------------|------------------|---|--------|
| $\overline{OE1}$ | $\overline{OE2}$ | A | Y |
| L | L | L | L |
| L | L | H | H |
| H | X | X | Z |
| X | H | X | Z |

logic diagram (positive logic)



To Eight Other Channels



To Eight Other Channels

SN54ABT162825, SN74ABT162825 18-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|-----------------|
| Supply voltage range, V_{CC} | –0.5 V to 7 V |
| Input voltage range, V_I (see Note 1) | –0.5 V to 7 V |
| Voltage range applied to any output in the high or power-off state, V_O | –0.5 V to 5.5 V |
| Current into any output in the low state, I_O | 30 mA |
| Input clamp current, I_{IK} ($V_I < 0$) | –18 mA |
| Output clamp current, I_{OK} ($V_O < 0$) | –50 mA |
| Package thermal impedance, θ_{JA} (see Note 2): DL package | 56°C/W |
| Storage temperature range, T_{stg} | –65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

| | | SN54ABT162825 | | SN74ABT162825 | | UNIT |
|--------------------------|------------------------------------|----------------|----------|---------------|----------|-----------|
| | | MIN | MAX | MIN | MAX | |
| V_{CC} | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| V_{IH} | High-level input voltage | 2 | | 2 | | V |
| V_{IL} | Low-level input voltage | | 0.8 | | 0.8 | V |
| V_I | Input voltage | 0 | V_{CC} | 0 | V_{CC} | V |
| I_{OH} | High-level output current | | –3 | | –12 | mA |
| I_{OL} | Low-level output current | | 8 | | 12 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | Control inputs | | 9 | 9 | ns/V |
| | | Data inputs | | 10 | 10 | |
| $\Delta t/\Delta V_{CC}$ | Power-up ramp rate | 200 | | 200 | | μ s/V |
| T_A | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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18-BIT BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | T _A = 25°C | | | SN54ABT162825 | | SN74ABT162825 | | UNIT | |
|--------------------|--|--|------------------|------|---------------|------|---------------|------|------|----|
| | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | | |
| V _{IK} | V _{CC} = 4.5 V, I _I = -18 mA | | | -1.2 | | -1.2 | | -1.2 | V | |
| V _{OH} | V _{CC} = 4.5 V, I _{OH} = -1 mA | | | 2.5 | | 2.5 | | 2.5 | V | |
| | V _{CC} = 5 V, I _{OH} = -1 mA | | | 3 | | 3 | | 3 | | |
| | V _{CC} = 4.5 V | I _{OH} = -3 mA | | 2.4 | | 2.4 | | 2.4 | | |
| | | | | | | | | 2 | | |
| V _{OL} | V _{CC} = 4.5 V | I _{OL} = 8 mA | | 0.4 | | 0.8 | | 0.65 | V | |
| | | I _{OL} = 12 mA | | | | 0.8* | | 0.8 | | |
| V _{hys} | | | | 100 | | | | | mV | |
| I _I | V _{CC} = 0 to 5.5 V, V _I = V _{CC} or GND | | | ±1 | | ±1 | | ±1 | µA | |
| I _{OZPU} | V _{CC} = 0 to 2.1 V, V _O = 0.5 V to 2.7 V, $\overline{OE} = X$ | | | ±50 | | ±50 | | ±50 | µA | |
| I _{OZPD} | V _{CC} = 2.1 V to 0, V _O = 0.5 V to 2.7 V, $\overline{OE} = X$ | | | ±50 | | ±50 | | ±50 | µA | |
| I _{OZH} ‡ | V _{CC} = 2.1 V to 5.5 V, V _O = 2.7 V, $\overline{OE} \geq 2$ V | | | 10 | | 10 | | 10 | µA | |
| I _{OZL} ‡ | V _{CC} = 2.1 V to 5.5 V, V _O = 0.5 V, $\overline{OE} \geq 2$ V | | | -10 | | -10 | | -10 | µA | |
| I _{off} | V _{CC} = 0, V _I or V _O ≤ 4.5 V | | | ±100 | | | | ±100 | µA | |
| I _{CEx} | Outputs high | V _{CC} = 5.5 V, V _O = 5.5 V | | 50 | | 50 | | 50 | µA | |
| I _O § | | V _{CC} = 5.5 V, V _O = 2.5 V | -25 | -75 | -100 | -25 | -100 | -25 | -100 | mA |
| I _{CC} | Outputs high | | | 2 | | 2 | | 2 | mA | |
| | Outputs low | V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND | | 32 | | 32 | | 32 | | |
| | Outputs disabled | | | 2 | | 2 | | 2 | | |
| ΔI _{CC} ¶ | Data inputs | V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND | Outputs enabled | | 1 | | 1.5 | | 1 | mA |
| | | | Outputs disabled | | 0.05 | | 1 | | 0.05 | |
| | Control inputs | V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND | | 1.5 | | 1.5 | | 1.5 | | |
| C _i | | V _I = 2.5 V or 0.5 V | | 3.5 | | | | | pF | |
| C _o | | V _O = 2.5 V or 0.5 V | | 8 | | | | | pF | |

† All typical values are at V_{CC} = 5 V.

‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

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18-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 5$ V, $T_A = 25^\circ$ C | | | SN54ABT162825 | | SN74ABT162825 | | UNIT |
|-----------|-----------------|----------------|---------------------------------------|-----|-----|---------------|-----|---------------|-----|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t_{PLH} | A | Y | 1 | 2.1 | 3.6 | 1 | 4.1 | 1 | 3.9 | ns |
| t_{PHL} | | | 1.1 | 2.8 | 4.2 | 1.1 | 5 | 1.1 | 4.7 | |
| t_{PZH} | \overline{OE} | Y | 1.5 | 3.4 | 6.3 | 1.5 | 7.2 | 1.5 | 6.9 | ns |
| t_{PZL} | | | 1.6 | 3.5 | 7.3 | 1.6 | 6.6 | 1.6 | 6.3 | |
| t_{PHZ} | \overline{OE} | Y | 2.1 | 4.1 | 6.5 | 2.1 | 6.8 | 2.1 | 6.6 | ns |
| t_{PLZ} | | | 1.5 | 3.5 | 5.9 | 1.5 | 7.3 | 1.5 | 6.3 | |

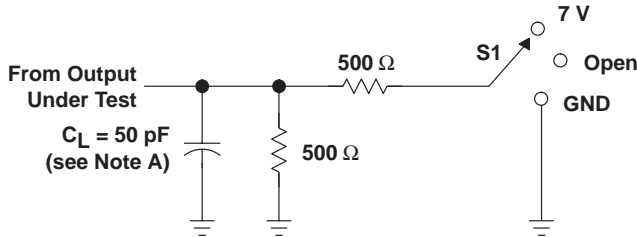
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WITH 3-STATE OUTPUTS

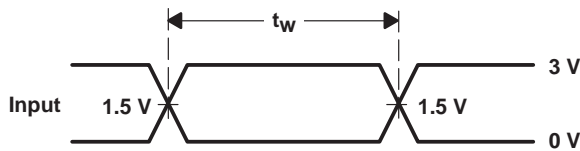
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PARAMETER MEASUREMENT INFORMATION

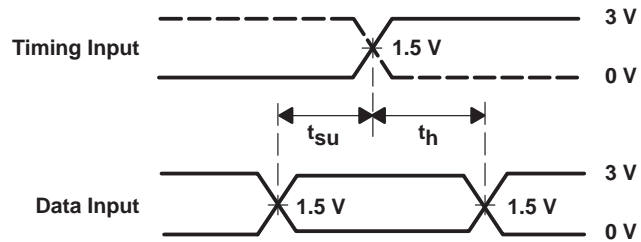


| TEST | S1 |
|-------------------|------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | 7 V |
| t_{PHZ}/t_{PZH} | Open |

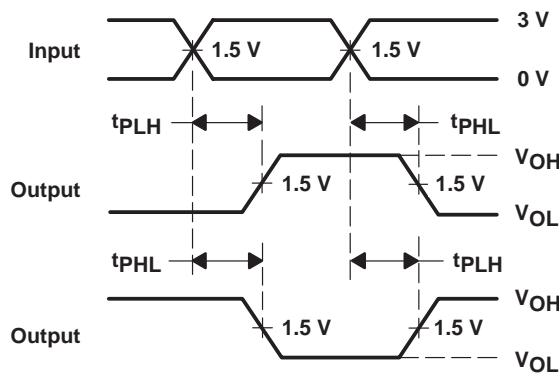
LOAD CIRCUIT



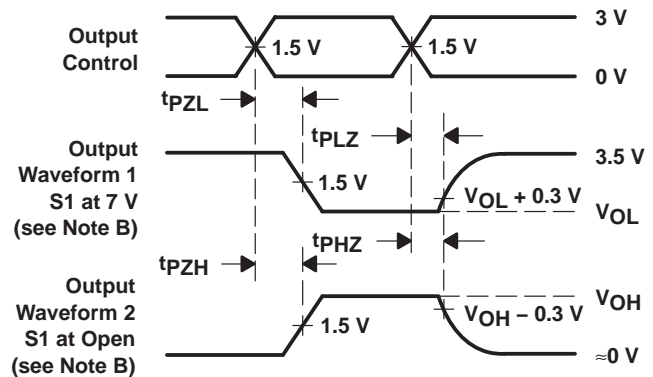
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

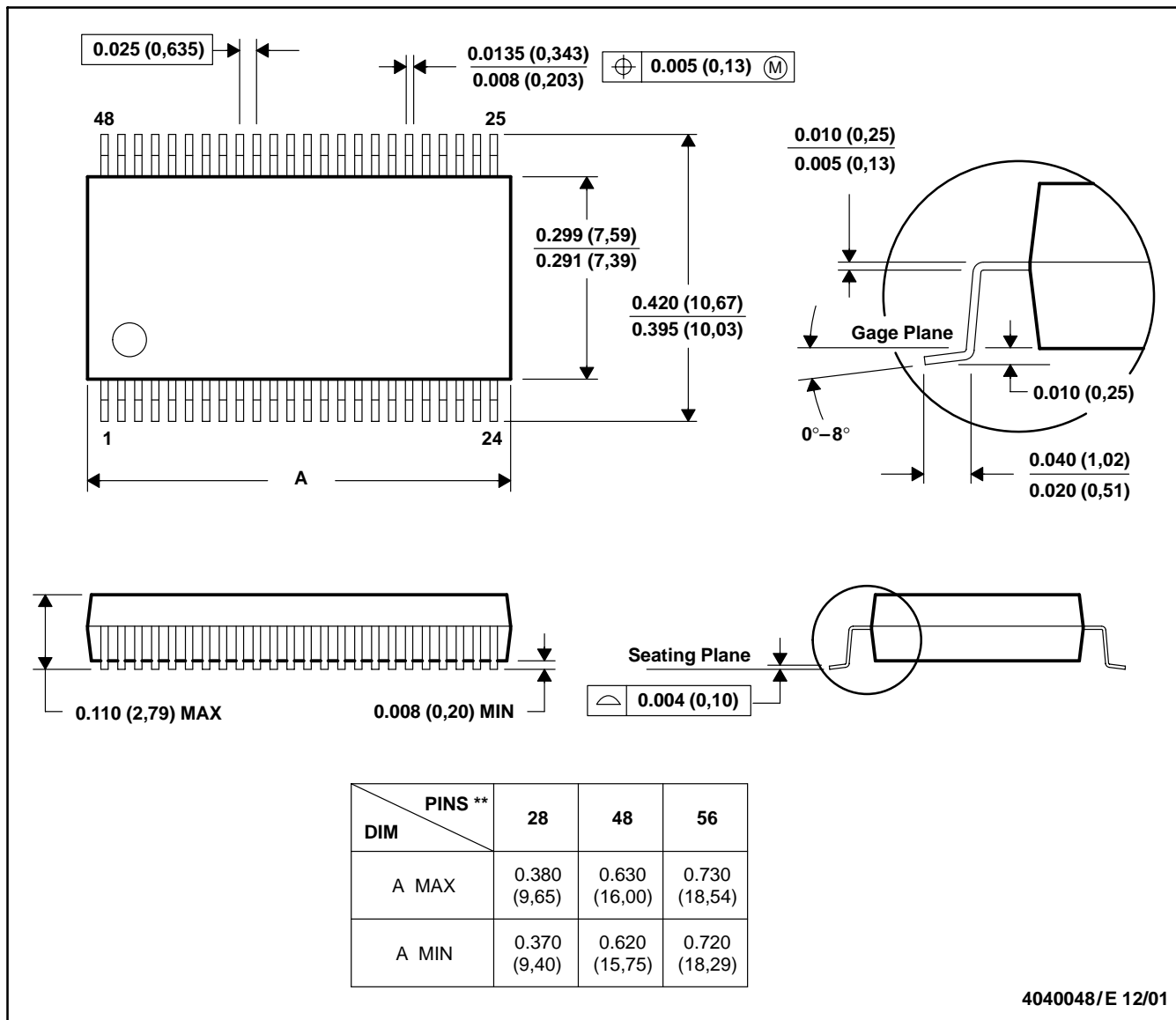
- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

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