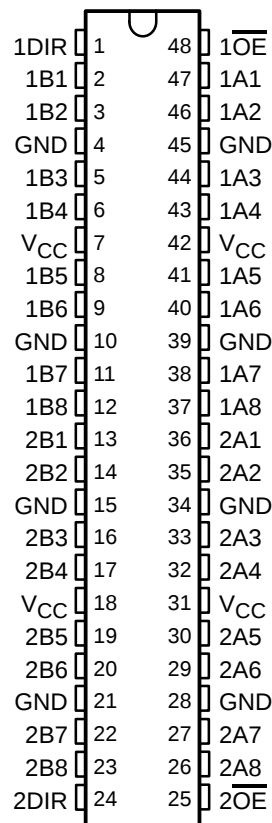


SN54ALVTHR16245, SN74ALVTHR16245 2.5-V/3.3-V 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCES075D – JUNE 1996 – REVISED DECEMBER 2002

- State-of-the-Art Advanced BiCMOS Technology (ABT) Widebus™ Design for 2.5-V and 3.3-V Operation and Low Static-Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 2.3-V to 3.6-V V_{CC})
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- High Drive ($-12/12$ mA at 3.3-V V_{CC})
- I_{off} and Power-Up 3-State Support Hot Insertion
- Use Bus Hold on Data Inputs in Place of External Pullup/Pulldown Resistors to Prevent the Bus From Floating
- Output Ports Have Equivalent 30- Ω Series Resistors, So No External Resistors Are Required
- Flow-Through Architecture Facilitates Printed Circuit Board Layout
- Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

SN54ALVTHR16245 . . . WD PACKAGE
SN74ALVTHR16245 . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)



description/ordering information

The 'ALVTHR16245 devices are 16-bit (dual-octal) noninverting 3-state transceivers designed for 2.5-V or 3.3-V V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP – DL	Tape and reel	SN74ALVTHR16245LR	ALVTHR16245
	TSSOP – DGG	Tape and reel	SN74ALVTHR16245GR	ALVTHR16245
	TVSOP – DGV	Tape and reel	SN74ALVTHR16245VR	TR245
	VFBGA – GQL	Tape and reel	SN74ALVTHR16245KR	TR245
-55°C to 125°C	CFP – WD	Tube	SNJ54ALVTHR16245W	SNJ54ALVTHR16245W

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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SN54ALVTHR16245, SN74ALVTHR16245

2.5-V/3.3-V 16-BIT BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

SCES075D – JUNE 1996 – REVISED DECEMBER 2002

description/ordering information (continued)

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

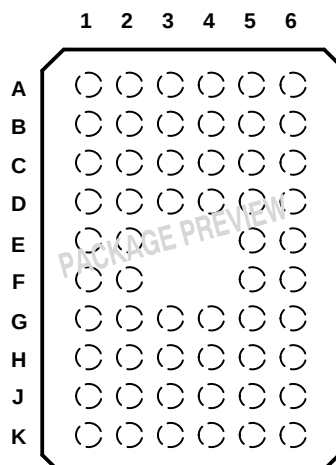
All outputs are designed to sink up to 12 mA, and include equivalent 30- Ω resistors to reduce overshoot and undershoot.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 and 1.2 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.2 V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

SN74ALVTHR16245 . . . GQL PACKAGE (TOP VIEW)



terminal assignments

	1	2	3	4	5	6
A	1DIR	NC	NC	NC	NC	$\overline{1OE}$
B	1B2	1B1	GND	GND	1A1	1A2
C	1B4	1B3	V_{CC}	V_{CC}	1A3	1A4
D	1B6	1B5	GND	GND	1A5	1A6
E	1B8	1B7			1A7	1A8
F	2B1	2B2			2A2	2A1
G	2B3	2B4	GND	GND	2A4	2A3
H	2B5	2B6	V_{CC}	V_{CC}	2A6	2A5
J	2B7	2B8	GND	GND	2A8	2A7
K	2DIR	NC	NC	NC	NC	$\overline{2OE}$

NC – No internal connection

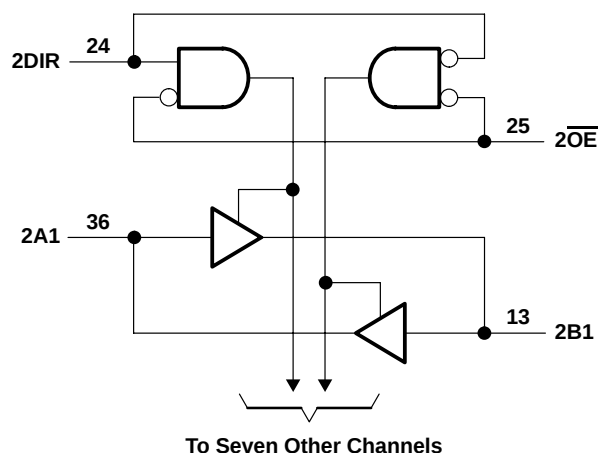
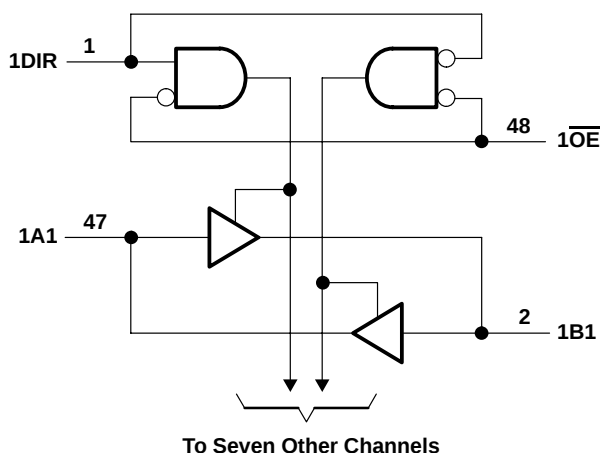
FUNCTION TABLE (each 8-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

SN54ALVTHR16245, SN74ALVTHR16245 2.5-V/3.3-V 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCES075D – JUNE 1996 – REVISED DECEMBER 2002

logic diagram (positive logic)



Pin numbers shown are for the DGG, DGV, DL, and WD packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Output current in the low state, I_O : SN54ALVTHR16245	96 mA
SN74ALVTHR16245	128 mA
Output current in the high state, I_O : SN54ALVTHR16245	–48 mA
SN74ALVTHR16245	–64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package	70°C/W
DGV package	58°C/W
DL package	63°C/W
GQL package	42°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

SN54ALVTHR16245, SN74ALVTHR16245

2.5-V/3.3-V 16-BIT BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

SCES075D – JUNE 1996 – REVISED DECEMBER 2002

recommended operating conditions, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (see Note 3)

		SN54ALVTHR16245			SN74ALVTHR16245			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	2.3		2.7	2.3		2.7	V
V_{IH}	High-level input voltage	1.7			1.7			V
V_{IL}	Low-level input voltage			0.7			0.7	V
V_I	Input voltage	0	V_{CC}	5.5	0	V_{CC}	5.5	V
I_{OH}	High-level output current			–6			–8	mA
I_{OL}	Low-level output current			6			12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10			ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200			200			$\mu\text{s/V}$
T_A	Operating free-air temperature	–55		125	–40		85	$^{\circ}\text{C}$

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

recommended operating conditions, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (see Note 3)

		SN54ALVTHR16245			SN74ALVTHR16245			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	3		3.6	3		3.6	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_I	Input voltage	0	V_{CC}	5.5	0	V_{CC}	5.5	V
I_{OH}	High-level output current			–8			–12	mA
I_{OL}	Low-level output current			8			12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10			ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200			200			$\mu\text{s/V}$
T_A	Operating free-air temperature	–55		125	–40		85	$^{\circ}\text{C}$

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54ALVTHR16245, SN74ALVTHR16245 2.5-V/3.3-V 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCES075D – JUNE 1996 – REVISED DECEMBER 2002

electrical characteristics over recommended operating free-air temperature range,
 $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALVTHR16245			SN74ALVTHR16245			UNIT	
				MIN	TYP†	MAX	MIN	TYP†	MAX		
V _{IK}		V _{CC} = 2.3 V, I _I = −18 mA		−1.2			−1.2			V	
V _{OH}		V _{CC} = 2.3 V to 2.7 V, I _{OH} = −100 μA		V _{CC} −0.2			V _{CC} −0.2			V	
		V _{CC} = 2.3 V		I _{OH} = −6 mA			1.7				
				I _{OH} = −8 mA			1.7				
V _{OL}		V _{CC} = 2.3 V to 2.7 V, I _{OL} = 100 μA		0.2			0.2			V	
		V _{CC} = 2.3 V		I _{OL} = 6 mA			0.7				
				I _{OL} = 12 mA			0.7				
I _I	Control inputs	V _{CC} = 2.7 V, V _I = V _{CC} or GND		±1			±1			μA	
		V _{CC} = 0 or 2.7 V, V _I = 5.5 V		10			10				
	A or B ports	V _{CC} = 2.7 V, V _I = 5.5 V		20			20				
		V _I = V _{CC}		1			1				
		V _I = 0		−5			−5				
I _{off}		V _{CC} = 0, V _I or V _O = 0 to 4.5 V					±100			μA	
I _{BHL} [‡]		V _{CC} = 2.3 V, V _I = 0.7 V		115			115			μA	
I _{BHH} [§]		V _{CC} = 2.3 V, V _I = 1.7 V		−10			−10			μA	
I _{BHLO} [¶]		V _{CC} = 2.7 V, V _I = 0 to V _{CC}		300			300			μA	
I _{BHHO} [#]		V _{CC} = 2.7 V, V _I = 0 to V _{CC}		−300			−300			μA	
I _{EX}		V _{CC} = 2.3 V, V _O = 5.5 V		125			125			μA	
I _{OZ(PU/PD)} [*]		V _{CC} ≤ 1.2 V, V _O = 0.5 V to V _{CC} , V _I = GND or V _{CC} , OE = don't care		±100			±100			μA	
I _{CC}		V _{CC} = 2.7 V, I _O = 0, V _I = V _{CC} or GND		Outputs high		0.04	0.1	0.04		0.1	mA
				Outputs low		2.5	4.5	2.5		4.5	
				Outputs disabled		0.04	0.1	0.04		0.1	
C _i		V _{CC} = 2.5 V, V _I = 2.5 V or 0		3.5			3.5			pF	
C _{io}		V _{CC} = 2.5 V, V _O = 2.5 V or 0		8			8			pF	

[†] All typical values are at $V_{CC} = 2.5 \text{ V}$, $T_A = 25^\circ\text{C}$.

[‡] The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.

[§] The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.

[¶] An external driver must source at least I_{BHLO} to switch this node from low to high.

[#] An external driver must sink at least I_{BHHO} to switch this node from high to low.

^{||} Current into an output in the high state when $V_O > V_{CC}$

[☆] High-impedance state during power up or power down

SN54ALVTHR16245, SN74ALVTHR16245

2.5-V/3.3-V 16-BIT BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

SCES075D – JUNE 1996 – REVISED DECEMBER 2002

electrical characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALVTHR16245		SN74ALVTHR16245		UNIT
				MIN	TYP†	MAX	MIN	
V _{IK}		V _{CC} = 3 V, I _I = −18 mA		−1.2		−1.2		V
V _{OH}		V _{CC} = 3 V to 3.6 V, I _{OH} = −100 μA		V _{CC} −0.2		V _{CC} −0.2		V
		V _{CC} = 3 V, I _{OH} = −8 mA		2				
		I _{OH} = −12 mA				2		
V _{OL}		V _{CC} = 3 V to 3.6 V, I _{OL} = 100 μA		0.2		0.2		V
		V _{CC} = 3 V, I _{OL} = 8 mA		0.8				
		I _{OL} = 12 mA				0.8		
I _I	Control inputs	V _{CC} = 3.6 V, V _I = V _{CC} or GND		±1		±1		μA
		V _{CC} = 0 or 3.6 V, V _I = 5.5 V		10		10		
	A or B ports	V _{CC} = 3.6 V, V _I = 5.5 V		20		20		
		V _I = V _{CC}		1		1		
		V _I = 0		−5		−5		
I _{off}		V _{CC} = 0, V _I or V _O = 0 to 4.5 V				±100		μA
I _{BHL} [‡]		V _{CC} = 3 V, V _I = 0.8 V		75		75		μA
I _{BHH} [§]		V _{CC} = 3 V, V _I = 2 V		−75		−75		μA
I _{BHLO} [¶]		V _{CC} = 3.6 V, V _I = 0 to V _{CC}		500		500		μA
I _{BHHO} [#]		V _{CC} = 3.6 V, V _I = 0 to V _{CC}		−500		−500		μA
I _{EX}		V _{CC} = 3 V, V _O = 5.5 V		125		125		μA
I _{OZ(PU/PD)} [*]		V _{CC} ≤ 1.2 V, V _O = 0.5 V to V _{CC} , V _I = GND or V _{CC} , OE = don't care		±100		±100		μA
I _{CC}		V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND		Outputs high		0.07 0.1		mA
				Outputs low		3.5 5		
				Outputs disabled		0.07 0.1		
ΔI _{CC} [□]		V _{CC} = 3 V to 3.6 V, One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND		0.4		0.4		mA
C _i		V _{CC} = 3.3 V, V _I = 3.3 V or 0		3.5		3.5		pF
C _{i0}		V _{CC} = 3.3 V, V _O = 3.3 V or 0		8		8		pF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

[‡] The bus-hold circuit can sink at least the minimum low sustaining current at $V_{IL} \text{ max}$. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to $V_{IL} \text{ max}$.

^{\S} The bus-hold circuit can source at least the minimum high sustaining current at $V_{IH} \text{ min}$. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to $V_{IH} \text{ min}$.

^{\P} An external driver must source at least I_{BHLO} to switch this node from low to high.

^{\#} An external driver must sink at least I_{BHHO} to switch this node from high to low.

^{\parallel} Current into an output in the high state when $V_O > V_{CC}$

^{\star} High-impedance state during power up or power down

^{\square} This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

SN54ALVTHR16245, SN74ALVTHR16245 2.5-V/3.3-V 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCES075D – JUNE 1996 – REVISED DECEMBER 2002

switching characteristics over recommended operating free-air temperature range, $C_L = 30$ pF, $V_{CC} = 2.5$ V $\pm$ 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALVTHR16245		SN74ALVTHR16245		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	0.5	4.3	0.5	4.3	ns
t_{PHL}			0.5	3.7	0.5	3.7	
t_{PZH}	$\overline{OE}$	A or B	1.8	5.6	1.8	5.6	ns
t_{PZL}			1.6	4.7	1.6	4.7	
t_{PHZ}	$\overline{OE}$	A or B	1.7	5	1.7	5	ns
t_{PLZ}			1.4	4.4	1.4	4.4	

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF, $V_{CC} = 3.3$ V $\pm$ 0.3 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALVTHR16245		SN74ALVTHR16245		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	0.5	3.7	0.5	3.7	ns
t_{PHL}			0.5	3.9	0.5	3.9	
t_{PZH}	$\overline{OE}$	A or B	1.3	5.2	1.3	5.2	ns
t_{PZL}			1.3	4	1.3	4	
t_{PHZ}	$\overline{OE}$	A or B	2	5.1	2	5.1	ns
t_{PLZ}			1.5	4.8	1.5	4.8	

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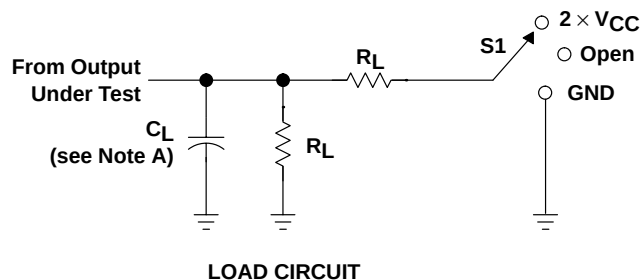
SN54ALVTHR16245, SN74ALVTHR16245

2.5-V/3.3-V 16-BIT BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

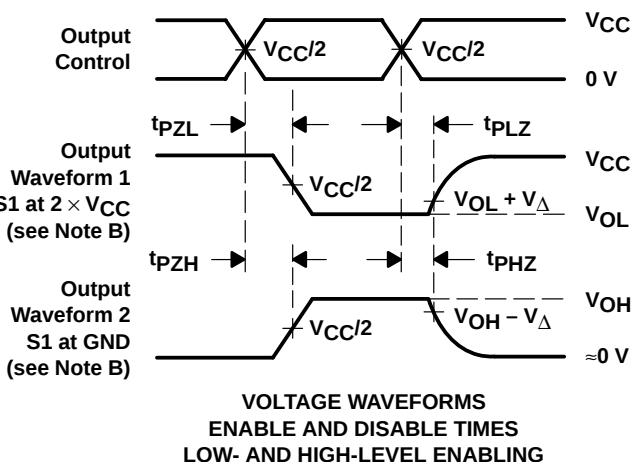
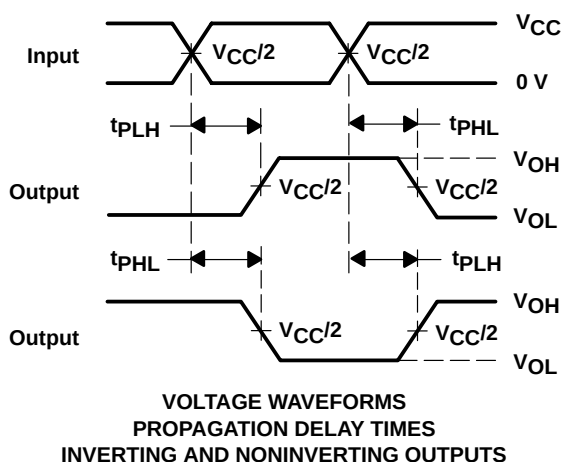
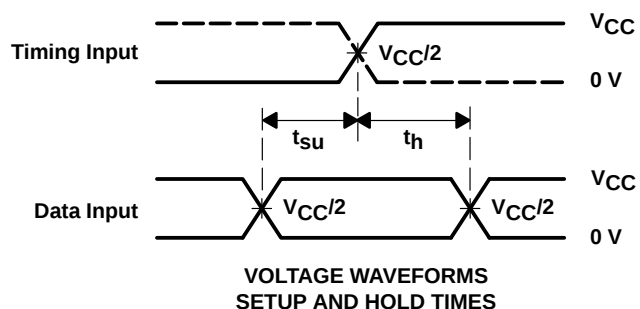
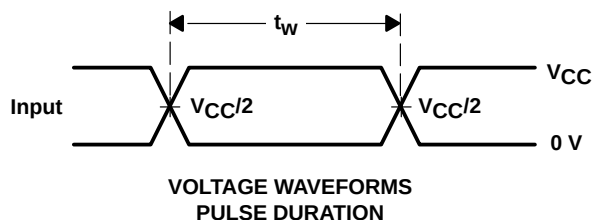
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PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

V_{CC}	C_L	R_L	V_{Δ}
$2.5 \text{ V} \pm 0.2 \text{ V}$	30 pF	500 Ω	0.15 V
$3.3 \text{ V} \pm 0.3 \text{ V}$	50 pF	500 Ω	0.3 V

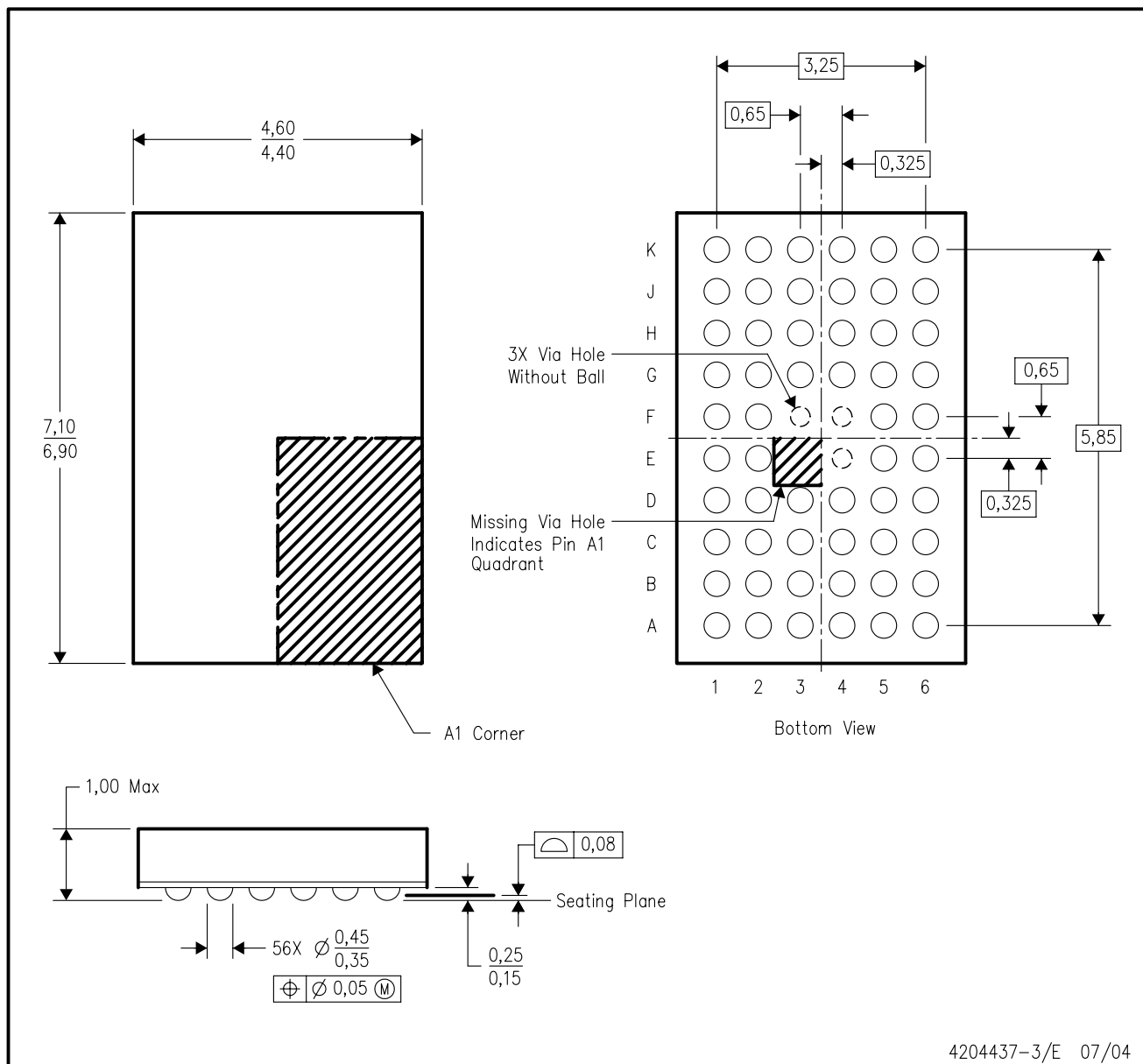


- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

ZQL (R-PBGA-N56)

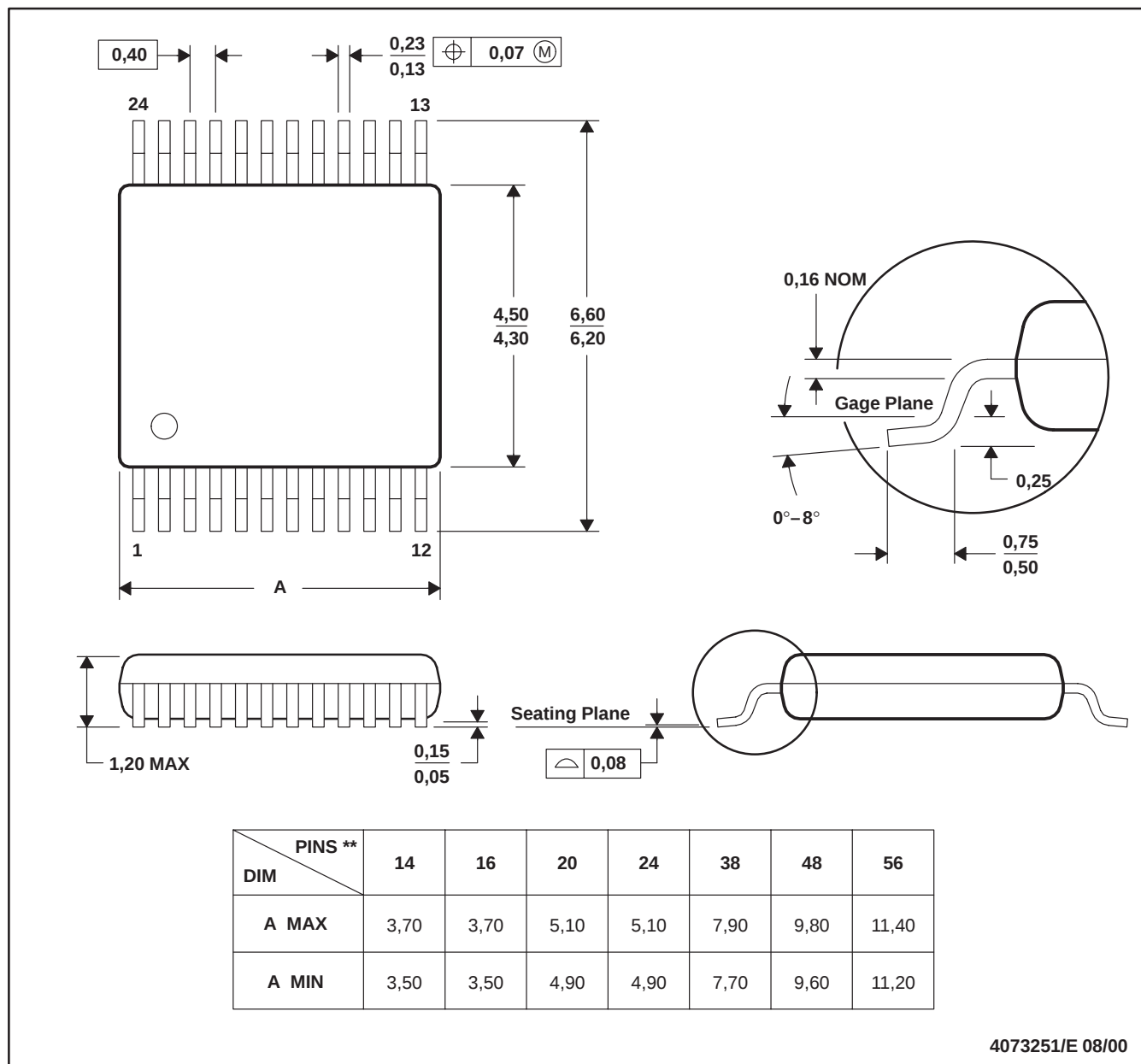
PLASTIC BALL GRID ARRAY



DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

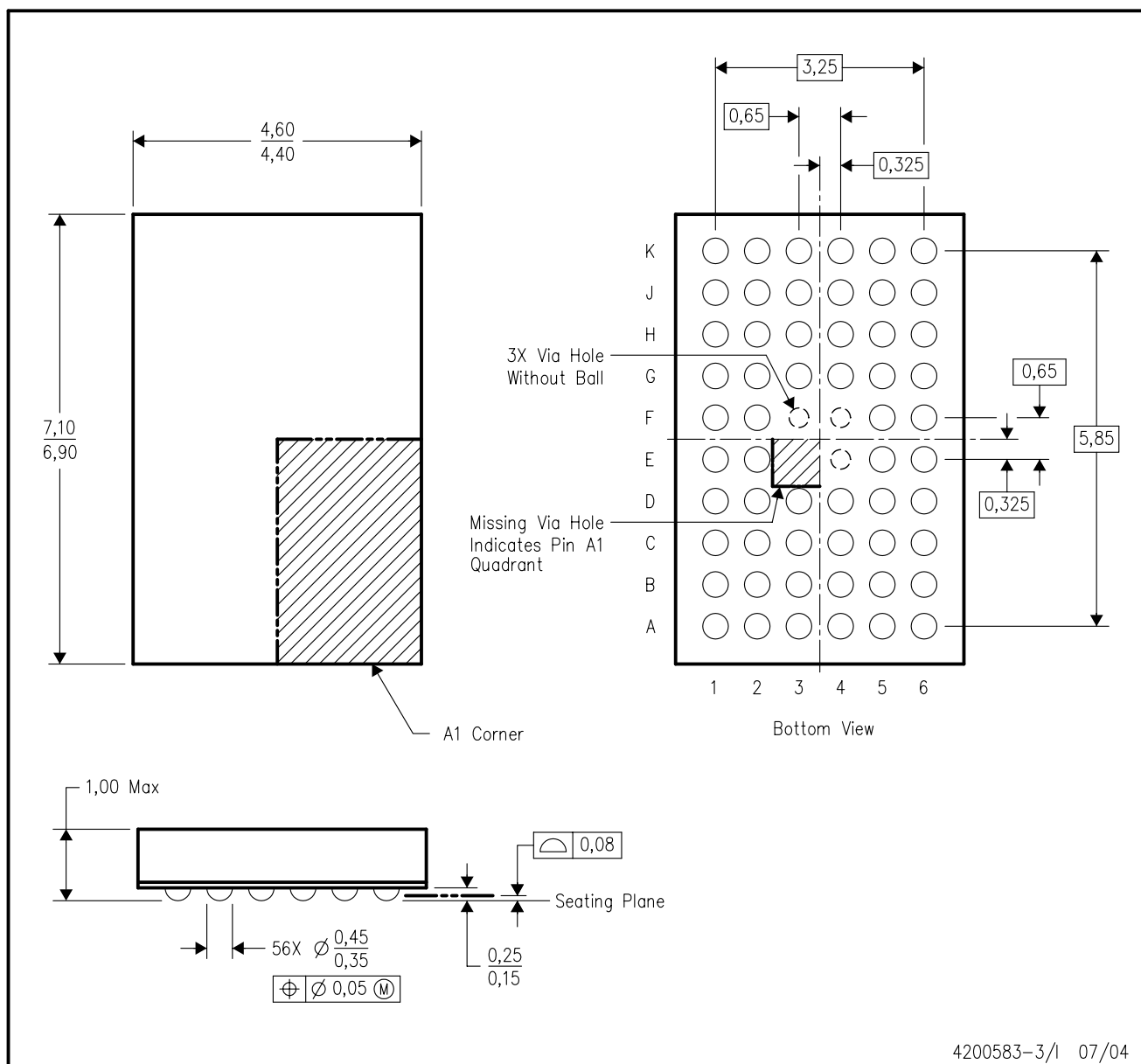
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

GQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY

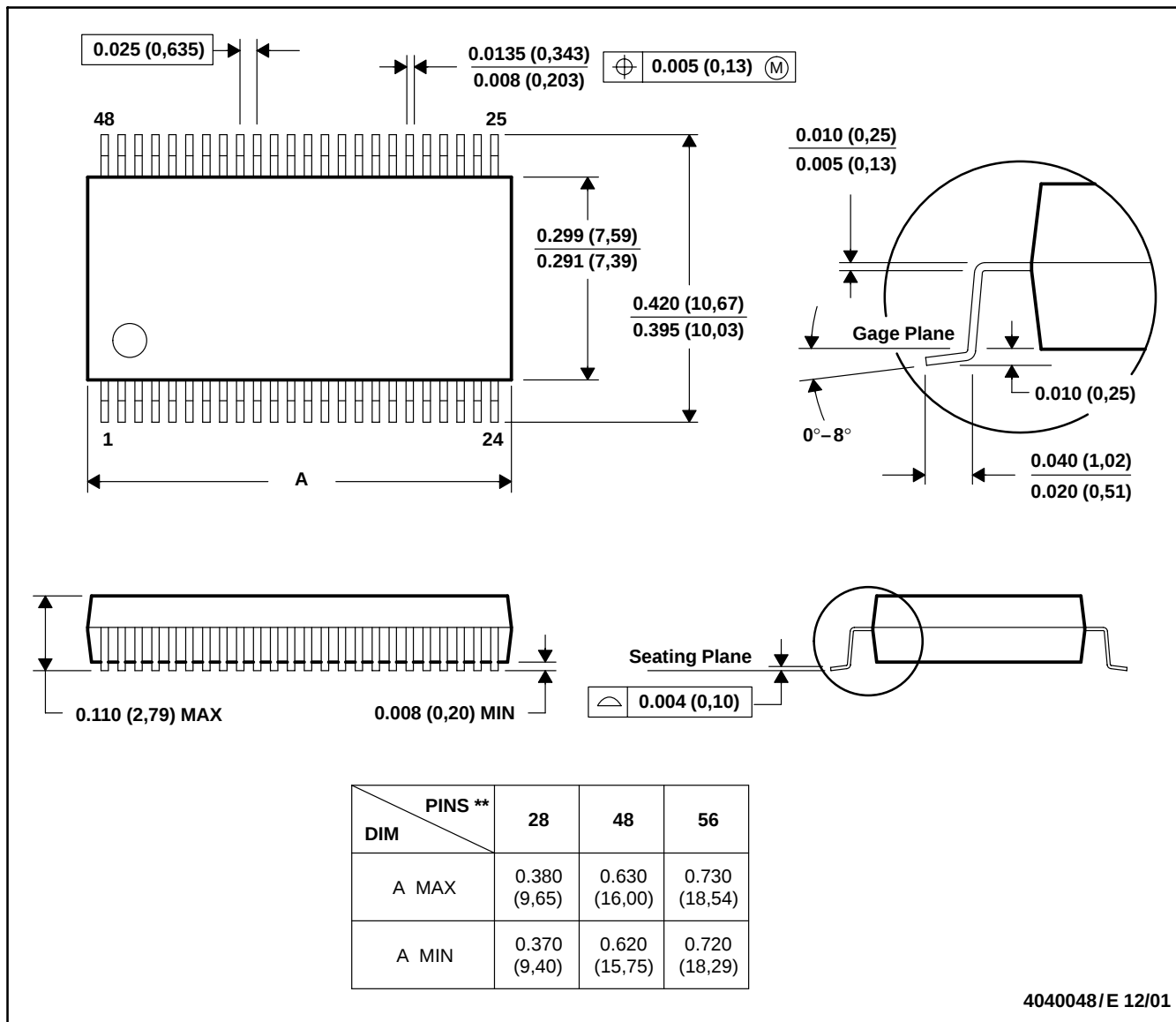


- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Falls within JEDEC MO-225 variation BA.
 - This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

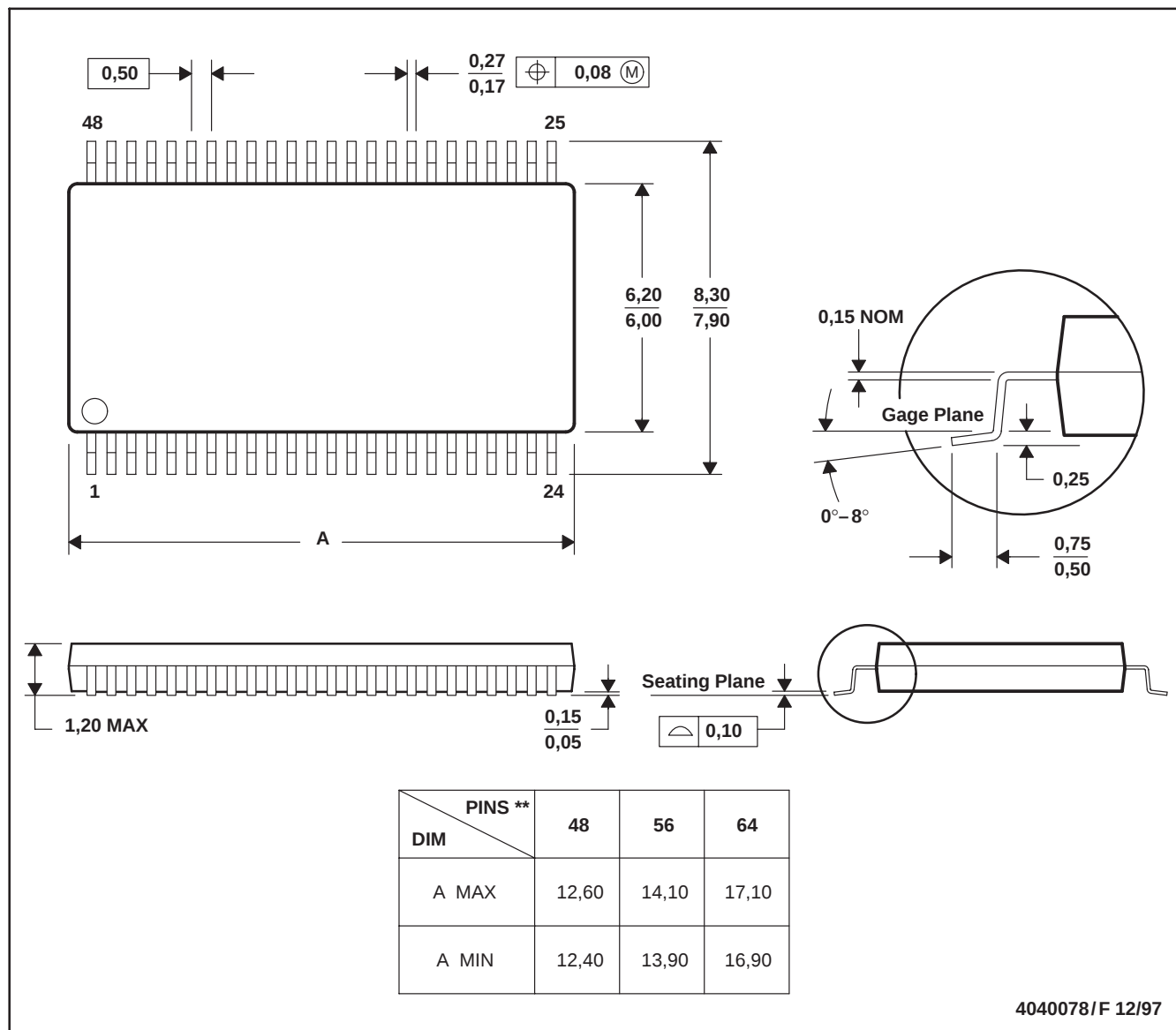


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

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