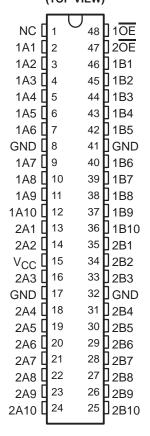
- Member of Texas Instruments' Widebus™ **Family**
- 5- Ω Switch Connection Between Two Ports
- **TTL-Compatible Input Levels**

description

The SN74CBT16210 provides 20 bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as a dual 10-bit bus switch with separate output-enable (\overline{OE}) inputs. It can be used as two 10-bit bus switches or as one 20-bit bus switch. When \overline{OE} is low, the associated 10-bit bus switch is on, and port A is connected to port B. When OE is high, the switch is open, and the high-impedance state exists between the ports.

DGG, DGV, OR DL PACKAGE (TOP VIEW)



NC - No internal connection

ORDERING INFORMATION

TA	PACKA	_{GE} †	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	SSOP – DL	Tube	SN74CBT16210DL	CBT16210
–40°C to 85°C	330F - DL	Tape and reel	SN74CBT616210DLR	CB110210
-40 C to 65 C	TSSOP – DGG	Tape and reel	SN74CBT16210DGGR	CBT16210
	TVSOP – DGV Ta		SN74CBT16210DGVR	CY210

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each 10-bit bus switch)

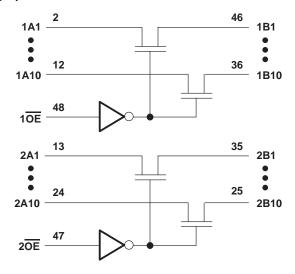
INPUT OE	FUNCTION			
L	A port = B port			
Н	Disconnect			



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Widebus is a trademark of Texas Instruments.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		-0.5	V to 7 V
Input voltage range, V _I (see Note 1)		-0.5	$V \ to \ 7 \ V$
Continuous channel current			128 mA
Input clamp current, I _{IK} (V _I < 0)			-50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DGG package		70°C/W
	DGV package		58°C/W
	DL package		63°C/W
Storage temperature range, T _{sta}	6	5°C t	o 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4	5.5	V
VIH	High-level control input voltage	2		V
V _{IL}	Low-level control input voltage		0.8	V
TA	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

^{2.} The package thermal impedance is calculated in accordance with JESD 51-7.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAR	AMETER		TEST CONDITION	MIN	TYP†	MAX	UNIT		
VIK		V _{CC} = 4.5 V,	$I_{I} = -18 \text{ mA}$				-1.2	V	
1.		$V_{CC} = 0 V$	V _I = 5.5 V				10		
<u>"</u>		$V_{CC} = 5.5 \text{ V},$	$V_I = 5.5 \text{ V or GND}$				±1	μΑ	
ICC		$V_{CC} = 5.5 \text{ V},$	$I_{O} = 0,$	$V_I = V_{CC}$ or GND			3	μΑ	
∆lcc [‡]	Control inputs	$V_{CC} = 5.5 \text{ V},$	One input at 3.4 V,	Other inputs at V _{CC} or GND			2.5	mA	
Ci	Control inputs	$V_I = 3 V \text{ or } 0$				4.5		pF	
C _{io(OFF)}		$V_0 = 3 \text{ V or } 0,$	OE = V _{CC}			5.5		pF	
		$V_{CC} = 4 \text{ V},$ TYP at $V_{CC} = 4 \text{ V}$	V _I = 2.4 V,	I _I = 15 mA		14	20		
ron§			V _I = 0	I _I = 64 mA		5	7	Ω	
		V _{CC} = 4.5 V	v - 0	I _I = 30 mA		5	7		
			V _I = 2.4 V,	I _I = 15 mA		8	12		

[†] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

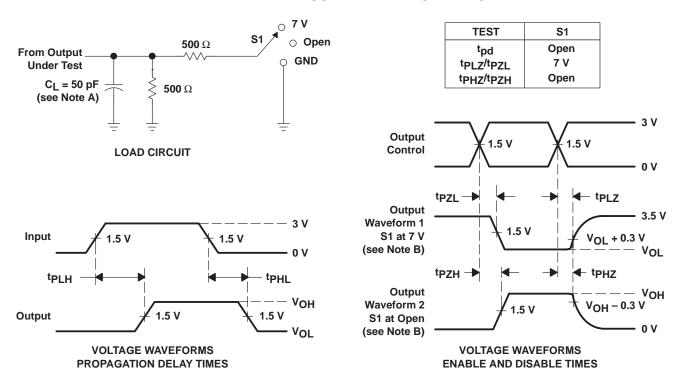
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4 V		V _{CC} = 5 V ± 0.5 V		UNIT
	(INFOT)	(001701)	MIN	MAX	MIN	MAX	
t _{pd} ¶	A or B	B or A		0.35		0.25	ns
t _{en}	ŌĒ	A or B		9.3	3.3	8.6	ns
t _{dis}	ŌĒ	A or B		7.1	2.8	7.9	ns

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

[‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

[§] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_I includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms







com 18-Jul-2006

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74CBT16210DGGRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CBT16210DGVRE4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT16210DGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT16210DGVR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT16210DL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT16210DLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT16210DLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT16210DLRG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT16210GQLR	PREVIEW	BGA MI CROSTA R JUNI OR	GQL	56	1000	TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DGV (R-PDSO-G**)

24 PINS SHOWN

PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

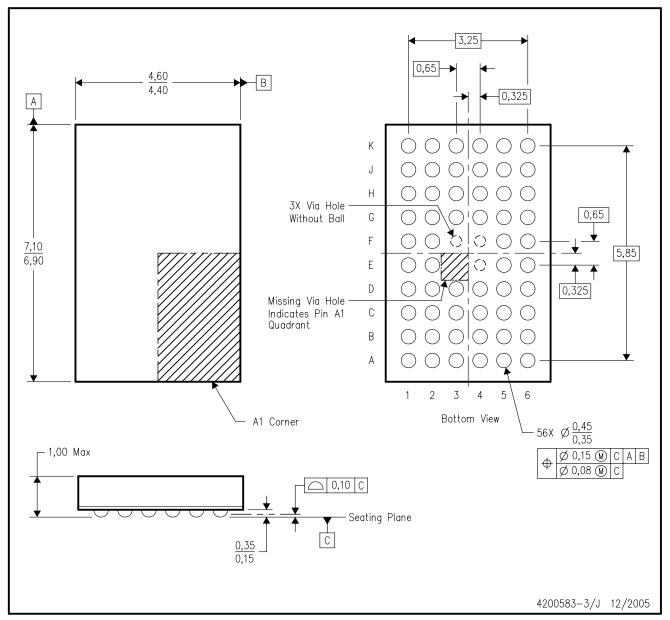
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194



GQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-225 variation BA.
- D. This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.



DL (R-PDSO-G**)

48 PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MO-118

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

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