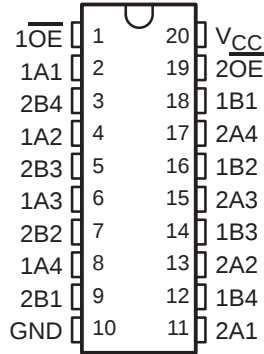


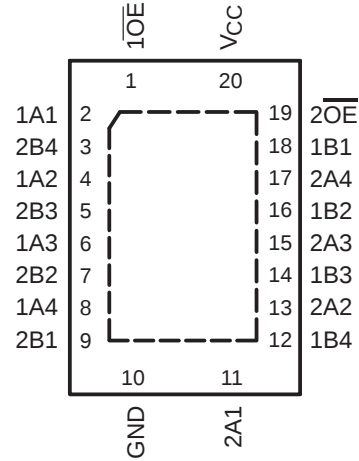
- Standard '244-Type Pinout
- 5-Ω Switch Connection Between Two Ports

- TTL-Compatible Input Levels

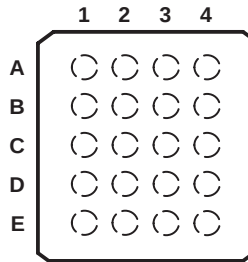
DB, DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



RGY PACKAGE
(TOP VIEW)



GQN OR ZQN PACKAGE
(TOP VIEW)



terminal assignments

	1	2	3	4
A	1A1	1OE	V _{CC}	2OE
B	1A2	2A4	2B4	1B1
C	1A3	2B3	2A3	1B2
D	1A4	2A2	2B2	1B3
E	GND	2B1	2A1	1B4

description/ordering information

ORDERING INFORMATION

T _A	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QFN – RGY	Tape and reel	SN74CBT3244RGYR	CU244
	SOIC – DW	Tube	SN74CBT3244DW	CBT3244
		Tape and reel	SN74CBT3244DWR	
	SSOP – DB	Tape and reel	SN74CBT3244DBR	CU244
	SSOP (QSOP) – DBQ	Tape and reel	SN74CBT3244DBQR	CBT3244
	TSSOP – PW	Tube	SN74CBT3244PW	CU244
		Tape and reel	SN74CBT3244PWR	
	TVSOP – DGV	Tape and reel	SN74CBT3244DGV	CU244
	VFBGA – GQN	Tape and reel	SN74CBT3244GQNR	CU244
	VFBGA – ZQN (Pb-free)		SN74CBT3244ZQNR	

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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SN74CBT3244
OCTAL FET BUS SWITCH

SCDS001N – NOVEMBER 1992 – REVISED SEPTEMBER 2003

description/ordering information (continued)

The SN74CBT3244 provides eight bits of high-speed TTL-compatible bus switching. The SOIC, SSOP, TSSOP, and TVSOP packages provide a standard '244 device pinout. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

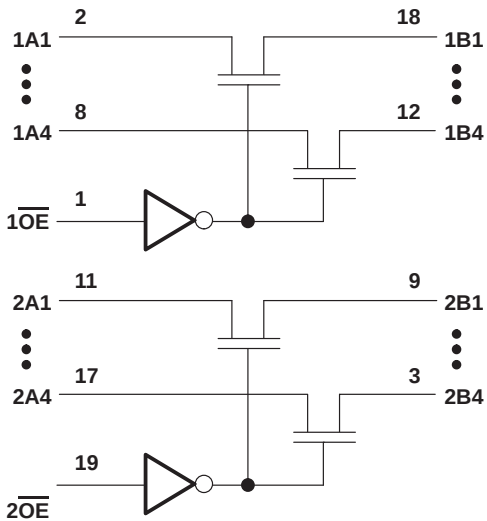
The device is organized as two 4-bit low-impedance switches with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the switch is on, and data can flow from port A to port B, or vice versa. When $\overline{OE}$ is high, the switch is open, and the high-impedance state exists between the two ports.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE
(each 4-bit bus switch)

INPUT $\overline{OE}$	FUNCTION
L	A port = B port
H	Disconnect

logic diagram (positive logic)



Pin numbers shown are for the DB, DBQ, DGV, DW, RGY, and PW packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Continuous channel current	128 mA
Clamp current, I_K ($V_{I/O} < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package	70°C/W
(see Note 2): DBQ package	68°C/W
(see Note 2): DGV package	92°C/W
(see Note 2): DW package	58°C/W
(see Note 2): GQN/ZQN package	78°C/W
(see Note 2): PW package	83°C/W
(see Note 3): RGY package	37°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.
3. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 4)

	MIN	MAX	UNIT
V_{CC} Supply voltage	4.5	5.5	V
V_{IH} High-level control input voltage	2		V
V_{IL} Low-level control input voltage		0.8	V
T_A Operating free-air temperature	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP [‡]	MAX	UNIT	
V _{IK}		V _{CC} = 4.5 V, I _I = -18 mA					-1.2	V	
I _I		V _{CC} = 5.5 V, V _I = 5.5 V or GND					±5	μA	
I _{CC}		V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND					50	μA	
ΔI _{CC} [§]	Control inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND					3.5	mA	
C _i	Control inputs	V _I = 3 V or 0					3	pF	
C _{io} (OFF)		V _O = 3 V or 0, $\overline{OE}$ = V _{CC}					6	pF	
r _{on} [¶]		V _{CC} = 4.5 V	V _I = 0	I _I = 64 mA			5	7	Ω
				I _I = 30 mA			5	7	
			V _I = 2.4 V, I _I = 15 mA				10	15	

[‡] All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

^{\S} This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

^{\parallel} Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

SN74CBT3244

OCTAL FET BUS SWITCH

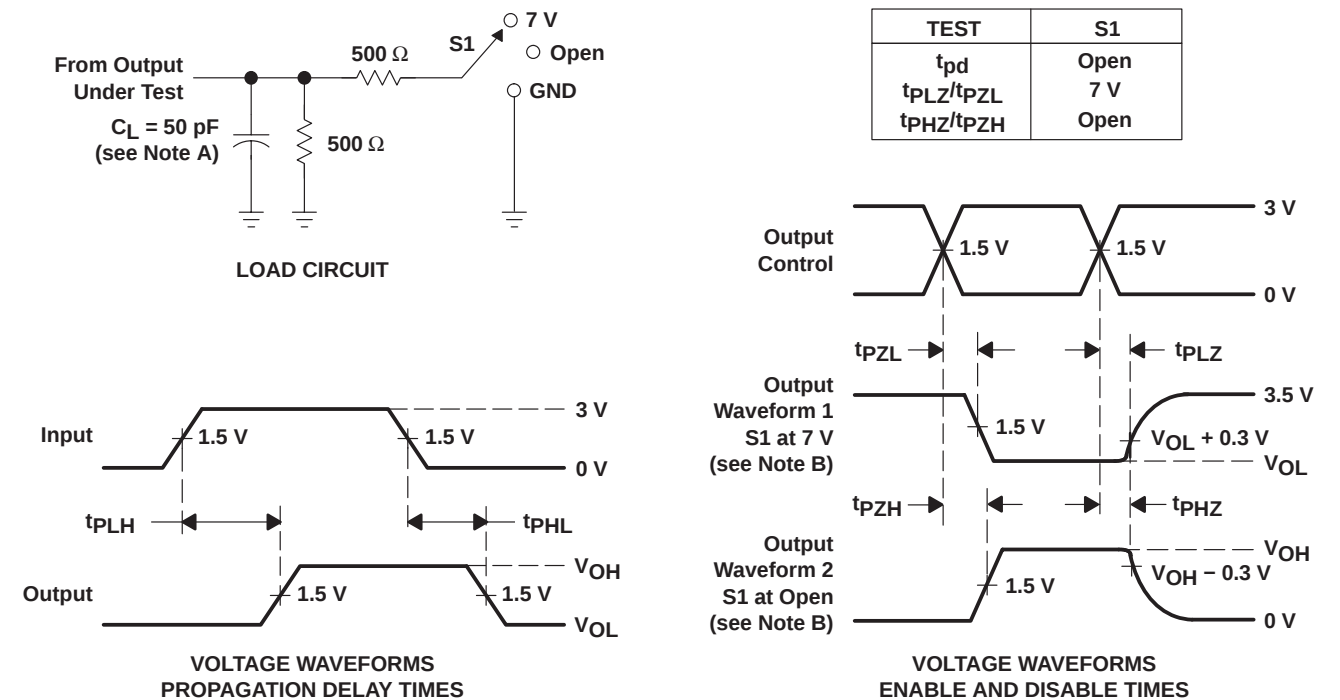
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switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
$t_{pd}^\dagger$	A or B	B or A		0.25	ns
t_{en}	$\overline{OE}$	A or B	1	8.9	ns
t_{dis}	$\overline{OE}$	A or B	1	7.4	ns

[†] This propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

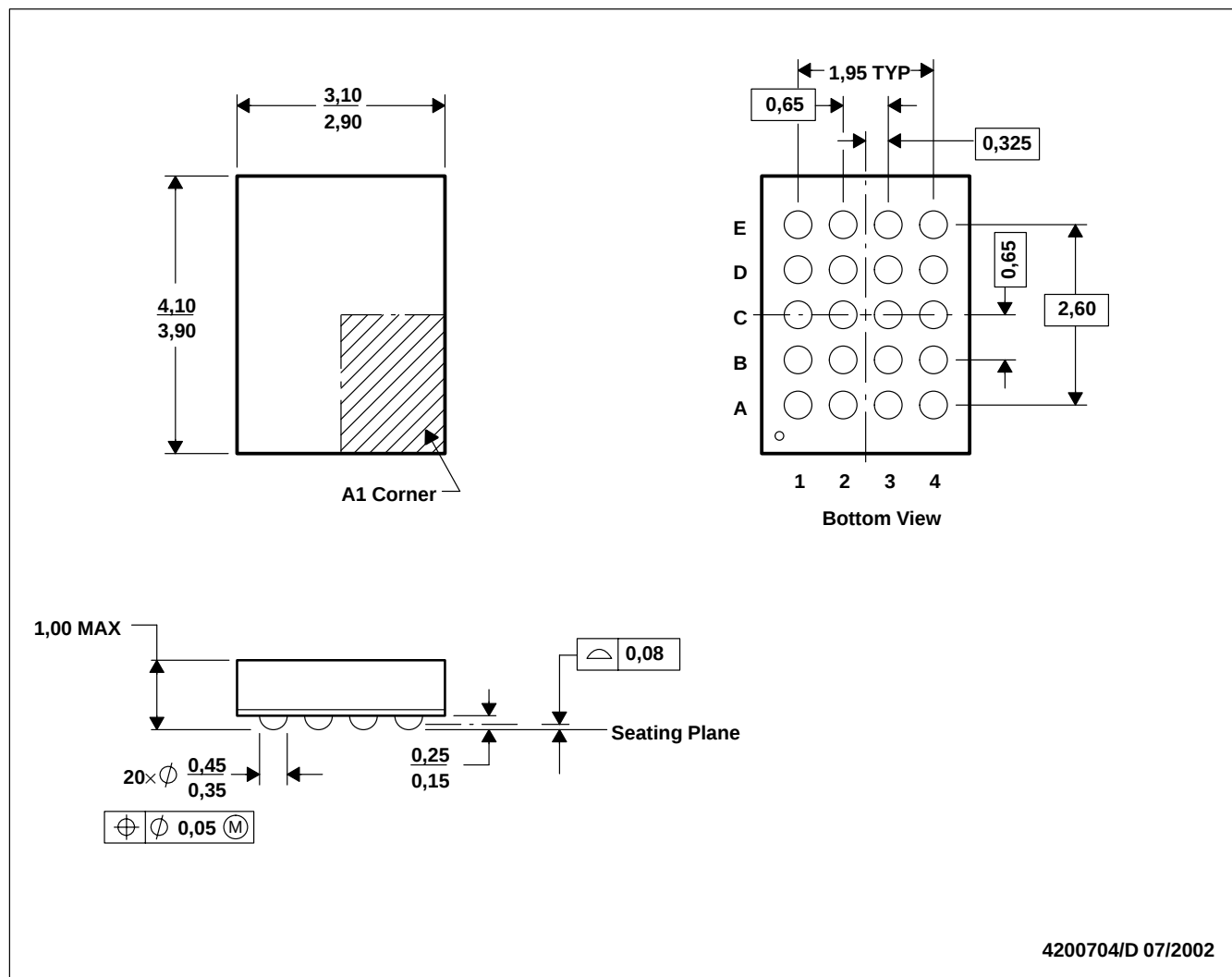


- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

GQN (R-PBGA-N20)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. MicroStar Junior™ configuration
 - D. Falls within JEDEC MO-225 variation BC.
 - E. This package is tin-lead (SnPb). Refer to the 20 ZQN package (drawing 4204492) for lead-free.

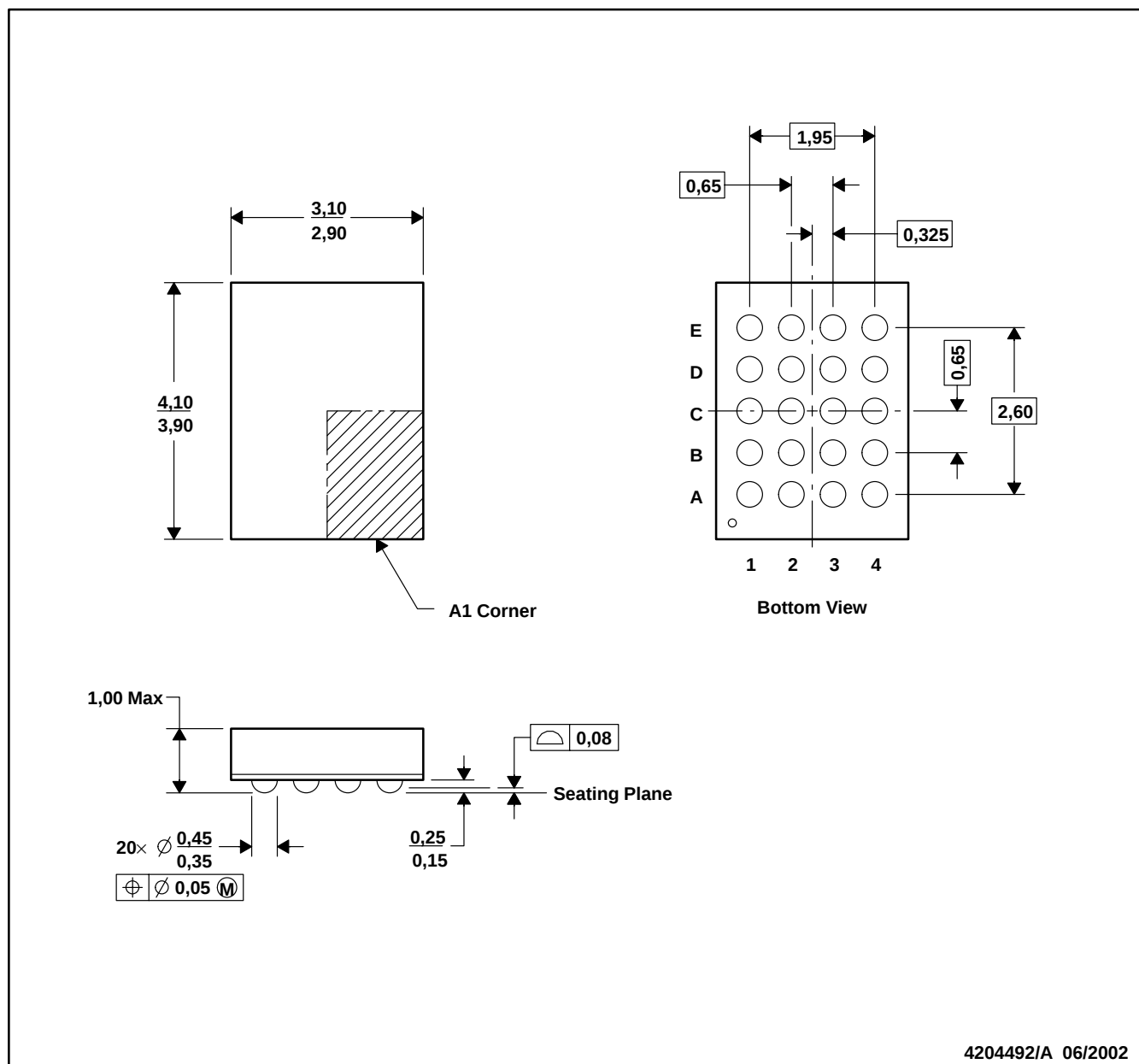
MicroStar Junior is a trademark of Texas Instruments.



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ZQN (R-PBGA-N20)

PLASTIC BALL GRID ARRAY



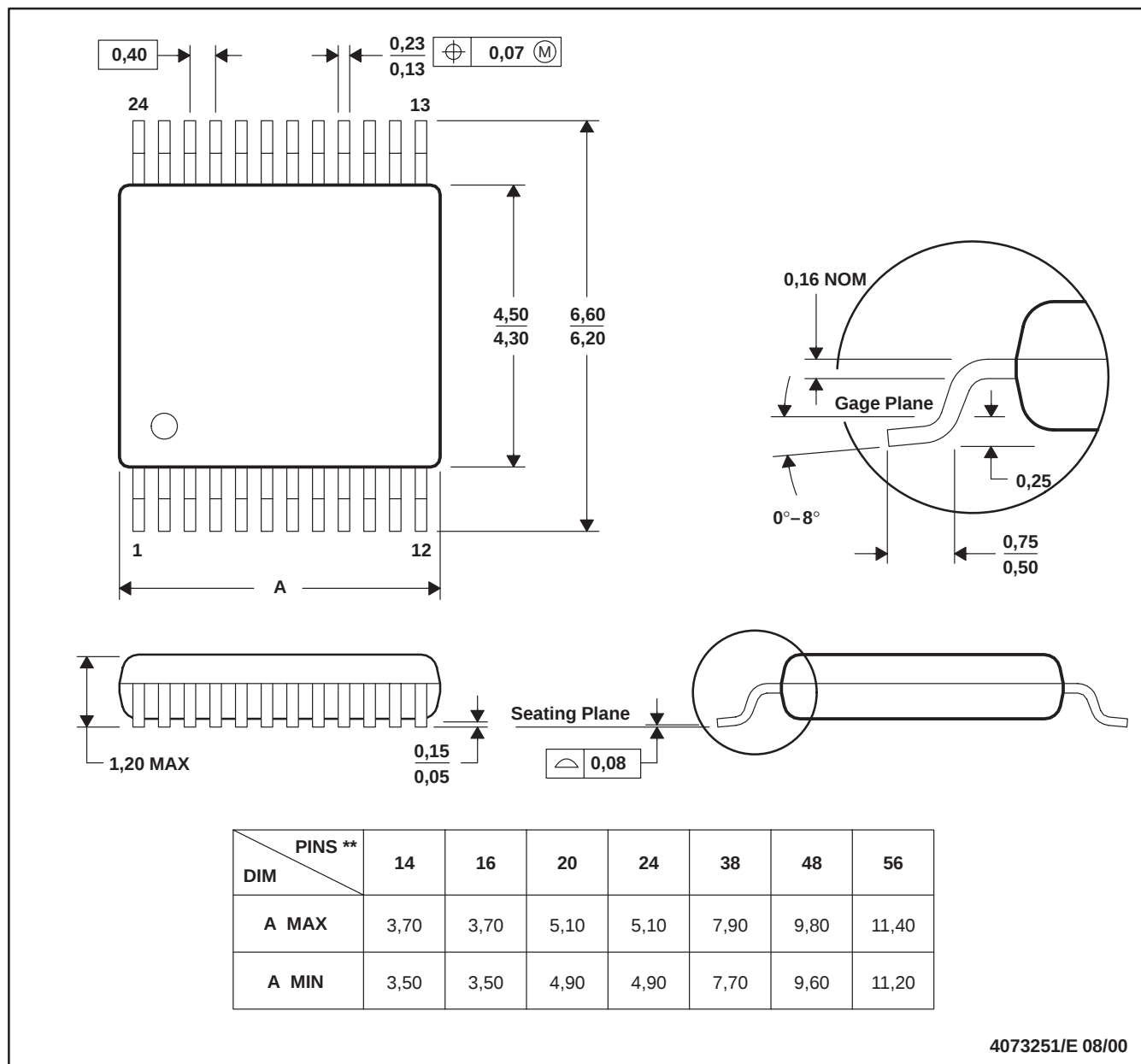
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. MicroStar Junior™ configuration.
 - D. Fall within JEDEC MO-225 variation BC.
 - E. This package is lead-free. Refer to the 20 GQN package (drawing 4200704) for tin-lead (SnPb).

MicroStar Junior is a trademark of Texas Instruments.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

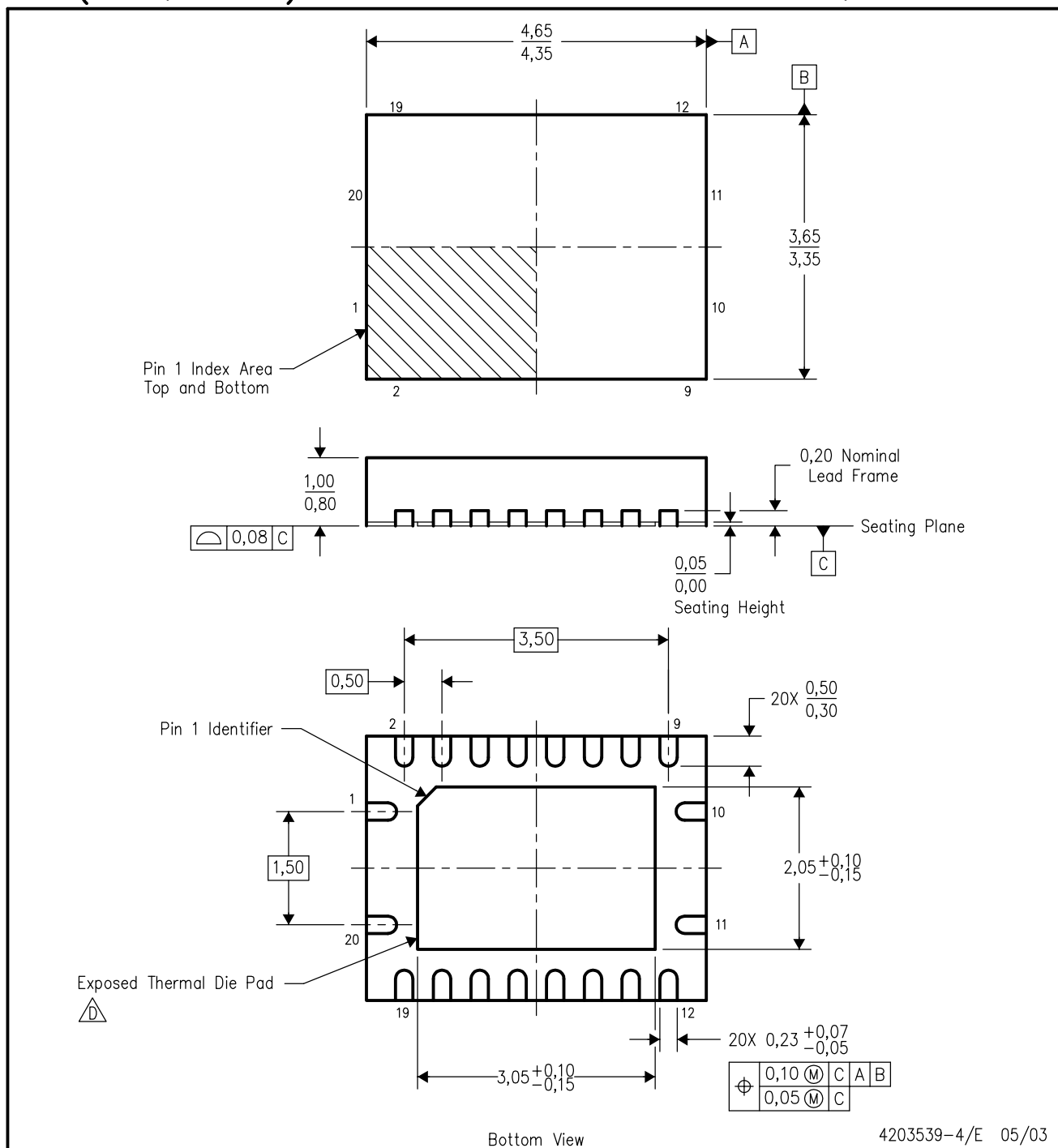
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

RGY (R-PQFP-N20)

PLASTIC QUAD FLATPACK

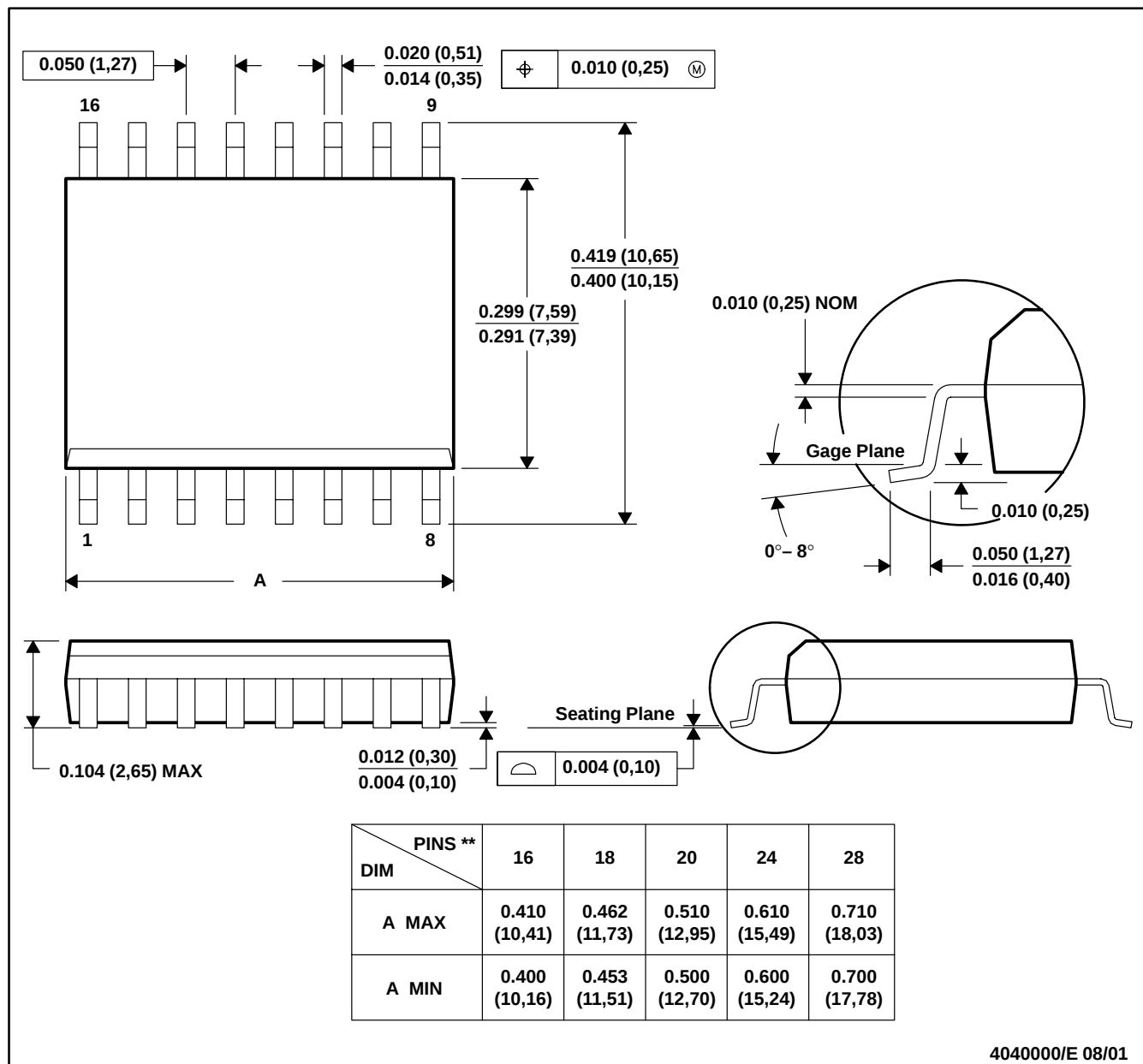


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 -  D. The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected ground leads.
 - E. Package complies to JEDEC MO-241 variation BC.

DW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

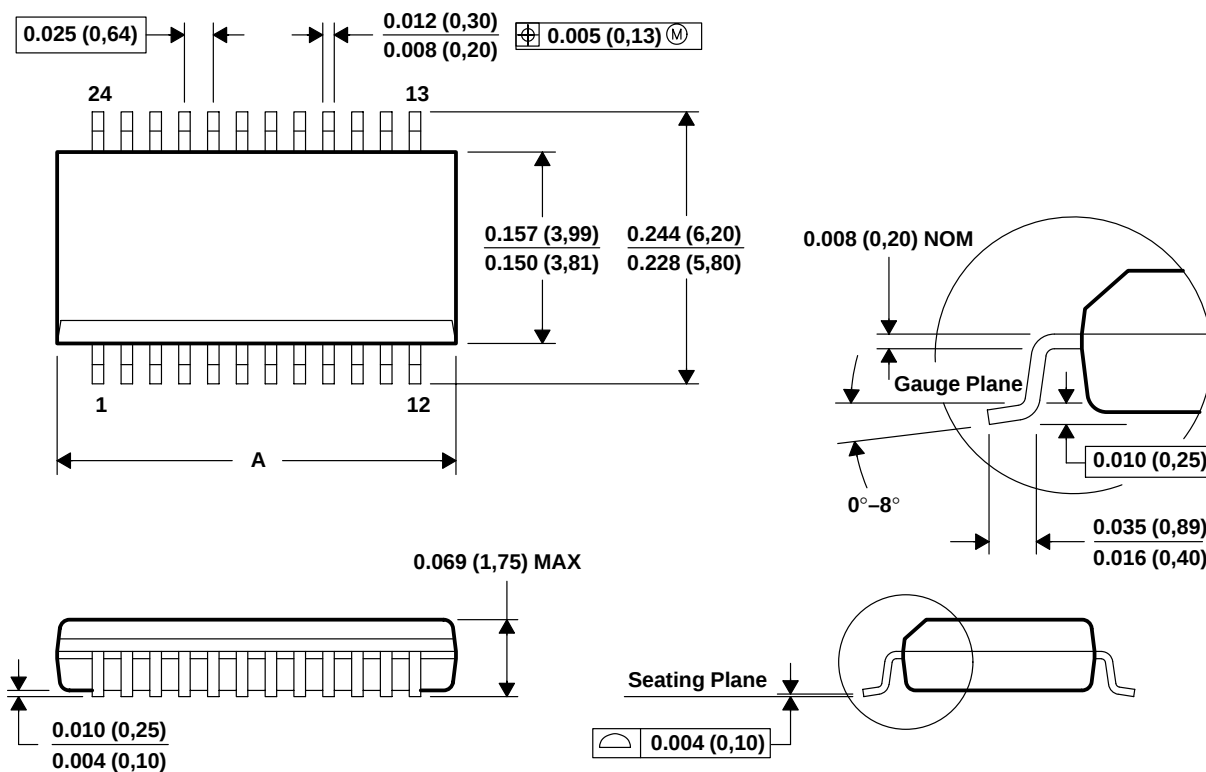
16 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-013

DBQ (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE



PINS **	16	20	24	28
DIM				
A MAX	0.197 (5,00)	0.344 (8,74)	0.344 (8,74)	0.394 (10,01)
A MIN	0.189 (4,80)	0.337 (8,56)	0.337 (8,56)	0.386 (9,80)
M0-137 VARIATION	AB	AD	AE	AF

4073301/F 02/02

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-137.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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