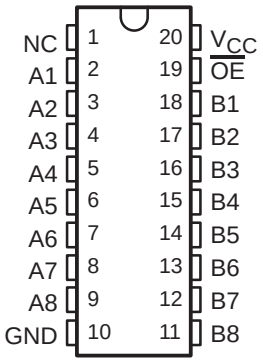
SCDS002P − NOVEMBER 1992 − REVISED SEPTEMBER 2003

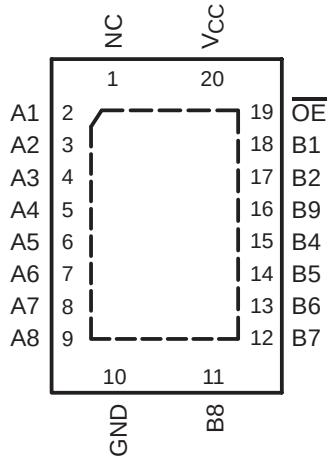
- **Standard ’245-Type Pinout**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**

**DB, DBQ, DGV, DW, OR PW PACKAGE**
**(TOP VIEW)**



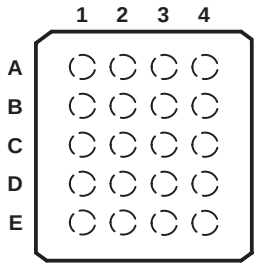

NC − No internal connection

**RGY PACKAGE**
**(TOP VIEW)**




NC − No internal connection

**GQN OR ZQN PACKAGE**
**(TOP VIEW)**




### terminal assignments

| | 1 | 2 | 3 | 4 |
|---|---|---|---|---|
| **A** | A1 | NC | $V_{CC}$ | $\overline{OE}$ |
| **B** | A3 | B2 | A2 | B1 |
| **C** | A5 | A4 | B4 | B3 |
| **D** | A7 | B6 | A6 | B5 |
| **E** | GND | A8 | B8 | B7 |

NC − No internal connection

## description/ordering information

The SN74CBT3245A provides eight bits of high-speed TTL-compatible bus switching. The SOIC, SSOP, TSSOP, and TVSOP packages provide a standard ’245 device pinout. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as one 8-bit switch. When the output-enable ($\overline{OE}$) input is low, the switch is on, and port A is connected to port B. When $\overline{OE}$ is high, the switch is open, and the high-impedance state exists between the two ports.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## description/ordering information (continued)

**ORDERING INFORMATION**

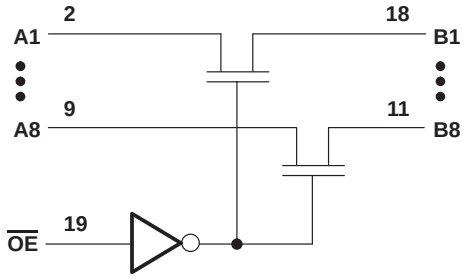
| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| −40°C to 85°C | QFN − RGY | Tape and reel | SN74CBT3245ARGYR | CU245A |
| | SOIC − DW | Tube | SN74CBT3245ADW | CBT3245A |
| | | Tape and reel | SN74CBT3245ADWR | |
| | SSOP − DB | Tape and reel | SN74CBT3245ADBR | CU245A |
| | SSOP (QSOP) − DBQ | Tape and reel | SN74CBT3245ADBQR | CBT3245A |
| | TSSOP − PW | Tube | SN74CBT3245APW | CU245A |
| | | Tape and reel | SN74CBT3245APWR | |
| | TVSOP − DGV | Tape and reel | SN74CBT3245ADGVR | CU245A |
| | VFBGA − GQN | Tape and reel | SN74CBT3245AGQNR | CU245A |
| | VFBGA − ZQN (Pb-free) | | SN74CBT3245AZQNR | |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

**FUNCTION TABLE**

| INPUT $\overline{OE}$ | FUNCTION |
|---|---|
| L | A port = B port |
| H | Disconnect |

## logic diagram (positive logic)




Pin numbers shown are for the DB, DBQ, DGV, DW, PW, and RGY packages.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . −0.5 V to 7 V
Continuous channel current . . . . . 128 mA
Input clamp current, $I_{IK}$ ($V_{I/O}$ < 0) . . . . . −50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package . . . . . 70°C/W
(see Note 2): DBQ package . . . . . 68°C/W
(see Note 2): DGV package . . . . . 92°C/W
(see Note 2): DW package . . . . . 58°C/W
(see Note 2): GQN/ZQN package . . . . . 78°C/W
(see Note 2): PW package . . . . . 83°C/W
(see Note 3): RGY package . . . . . 37°C/W
Storage temperature range, $T_{stg}$ . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.
3. The package thermal impedance is calculated in accordance with JESD 51-5.

### recommended operating conditions (see Note 4)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4 | 5.5 | V |
| $V_{IH}$ | High-level control input voltage | 2 | | V |
| $V_{IL}$ | Low-level control input voltage | | 0.8 | V |
| $T_A$ | Operating free-air temperature | −40 | 85 | °C |

NOTE 4: All unused control inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | | −1.2 | V |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 5.5 V or GND | | | | ±5 | μA |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V, | $I_O$ = 0, | $V_I$ = $V_{CC}$ or GND | | | 50 | μA |
| $\Delta I_{CC}$§ | Control inputs | $V_{CC}$ = 5.5 V, | One input at 3.4 V, | Other inputs at $V_{CC}$ or GND | | | 3.5 | mA |
| $C_i$ | Control inputs | $V_I$ = 3 V or 0 | | | | 4 | | pF |
| $C_{io(OFF)}$ | | $V_O$ = 3 V or 0, | $\overline{OE}$ = $V_{CC}$ | | | 4 | | pF |
| $r_{on}$¶ | | $V_{CC}$ = 4.5 V | $V_I$ = 0 | $I_I$ = 64 mA | | 5 | 7 | Ω |
| | | | | $I_I$ = 30 mA | | 5 | 7 | |
| | | | $V_I$ = 2.4 V, | $I_I$ = 15 mA | | 10 | 15 | |

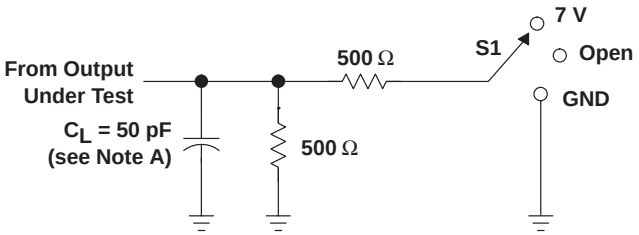
‡ All typical values are at $V_{CC}$ = 5 V (unless otherwise noted), $T_A$ = 25°C.
§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than $V_{CC}$ or GND.
¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

**switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 4 V | | $V_{CC}$ = 5 V ± 0.5 V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_{pd}$† | A or B | B or A | | 0.35 | | 0.25 | ns |
| $t_{en}$ | $\overline{OE}$ | A or B | | 6.4 | 1.9 | 5.9 | ns |
| $t_{dis}$ | $\overline{OE}$ | A or B | | 5.7 | 2.1 | 6 | ns |

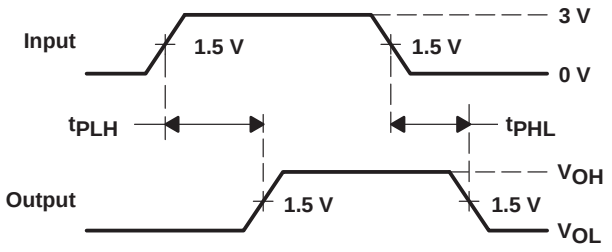
† The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

## PARAMETER MEASUREMENT INFORMATION

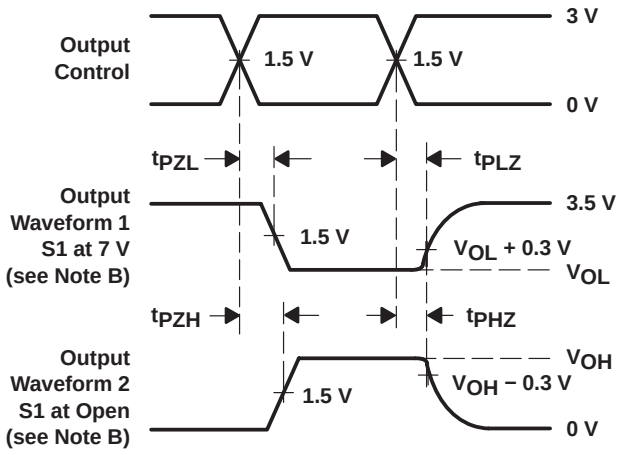



LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V |
| $t_{PHZ}/t_{PZH}$ | Open |




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

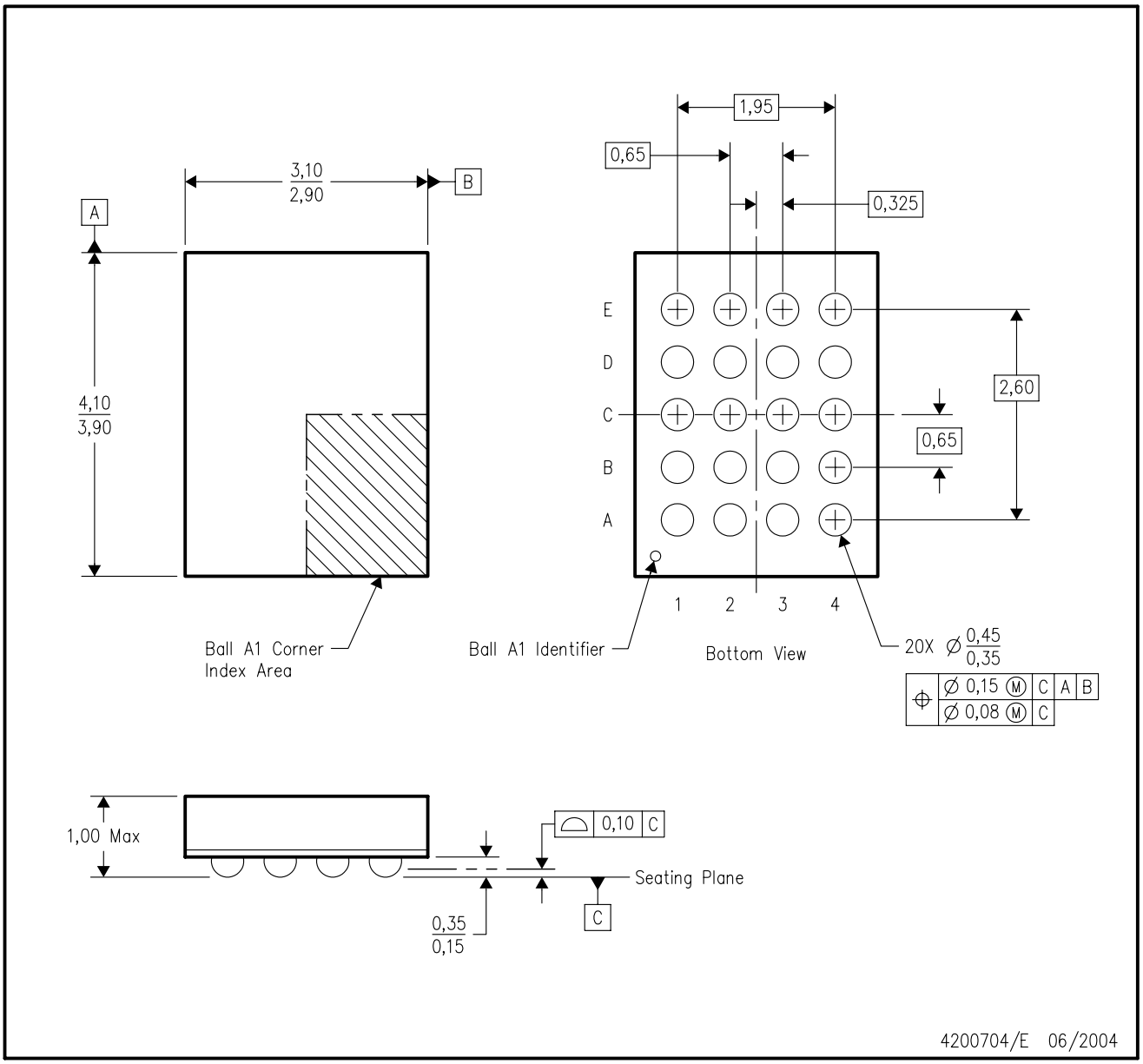



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
H. All parameters and waveforms are not applicable to all devices.

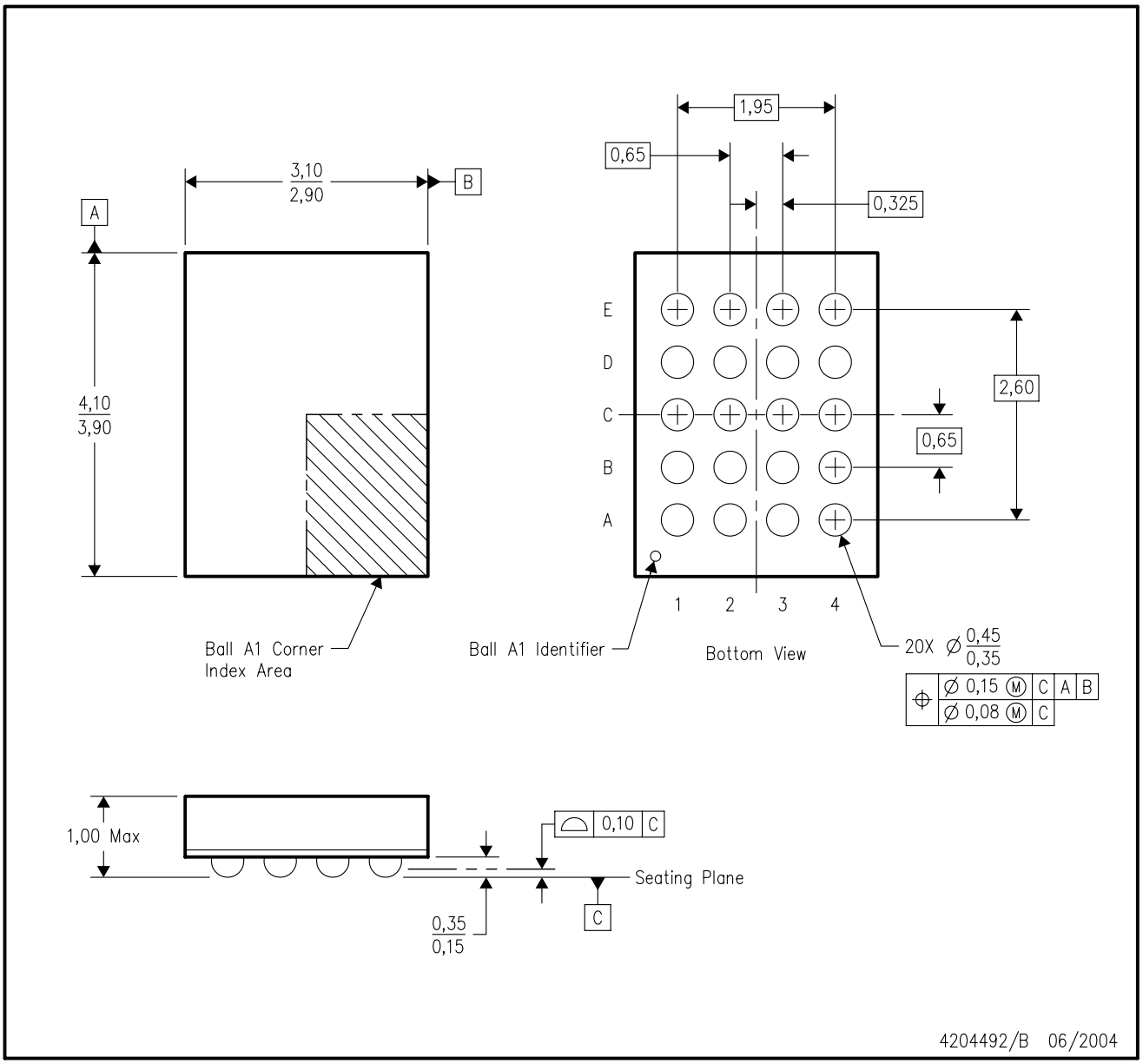
**Figure 1. Load Circuit and Voltage Waveforms**

## GQN (R–PBGA–N20) PLASTIC BALL GRID ARRAY




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–225 variation BC.
D. This package is tin–lead (SnPb). Refer to the 20 ZQN package (drawing 4204492) for lead–free.

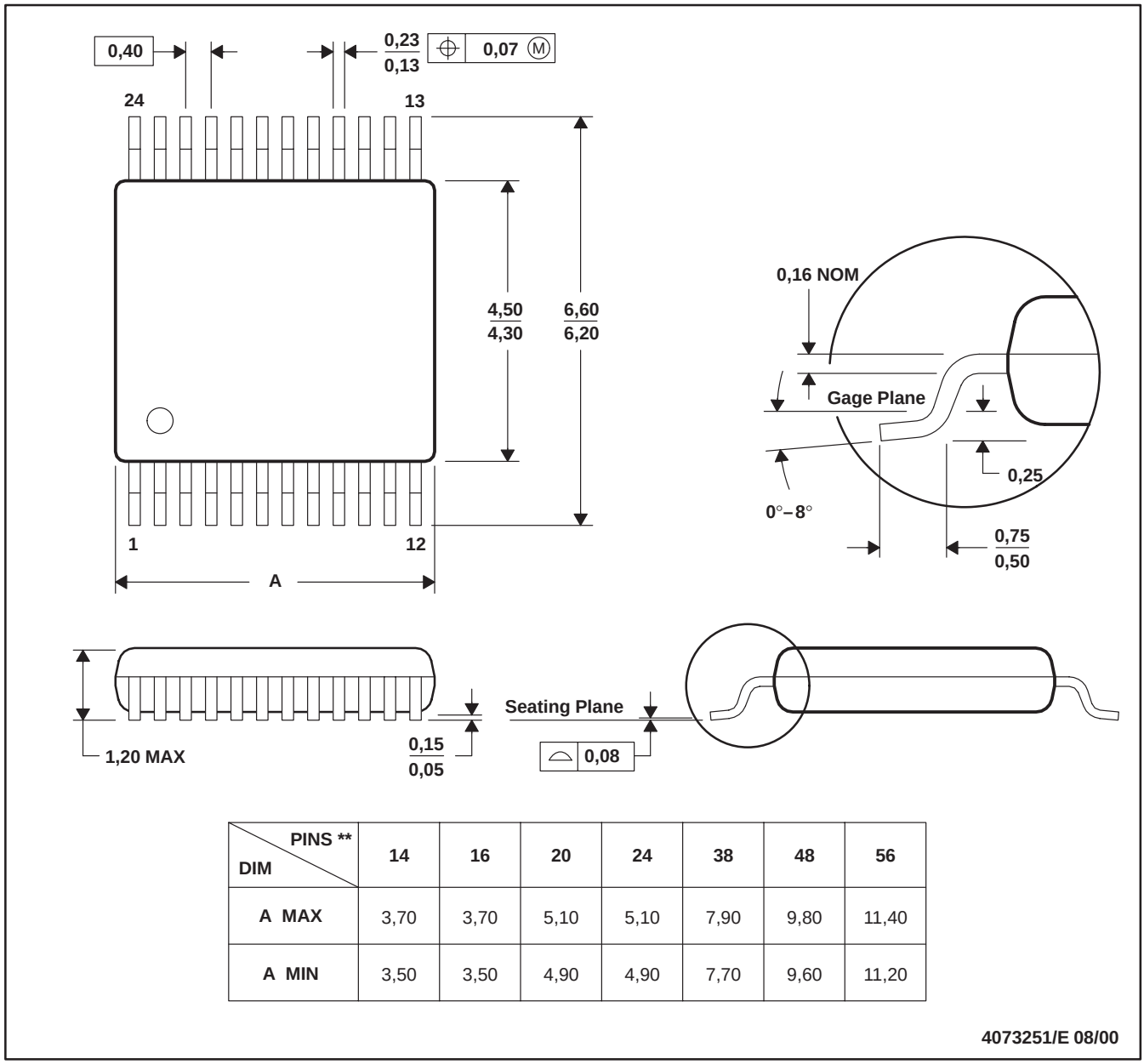
## ZQN (R–PBGA–N20) PLASTIC BALL GRID ARRAY




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–225 variation BC.
D. This package is lead–free. Refer to the 20 GQN package (drawing 4200704) for tin–lead (SnPb).

**DGV (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**24 PINS SHOWN**

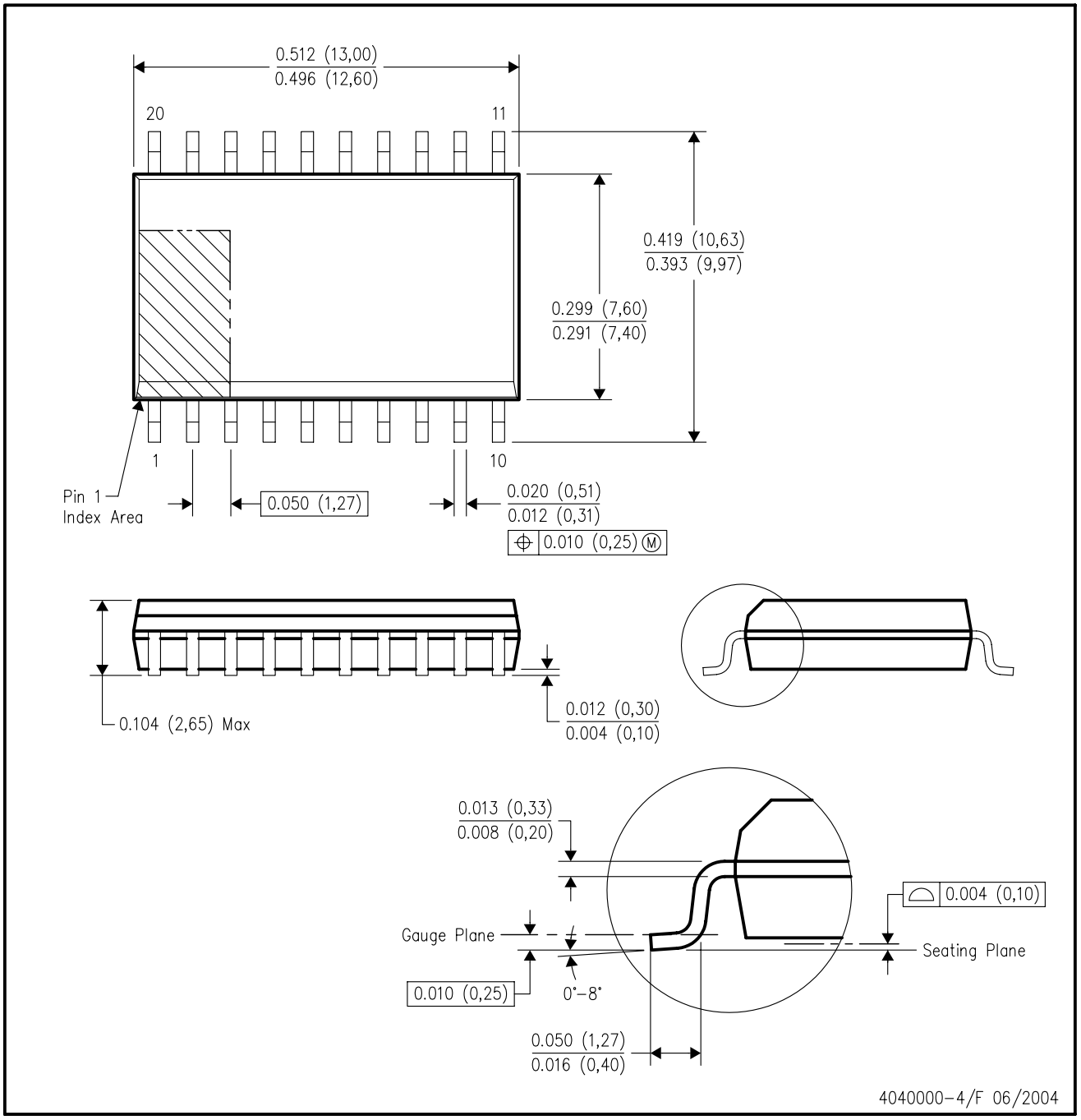



| DIM \ PINS ** | 14 | 16 | 20 | 24 | 38 | 48 | 56 |
|---|---|---|---|---|---|---|---|
| A MAX | 3,70 | 3,70 | 5,10 | 5,10 | 7,90 | 9,80 | 11,40 |
| A MIN | 3,50 | 3,50 | 4,90 | 4,90 | 7,70 | 9,60 | 11,20 |

**4073251/E 08/00**

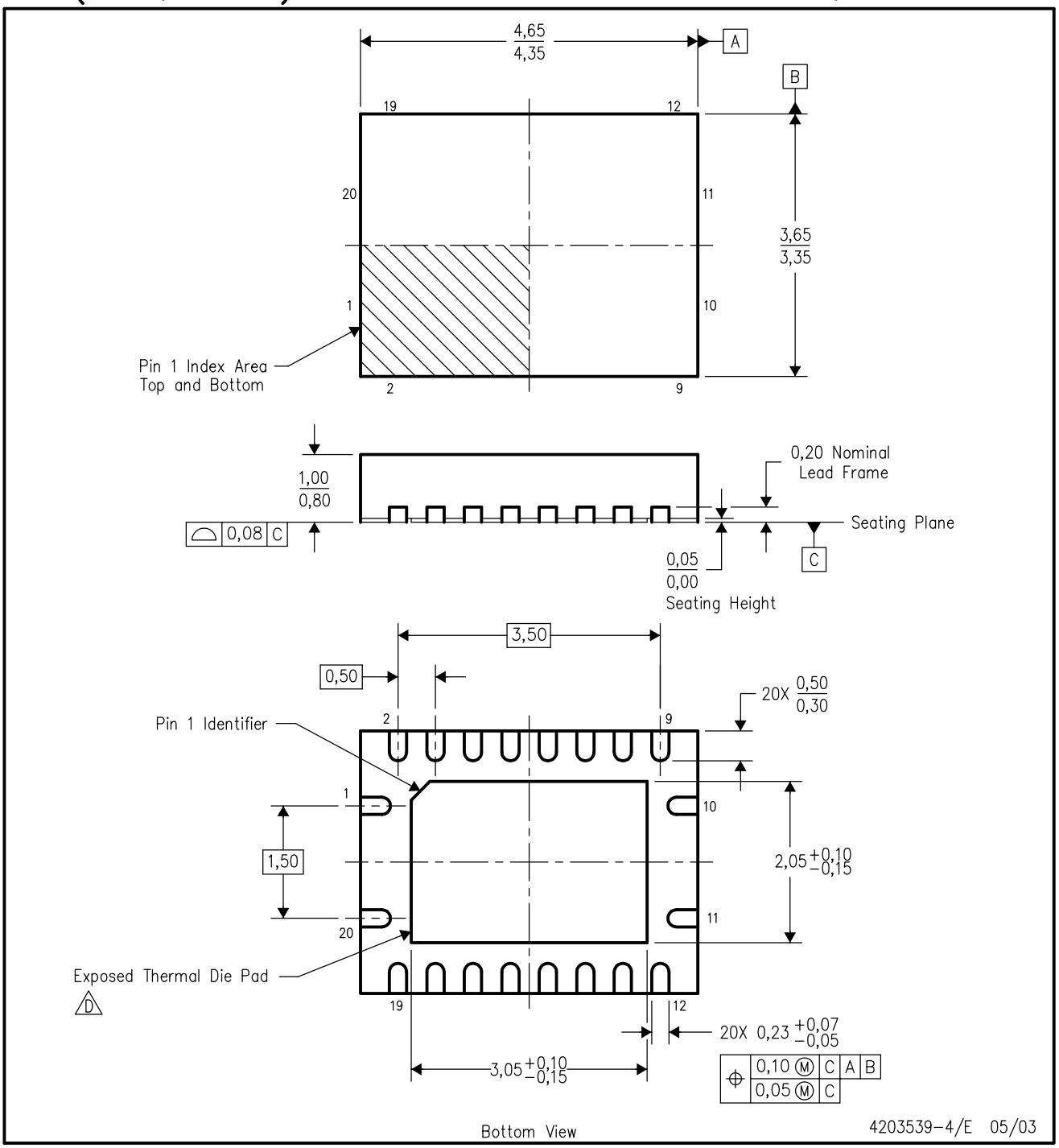
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

## DW (R–PDSO–G20) PLASTIC SMALL–OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AC.

RGY (R–PQFP–N20) PLASTIC QUAD FLATPACK




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected ground leads.
E. Package complies to JEDEC MO–241 variation BC.

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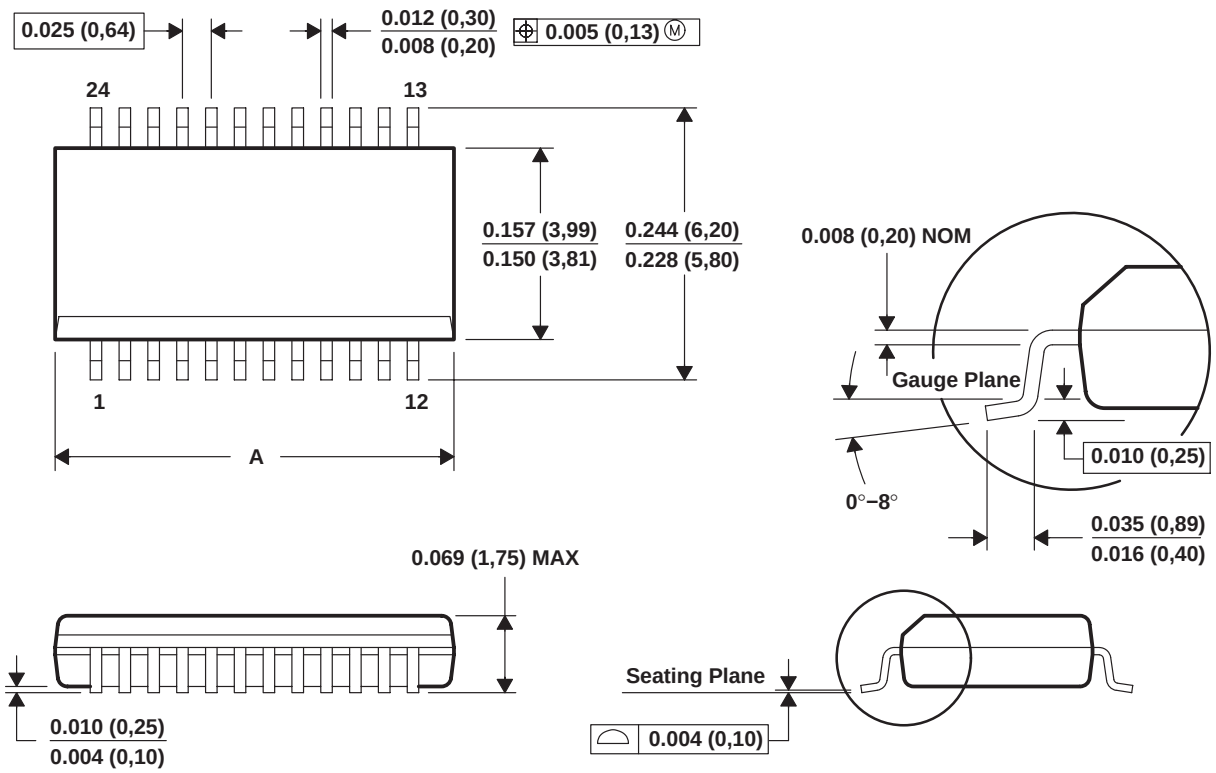
**DBQ (R−PDSO−G**)** **PLASTIC SMALL−OUTLINE PACKAGE**




| DIM \ PINS ** | 16 | 20 | 24 | 28 |
|---|---|---|---|---|
| A MAX | 0.197 (5,00) | 0.344 (8,74) | 0.344 (8,74) | 0.394 (10,01) |
| A MIN | 0.189 (4,80) | 0.337 (8,56) | 0.337 (8,56) | 0.386 (9,80) |
| M0−137 VARIATION | AB | AD | AE | AF |

4073301/F 02/2002

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO−137.

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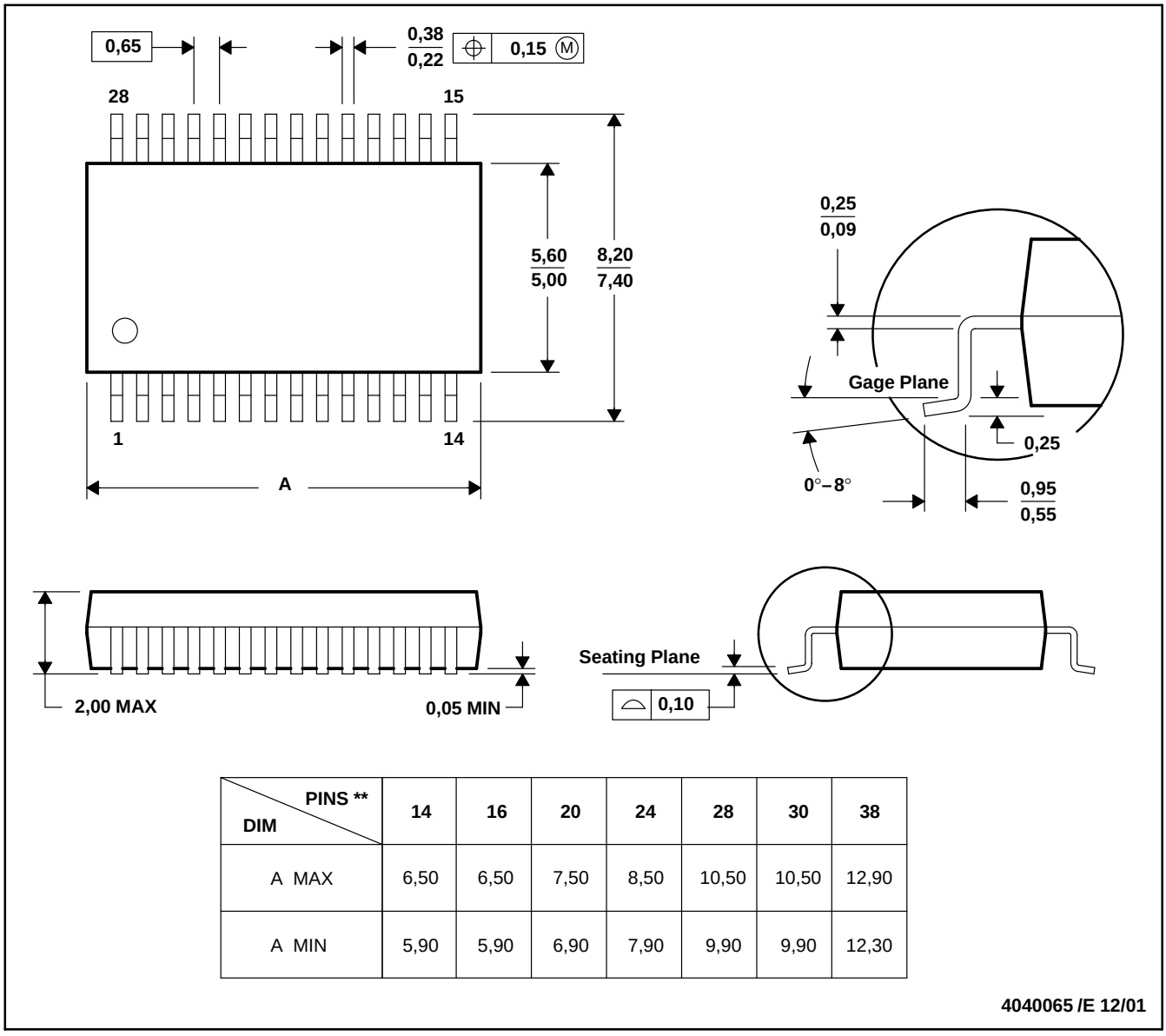
**DB (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**28 PINS SHOWN**



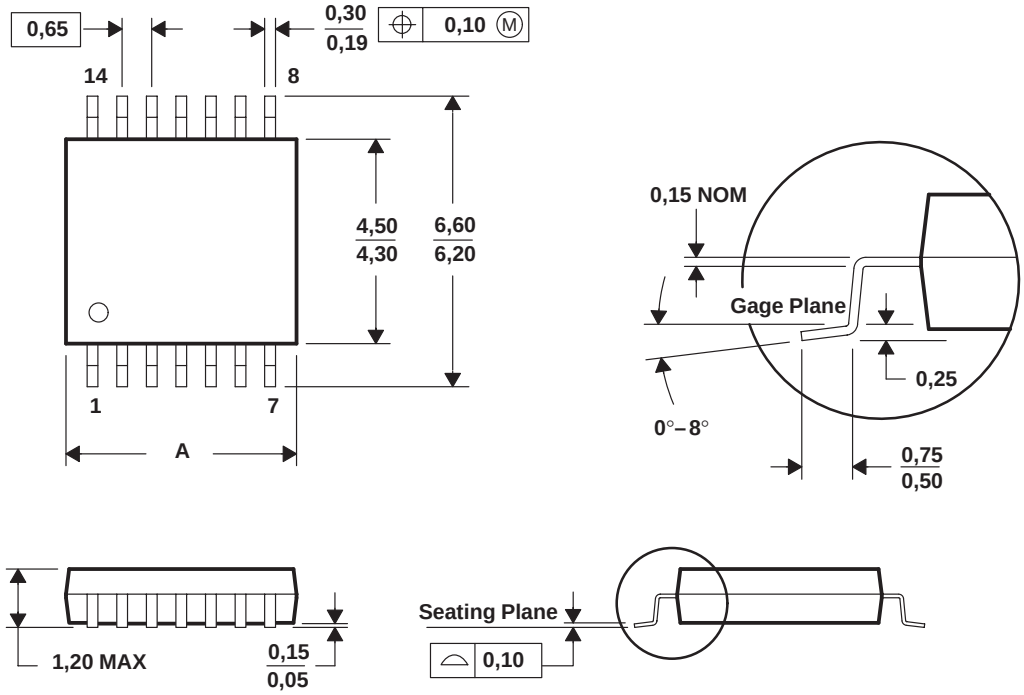

| DIM \ PINS ** | 14 | 16 | 20 | 24 | 28 | 30 | 38 |
|---|---|---|---|---|---|---|---|
| A MAX | 6,50 | 6,50 | 7,50 | 8,50 | 10,50 | 10,50 | 12,90 |
| A MIN | 5,90 | 5,90 | 6,90 | 7,90 | 9,90 | 9,90 | 12,30 |

**4040065 /E 12/01**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

**PW (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14 PINS SHOWN**




| DIM \ PINS ** | 8 | 14 | 16 | 20 | 24 | 28 |
|---|---|---|---|---|---|---|
| A MAX | 3,10 | 5,10 | 5,10 | 6,60 | 7,90 | 9,80 |
| A MIN | 2,90 | 4,90 | 4,90 | 6,40 | 7,70 | 9,60 |

**4040064/F 01/97**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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