

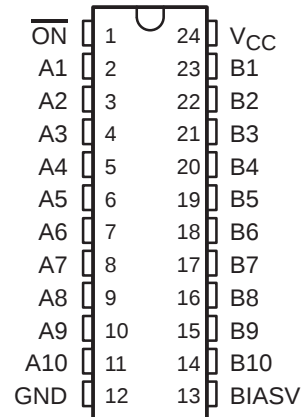
SN74CBTK6800

10-BIT FET BUS SWITCH WITH PRECHARGED OUTPUTS AND ACTIVE-CLAMP UNDERSHOOT-PROTECTION CIRCUIT

SCDS107B – APRIL 2000 – REVISED OCTOBER 2000

- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Power Off Disables Outputs, Permitting Live Insertion
- Outputs Are Precharged by Bias Voltage to Minimize Signal Distortion During Live Insertion
- Active-Clamp Undershoot-Protection Circuit on the I/Os Clamps Undershoots Down to -2 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



description

The SN74CBTK6800 device provides ten bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows bidirectional connections to be made while adding near-zero propagation delay. The device also precharges the B port to a user-selectable bias voltage (BIASV) to minimize live-insertion noise.

The A and B ports have an active-clamp undershoot-protection circuit. When there is an undershoot, the active-clamp circuit is enabled and current from V_{CC} is supplied to clamp the output, preventing the pass transistor from turning on.

The SN74CBTK6800 is organized as one 10-bit switch with a single enable ($\overline{ON}$) input. When $\overline{ON}$ is low, the switch is on, and port A is connected to port B. When $\overline{ON}$ is high, the switch between port A and port B is open. When $\overline{ON}$ is high or V_{CC} is 0 V, B port is precharged to BIASV through the equivalent of a 10-kΩ resistor.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SOIC – DW	Tube	SN74CBTK6800DW	CBTK6800
		Tape and reel	SN74CBTK6800DWR	
	SSOP (QSOP) – DBQ	Tape and reel	SN74CBTK6800DBQR	CBTK6800
	TSSOP – PW	Tape and reel	SN74CBTK6800PWR	BK6800
	TVSOP – DGV	Tape and reel	SN74CBTK6800DGVR	BK6800

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUT $\overline{ON}$	FUNCTION
L	A port = B port
H	A port = Z B port = BIASV



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 **TEXAS
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
V_{IK}		$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$			-1.2	V
V_{IKU}		$V_{CC} = 5.5\text{ V}$, $0\text{ mA} \geq I_I \geq -50\text{ mA}$, $\overline{OE} = 5.5\text{ V}$			-2	V
I_I		$V_{CC} = 5.5\text{ V}$, $V_I = 5.5\text{ V}$ or GND			± 5	μA
I_{off}		$V_{CC} = 0$, V_I or $V_O = 0$ to 5.5 V , $\text{BIASV} = \text{Open}$			20	μA
I_O		$V_{CC} = 4.5\text{ V}$, $V_O = 0$, $\text{BIASV} = 2.4\text{ V}$	0.25			mA
I_{CC}		$V_{CC} = 5.5\text{ V}$, $V_I = V_{CC}$ or GND, $I_O = 0$			20	μA
$\Delta I_{CC}^\ddagger$	Control inputs	$V_{CC} = 5.5\text{ V}$, One input at 3.4 V , Other inputs at V_{CC} or GND			2.5	mA
C_i	Control inputs	$V_I = 3\text{ V}$ or 0		3		pF
$C_{O(OFF)}$		$V_O = 3\text{ V}$ or 0, Switch off		8.5		pF
$r_{on}^\S$		$V_{CC} = 4\text{ V}$, TYP at $V_{CC} = 4\text{ V}$, $V_I = 2.4\text{ V}$, $I_I = 15\text{ mA}$		11	20	Ω
		$V_{CC} = 4.5\text{ V}$, $V_I = 0$, $I_I = 64\text{ mA}$		3	7	
		$V_{CC} = 4.5\text{ V}$, $V_I = 0$, $I_I = 30\text{ mA}$		3	7	
		$V_{CC} = 4.5\text{ V}$, $V_I = 2.4\text{ V}$, $I_I = 15\text{ mA}$		6	15	

[†] All typical values are at $V_{CC} = 5\text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

[‡] This is the increase in supply current for each input that is at the specified TTL-voltage level rather than V_{CC} or GND.

[§] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$V_{CC} = 4\text{ V}$		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
				MIN	MAX	MIN	MAX	
$t_{pd}^\parallel$	A or B	B or A			0.35		0.25	ns
t_{PZH}	$\overline{ON}$	A or B	$\text{BIASV} = \text{GND}$		6	2	5.1	ns
t_{PZL}			$\text{BIASV} = 3\text{ V}$		6	2	5.6	
t_{PHZ}	$\overline{ON}$	A or B	$\text{BIASV} = \text{GND}$		5.5	1	5	ns
t_{PLZ}			$\text{BIASV} = 3\text{ V}$		5.5	2	5.9	

^{||} The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

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undershoot characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V _{OUTU}	See Figures 1 and 2, and Table 1	2	V _{OH} –0.3		V

† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

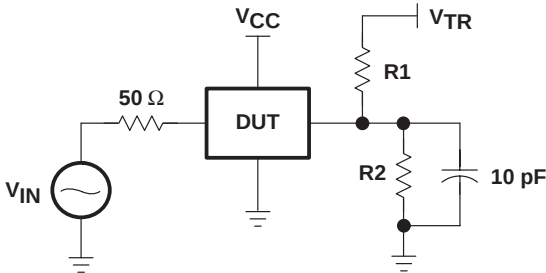


Figure 1. Device Test Setup

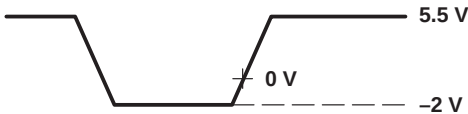


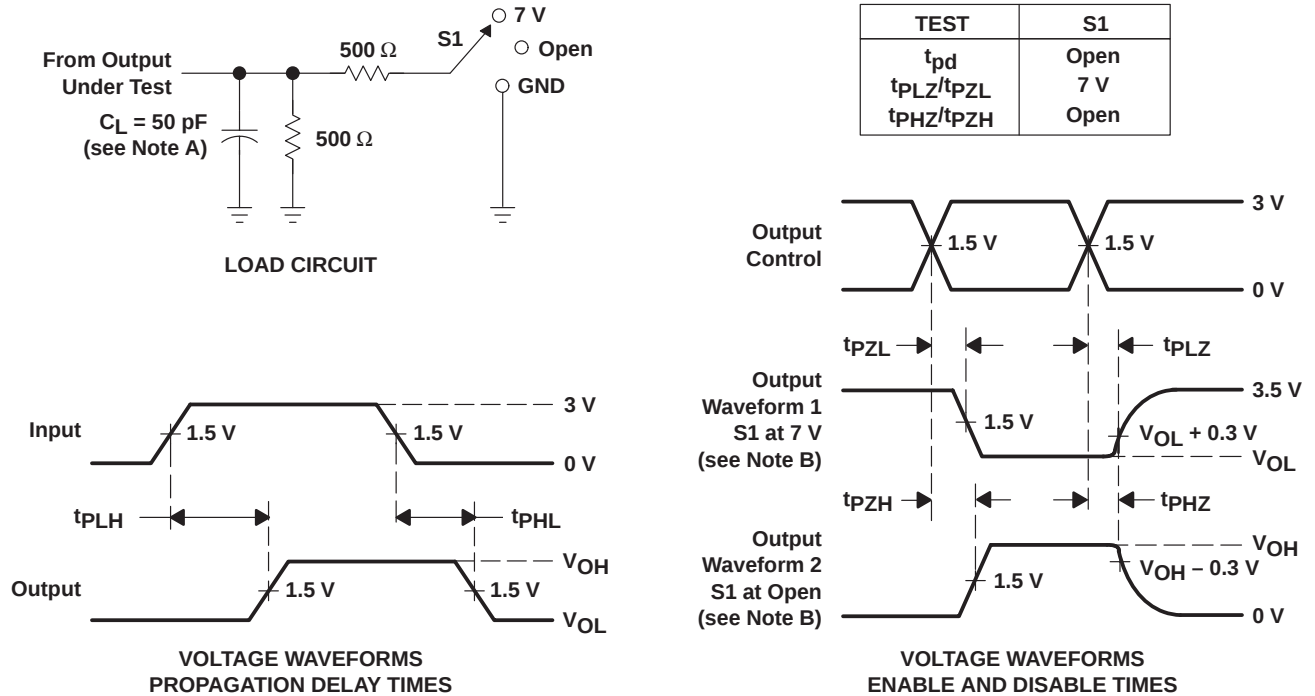
Figure 2. Transient Input Voltage Waveform

Table 1. Device Test Conditions

PARAMETER	VALUE	UNIT
B port under test‡	See Figure 1	
V _{IN}	See Figure 2	V
t _w	20	ns
t _r	2	ns
t _f	2	ns
R1 = R2	100	kΩ
V _{TR}	11	V
V _{CC}	5.5	V
BIASV	Open	

‡ Other B-port outputs are open.

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

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