

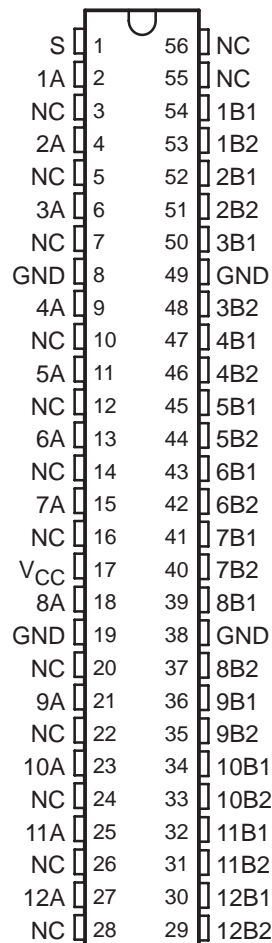
# SN74CBTLVR16292

## LOW-VOLTAGE 12-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER WITH INTERNAL PULLDOWN RESISTORS

SCDS056H – MARCH 1998 – REVISED OCTOBER 2003

- Member of the Texas Instruments Widebus™ Family
- Rail-to-Rail Switching on Data I/O Ports
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- Make-Before-Break Feature
- Internal 500-Ω Pulldown Resistors to Ground
- Input/Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22 – 2000-V Human-Body Model (A114-A)

DGG, DGV, OR DL PACKAGE  
(TOP VIEW)



### description/ordering information

The SN74CBTLVR16292 is a 12-bit 1-of-2 high-speed FET multiplexer/demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

When the select (S) input is low, port A is connected to port B1, and R<sub>INT</sub> is connected to port B2. When S is high, port A is connected to port B2, and R<sub>INT</sub> is connected to port B1.

The input/output ports include equivalent 25-Ω series resistors to reduce overshoot and undershoot.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

NC – No internal connection

### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tube	SN74CBTLVR16292L	CBTLVR16292
		Tape and reel	SN74CBTLVR16292LR	
	TVSOP – DGV	Tape and reel	SN74CBTLVR16292GR	CBTLVR16292
		Tape and reel	SN74CBTLVR16292VR	CE292

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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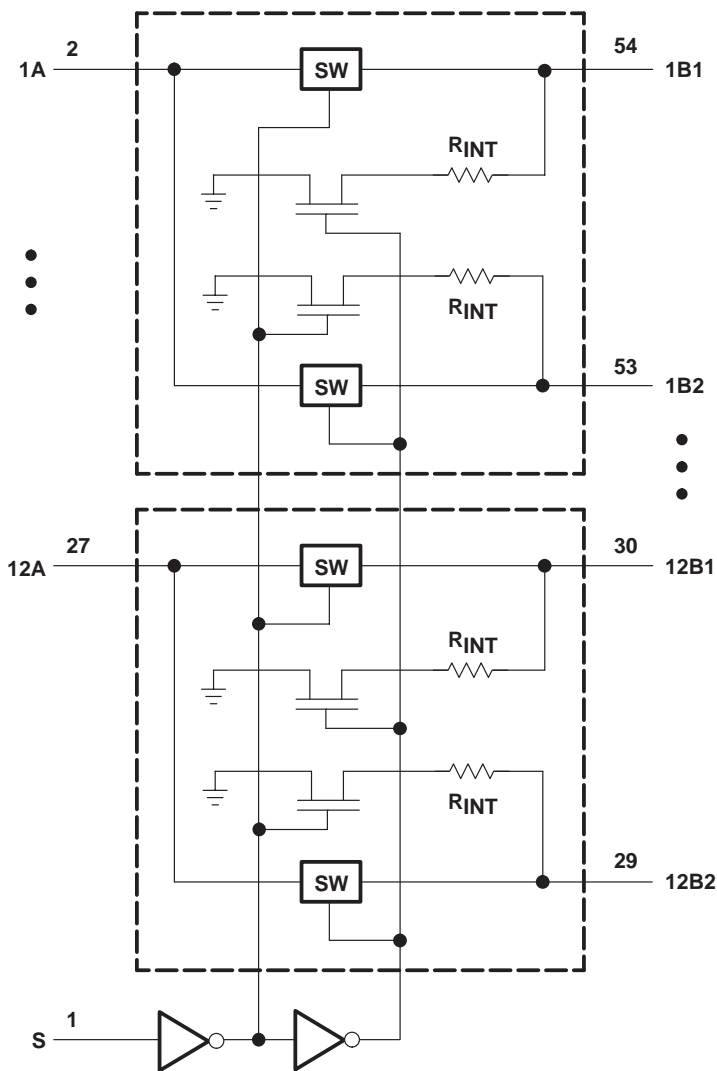
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FUNCTION TABLE

INPUT S	FUNCTION
L	A port = B1 port R <sub>INT</sub> = B2 port
H	A port = B2 port R <sub>INT</sub> = B1 port

logic diagram (positive logic)





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## LOW-VOLTAGE 12-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER WITH INTERNAL PULLDOWN RESISTORS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT	
$V_{IK}$		$V_{CC} = 3\text{ V}$ ,	$I_I = -18\text{ mA}$			-1.2	V	
$I_I$		$V_{CC} = 3.6\text{ V}$ ,	$V_I = V_{CC}$ or GND			$\pm 1$	$\mu\text{A}$	
$I_{off}$		$V_{CC} = 0$ ,	$V_I$ or $V_O = 0$ to $3.6\text{ V}$			10	$\mu\text{A}$	
$I_{CC}$		$V_{CC} = 3.6\text{ V}$ ,	$I_O = 0$ , $V_I = V_{CC}$ or GND			10	$\mu\text{A}$	
$\Delta I_{CC}^\ddagger$	Control input	$V_{CC} = 3.6\text{ V}$ ,	One input at $3\text{ V}$ , Other inputs at $V_{CC}$ or GND			300	$\mu\text{A}$	
$C_i$	Control input	$V_I = 3.3\text{ V}$ or $0$				3.5	pF	
$C_{io}$	A or B port	$V_O = 3.3\text{ V}$ or $0$				23	pF	
$r_{on}^\S$	$V_{CC} = 2.3\text{ V}$ , TYP at $V_{CC} = 2.5\text{ V}$	$V_I = 0$	$I_I = 64\text{ mA}$			30	47	$\Omega$
			$I_I = 24\text{ mA}$			30	47	
		$V_I = 1.7\text{ V}$ ,	$I_I = 15\text{ mA}$			36	80	
	$V_{CC} = 3\text{ V}$	$V_I = 0$	$I_I = 64\text{ mA}$			30	42	
			$I_I = 24\text{ mA}$			30	42	
		$V_I = 2.4\text{ V}$ ,	$I_I = 15\text{ mA}$			32	47	

† All typical values are at  $V_{CC} = 3.3\text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

‡ This is the increase in supply current for each input that is at the specified voltage level, rather than  $V_{CC}$  or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
$t_{pd}^\parallel$	A or B	B or A	0.15		0.25		ns
$t_{pd}^\#$	S	A	3.2	8.5	3.2	8	ns
$t_{en}$	S	B	1	6.5	1	5.8	ns
$t_{dis}$	S	B	1	5.3	1	4.6	ns

¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

# This propagation delay was measured by observing the change of voltage on the A output introduced by static levels equal to  $3\text{-V}$  or  $0$  for  $3.3\text{ V} \pm 0.3\text{ V}$  or  $V_{CC}$  or  $0$  for  $2.5\text{ V} \pm 0.2\text{ V}$  on B1 and B2 to achieve the desired transition.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	DESCRIPTION	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
		MIN	MAX	MIN	MAX	
$t_{mbb}^\parallel$	Make-before-break time	0	2	0	2	ns

¶ The make-before-break time is the time interval between make and break, during the transition from one selected port to the other.

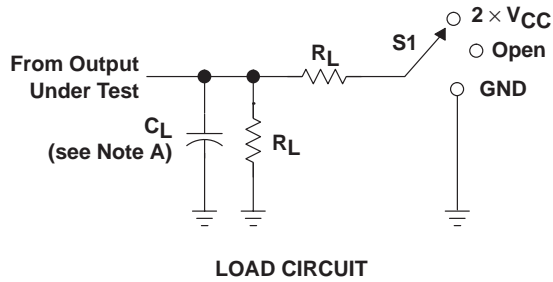


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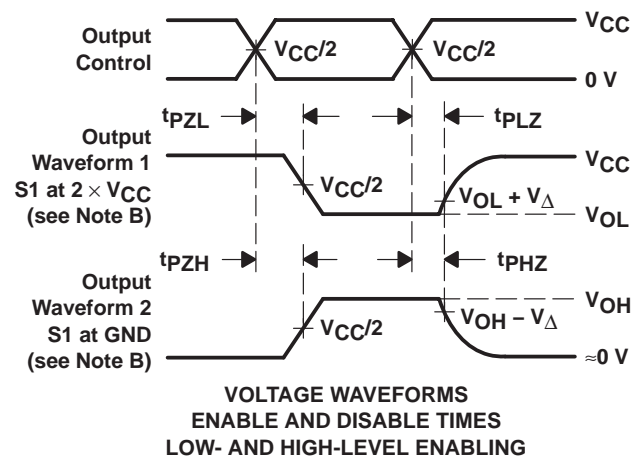
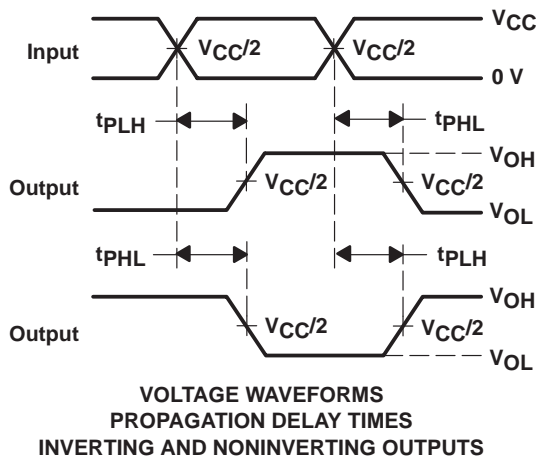
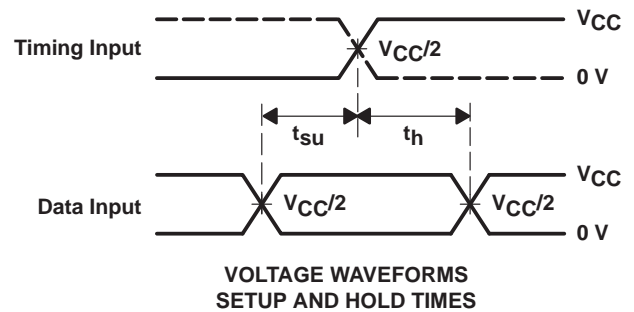
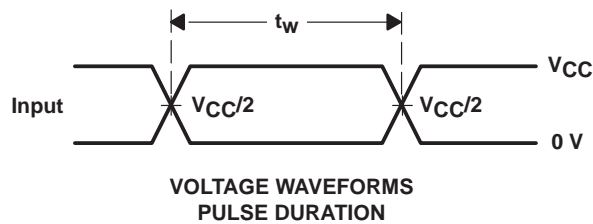
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### PARAMETER MEASUREMENT INFORMATION



TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

$V_{CC}$	$C_L$	$R_L$	$V_{\Delta}$
$2.5 \text{ V} \pm 0.2 \text{ V}$	30 pF	500 $\Omega$	0.15 V
$3.3 \text{ V} \pm 0.3 \text{ V}$	50 pF	500 $\Omega$	0.3 V



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2$  ns,  $t_f \leq 2$  ns.  
 D. The outputs are measured one at a time with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .  
 H. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74CBTLVR16292DL	ACTIVE	SSOP	DL	56		TBD	Call TI	Call TI
SN74CBTLVR16292GR	ACTIVE	TSSOP	DGG	56		TBD	Call TI	Call TI
SN74CBTLVR16292LR	ACTIVE	SSOP	DL	56		TBD	Call TI	Call TI
SN74CBTLVR16292VR	ACTIVE	TVSOP	DGV	56		TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

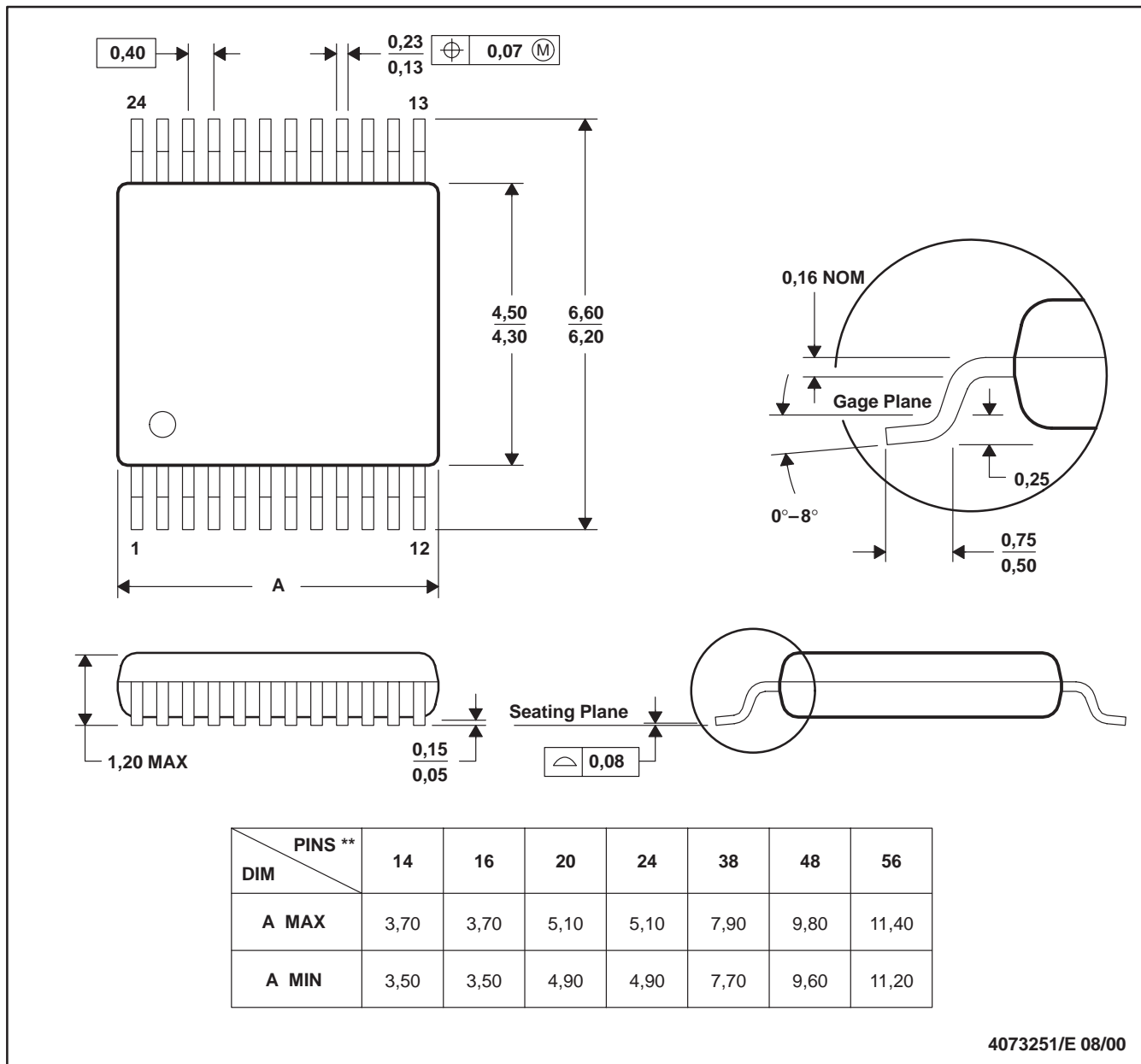
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DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

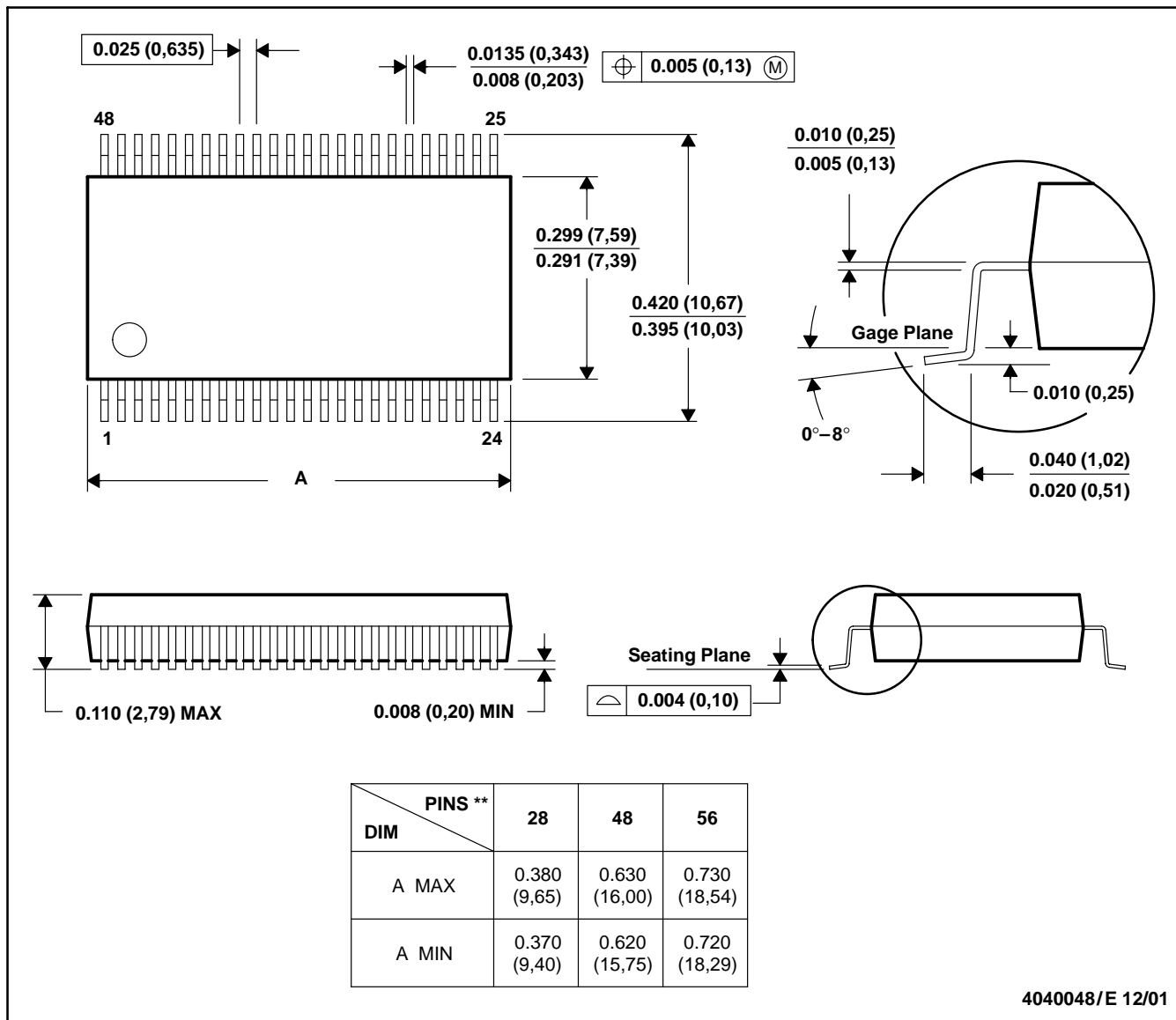


- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

DL (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

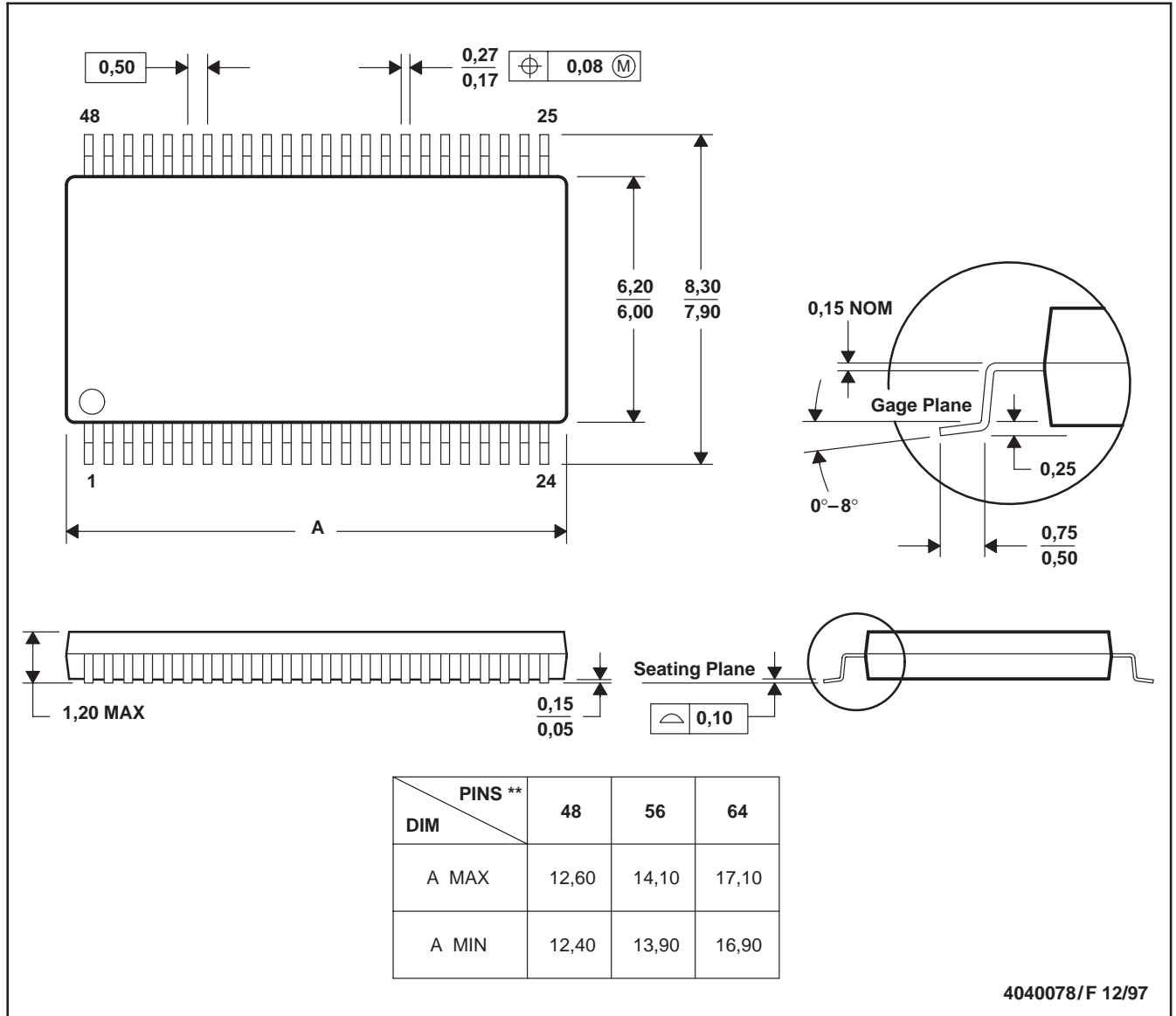


- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MO-118

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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