

SN74GTLPH32912

36-BIT LVTTTL-TO-GTLP UNIVERSAL BUS TRANSCEIVER

SCES379A – JANUARY 2002 – REVISED MAY 2002

- Member of the Texas Instruments Widebus+™ Family
- UBT™ Transceiver Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, and Clock-Enabled Modes
- TI-OPC™ Circuitry Limits Ringing on Unevenly Loaded Backplanes
- OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference
- Bidirectional Interface Between GTLP Signal Levels and LVTTTL Logic Levels
- LVTTTL Interfaces Are 5-V Tolerant
- Medium-Drive GTLP Outputs (50 mA)
- LVTTTL Outputs (–24 mA/24 mA)
- GTLP Rise and Fall Times Designed for Optimal Data-Transfer Rate and Signal Integrity in Distributed Loads
- I_{off} , Power-Up 3-State, and BIAS V_{CC} Support Live Insertion
- Bus Hold on A-Port Data Inputs
- Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

description

The SN74GTLPH32912 is a medium-drive, 36-bit UBT™ transceiver that provides LVTTTL-to-GTLP and GTLP-to-LVTTTL signal-level translation. It allows for transparent, latched, clocked, and clock-enabled modes of data transfer. The device provides a high-speed interface between cards operating at LVTTTL logic levels and a backplane operating at GTLP signal levels. High-speed (about three times faster than standard TTL or LVTTTL) backplane operation is a direct result of GTLP's reduced output swing (<1 V), reduced input threshold levels, improved differential input, OEC™ circuitry, and TI-OPC™ circuitry. Improved GTLP OEC and TI-OPC circuits minimize bus-settling time and have been designed and tested using several backplane models. The medium drive allows incident-wave switching in heavily loaded backplanes with equivalent load impedance down to 19Ω .

GTLP is the Texas Instruments derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The ac specification of the SN74GTLPH32912 is given only at the preferred higher noise-margin GTLP, but the user has the flexibility of using this device at either GTL ($V_{TT} = 1.2$ V and $V_{REF} = 0.8$ V) or GTLP ($V_{TT} = 1.5$ V and $V_{REF} = 1$ V) signal levels.

Normally, the B port operates at GTLP signal levels. The A-port and control inputs operate at LVTTTL logic levels, but are 5-V tolerant and are compatible with TTL and 5-V CMOS inputs. V_{REF} is the B-port differential input reference voltage.

This device is fully specified for live-insertion applications using I_{off} , power-up 3-state, and BIAS V_{CC} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS V_{CC} circuitry precharges and preconditions the B-port input/output connections, preventing disturbance of active data on the backplane during card insertion or removal, and permits true live-insertion capability.

This GTLP device features TI-OPC circuitry, which actively limits overshoot caused by improperly terminated backplanes, unevenly distributed cards, or empty slots during low-to-high signal transitions. This improves signal integrity, which allows adequate noise margin to be maintained at higher frequencies.



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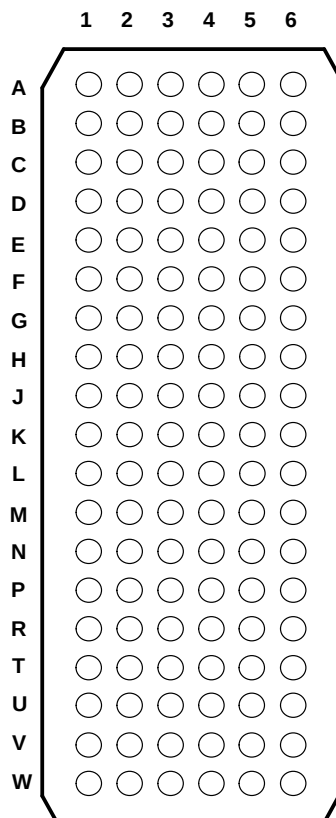
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description (continued)

Active bus-hold circuitry holds unused or undriven LVTTL data inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, the output-enable ($\overline{OE}$) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

**GKF PACKAGE
(TOP VIEW)**



terminal assignments

	1	2	3	4	5	6
A	1A2	1A1	1LEAB	1CLKAB	1B1	1B2
B	1A4	1A3	1OEAB	1CEAB	1B3	1B4
C	1A6	1A5	GND	GND	1B5	1B6
D	1A8	1A7	1V _{CC}	1BIAS V _{CC}	1B7	1B8
E	1A10	1A9	GND	GND	1B9	1B10
F	1A12	1A11	GND	GND	1B11	1B12
G	1A14	1A13	1V _{CC}	1V _{REF}	1B13	1B14
H	1A15	1A16	GND	GND	1B16	1B15
J	1A17	1A18	1OEBA	1CLKBA	1B18	1B17
K	NC	2LEAB	1LEBA	1CEBA	2CLKAB	NC
L	2A2	2A1	2OEAB	2CEAB	2B1	2B2
M	2A4	2A3	GND	GND	2B3	2B4
N	2A6	2A5	2V _{CC}	2BIAS V _{CC}	2B5	2B6
P	2A8	2A7	GND	GND	2B7	2B8
R	2A10	2A9	GND	GND	2B9	2B10
T	2A12	2A11	2V _{CC}	2V _{REF}	2B11	2B12
U	2A14	2A13	GND	GND	2B13	2B14
V	2A15	2A16	2OEBA	2CLKBA	2B16	2B15
W	2A17	2A18	2LEBA	2CEBA	2B18	2B17

NC – No internal connection

ORDERING INFORMATION

T _A	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	LFBGA – GKF	Tape and reel	SN74GTLPH32912KR	

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

functional description

The SN74GTLPH32912 is a medium-drive (50 mA), 36-bit UBT transceiver containing D-type latches and D-type flip-flops for data-path operation in transparent, latched, clocked, or clock-enabled modes and can replace any of the functions shown in Table 1. Data polarity is noninverting.

Table 1. SN74GTLPH32912 UBT Transceiver Replacement Functions

FUNCTION	8 BIT	9 BIT	10 BIT	16 BIT	18 BIT
Transceiver	'245, '623, '645	'863	'861	'16245, '16623	'16863
Buffer/driver	'241, '244, '541		'827	'16241, '16244, '16541	'16825
Latched transceiver	'543			'16543	'16472
Latch	'373, '573	'843	'841	'16373	'16843
Registered transceiver	'646, '652			'16646, '16652	'16474
Flip-flop	'374, '574		'821	'16374	
Standard UBT					'16500, '16501
Universal bus driver					'16835
Registered transceiver with clock enable	'2952			'16470, '16952	
Flip-flop with clock enable	'377	'823			'16823
Standard UBT with clock enable					'16600, '16601
SN74GTLPH32912 UBT transceiver replaces all above functions					

Data flow in each direction is controlled by clock enables ($\overline{\text{CEAB}}$ and $\overline{\text{CEBA}}$), latch enables ($\overline{\text{LEAB}}$ and $\overline{\text{LEBA}}$), clock (CLKAB and CLKBA), and output enables ($\overline{\text{OEAB}}$ and $\overline{\text{OEBA}}$). $\overline{\text{CEAB}}$ and $\overline{\text{CEBA}}$ and $\overline{\text{OEAB}}$ and $\overline{\text{OEBA}}$ control the 18 bits of data for the A-to-B and B-to-A directions, respectively.

For A-to-B data flow, when $\overline{\text{CEAB}}$ is low, the device operates on the low-to-high transition of CLKAB for the flip-flop and on the high-to-low transition of $\overline{\text{LEAB}}$ for the latch path, i.e., if $\overline{\text{CEAB}}$ and $\overline{\text{LEAB}}$ are low, the A data is latched, regardless of the state of CLKAB (high or low). If $\overline{\text{LEAB}}$ is high, the device is in transparent mode. When $\overline{\text{OEAB}}$ is low, the outputs are active. When $\overline{\text{OEAB}}$ is high, the outputs are in the high-impedance state.

The data flow for B to A is similar to that of A to B, except $\overline{\text{CEBA}}$, $\overline{\text{OEBA}}$, $\overline{\text{LEBA}}$, and CLKBA are used.

FUNCTION TABLE[†]

INPUTS					OUTPUT B	MODE
$\overline{\text{CEAB}}$	$\overline{\text{OEAB}}$	$\overline{\text{LEAB}}$	CLKAB	A		
X	H	X	X	X	Z	Isolation
L	L	L	H	X	$\text{B}_0^{\ddagger}$	Latched storage of A data
L	L	L	L	X	$\text{B}_0^{\S}$	
X	L	H	X	L	L	True transparent
X	L	H	X	H	H	
L	L	L	$\uparrow$	L	L	Clocked storage of A data
L	L	L	$\uparrow$	H	H	
H	L	L	X	X	$\text{B}_0^{\S}$	Clock inhibit

[†] A-to-B data flow is shown. B-to-A data flow is similar, but uses $\overline{\text{CEBA}}$, $\overline{\text{OEBA}}$, $\overline{\text{LEBA}}$, and CLKBA . The condition when $\overline{\text{OEAB}}$ and $\overline{\text{OEBA}}$ are both low at the same time is not recommended.

[‡] Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before $\overline{\text{LEAB}}$ went low

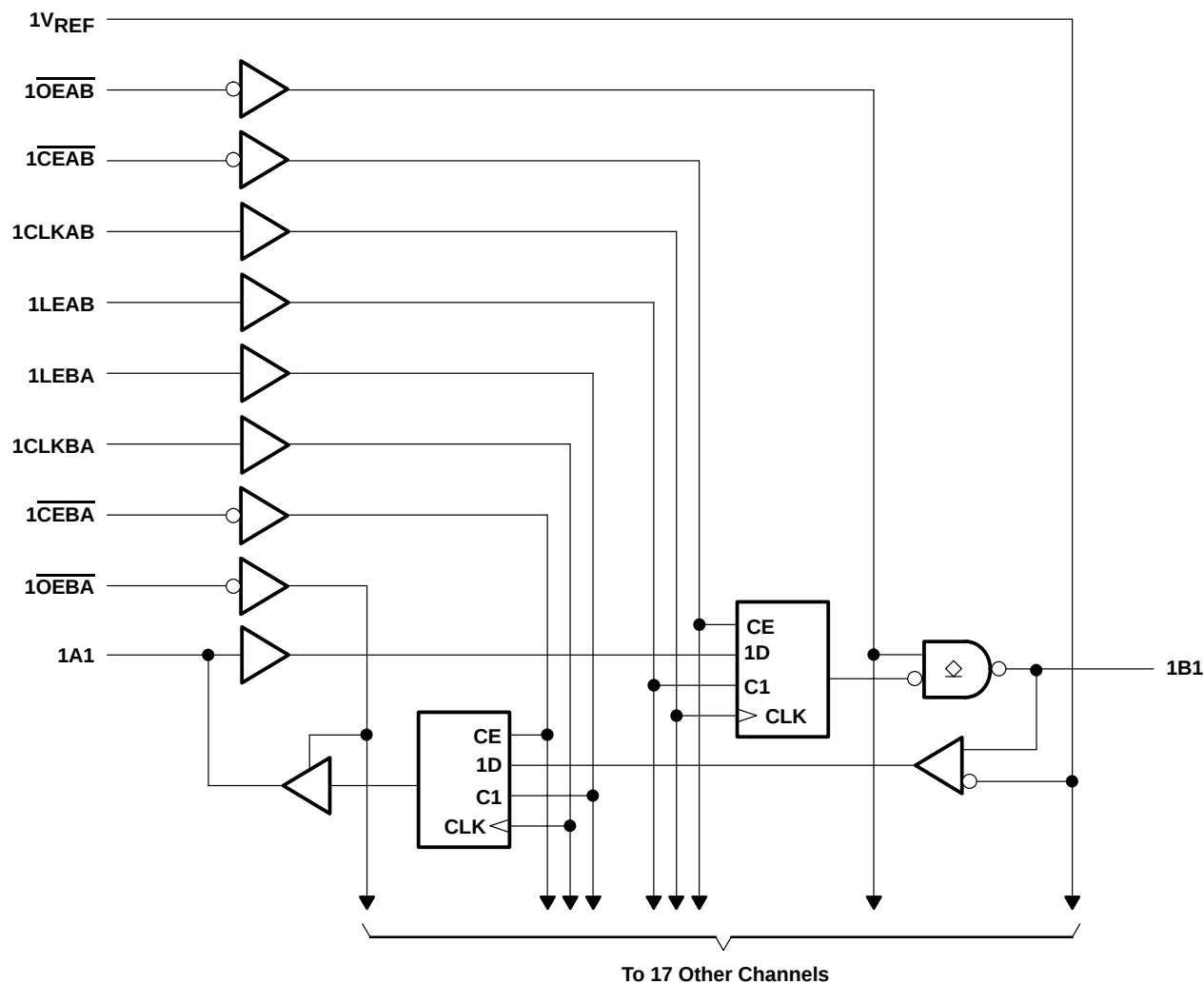
[§] Output level before the indicated steady-state input conditions were established

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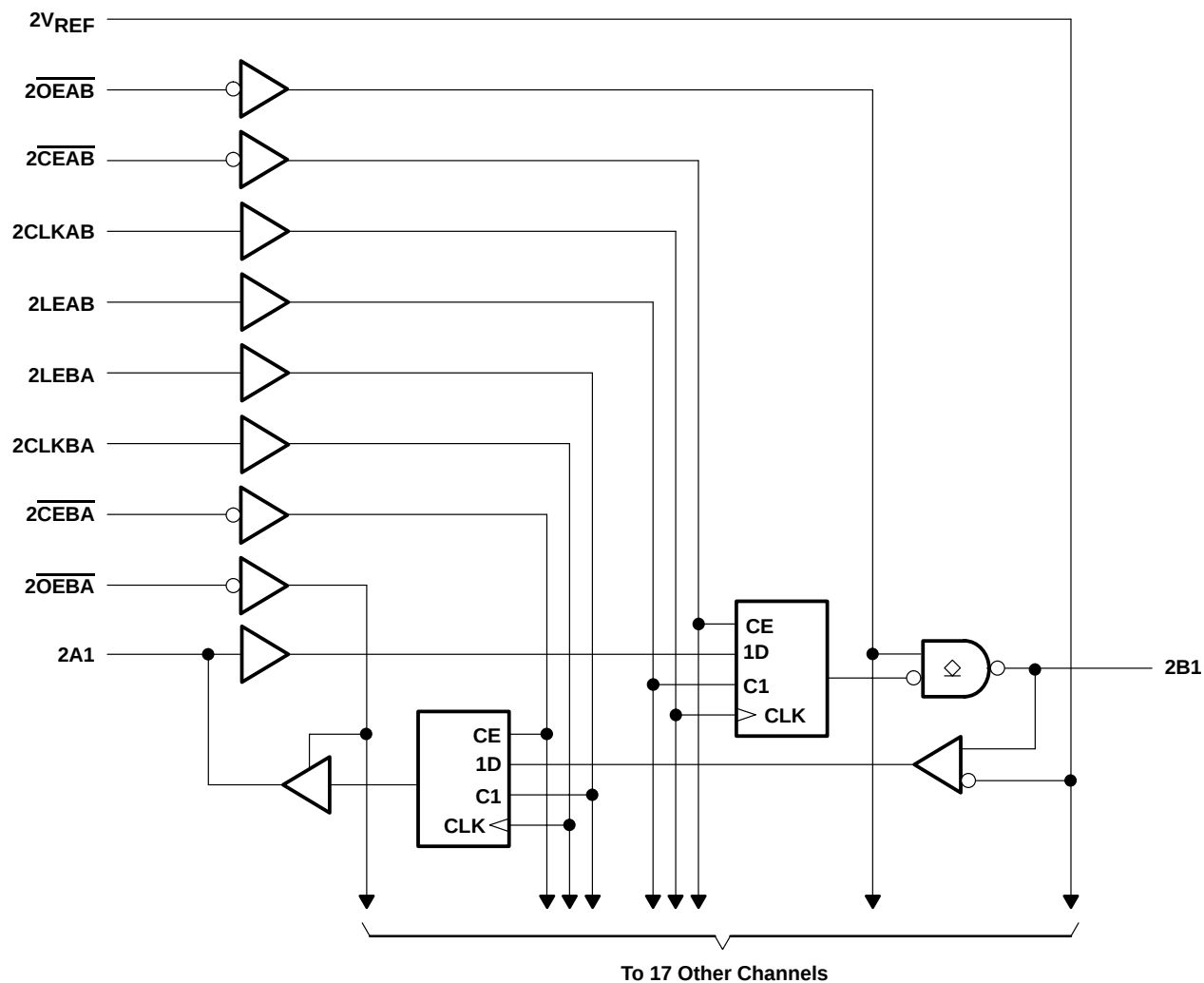
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logic diagram (positive logic)[†]



[†] 1V_{CC} and 1BIAS V_{CC} are associated with these channels.

logic diagram (positive logic) (continued)[†]



[†] $2V_{CC}$ and $2BIAS V_{CC}$ are associated with these channels.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} and BIAS V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1): A-port and control inputs	–0.5 V to 7 V
B port and V_{REF}	–0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, V_O	
(see Note 1): A port	–0.5 V to 7 V
B port	–0.5 V to 4.6 V
Current into any output in the low state, I_O : A port	48 mA
B port	100 mA
Current into any A port output in the high state, I_O (see Note 2)	48 mA
Continuous current through each V_{CC} or GND	±100 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3)	36°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.



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recommended operating conditions (see Notes 4 through 7)

			MIN	NOM	MAX	UNIT
V _{CC} , BIAS V _{CC}	Supply voltage		3.15	3.3	3.45	V
V _{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTLP	1.35	1.5	1.65	
V _{REF}	Reference voltage	GTL	0.74	0.8	0.87	V
		GTLP	0.87	1	1.1	
V _I	Input voltage	B port	V _{TT}			V
		Except B port	V _{CC} 5.5			
V _{IH}	High-level input voltage	B port	V _{REF} +0.05			V
		Except B port	2			
V _{IL}	Low-level input voltage	B port	V _{REF} −0.05			V
		Except B port	0.8			
I _{IK}	Input clamp current		−18			mA
I _{OH}	High-level output current	A port	−24			mA
I _{OL}	Low-level output current	A port	24			mA
		B port	50			
Δt/Δv	Input transition rise or fall rate	Outputs enabled	10			ns/V
Δt/ΔV _{CC}	Power-up ramp rate		20			μs/V
T _A	Operating free-air temperature		−40 85			°C

- NOTES:
- All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
 - Proper connection sequence for use of the B-port I/O precharge feature is GND and BIAS $V_{CC} = 3.3$ V first, I/O second, and $V_{CC} = 3.3$ V last, because the BIAS V_{CC} precharge circuitry is disabled when any V_{CC} pin is connected. The control and V_{REF} inputs can be connected anytime, but normally are connected during the I/O stage. If B-port precharge is not required, any connection sequence is acceptable, but generally, GND is connected first.
 - V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.
 - V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT} . TI-OPC circuitry is enabled in the A-to-B direction and is activated when $V_{TT} > 0.7$ V above V_{REF} . If operated in the A-to-B direction, V_{REF} should be set to within 0.6 V of V_{TT} to minimize current drain.



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electrical characteristics over recommended operating free-air temperature range for GTLP (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
V_{IK}		$V_{CC} = 3.15\text{ V}$, $I_I = -18\text{ mA}$			-1.2	V
V_{OH}	A port	$V_{CC} = 3.15\text{ V to } 3.45\text{ V}$, $I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC}-0.2$			V
		$V_{CC} = 3.15\text{ V}$, $I_{OH} = -12\text{ mA}$	2.4			
		$V_{CC} = 3.15\text{ V}$, $I_{OH} = -24\text{ mA}$	2			
V_{OL}	A port	$V_{CC} = 3.15\text{ V to } 3.45\text{ V}$, $I_{OL} = 100\text{ }\mu\text{A}$			0.2	V
		$V_{CC} = 3.15\text{ V}$, $I_{OL} = 12\text{ mA}$			0.4	
		$V_{CC} = 3.15\text{ V}$, $I_{OL} = 24\text{ mA}$			0.5	
	B port	$V_{CC} = 3.15\text{ V to } 3.45\text{ V}$, $I_{OL} = 100\text{ }\mu\text{A}$			0.2	
		$V_{CC} = 3.15\text{ V}$, $I_{OL} = 10\text{ mA}$			0.2	
		$V_{CC} = 3.15\text{ V}$, $I_{OL} = 40\text{ mA}$			0.4	
		$V_{CC} = 3.15\text{ V}$, $I_{OL} = 50\text{ mA}$			0.55	
I_I	Control inputs	$V_{CC} = 3.45\text{ V}$, $V_I = 0\text{ or } 5.5\text{ V}$			± 10	μA
$I_{OZH}^{\ddagger}$	A port	$V_{CC} = 3.45\text{ V}$			10	μA
	B port				10	
$I_{OZL}^{\ddagger}$	A and B ports	$V_{CC} = 3.45\text{ V}$, $V_O = \text{GND}$			-10	μA
$I_{BHL}^{\S}$	A port	$V_{CC} = 3.15\text{ V}$, $V_I = 0.8\text{ V}$	75			μA
$I_{BHH}^{\parallel}$	A port	$V_{CC} = 3.15\text{ V}$, $V_I = 2\text{ V}$	-75			μA
$I_{BHLO}^{\#}$	A port	$V_{CC} = 3.45\text{ V}$, $V_I = 0\text{ to } V_{CC}$	500			μA
$I_{BHHO}^{\parallel}$	A port	$V_{CC} = 3.45\text{ V}$, $V_I = 0\text{ to } V_{CC}$	-500			μA
I_{CC}	A or B port	$V_{CC} = 3.45\text{ V}$, $I_O = 0$, V_I (A-port or control input) = V_{CC} or GND, V_I (B port) = V_{TT} or GND	Outputs high		100	mA
			Outputs low		100	
			Outputs disabled		100	
$\Delta I_{CC}^{\star}$		$V_{CC} = 3.45\text{ V}$, One A-port or control input at $V_{CC} - 0.6\text{ V}$, Other A-port or control inputs at V_{CC} or GND			1.5	mA
C_i	Control inputs	$V_I = 3.15\text{ V or } 0$		4	5.5	pF
C_{io}	A port	$V_O = 3.15\text{ V or } 0$		7	9	pF
	B port	$V_O = 1.5\text{ V or } 0$		9	11	

[†] All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

[‡] For I/O ports, the parameters I_{OZH} and I_{OZL} include the input leakage current.

^{\S} The bus-hold circuit can sink at least the minimum low sustaining current at $V_{IL\text{max}}$. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to $V_{IL\text{max}}$.

^{\parallel} The bus-hold circuit can source at least the minimum high sustaining current at $V_{IH\text{min}}$. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to $V_{IH\text{min}}$.

^{\#} An external driver must source at least I_{BHLO} to switch this node from low to high.

^{\parallel} An external driver must sink at least I_{BHHO} to switch this node from high to low.

^{\star} This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

hot-insertion specifications for A port over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	$V_{CC} = 0$,	BIAS $V_{CC} = 0$,	V_I or $V_O = 0\text{ to } 5.5\text{ V}$		10	μA
I_{OZPU}	$V_{CC} = 0\text{ to } 1.5\text{ V}$,	$V_O = 0.5\text{ V to } 3\text{ V}$,	$\overline{OE} = 0$		± 30	μA
I_{OZPD}	$V_{CC} = 1.5\text{ V to } 0$,	$V_O = 0.5\text{ V to } 3\text{ V}$,	$\overline{OE} = 0$		± 30	μA



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live-insertion specifications for B port over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	$V_{CC} = 0$,	BIAS $V_{CC} = 0$,	V_I or $V_O = 0$ to 1.5 V		10	μA
I_{OZPU}	$V_{CC} = 0$ to 1.5 V,	BIAS $V_{CC} = 0$,	$V_O = 0.5$ V to 1.5 V, $\overline{OE} = 0$		± 30	μA
I_{OZPD}	$V_{CC} = 1.5$ V to 0,	BIAS $V_{CC} = 0$,	$V_O = 0.5$ V to 1.5 V, $\overline{OE} = 0$		± 30	μA
I_{CC} (BIAS V_{CC})	$V_{CC} = 0$ to 3.15 V	BIAS $V_{CC} = 3.15$ V to 3.45 V,	V_O (B port) = 0 to 1.5 V		5	mA
	$V_{CC} = 3.15$ V to 3.45 V				10	μA
V_O	$V_{CC} = 0$,	BIAS $V_{CC} = 3.3$ V,	$I_O = 0$	0.95	1.05	V
I_O	$V_{CC} = 0$,	BIAS $V_{CC} = 3.15$ V to 3.45 V,	V_O (B port) = 0.6 V	-1		μA

timing requirements over recommended ranges of supply voltage and operating free-air temperature, $V_{TT} = 1.5$ V and $V_{REF} = 1$ V for GTLP (unless otherwise noted)

		MIN	MAX	UNIT
f_{clock}	Clock frequency		175	MHz
t_w	Pulse duration	LEAB or LEBA high	2.8	ns
		CLKAB or CLKBA high or low	2.8	
t_{su}	Setup time	A before CLKAB $\uparrow$	1.8	ns
		B before CLKBA $\uparrow$	1.5	
		A before LEAB $\downarrow$	1	
		B before LEBA $\downarrow$	2	
		$\overline{CEAB}$ before CLKAB $\uparrow$	1.5	
		$\overline{CEBA}$ before CLKBA $\uparrow$	1.5	
t_h	Hold time	A after CLKAB $\uparrow$	0.3	ns
		B after CLKBA $\uparrow$	0.4	
		A after LEAB $\downarrow$	1.1	
		B after LEBA $\downarrow$	0.5	
		$\overline{CEAB}$ after CLKAB $\uparrow$	1	
		$\overline{CEBA}$ after CLKBA $\uparrow$	1	



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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $V_{TT} = 1.5$ V and $V_{REF} = 1$ V for GTLP (see Figure 1)

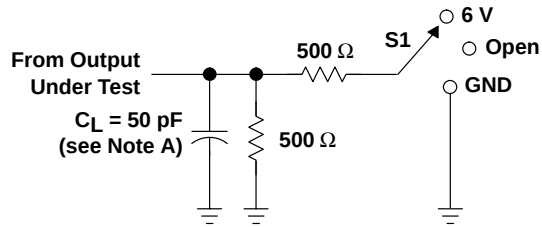
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP [†]	MAX	UNIT
f _{max}			175			MHz
t _{PLH}	A	B	2.1		6	ns
t _{PHL}			2.1		6	
t _{PLH}	LEAB	B	2.2		6.5	ns
t _{PHL}			2.2		6.5	
t _{PLH}	CLKAB	B	2.2		6.5	ns
t _{PHL}			2.2		6.5	
t _{en}	$\overline{OEAB}$	B	2.2		6.5	ns
t _{dis}			2.2		6.5	
t _r	Rise time, B outputs (20% to 80%)		2.4			ns
t _f	Fall time, B outputs (80% to 20%)		2			ns
t _{PLH}	B	A	1.8		5.8	ns
t _{PHL}			1.8		5.8	
t _{PLH}	LEBA	A	1.5		5.3	ns
t _{PHL}			1.5		5.3	
t _{PLH}	CLKBA	A	1.8		5.7	ns
t _{PHL}			1.8		5.7	
t _{en}	$\overline{OEBA}$	A	1		6.2	ns
t _{dis}			1		5.9	

[†] All typical values are at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$.



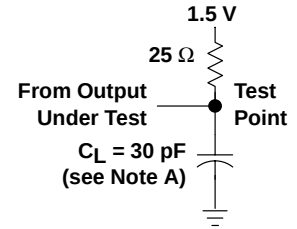
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PARAMETER MEASUREMENT INFORMATION

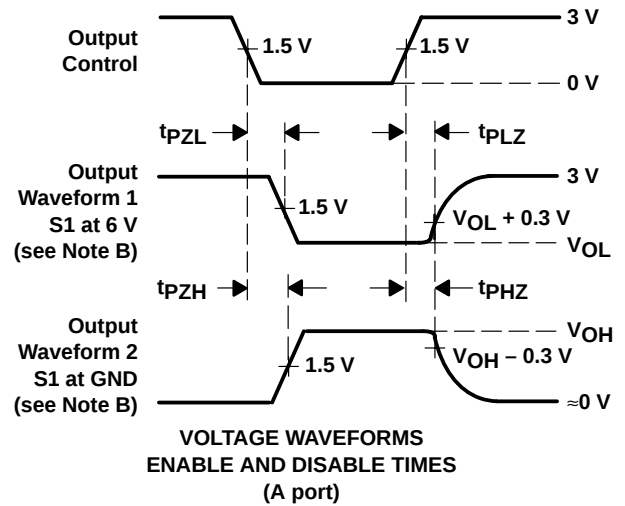
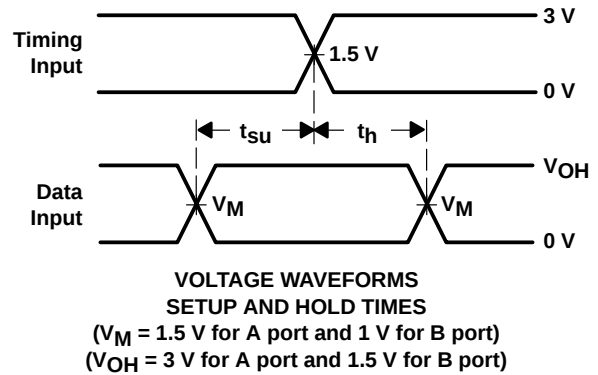
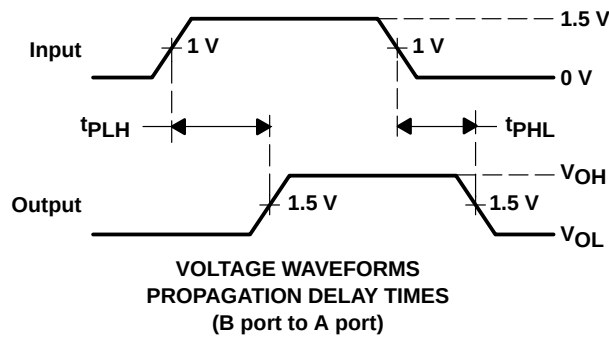
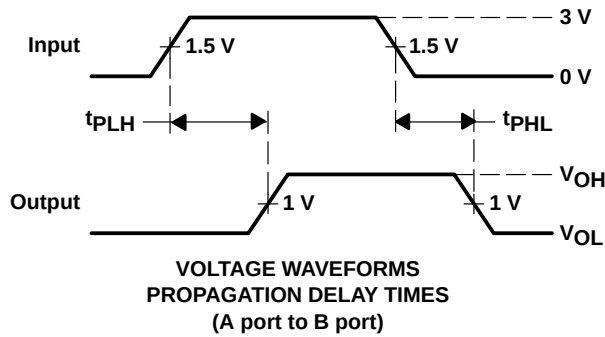
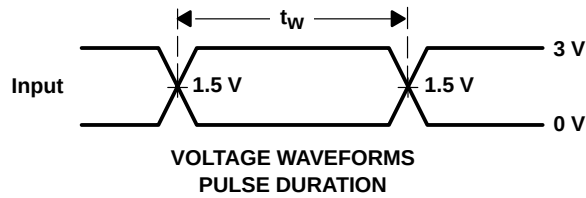


LOAD CIRCUIT FOR A OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



LOAD CIRCUIT FOR B OUTPUTS



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR $\approx$ 10 MHz, $Z_O = 50 \Omega$, $t_r \approx 2$ ns, $t_f \approx 2$ ns.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

SN74GTLPH32912

36-BIT LVTTTL-TO-GTLP UNIVERSAL BUS TRANSCEIVER

SCES379A – JANUARY 2002 – REVISED MAY 2002

DISTRIBUTED-LOAD BACKPLANE SWITCHING CHARACTERISTICS

The preceding switching characteristics table shows the switching characteristics of the device into a lumped load (Figure 1). However, the designer's backplane application probably is a distributed load. The physical representation is shown in Figure 2. This backplane, or distributed load, can be approximated closely to a resistor inductance capacitance (RLC) circuit, as shown in Figure 3. This device has been designed for optimum performance in this RLC circuit. The following switching characteristics table shows the switching characteristics of the device into the RLC load, to help the designer better understand the performance of the GTLP device in this typical backplane. See www.ti.com/sc/gtlp for more information.

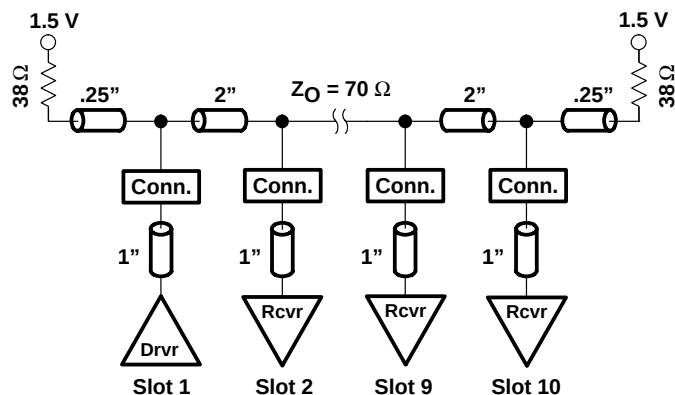


Figure 2. Medium-Drive Test Backplane

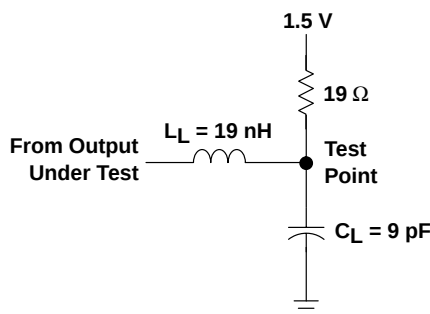


Figure 3. Medium-Drive RLC Network

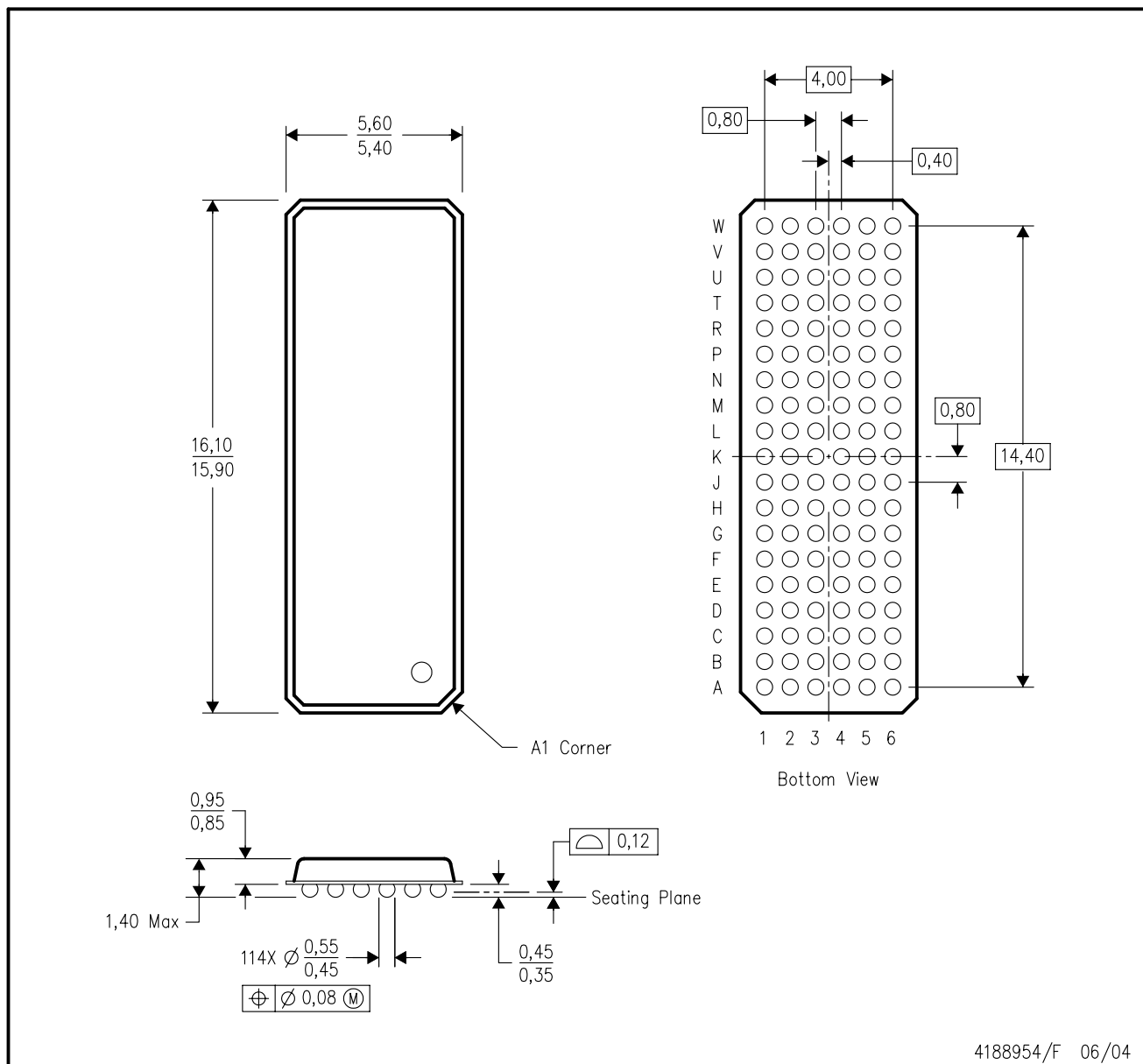
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $V_{TT} = 1.5\text{ V}$ and $V_{REF} = 1\text{ V}$ for GTLP (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TYP†	UNIT
tPLH	A	B	4.5	ns
tPHL			4.5	
tPLH	LEAB	B	4.7	ns
tPHL			4.7	
tPLH	CLKAB	B	4.7	ns
tPHL			4.7	
ten	OEAB	B	4.8	ns
tdis			4.4	
tr	Rise time, B outputs (20% to 80%)		1.2	ns
tf	Fall time, B outputs (80% to 20%)		2.5	ns

[†] All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$. All values are derived from TI-SPICE models.

GKF (R-PBGA-N114)

PLASTIC BALL GRID ARRAY



4188954/F 06/04

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