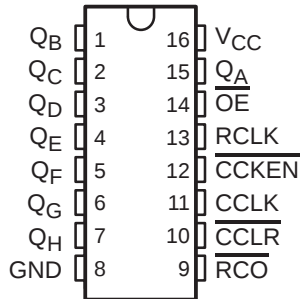


SN54HC590A, SN74HC590A 8-BIT BINARY COUNTERS WITH 3-STATE OUTPUT REGISTERS

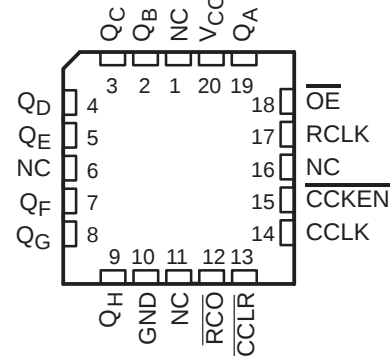
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- 2-V to 6-V V_{CC} Operation
- High-Current 3-State Parallel Register Outputs Can Drive Up To 15 LSTTL Loads
- Low Power Consumption, 80- μ A Max I_{CC}
- Typical $t_{pd} = 14$ ns
- ± 6 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max
- 8-Bit Counter With Register
- Counter Has Direct Clear

SN54HC590A . . . J OR W PACKAGE
SN74HC590A . . . D, DW, OR N PACKAGE
(TOP VIEW)



SN54HC590A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The 'HC590A devices contain an 8-bit binary counter that feeds an 8-bit storage register. The storage register has parallel outputs. Separate clocks are provided for both the binary counter and storage register. The binary counter features direct clear ($\overline{CCLR}$) and count-enable ($\overline{CCKEN}$) inputs. A ripple-carry output ($\overline{RCO}$) is provided for cascading. Expansion is accomplished easily for two stages by connecting $\overline{RCO}$ of the first stage to $\overline{CCKEN}$ of the second stage. Cascading for larger count chains can be accomplished by connecting $\overline{RCO}$ of each stage to the counter clock (CCLK) input of the following stage.

CCLK and the register clock (RCLK) inputs are positive-edge triggered. If both clocks are connected together, the counter state always is one count ahead of the register. Internal circuitry prevents clocking from the clock enable.

ORDERING INFORMATION

T_A	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube of 25	SN74HC590AN	SN74HC590AN
		Tube of 40	SN74HC590AD	
	SOIC – D	Reel of 2500	SN74HC590ADR	HC590A
		Reel of 250	SN74HC590ADT	
	SOIC – DW	Tube of 40	SN74HC590ADW	HC590A
		Reel of 2000	SN74HC590ADWR	
-55°C to 125°C	CDIP – J	Tube of 25	SNJ54HC590AJ	SNJ54HC590AJ
	CFP – W	Tube of 150	SNJ54HC590AW	SNJ54HC590AW
	LCCC – FK	Tube of 55	SNJ54HC590AFK	SNJ54HC590AFK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at

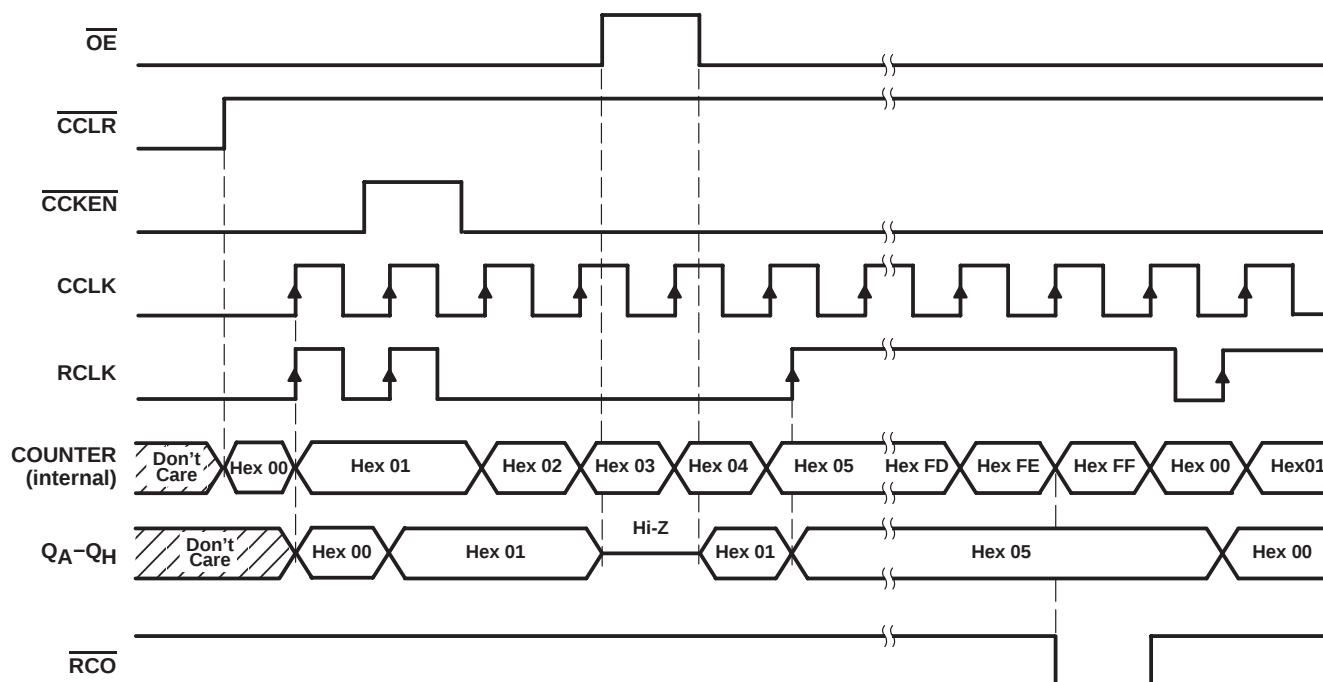
SN54HC590A, SN74HC590A

8-BIT BINARY COUNTERS

WITH 3-STATE OUTPUT REGISTERS

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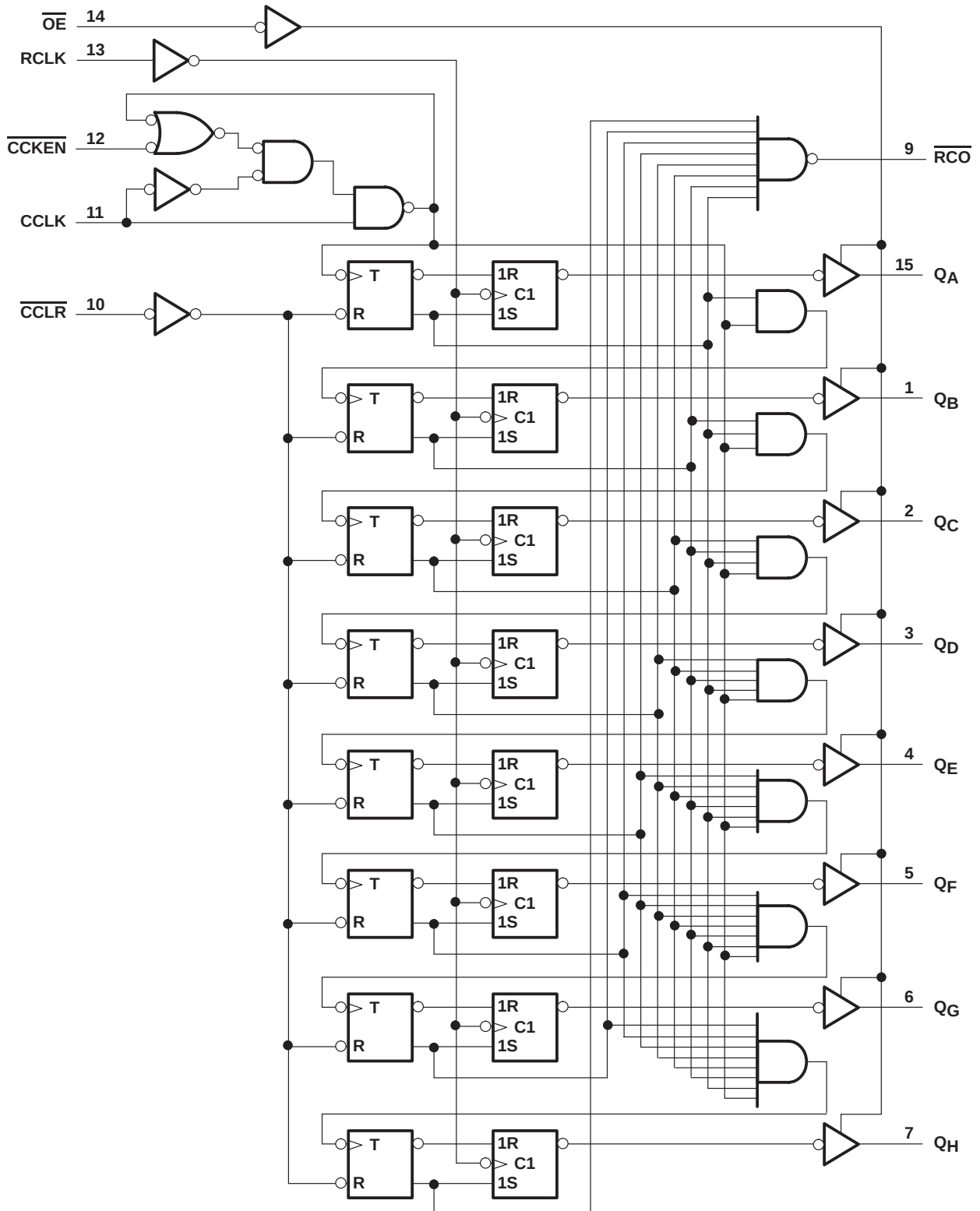
timing diagram



TIMING SEQUENCE

1. Clear Counter (asynchronous).
2. Count up: 0x01. Store 0x00 in register.
3. Inhibit counter clock ($\overline{\text{CCKEN}} = \text{HIGH}$). Store 0x01 in register.
4. Count 0x02, 0x03.
5. 3-state the outputs
6. Count up: 0x04
7. Enable outputs.
8. Continue up: 0x05
9. Store 0x05 in register.
10. Continue counting: 0x06...0xFD, 0xFE, 0xFF, 0x00, etc.
11. Store 0x00 in register.

logic diagram (positive logic)



Pin numbers shown are for the D, DW, J, N, and W packages.

SN54HC590A, SN74HC590A

8-BIT BINARY COUNTERS

WITH 3-STATE OUTPUT REGISTERS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±35 mA
Continuous current through V_{CC} or GND	±70 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	73°C/W
DW package	57°C/W
N package	67°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		SN54HC590A			SN74HC590A			UNIT	
		MIN	NOM	MAX	MIN	NOM	MAX		
V_{CC}	Supply voltage	2	5	6	2	5	6	V	
V_{IH}	High-level input voltage	$V_{CC} = 2$ V			1.5			V	
		$V_{CC} = 4.5$ V			3.15				
		$V_{CC} = 6$ V			4.2				
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V			0.5			V	
		$V_{CC} = 4.5$ V			1.35				
		$V_{CC} = 6$ V			1.8				
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V	
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V	
$t_t^{\ddagger}$	Input transition (rise and fall) time	$V_{CC} = 2$ V			1000			ns	
		$V_{CC} = 4.5$ V			500				

SN54HC590A, SN74HC590A
8-BIT BINARY COUNTERS
WITH 3-STATE OUTPUT REGISTERS
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	T _A = 25°C			SN54HC590A		SN74HC590A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = -20 µA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		$\overline{RCO}$, I _{OH} = -4 mA	4.5 V	3.98	4.3		3.7		3.84		
		Q _A -Q _H , I _{OH} = -6 mA		3.98	4.3		3.7		3.84		
		$\overline{RCO}$, I _{OH} = -5.2 mA	6 V	5.48	5.8		5.2		5.34		
		Q _A -Q _H , I _{OH} = -7.8 mA		5.48	5.8		5.2		5.34		
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 µA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		$\overline{RCO}$, I _{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		Q _A -Q _H , I _{OL} = 6 mA			0.17	0.26		0.4		0.33	
		$\overline{RCO}$, I _{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
		Q _A -Q _H , I _{OL} = 7.8 mA			0.15	0.26		0.4		0.33	
I _I	V _I = V _{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I _{OZ}	V _O = V _{CC} or 0		6 V		±0.01	±0.5		±10		±5	µA

SN54HC590A, SN74HC590A

8-BIT BINARY COUNTERS

WITH 3-STATE OUTPUT REGISTERS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V _{CC}	T _A = 25°C		SN54HC590A		SN74HC590A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	2 V		4		2.5		3.2	MHz
		4.5 V		20		13		16	
		6 V		24		16		19	
t _w	Pulse duration	2 V	125		200		155		ns
		4.5 V	25		38		31		
		6 V	21		32		26		
	$\overline{\text{CCLR}}$ low	2 V	100		150		125		
		4.5 V	20		30		25		
		6 V	17		26		21		
t _{su}	$\overline{\text{CCKEN}}$ low before CCLK↑	2 V	100		150		125		ns
		4.5 V	20		30		25		
		6 V	17		26		21		
	$\overline{\text{CCLR}}$ high (inactive) before CCLK↑	2 V	100		150		125		
		4.5 V	20		30		25		
		6 V	17		26		21		
	CCLK↑ before RCLK↑†	2 V	100		150		125		
		4.5 V	20		30		25		
		6 V	17		26		21		
t _h	$\overline{\text{CCKEN}}$ low after CCLK↑	2 V	50		75		60		ns
		4.5 V	10		15		12		
		6 V	9		13		11		

† This setup time ensures that the register gets stable data from the counter outputs. The clocks may be tied together, in which case the register is one clock pulse behind the counter.

SN54HC590A, SN74HC590A
8-BIT BINARY COUNTERS
WITH 3-STATE OUTPUT REGISTERS
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switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	SN54HC590A				UNIT	
				$T_A = 25^\circ\text{C}$			MIN MAX		
				MIN	TYP	MAX			
$f_{\max}$			2 V	4	8		2.5	MHz	
			4.5 V	20	35		13		
			6 V	24	40		16		
t_{pd}	CCLK $\uparrow$	$\overline{RCO}$	2 V		80	150		ns	
			4.5 V		20	31			
			6 V		15	26			
t_{PLH}	$\overline{CCLR}\downarrow$	$\overline{RCO}$	2 V		70	130		ns	
			4.5 V		18	28			
			6 V		14	23			
t_{pd}	RCLK $\uparrow$	Q	2 V		70	140		ns	
			4.5 V		18	31			
			6 V		14	25			
t_{en}	$\overline{OE}\downarrow$	Q	2 V		80	125		ns	
			4.5 V		20	30			
			6 V		15	28			
t_{dis}	$\overline{OE}\uparrow$	Q	2 V		80	125		ns	
			4.5 V		20	30			
			6 V		15	28			
t_t^*		$\overline{RCO}$	2 V		38	75		ns	
			4.5 V		8	15			
			6 V		6	13			

SN54HC590A, SN74HC590A
8-BIT BINARY COUNTERS
WITH 3-STATE OUTPUT REGISTERS

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switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF
(unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	SN74HC590A				UNIT	
				$T_A = 25^\circ\text{C}$			MIN MAX		
				MIN	TYP	MAX			
$f_{\max}$			2 V	4	8		3.2	MHz	
			4.5 V	20	35		16		
			6 V	24	40		19		
t_{pd}	CCLK $\uparrow$	$\overline{RCO}$	2 V		80	150		ns	
			4.5 V		20	30			
			6 V		15	26			
t_{PLH}	$\overline{CCLR}\downarrow$	$\overline{RCO}$	2 V		70	130		ns	
			4.5 V		18	26			
			6 V		14	22			
t_{pd}	RCLK $\uparrow$	Q	2 V		70	140		ns	
			4.5 V		18	28			
			6 V		14	24			
t_{en}	$\overline{OE}\downarrow$	Q	2 V		80	125		ns	
			4.5 V		20	25			
			6 V		15	21			
t_{dis}	$\overline{OE}\uparrow$	Q	2 V		80	125		ns	
			4.5 V		20	25			
			6 V		15	21			
t_t		$\overline{RCO}$	2 V		38	75		ns	
			4.5 V		8	15			
			6 V		6	13			

SN54HC590A, SN74HC590A
8-BIT BINARY COUNTERS
WITH 3-STATE OUTPUT REGISTERS
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switching characteristics over recommended operating free-air temperature range, $C_L = 150$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	SN54HC590A				UNIT	
				$T_A = 25^\circ\text{C}$			MIN MAX		
				MIN	TYP	MAX			
t_{pd}	RCLK $\uparrow$	Q	2 V		100	300	447	ns	
			4.5 V		24	60	90		
			6 V		20	51	77		
t_{en}	$\overline{OE}$	Q	2 V		90	200	300	ns	
			4.5 V		23	40	60		
			6 V		19	34	51		
t_t^*		Q	2 V		45	210	315	ns	
			4.5 V		17	42	63		
			6 V		13	36	53		

* This parameter is not production tested for the SN54HC590A.

switching characteristics over recommended operating free-air temperature range, $C_L = 150$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	SN74HC590A				UNIT	
				$T_A = 25^\circ\text{C}$			MIN MAX		
				MIN	TYP	MAX			
t_{pd}	RCLK $\uparrow$	Q	2 V		100	300	380	ns	
			4.5 V		24	60	76		
			6 V		20	51	65		
t_{en}	$\overline{OE}$	Q	2 V		90	200	250	ns	
			4.5 V		23	40	50		
			6 V		19	34	43		
t_t									

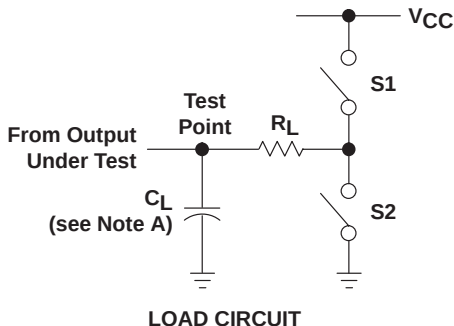
SN54HC590A, SN74HC590A

8-BIT BINARY COUNTERS

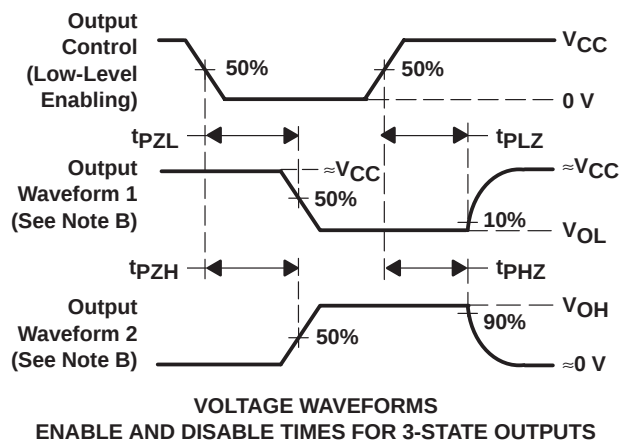
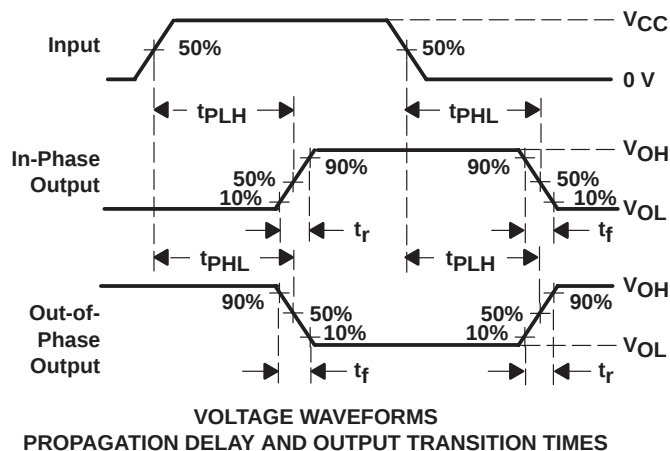
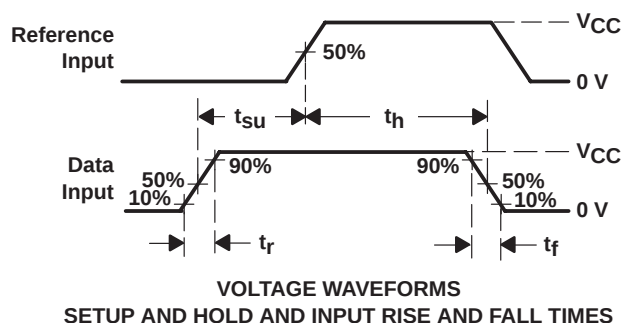
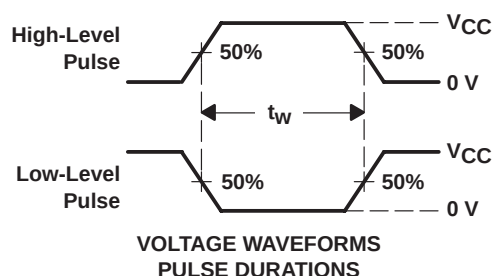
WITH 3-STATE OUTPUT REGISTERS

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PARAMETER MEASUREMENT INFORMATION



PARAMETER	R_L	C_L	S1	S2
t_{en}	1 k Ω	50 pF or 150 pF	Open	Closed
			Closed	Open
t_{dis}	1 k Ω	50 pF	Open	Closed
			Closed	Open
t_{pd} or t_t	---	50 pF or 150 pF	Open	Open



- NOTES:
- C_L includes probe and test-fixture capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 - The outputs are measured one at a time with one input transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

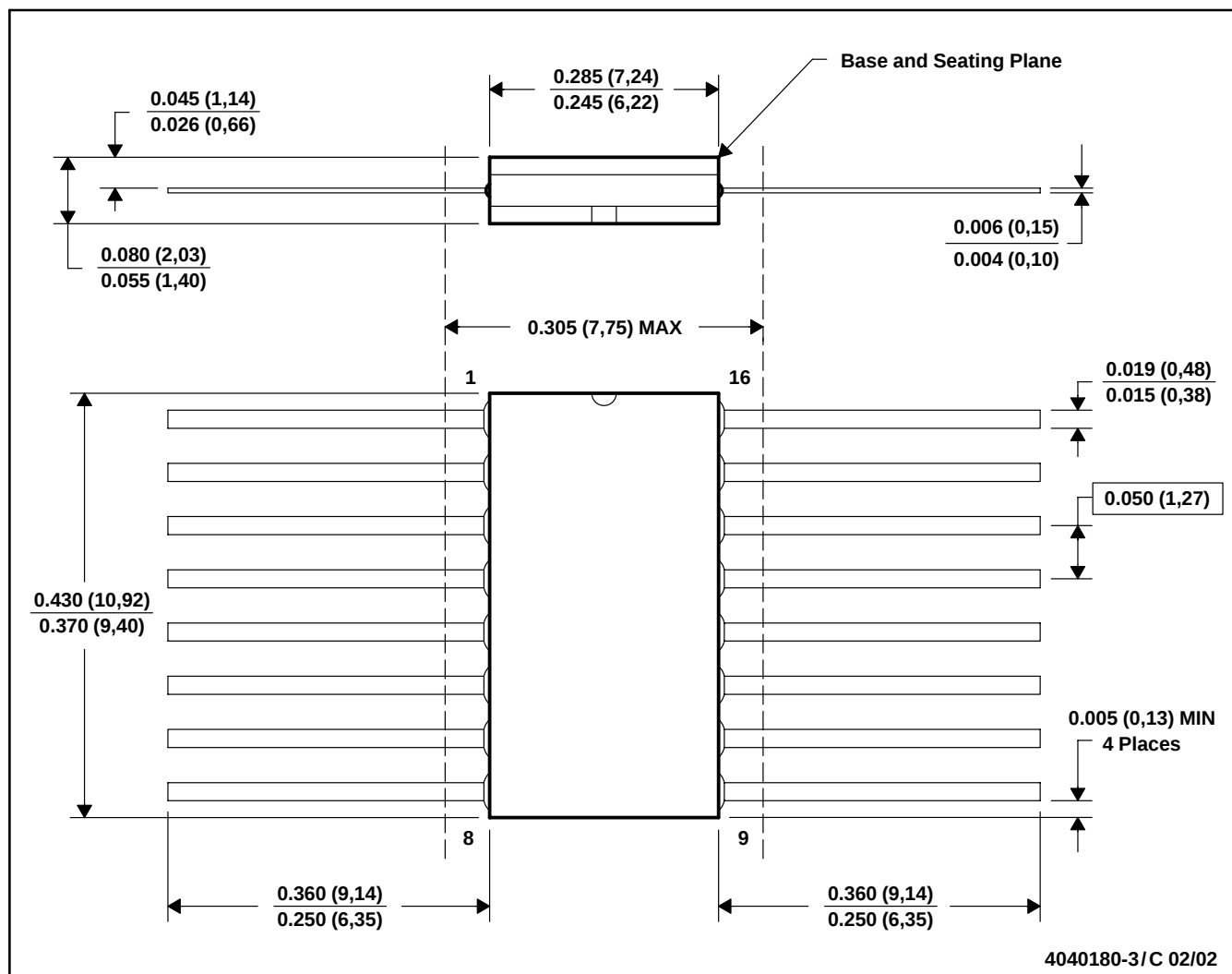


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification only.
 E. Falls within MIL STD 1835 GDFP-1F16 and JEDEC MO-092AC

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - The terminals are gold plated.
 - Falls within JEDEC MS-004

D (R-PDSO-G16)

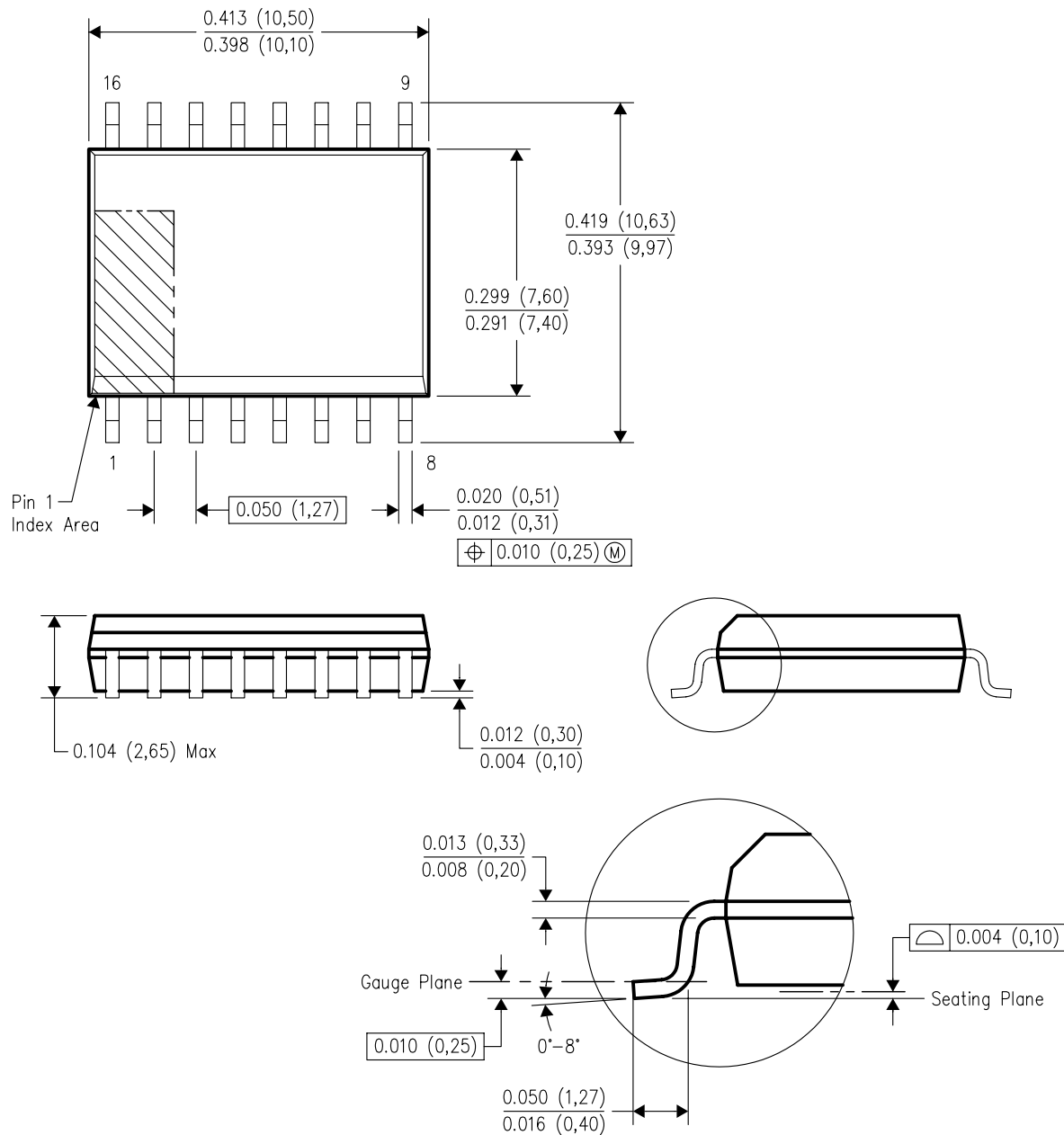
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-012 variation AC.

DW (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



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