SN54LS690, SN54LS691, SN54LS693
SN74LS690, SN74LS691, SN74LS693

Synchronous Counters with Output Registers and Multiplexed 3-State Outputs

These low-power Schottky LSI devices incorporate synchronous counters, four-bit D-type registers, and quadruple two-line to one-line multiplexers with three-state outputs in a single 20-pin package. The counters can be programmed from the data inputs and have enable P inputs and enable T inputs and a ripple-carry output for easy expansion. The register/counter select input, R/$\overline{C}$, selects the counter when low or the register when high for the three-state outputs, Q_A, Q_B, Q_C, and Q_D. These outputs are rated 12 and 24 milliamperes (54LS/74LS) for good bus-driving performance.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

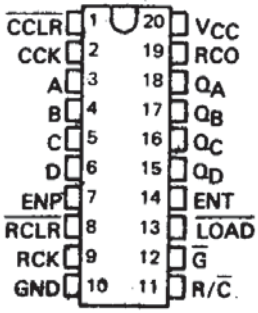
The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

SN54LS690, SN54LS691, SN54LS693, SN74LS690, SN74LS691, SN74LS693
SYNCHRONOUS COUNTERS WITH OUTPUT REGISTERS AND MULTIPLEXED 3-STATE OUTPUTS

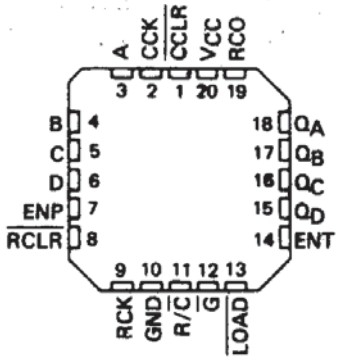
D2423, JANUARY 1981—REVISED MARCH 1988

- 4-Bit Counters/Registers
- Multiplexed Outputs for Counter or Latched Data
- 3-State Outputs Drive Bus Lines Directly
- 'LS690 . . .Decade Counter, Direct Clear
  'LS691 . . . Binary Counter, Direct Clear
  'LS693 . . . Binary Counter, Synchronous Clear

SN54LS690, SN54LS691, SN54LS693 . . . J PACKAGE
SN74LS690, SN74LS691, SN74LS693 . . . DW OR N PACKAGE
(TOP VIEW)



SN54LS690, SN54LS691, SN54LS693 . . . FK PACKAGE
(TOP VIEW)



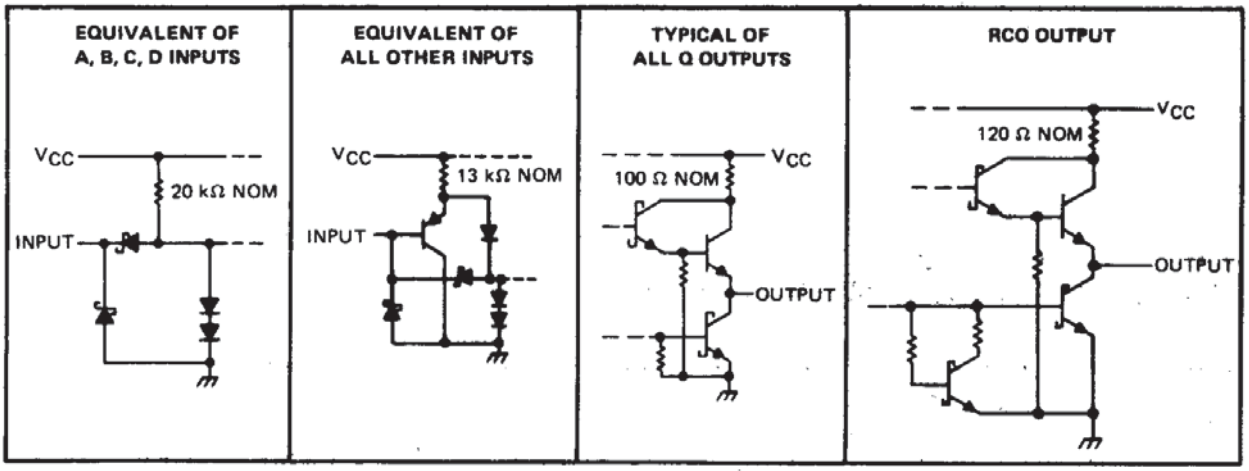
description

These low-power Schottky LSI devices incorporate synchronous counters, four-bit D-type registers, and quadruple two-line to one-line multiplexers with three-state outputs in a single 20-pin package. The counters can be programmed from the data inputs and have enable P inputs and enable T inputs and a ripple-carry output for easy expansion. The register/counter select input, R/$\overline{C}$, selects the counter when low or the register when high for the three-state outputs, Q_A, Q_B, Q_C, and Q_D. These outputs are rated at 12 and 24 milliamperes (54LS/74LS) for good bus-driving performance.

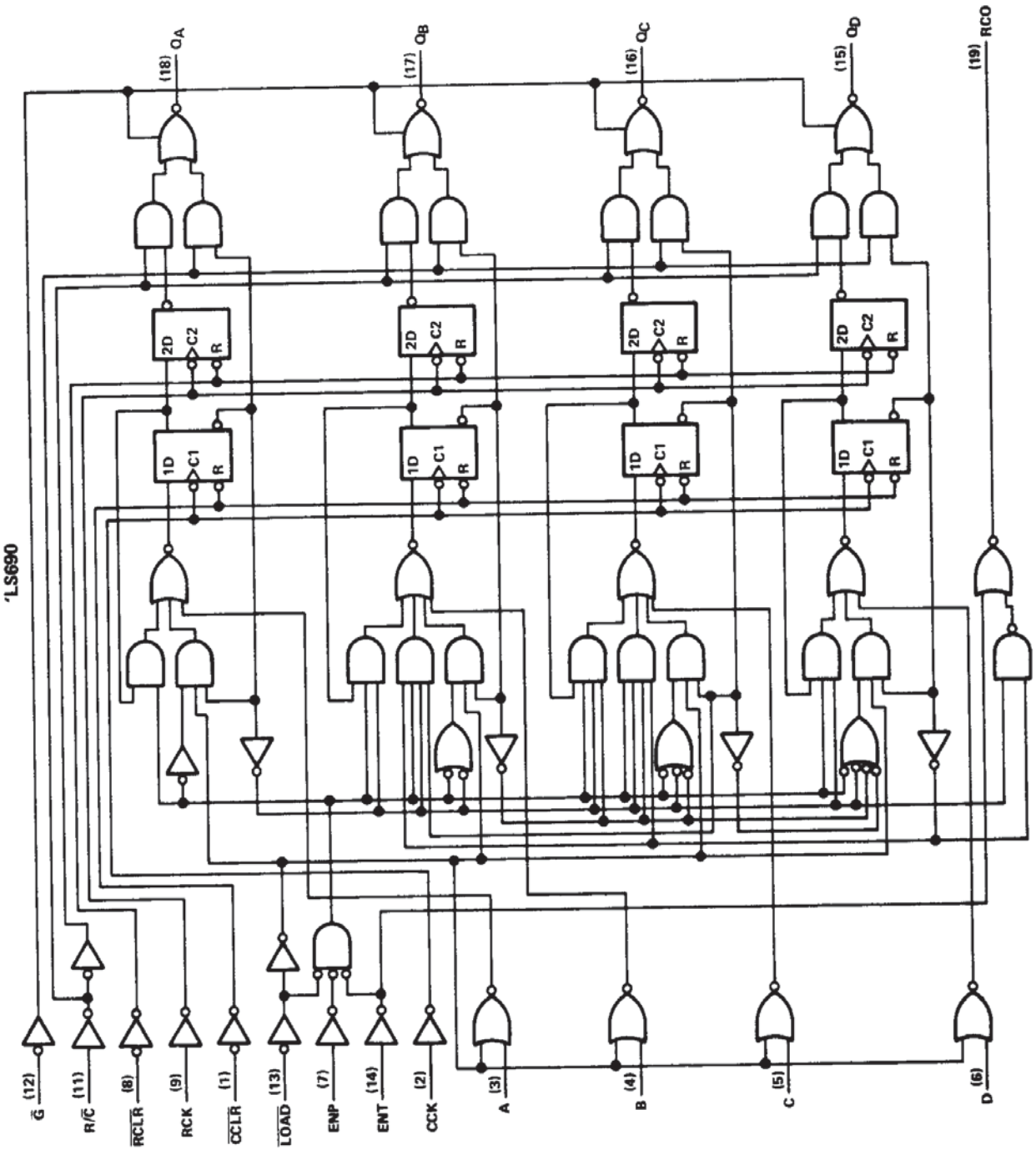
Individual clock and clear inputs are provided for both the counter and the register. Both clock inputs are positive-edge triggered: The clear line is active low and is asynchronous on the 'LS690 and 'LS691, synchronous on the 'LS693. Loading of the counter is accomplished when $\overline{LOAD}$ is taken low and a positive-transition occurs on the counter clock CCK.

Expansion is easily accomplished by connecting RCO of the first stage to ENT of the second state, etc. All ENP inputs can be tied common and used as master enable or disable control.

schematics of inputs and outputs



logic diagrams (positive logic)



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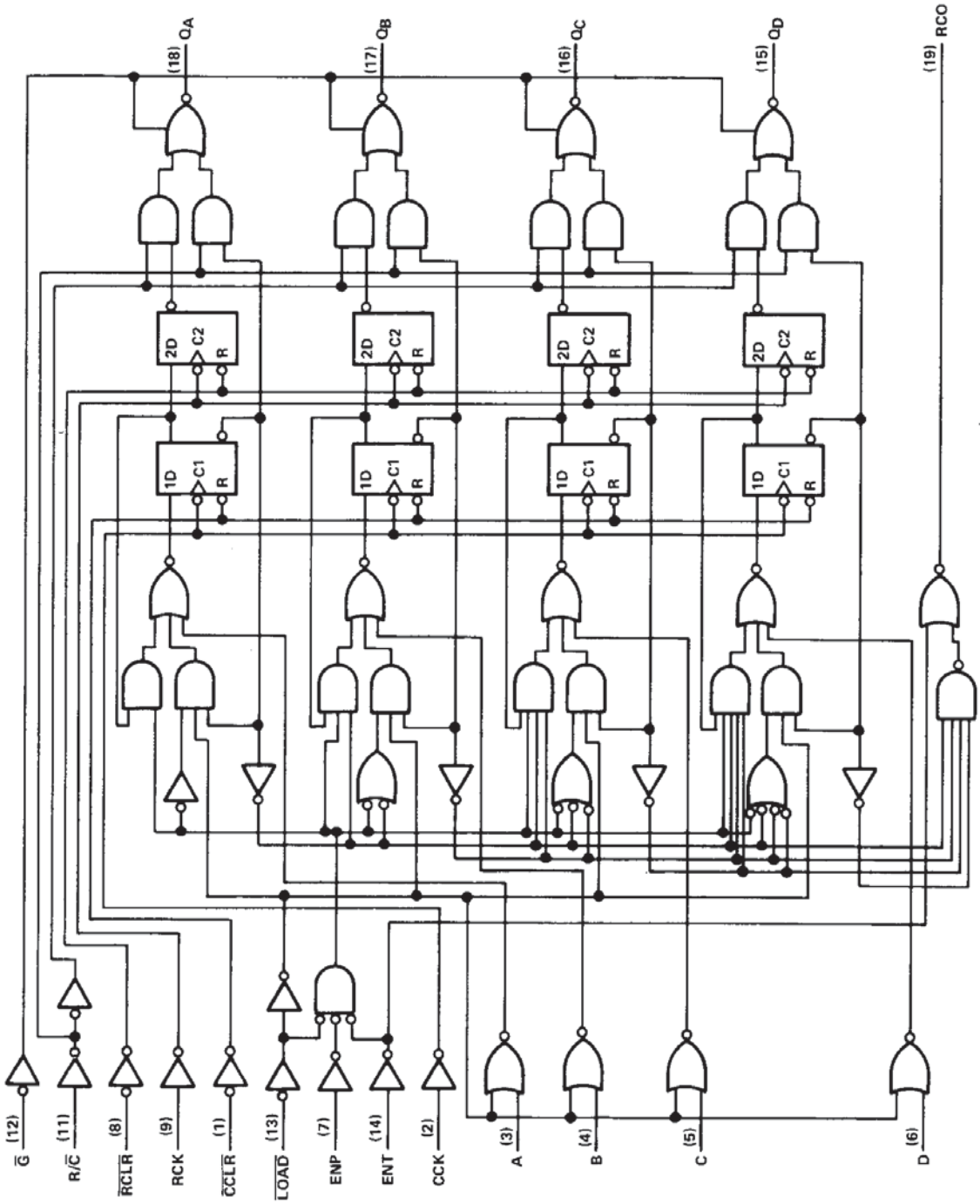
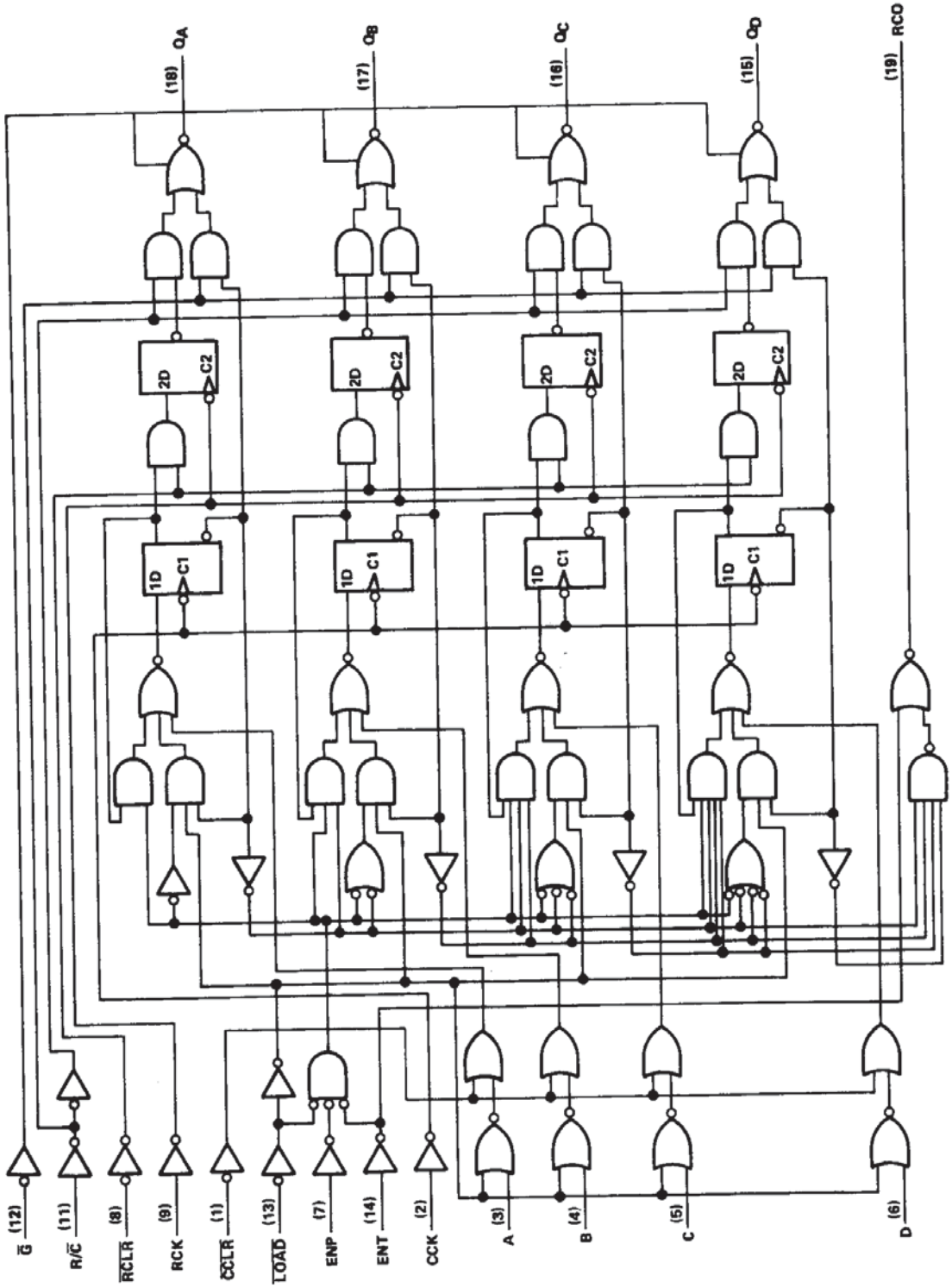
logic diagrams (positive logic) (continued)

'LS691



logic diagrams (positive logic) (continued)

'LS693



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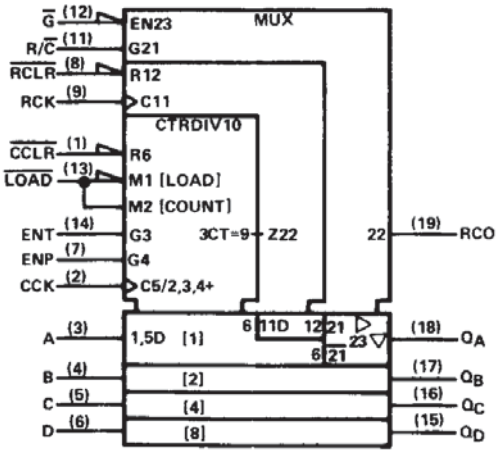
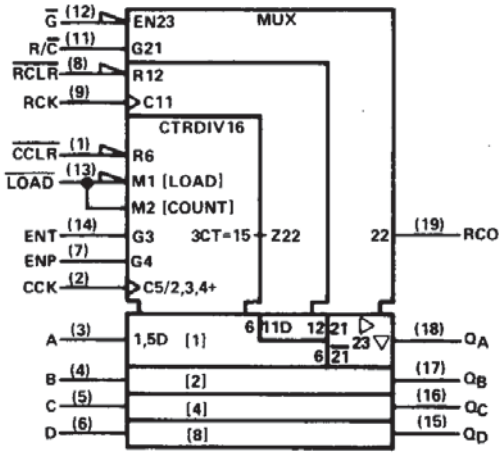
logic symbols†

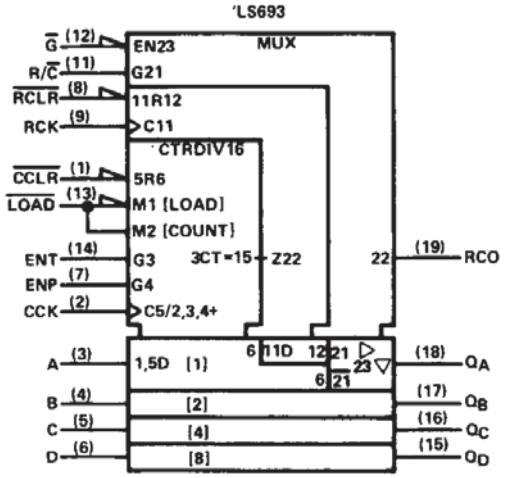
'LS690



'LS691



'LS693



†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (See Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS690, SN54LS691, SN54LS693 . . . . . −55°C to 125°C
SN74LS690, SN74LS691, SN74LS693 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

				SN54LS'			SN74LS'			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
I_{OH}	High-level output current		Q			−1			−2.6	mA
			RCO			−0.4			−0.4	mA
I_{OL}	Low-level output current		Q			12			24	mA
			RCO			4			8	mA
f_{clock}	Clock frequency		CCK	0		20	0		20	MHz
			RCK	0		20	0		20	MHz
t_w	Pulse duration		CCK high or low	25			25			ns
			RCK high or low	25			25			
		'LS690, 'LS691	$\overline{RCLR}$ low	20			20			
			$\overline{CCLR}$ low	20			20			
t_{su}	Setup time before CCK ↑		A thru D	30			30			ns
			ENP or ENT	30			30			
			$\overline{LOAD}$ ↓	30			30			
		'LS693	$\overline{CCLR}$ ↓	40			40			
		'LS690, 'LS691	$\overline{CCLR}$ ↑ inactive	25			25			
t_{su}	Setup time before RCK ↑		CCK ↑ (see Note 2)	30			30			ns
		'LS690, 'LS691	$\overline{RCLR}$ ↑ inactive	25			25			
		'LS693	RCLR ↓	20			20			
t_h	Hold time	Any input from CCK ↑ or RCK ↑		0			0			ns
T_A	Operating free-air temperature			−55		125	0		70	°C

NOTE 2: This set up time ensures the register will see stable data from the counter outputs. The clocks may be tied together in which case the register state will be one clock pulse behind the counter.

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[redacted]

Recommended Operating Conditions T-51-09-08

[redacted]

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 6)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS690, 'LS691			'LS693			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	CCK↑	RCO	R_L = 2 kΩ, C_L = 15 pF		23	40		23	40	ns
t_{PHL}					23	40		23	40	
t_{PLH}	ENT	RCO			13	20		13	20	ns
t_{PHL}					13	20		13	20	
t_{PLH}	CCK↑	Q	R_L = 667 Ω, C_L = 45 pF		12	20		12	20	ns
t_{PHL}					17	25		17	25	
t_{PLH}	RCK↑	Q			12	20		12	20	ns
t_{PHL}					17	25		17	25	
t_{PHL}	$\overline{CCLR}$↓	Q			23	40				ns
t_{PHL}	$\overline{RCLR}$↓	Q			20	30				ns
t_{PLH}	R/$\overline{C}$	Q			16	25		16	25	ns
t_{PHL}					16	25		16	25	
t_{PZH}	$\overline{G}$↓	Q			19	30		19	30	ns
t_{PZL}					19	30		19	30	
t_{PHZ}	$\overline{G}$↑	Q	R_L = 667 Ω, C_L = 5 pF		17	30		17	30	ns
t_{PLZ}					17	30		17	30	

NOTE 6: Load circuits and voltage waveforms are shown in Section 1.

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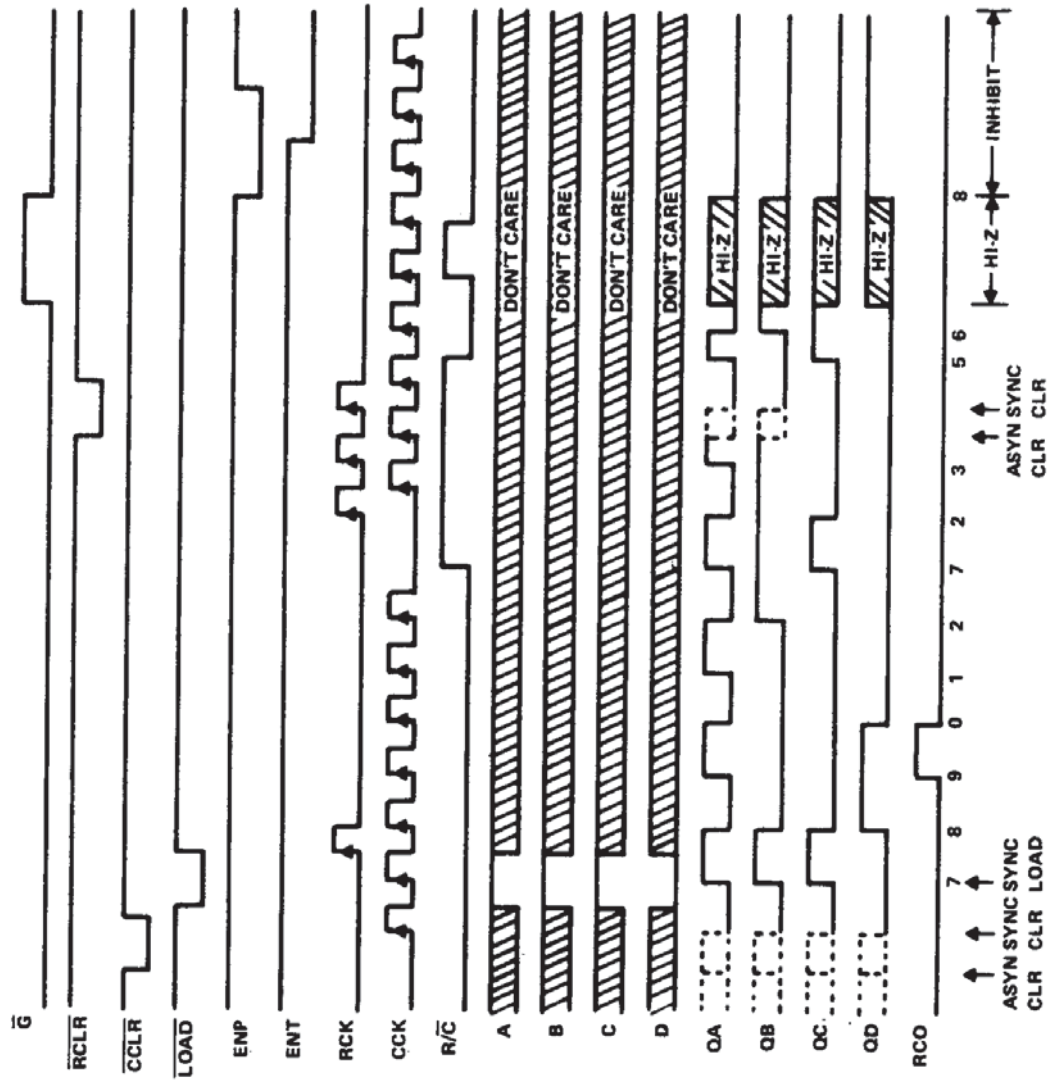
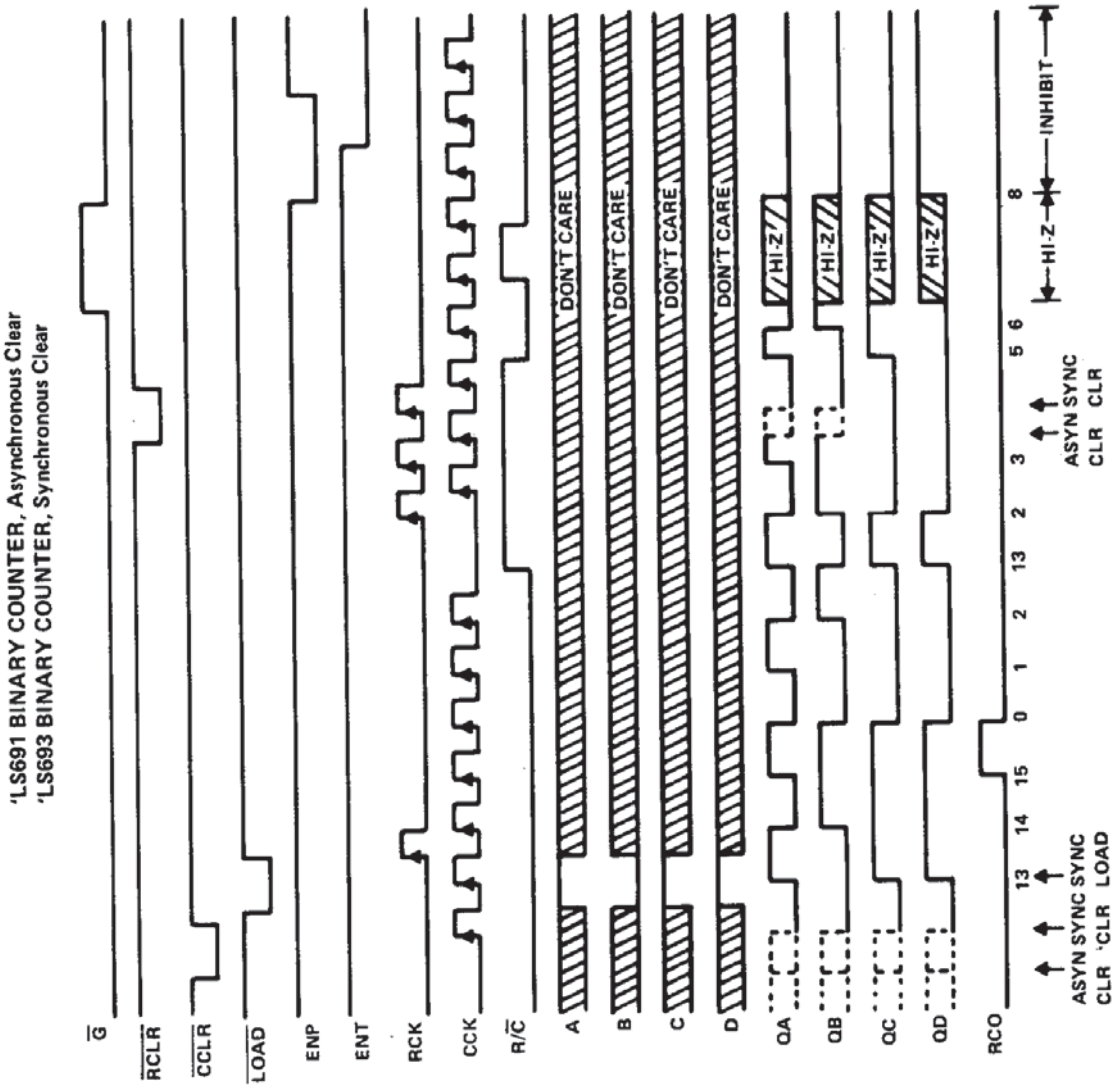
typical operating sequences

'LS690 DECADE COUNTER, Asynchronous Clear



typical operating sequences (continued)



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