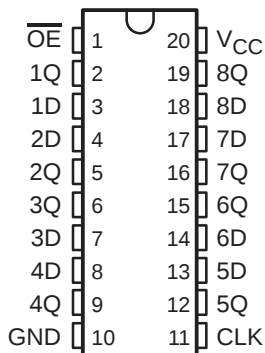


SN54LV374A, SN74LV374A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

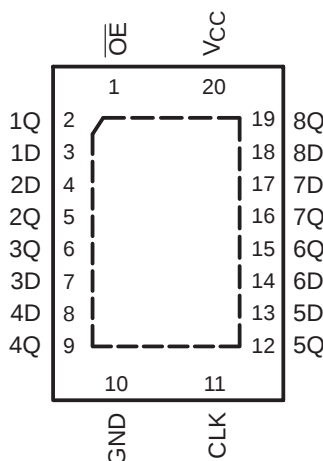
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- 2-V to 5.5-V V_{CC} Operation
- Max t_{pd} of 9.5 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce)
<0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot)
>2.3 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Voltage Operation on All Ports
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

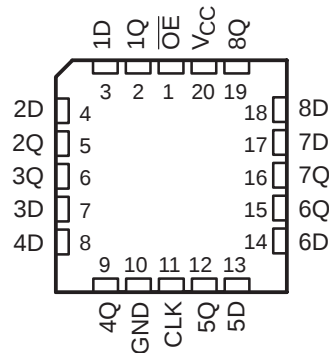
SN54LV374A . . . J OR W PACKAGE
SN74LV374A . . . DB, DGV, DW, NS,
OR PW PACKAGE
(TOP VIEW)



SN74LV374A . . . RGY PACKAGE
(TOP VIEW)



SN54LV374A . . . FK PACKAGE
(TOP VIEW)



description/ordering information

The 'LV374A devices are octal edge-triggered D-type flip-flops designed for 2-V to 5.5-V V_{CC} operation.

ORDERING INFORMATION

T_A	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QFN – RGY	Reel of 1000	SN74LV374ARGYR	LV374A
	SOIC – DW	Tube of 25	SN74LV374ADW	LV374A
		Reel of 2000	SN74LV374ADWR	
	SOP – NS	Reel of 2000	SN74LV374ANSR	74LV374A
	SSOP – DB	Reel of 2000	SN74LV374ADBR	LV374A
	TSSOP – PW	Tube of 70	SN74LV374APW	LV374A
		Reel of 2000	SN74LV374APWR	LV374A
		Reel of 250	SN74LV374APWT	LV374A
-55°C to 125°C	TVSOP – DGV	Reel of 2000	SN74LV374ADGVR	LV374A
	VFBGA – GQN	Reel of 1000	SN74LV374AGQNR	LV374A
	CDIP – J	Tube of 20	SNJ54LV374AJ	SNJ54LV374AJ
	CFP – W	Tube of 85	SNJ54LV374AW	SNJ54LV374AW
	LCCC – FK	Tube of 55	SNJ54LV374AFK	SNJ54LV374AFK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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**TEXAS
INSTRUMENTS**

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SN54LV374A, SN74LV374A
OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS
WITH 3-STATE OUTPUTS

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description/ordering information (continued)

These devices feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

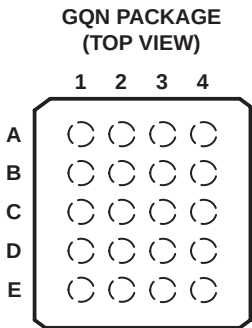
On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$ does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.



terminal assignments

	1	2	3	4
A	1Q	$\overline{OE}$	V_{CC}	8Q
B	2D	7D	1D	8D
C	3Q	2Q	6Q	7Q
D	4D	5D	3D	6D
E	GND	4Q	CLK	5Q

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT Q
$\overline{OE}$	CLK	D	
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

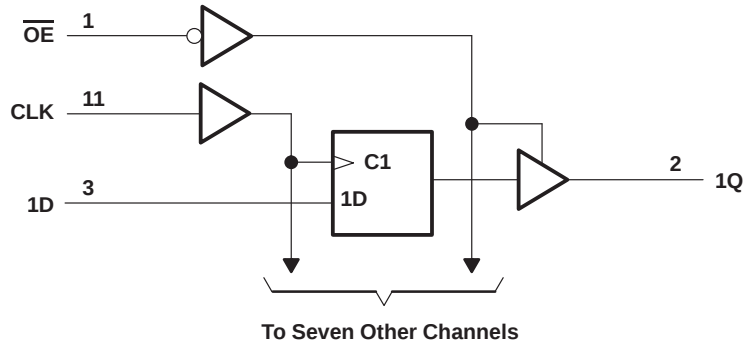
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OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS

WITH 3-STATE OUTPUTS

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logic diagram (positive logic)



Pin numbers shown are for the DB, DGV, DW, FK, J, NS, PW, RGY, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±35 mA
Continuous current through V_{CC} or GND	±70 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	70°C/W
(see Note 3): DGV package	92°C/W
(see Note 3): DW package	58°C/W
(see Note 3): GQN package	78°C/W
(see Note 3): NS package	60°C/W
(see Note 3): PW package	83°C/W
(see Note 4): RGY package	37°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 5.5 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.
 4. The package thermal impedance is calculated in accordance with JESD 51-5.

SN54LV374A, SN74LV374A

OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS

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recommended operating conditions (see Note 5)

			SN54LV374A		SN74LV374A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7		V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5		0.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3		V _{CC} × 0.3		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3		V _{CC} × 0.3		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3		V _{CC} × 0.3		
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage	High or low state	0	V _{CC}	0	V _{CC}	V
		3-state	0	5.5	0	5.5	
I _{OH}	High-level output current	V _{CC} = 2 V	−50		−50		μA
		V _{CC} = 2.3 V to 2.7 V	−2		−2		mA
		V _{CC} = 3 V to 3.6 V	−8		−8		
		V _{CC} = 4.5 V to 5.5 V	−16		−16		
I _{OL}	Low-level output current	V _{CC} = 2 V	50		50		μA
		V _{CC} = 2.3 V to 2.7 V	2		2		mA
		V _{CC} = 3 V to 3.6 V	8		8		
		V _{CC} = 4.5 V to 5.5 V	16		16		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V	200		200		ns/V
		V _{CC} = 3 V to 3.6 V	100		100		
		V _{CC} = 4.5 V to 5.5 V	20		20		
T _A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV374A			SN74LV374A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = −50 μA	2 V to 5.5 V	V _{CC} −0.1			V _{CC} −0.1			V
	I _{OH} = −2 mA	2.3 V	2			2			
	I _{OH} = −8 mA	3 V	2.48			2.48			
	I _{OH} = −16 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V	0.1			0.1			V
	I _{OL} = 2 mA	2.3 V	0.4			0.4			
	I _{OL} = 8 mA	3 V	0.44			0.44			
	I _{OL} = 16 mA	4.5 V	0.55			0.55			
I _I	V _I = 5.5 V or GND	0 to 5.5 V	±1			±1			μA
I _{OZ}	V _O = V _{CC} or GND	5.5 V	±5			±5			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	20			20			μA
I _{off}	V _I or V _O = 0 to 5.5 V	0	5			5			μA
C _i	V _I = V _{CC} or GND	3.3 V	2.9			2.9			pF

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timing requirements over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		SN54LV374A		SN74LV374A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration, CLK high or low	6		7		7		ns
t_{SU}	Setup time, data before CLK $\uparrow$	5		5.5		5.5		ns
t_H	Hold time, data after CLK $\uparrow$	2.5		2.5		2.5		ns

timing requirements over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		SN54LV374A		SN74LV374A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration, CLK high or low	5		5.5		5.5		ns
t_{SU}	Setup time, data before CLK $\uparrow$	4.5		4.5		4.5		ns
t_H	Hold time, data after CLK $\uparrow$	2		2		2		ns

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		SN54LV374A		SN74LV374A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration, CLK high or low	5		5		5		ns
t_{SU}	Setup time, data before CLK $\uparrow$	3		3		3		ns
t_H	Hold time, data after CLK $\uparrow$	2		2		2		ns

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV374A		SN74LV374A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}$	60*	105*		50*		50		MHz
			$C_L = 50\text{ pF}$	50	85		40		40		
t_{pd}	CLK	Q	$C_L = 15\text{ pF}$	9.7*	16.3*		1*	19*	1	19	ns
t_{en}	$\overline{OE}$	Q		8.9*	15.9*		1*	19*	1	19	
t_{dis}	$\overline{OE}$	Q		6.3*	12.6*		1*	15*	1	15	
t_{pd}	CLK	Q	$C_L = 50\text{ pF}$	11.8	19.3		1	23	1	23	ns
t_{en}	$\overline{OE}$	Q		10.9	18.8		1	22	1	22	
t_{dis}	$\overline{OE}$	Q		8.2	17.3		1	19	1	19	
$t_{sk(o)}$					2					2	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

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OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS

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switching characteristics over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV374A		SN74LV374A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}$	80*	150*		70*		70		MHz
			$C_L = 50\text{ pF}$	55	110		50		50		
t_{pd}	CLK	Q	$C_L = 15\text{ pF}$	6.8*	12.7*		1*	15*	1	15	ns
t_{en}	$\overline{\text{OE}}$	Q		6.3*	11*		1*	13*	1	13	
t_{dis}	$\overline{\text{OE}}$	Q		4.7*	10.5*		1*	12.5*	1	12.5	
t_{pd}	CLK	Q	$C_L = 50\text{ pF}$	8.3	16.2		1	18.5	1	18.5	ns
t_{en}	$\overline{\text{OE}}$	Q		7.7	14.5		1	16.5	1	16.5	
t_{dis}	$\overline{\text{OE}}$	Q		5.9	14		1	16	1	16	
$t_{\text{sk(o)}}$					1.5					1.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV374A		SN74LV374A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}$	130*	205*		110*		110		MHz
			$C_L = 50\text{ pF}$	85	170		75		75		
t_{pd}	CLK	Q	$C_L = 15\text{ pF}$	4.9*	8.1*		1*	9.5*	1	9.5	ns
t_{en}	$\overline{\text{OE}}$	Q		4.6*	7.6*		1*	9*	1	9	
t_{dis}	$\overline{\text{OE}}$	Q		3.4*	6.8*		1*	8*	1	8	
t_{pd}	CLK	Q	$C_L = 50\text{ pF}$	5.9	10.1		1	11.5	1	11.5	ns
t_{en}	$\overline{\text{OE}}$	Q		5.5	9.6		1	11	1	11	
t_{dis}	$\overline{\text{OE}}$	Q		4	8.8		1	10	1	10	
$t_{\text{sk(o)}}$					1					1	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 6)

PARAMETER		SN74LV374A			UNIT
		MIN	TYP	MAX	
$V_{\text{OL(P)}}$	Quiet output, maximum dynamic V_{OL}		0.6	0.8	V
$V_{\text{OL(V)}}$	Quiet output, minimum dynamic V_{OL}		−0.5	−0.8	V
$V_{\text{OH(V)}}$	Quiet output, minimum dynamic V_{OH}		2.9		V
$V_{\text{IH(D)}}$	High-level dynamic input voltage	2.31			V
$V_{\text{IL(D)}}$	Low-level dynamic input voltage		0.99		V

NOTE 6: Characteristics are for surface-mount packages only.

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	3.3 V	21.1	pF
				5 V	22.8	

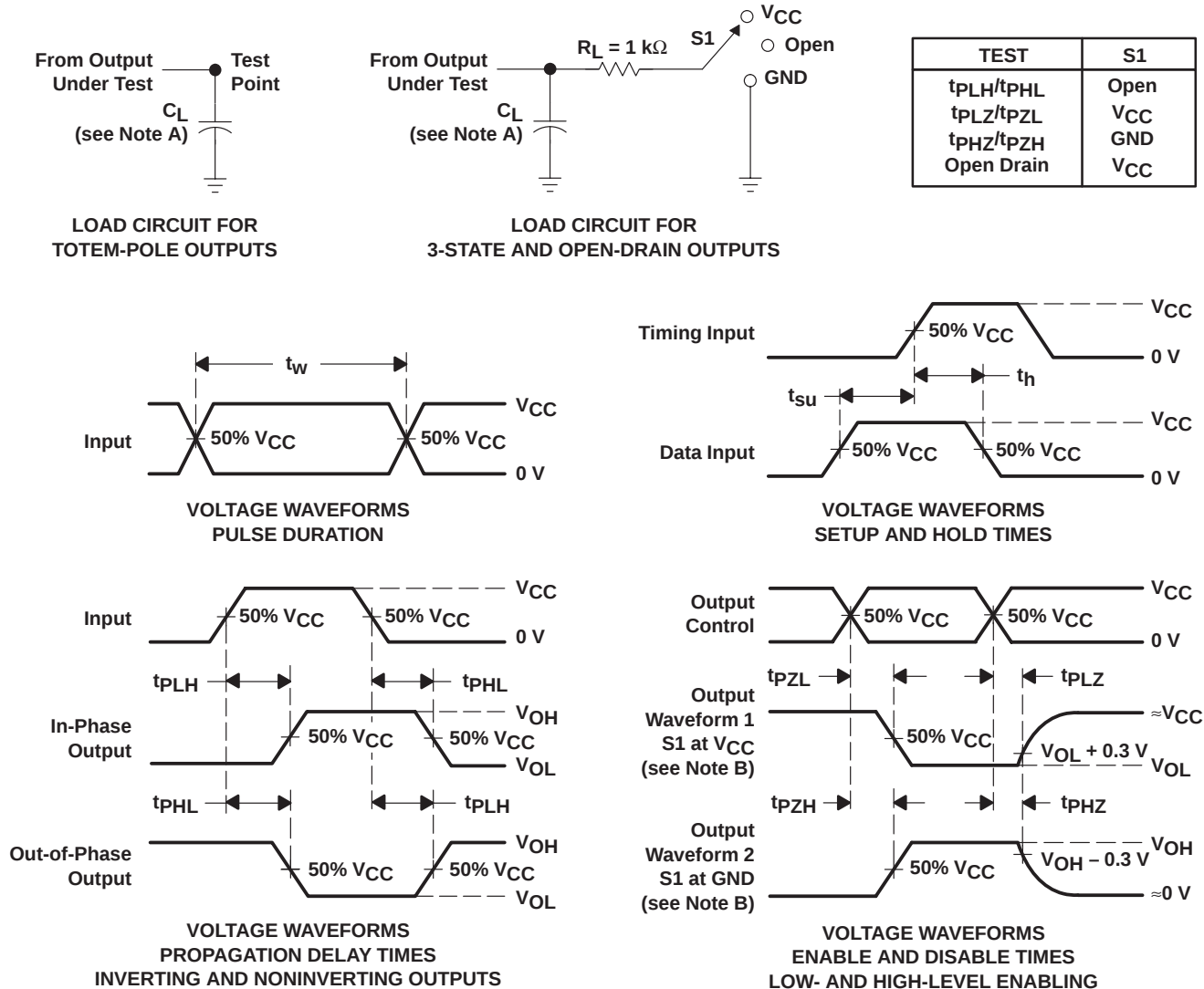
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SN54LV374A, SN74LV374A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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PARAMETER MEASUREMENT INFORMATION

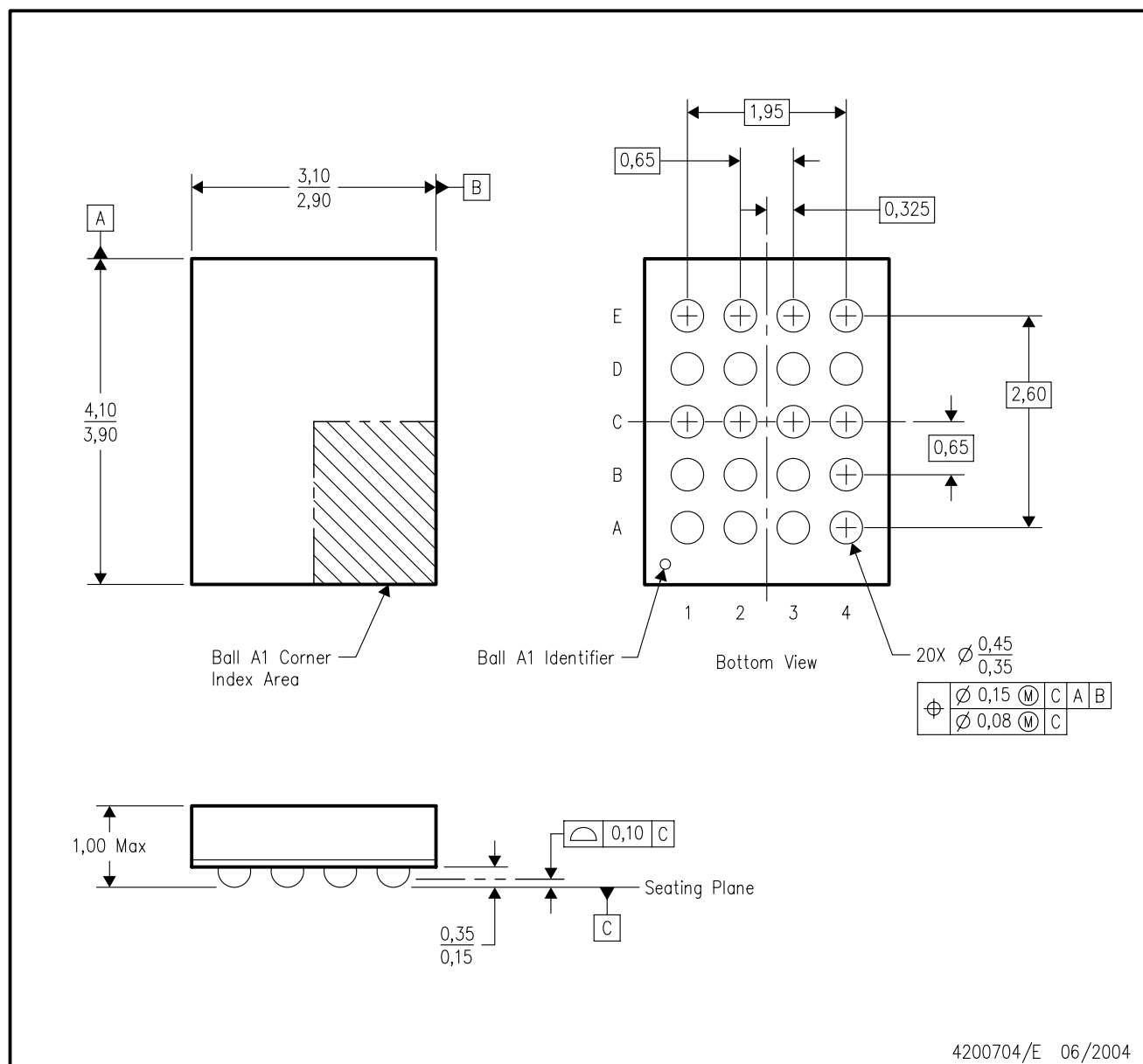


- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PHL} and t_{PLH} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

GQN (R-PBGA-N20)

PLASTIC BALL GRID ARRAY



- NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-225 variation BC.
D. This package is tin-lead (SnPb). Refer to the 20 ZQN package (drawing 4204492) for lead-free.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

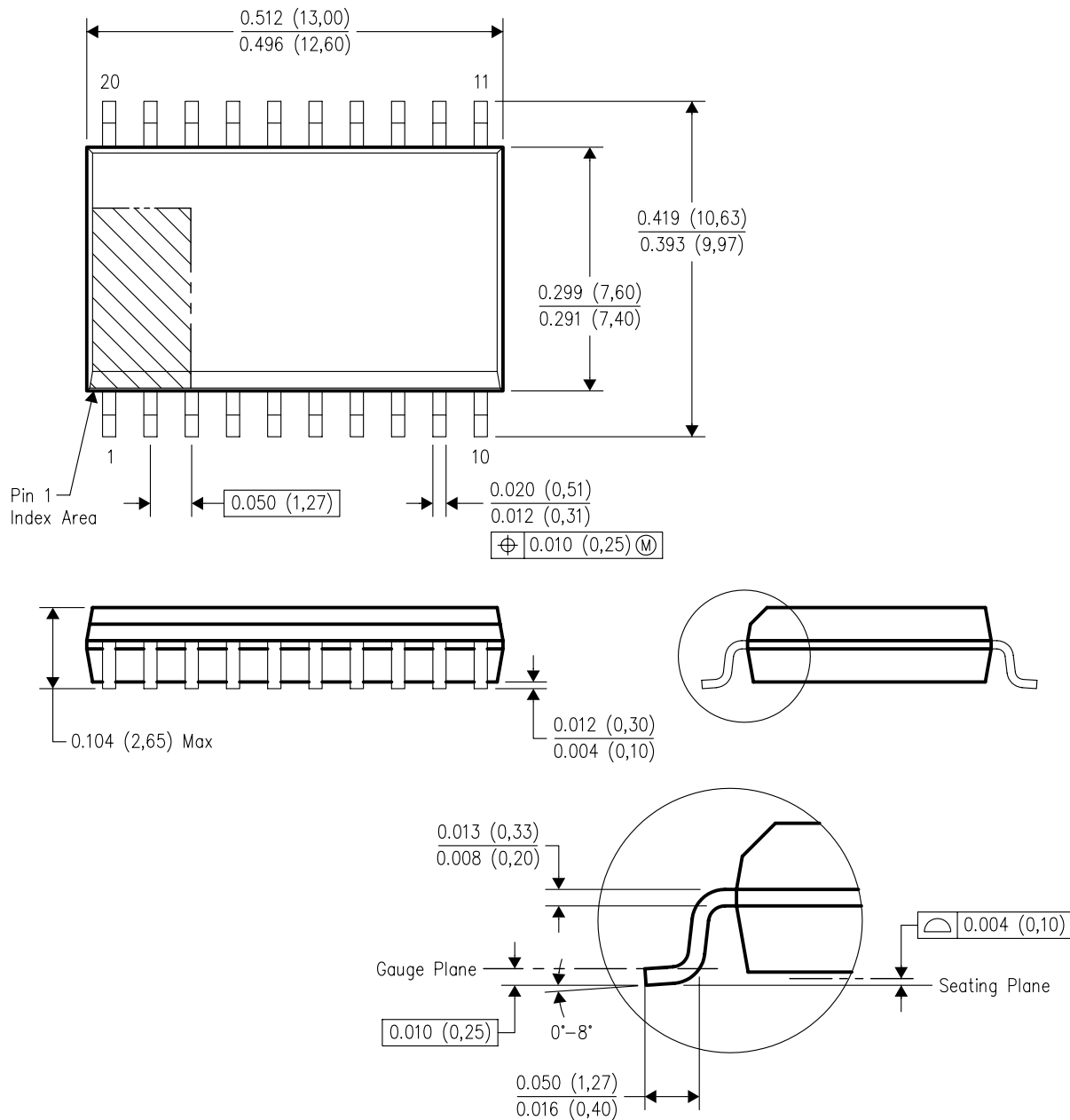
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE

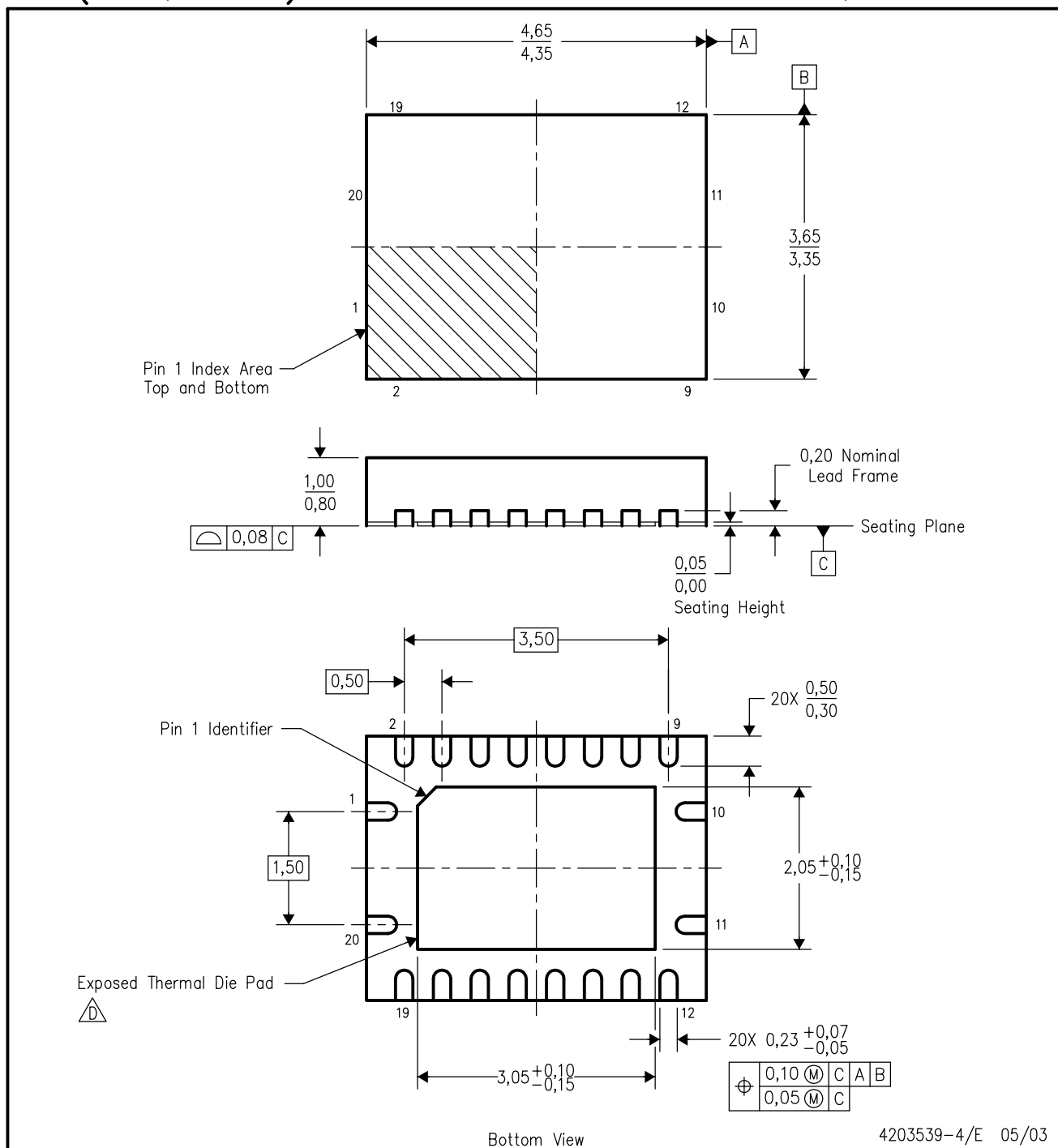


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- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AC.

RGY (R-PQFP-N20)

PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 -  D. The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected ground leads.
 - E. Package complies to JEDEC MO-241 variation BC.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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