

- Member of the Texas Instruments Widebus™ Family
- Supports SSTL_2 Data Inputs
- Outputs Meet SSTL_2 Class II Specifications
- Differential Clock (CLK and $\overline{\text{CLK}}$) Inputs
- Supports LVCMOS Switching Levels on the $\overline{\text{RESET}}$ Input
- $\overline{\text{RESET}}$ Input Disables Differential Input Receivers, Resets All Registers, and Forces All Outputs Low
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

description

This 14-bit registered buffer is designed for 2.3-V to 2.7-V V_{CC} operation.

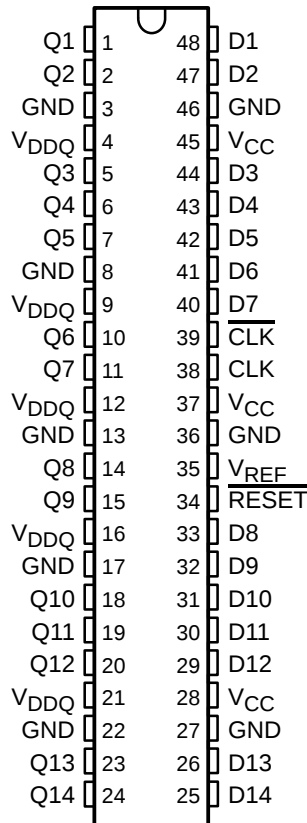
All inputs are SSTL_2, except the LVCMOS reset ($\overline{\text{RESET}}$) input. All outputs are SSTL_2, Class II compatible.

The SN74SSTV16857 operates from a differential clock (CLK and $\overline{\text{CLK}}$). Data are registered at the crossing of CLK going high and $\overline{\text{CLK}}$ going low.

The device supports low-power standby operation. When $\overline{\text{RESET}}$ is low, the differential input receivers are disabled and undriven (floating) data, clock, and reference voltage (V_{REF}) inputs are allowed. In addition, when $\overline{\text{RESET}}$ is low, all registers are reset and all outputs are forced low. The LVCMOS $\overline{\text{RESET}}$ input always must be held at a valid logic high or low level.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{\text{RESET}}$ must be held in the low state during power up.

DGG PACKAGE
(TOP VIEW)



ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	TSSOP – DGG	Tape and reel	SN74SSTV16857DGGR	SSTV16857

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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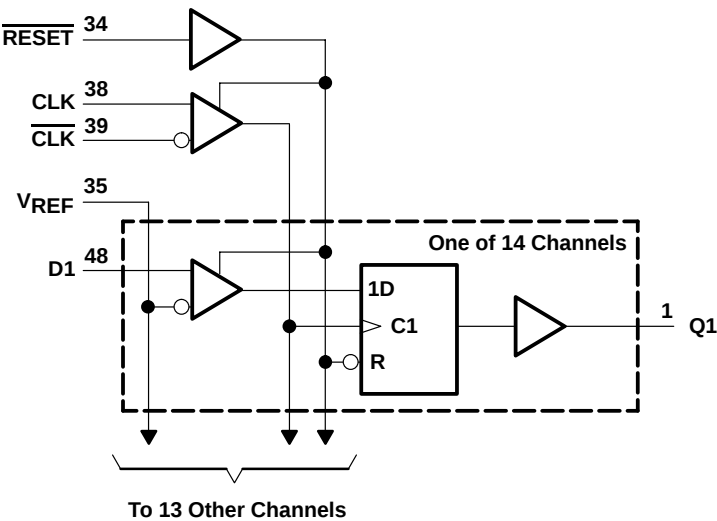
SN74SSTV16857
14-BIT REGISTERED BUFFER
WITH SSTL 2 INPUTS AND OUTPUTS

SCES344E – DECEMBER 2000 – REVISED NOVEMBER 2002

FUNCTION TABLE

INPUTS				OUTPUT
RESET	CLK	CLK	D	Q
H	↑	↓	H	H
H	↑	↓	L	L
H	L or H	L or H	X	Q ₀
L	X, or floating	X, or floating	X, or floating	L

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC} or V _{DDQ}	–0.5 V to 3.6 V
Input voltage range, V _I (see Notes 1 and 2)	–0.5 V to V _{CC} + 0.5 V
Output voltage range, V _O (see Notes 1 and 2)	–0.5 V to V _{DDQ} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{DDQ})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{DDQ})	±50 mA
Continuous current through each V _{CC} , V _{DDQ} , or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3)	70°C/W
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 3.6 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	V _{DDQ}		2.7	V
V _{DDQ}	Output supply voltage	2.3		2.7	V
V _{REF}	Reference voltage (V _{REF} = V _{DDQ} /2)	1.15	1.25	1.35	V
V _{TT}	Termination voltage	V _{REF} –40mV	V _{REF}	V _{REF} +40mV	V
V _I	Input voltage	0		V _{CC}	V
V _{IH}	AC high-level input voltage	Data inputs		V _{REF} +310mV	V
V _{IL}	AC low-level input voltage	Data inputs		V _{REF} –310mV	V
V _{IH}	DC high-level input voltage	Data inputs		V _{REF} +150mV	V
V _{IL}	DC low-level input voltage	Data inputs		V _{REF} –150mV	V
V _{IH}	High-level input voltage	RESET		1.7	V
V _{IL}	Low-level input voltage	RESET		0.7	V
V _{ICR}	Common-mode input voltage range	CLK, CLK		0.97	1.53
V _{I(PP)}	Peak-to-peak input voltage	CLK, CLK		360	mV
I _{OH}	High-level output current			–20	mA
I _{OL}	Low-level output current			20	
T _A	Operating free-air temperature			0	70
					°C

NOTE 4: The RESET input of the device must be held at a valid logic level (not floating) to ensure proper device operation. The differential inputs must not be floating unless RESET is low. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC} AND V _{DDQ}	MIN	TYP†	MAX	UNIT
V _{IK}		I _I = –18 mA	2.3 V			–1.2	V
V _{OH}		I _{OH} = –100 µA	2.3 V to 2.7 V	V _{DDQ} –0.2			V
		I _{OH} = –16 mA	2.3 V	1.95			
V _{OL}		I _{OL} = 100 µA	2.3 V to 2.7 V			0.2	V
		I _{OL} = 16 mA	2.3 V			0.35	
I _I	All inputs	V _I = V _{CC} or GND	2.7 V			±5	µA
I _{CC}	Static standby	RESET = GND	2.7 V			10	µA
	Static operating	RESET = V _{CC} , V _I = V _{IH} (AC) or V _{IL} (AC)			8	56	mA
I _{CCD}	Dynamic operating – clock only	RESET = V _{CC} , V _I = V _{IH} (AC) or V _{IL} (AC), CLK and CLK switching 50% duty cycle	2.5 V		28		µA/MHz
	Dynamic operating – per each data input	RESET = V _{CC} , V _I = V _{IH} (AC) or V _{IL} (AC), CLK and CLK switching 50% duty cycle, One data input switching at one-half clock frequency, 50% duty cycle			9		µA/clock MHz/D input
r _{OH}	Output high	I _{OH} = –20 mA	2.3 V to 2.7 V	7		20	Ω
r _{OL}	Output low	I _{OL} = 20 mA	2.3 V to 2.7 V	7		20	Ω
r _{O(Δ)}	r _{OH} – r _{OL}	I _O = 20 mA, T _A = 25°C	2.5 V			6	Ω
C _i	Data inputs	V _I = V _{REF} ± 310 mV	2.5 V	2.5	3	3.5	pF
	CLK, CLK	V _{ICR} = 1.25 V, V _{I(PP)} = 360 mV		2.5	3	3.5	
	RESET	V _I = V _{CC} or GND		2.5	3	3.5	

† All typical values are at V_{CC} = 2.5 V, T_A = 25°C.

SN74SSTV16857

14-BIT REGISTERED BUFFER

WITH SSTL 2 INPUTS AND OUTPUTS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			V _{CC} = 2.5 V ± 0.2 V†		UNIT
			MIN	MAX	
f _{clock}	Clock frequency		200		MHz
t _w	Pulse duration	CLK, $\overline{\text{CLK}}$ high or low	2.5		ns
t _{act}	Differential inputs active time (see Note 5)		22		ns
t _{inact}	Differential inputs inactive time (see Note 6)		22		ns
t _{su}	Setup time	Fast slew rate (see Notes 7 and 9)	Data before CLK↑, $\overline{\text{CLK}}$ ↓	0.75	ns
		Slow slew rate (see Notes 8 and 9)		0.9	
t _h	Hold time	Fast slew rate (see Notes 7 and 9)	Data after CLK↑, $\overline{\text{CLK}}$ ↓	0.75	ns
		Slow slew rate (see Notes 8 and 9)		0.9	

† For this test condition, V_{DDQ} always is equal to V_{CC} .

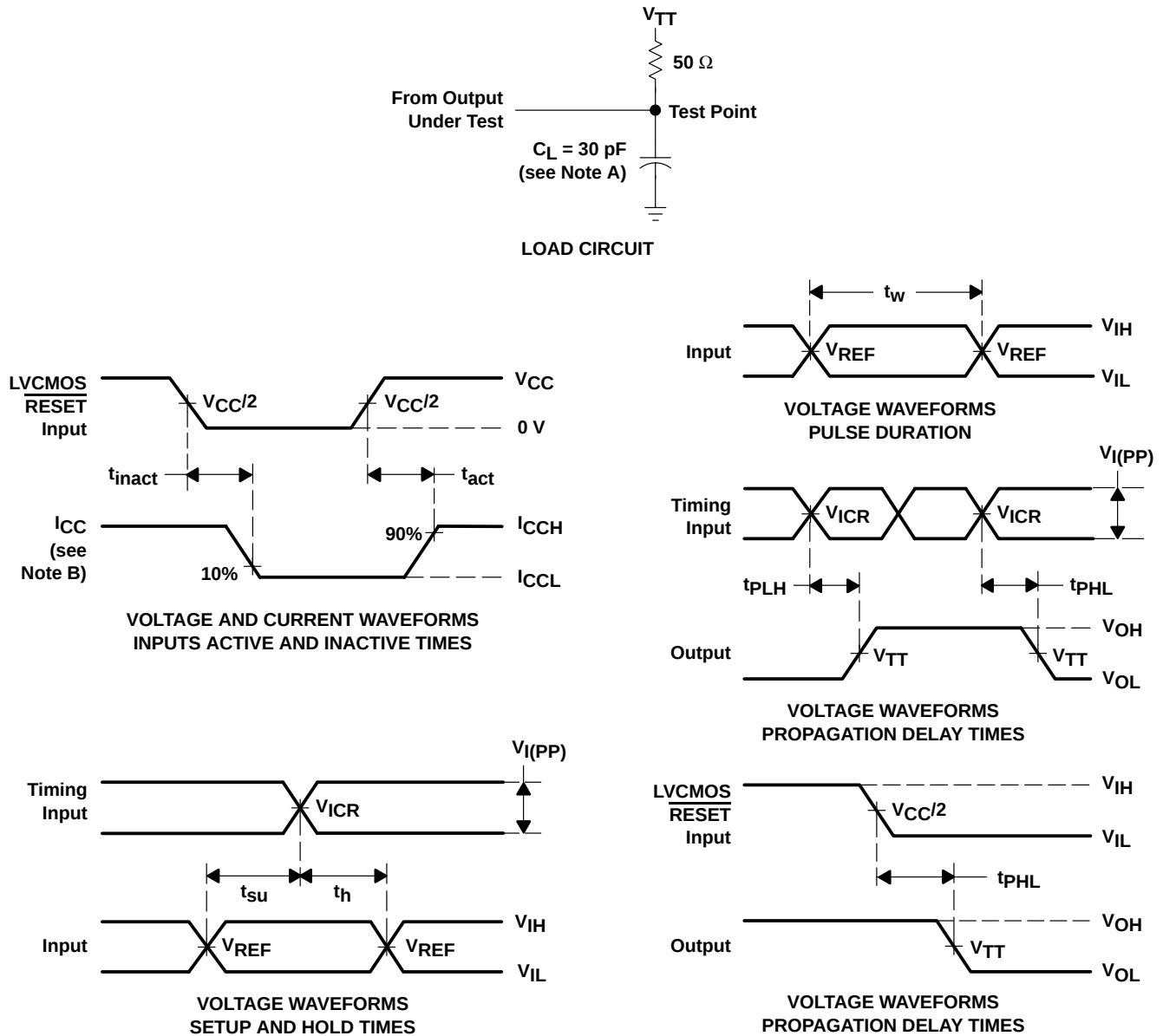
- NOTES:
5. Data inputs must be held low for a minimum time of t_{act} min, after $\overline{\text{RESET}}$ is taken high.
 6. Data and clock inputs must be held at valid levels (not floating) for a minimum time of t_{inact} min, after $\overline{\text{RESET}}$ is taken low.
 7. Data signal input slew rate $\geq 1\text{ V/ns}$
 8. Data signal input slew rate $\geq 0.5\text{ V/ns}$ and $< 1\text{ V/ns}$
 9. CLK, $\overline{\text{CLK}}$ input slew rates are $\geq 1\text{ V/ns}$.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}^\dagger$		UNIT
			MIN	MAX	
f_{max}			200		MHz
t_{pd}	CLK and $\overline{\text{CLK}}$	Q	1.1	2.8	ns
t_{PHL}	$\overline{\text{RESET}}$	Q		5	ns

† For this test condition, V_{DDQ} always is equal to V_{CC} .

PARAMETER MEASUREMENT INFORMATION



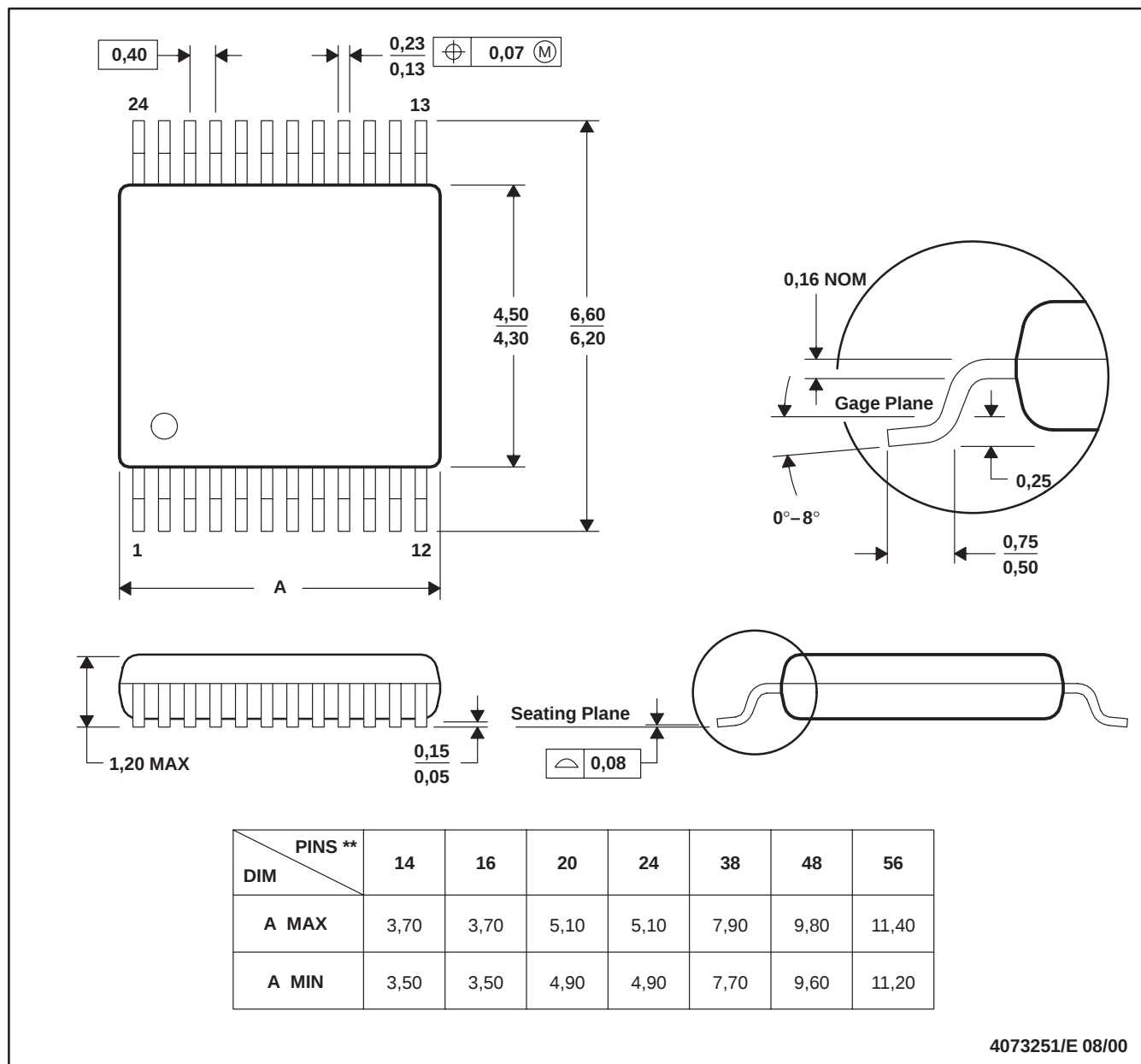
- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. I_{CC} tested with clock and data inputs held at V_{CC} or GND, and $I_O = 0$ mA.
 - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50 \Omega$, input slew rate = 1 V/ns $\pm 20\%$ (unless otherwise noted).
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. $V_{TT} = V_{REF} = V_{DDQ}/2$
 - F. $V_{IH} = V_{REF} + 310$ mV (ac voltage levels) for differential inputs. $V_{IH} = V_{CC}$ for LVC MOS input.
 - G. $V_{IL} = V_{REF} - 310$ mV (ac voltage levels) for differential inputs. $V_{IL} = \text{GND}$ for LVC MOS input.
 - H. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

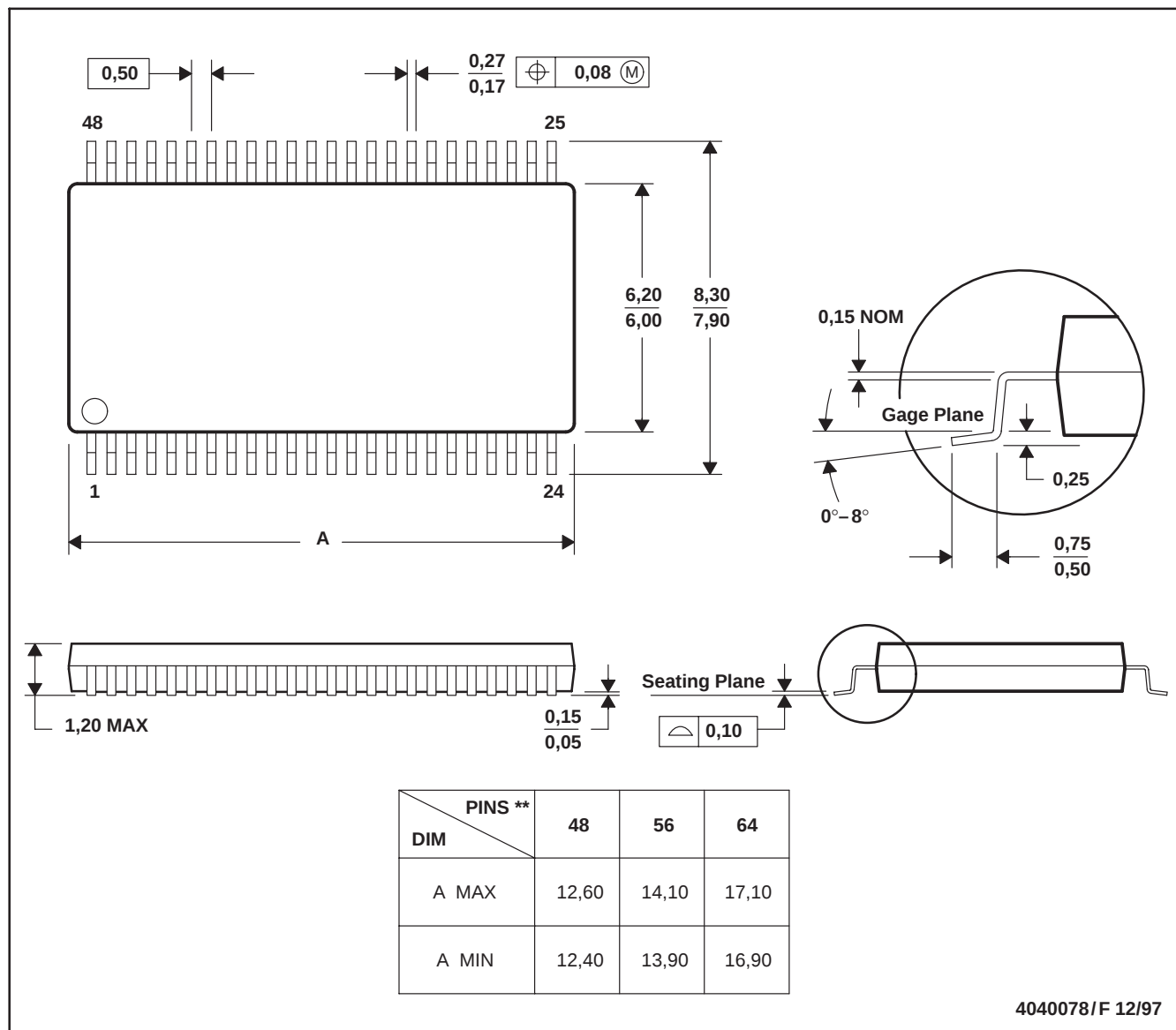


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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