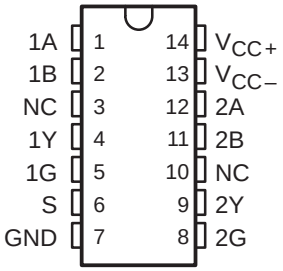
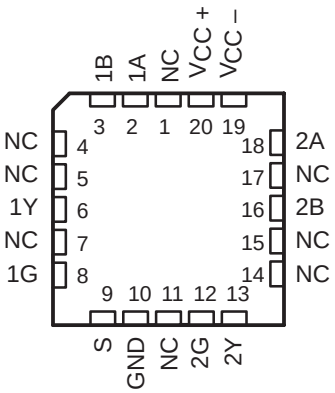
- **High Speed**
- **Standard Supply Voltage**
- **Dual Channels**
- **High Common-Mode Rejection Ratio**
- **High Input Impedance**
- **High Input Sensitivity**
- **Differential Common-Mode Input Voltage Range of ±3 V**
- **Strobe Inputs for Receiver Selection**
- **Gate Inputs for Logic Versatility**
- **TTL Drive Capability**
- **High dc Noise Margin**
- **Totem-Pole Outputs**
- **B Version Has Diode-Protected Input for Power-Off Condition**

SN55107A . . . J OR W PACKAGE
SN75107A, SN75107B, SN75108A . . . D OR N PACKAGE
(TOP VIEW)



SN55107A . . . FK PACKAGE
(TOP VIEW)

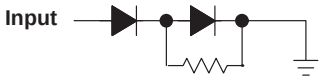


NC – No internal connection

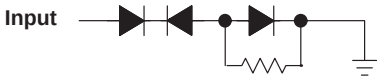
description

These circuits are TTL-compatible, high-speed line receivers. Each is a monolithic dual circuit featuring two independent channels. They are designed for general use, as well as for such specific applications as data comparators and balanced, unbalanced, and party-line transmission systems. These devices are unilaterally interchangeable with and are replacements for the SN55107, SN75107, and SN75108, but offer diode-clamped strobe inputs to simplify circuit design.

The essential difference between the A and B versions can be seen in the schematics. Input-protection diodes are in series with the collectors of the differential-input transistors of the B versions. These diodes are useful in certain party-line systems that have multiple V_{CC+} power supplies and can be operated with some of the V_{CC+} supplies turned off. In such a system, if a supply is turned off and allowed to go to ground, the equivalent input circuit connected to that supply would be as follows:



A Version



B Version

This would be a problem in specific systems that might have the transmission lines biased to some potential greater than 1.4 V.

The SN55107A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN75107A, SN75107B, and SN75108A are characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 3) . . . . . 7 V
Supply voltage, V_{CC-} . . . . . –7 V
Differential input voltage, V_{ID} (see Note 4) . . . . . ±6 V
Common-mode input voltage, V_{IC} (see Note 5) . . . . . ±5 V
Strobe input voltage . . . . . 5.5 V
Continuous total dissipation . . . . . See Dissipation Rating Table
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Case temperature for 60 seconds, T_c: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or W package . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 3. All voltage values, except differential voltages, are with respect to network ground terminal.
4. Differential voltage values are at the noninverting (A) terminal with respect to the inverting (B) terminal.
5. Common-mode input voltage is the average of the voltages at the A and B inputs.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	—
W	1000 mW	8.0 mW/°C	640 mW	200 mW

recommended operating conditions (see Note 6)

	SN55107A			SN75107A, SN75107B, SN75108A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC+}	4.5	5	5.5	4.75	5	5.25	V
Supply voltage, V_{CC-}	–4.5	–5	–5.5	–4.75	–5	–5.25	V
High-level input voltage between differential inputs, V_{IDH} (see Note 7)	0.025		5	0.025		5	V
Low-level input voltage between differential inputs, V_{IDL} (see Note 7)	–5‡		–0.025	–5‡		–0.025	V
Common-mode input voltage, V_{IC} (see Notes 7 and 8)	–3‡		3	–3‡		3	V
Input voltage, any differential input to GND (see Note 8)	–5‡		3	–5‡		3	V
High-level input voltage at strobe inputs, $V_{IH(S)}$	2		5.5	2		5.5	V
Low-level input voltage at strobe inputs, $V_{IL(S)}$	0		0.8	0		0.8	V
Low-level output current, I_{OL}			–16			–16	mA
Operating free-air temperature, T_A	–55		125	0		70	°C

‡ The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for input voltage levels only.

NOTES: 6. When using only one channel of the line receiver, the strobe input (G) of the unused channel should be grounded and at least one of the differential inputs of the unused receiver should be terminated at some voltage between –3 V and 3 V.
7. The recommended combinations of input voltages fall within the shaded area in Figure 1.
8. The common-mode voltage may be as low as –4 V provided that the more positive of the two inputs is not more negative than –3 V.

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		'107A, SN75107B			SN75108A			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{OH}	High-level output voltage		$V_{CC\pm}$ = MIN, V_{IDH} = 25 mV, V_{IC} = –3 V to 3 V	$V_{IL(S)}$ = 0.8 V, I_{OH} = –400 µA,	2.4						V
V_{OL}	Low-level output voltage		$V_{CC\pm}$ = MIN, V_{IDL} = –25 mV, V_{IC} = –3 V to 3 V	$V_{IH(S)}$ = 2 V, I_{OL} = 16 mA,			0.4			0.4	V
I_{IH}	High-level input current	A	$V_{CC\pm}$ = MAX	V_{ID} = 5 V		30	75		30	75	µA
		B		V_{ID} = –5 V		30	75		30	75	
I_{IL}	Low-level input current	A	$V_{CC\pm}$ = MAX	V_{ID} = –5 V			–10			–10	µA
		B		V_{ID} = 5 V			–10			–10	
I_{IH}	High-level input current into 1G or 2G		$V_{CC\pm}$ = MAX,	$V_{IH(G)}$ = 2.4 V			40			40	µA
			$V_{CC\pm}$ = MAX, $V_{IH(G)}$ = MAX V_{CC+}				1			1	mA
I_{IL}	Low-level input current into 1G or 2G		$V_{CC\pm}$ = MAX,	$V_{IL(G)}$ = 0.4 V			–1.6			–1.6	mA
I_{IH}	High-level input current into S		$V_{CC\pm}$ = MAX,	$V_{IH(S)}$ = 2.4 V			80			80	µA
			$V_{CC\pm}$ = MAX, $V_{IH(S)}$ = MAX V_{CC+}				2			2	mA
I_{IL}	Low-level input current into S		$V_{CC\pm}$ = MAX,	$V_{IL(S)}$= 0.4 V			–3.2			–3.2	mA
I_{OH}	High-level output current		$V_{CC\pm}$ = MIN, V_{OH} = MAX V_{CC+}							250	µA
I_{OS}	Short-circuit output current§		$V_{CC\pm}$ = MAX		–18		–70				mA
I_{CCH+}	Supply current from V_{CC+}, outputs high		$V_{CC\pm}$ = MAX,	T_A = 25°C		18	30		18	30	mA
I_{CCH-}	Supply current from V_{CC-}, outputs high		$V_{CC\pm}$ = MAX,	T_A = 25°C		–8.4	–15		–8.4	–15	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC+} = 5 V, V_{CC-} = –5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics, $V_{CC\pm}$ = ±5 V, T_A = 25°C, R_L = 390 Ω (see Figure 2)

PARAMETER		TEST CONDITIONS	'107A, SN75107B			SN75108A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$t_{PLH(D)}$	Propagation delay time, low- to high-level output, from differential inputs A and B	C_L = 50 pF		17	25				ns
		C_L = 15 pF					19	25	
$t_{PHL(D)}$	Propagation delay time, high- to low-level output, from differential inputs A and B	C_L = 50 pF		17	25				ns
		C_L = 15 pF					19	25	
$t_{PLH(S)}$	Propagation delay time, low- to high-level output, from strobe input G or S	C_L = 50 pF		10	15				ns
		C_L = 15 pF					13	20	
$t_{PHL(S)}$	Propagation delay time, high- to low-level output, from strobe input G or S	C_L = 50 pF		8	15				ns
		C_L = 15 pF					13	20	

APPLICATION INFORMATION

SN75108A dot-AND output connections

The SN75108A line receiver features an open-collector-output circuit that can be connected in the dot-AND logic configuration with other similar open-collector outputs. This allows a level of logic to be implemented without additional logic delay.

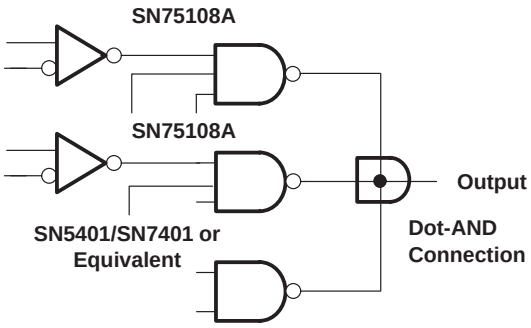


Figure 14. Dot-AND Connection

increasing common-mode input voltage range of receiver

The common-mode voltage range (CMVR) is defined as the range of voltage applied simultaneously to both input terminals that, if exceeded, does not allow normal operation of the receiver.

The recommended operating CMVR is ±3 V, making it useful in all but the noisiest environments. In extremely noisy environments, common-mode voltage can easily reach ±10 V to ±15 V if some precautions are not taken to reduce ground and power supply noise, as well as crosstalk problems. When the receiver must operate in such conditions, input attenuators should be used to decrease the system common-mode noise to a tolerable level at the receiver inputs. Differential noise is also reduced by the same ratio. These attenuators were omitted intentionally from the receiver input terminals so the designer can select resistors that are compatible with his particular application or environment. Furthermore, the use of attenuators adversely affects the input sensitivity, the propagation delay time, the power dissipation, and in some cases (depending on the selected resistor values) the input impedance; thereby reducing the versatility of the receiver.

The ability of the receiver to operate with approximately ±15 V common-mode voltage at the inputs has been checked using the circuit shown in Figure 15. Resistors R1 and R2 provide a voltage-divider network. Dividers with three different values presenting a 5-to-1 attenuation were used to operate the differential inputs at approximately ±3 V common-mode voltage. Careful matching of the two attenuators is needed to balance the overdrive at the input stage. The resistors used are shown in Table 1.

Table 1

Attenuator 1:	R1 = 2 kΩ,	R2 = 0.5 kΩ
Attenuator 2:	R1 = 6 kΩ,	R2 = 1.5 kΩ
Attenuator 3:	R1 = 12 kΩ,	R2 = 3 kΩ

APPLICATION INFORMATION

increasing common-mode input voltage range of receiver (continued)

Table 2 shows some of the typical switching results obtained under such conditions.

Table 2. Typical Propagation Delays for Receiver With Attenuator Test Circuit Shown in Figure 15

DEVICE	PARAMETERS	INPUT ATTENUATOR	TYPICAL (NS)
'107A SN75107B	t_{PLH}	1	20
		2	32
		3	42
	t_{PHL}	1	22
		2	31
		3	33
SN75108A	t_{PLH}	1	36
		2	47
		3	57
	t_{PHL}	1	29
		2	38
		3	41

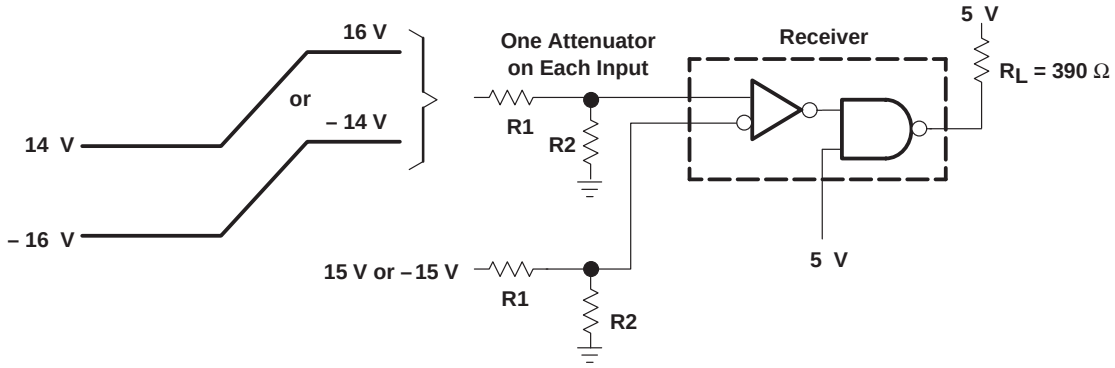
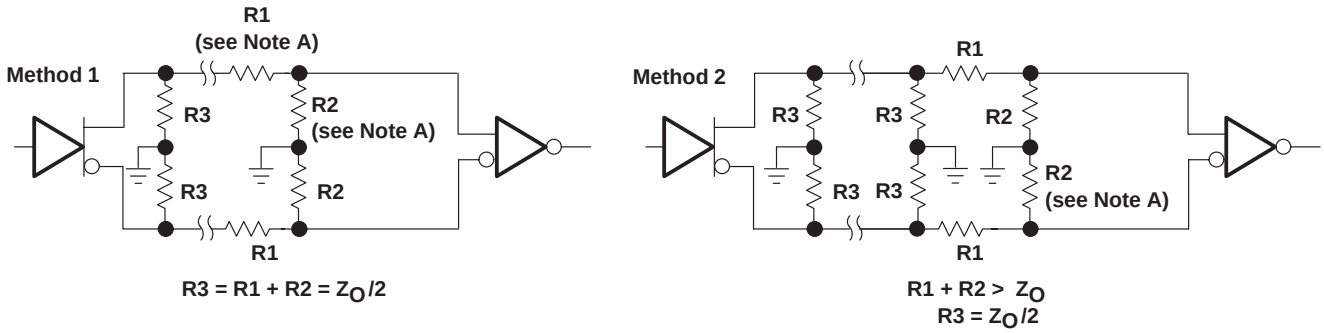


Figure 15. Common-Mode Circuit for Testing Input Attenuators With Results Shown in Table 2

Two methods of terminating a transmission line to reduce reflections are shown in Figure 16. The first method uses the resistors as the attenuation network and line termination. The second method uses two additional resistors for the line terminations.

APPLICATION INFORMATION



NOTE A: To minimize the loading, the values of R1 and R2 should be fairly large. Examples of possible values are shown in Table 1.

Figure 16. Termination Techniques

For party-line operation, method 2 should be used as shown in Figure 17.

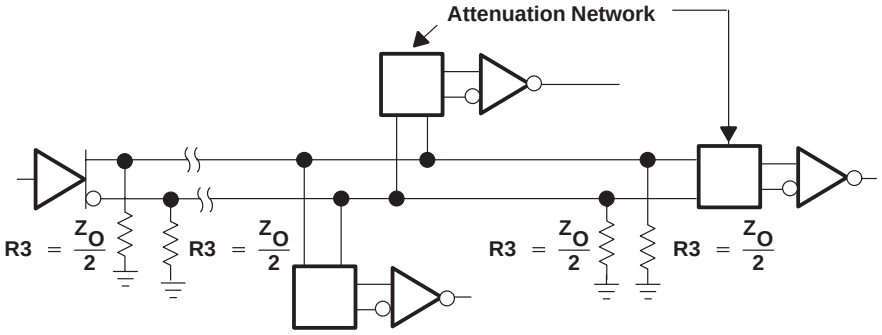


Figure 17. Party-Line Termination Technique

APPLICATION INFORMATION

furnace control using the SN75108A

The furnace control circuit in Figure 18 is an example of the possible use of the SN75108A series in areas other than what would normally be considered electronic systems. A description of the operation of this control follows. When the room temperature is below the desired level, the resistance of the room temperature sensor is high and channel 1 noninverting input is below (less positive than) the reference level set on the input differential amplifier. This situation causes a low output, operating the heat-on relay and turning on the heat. The channel 2 noninverting input is below the reference level when the bonnet temperature of the furnace reaches the desired level. This causes a low output, thus operating the blower relay. Normally the furnace is shut down when the room temperature reaches the desired level and the channel 1 output goes high, turning the heat off. The blower remains on as long as the bonnet temperature is high, even after the heat-on relay is off. There is also a safety switch in the bonnet that shuts down the furnace if the temperature there exceeds desired limits. The types of temperature-sensing devices and bias-resistor values used are determined by the particular operating conditions encountered.

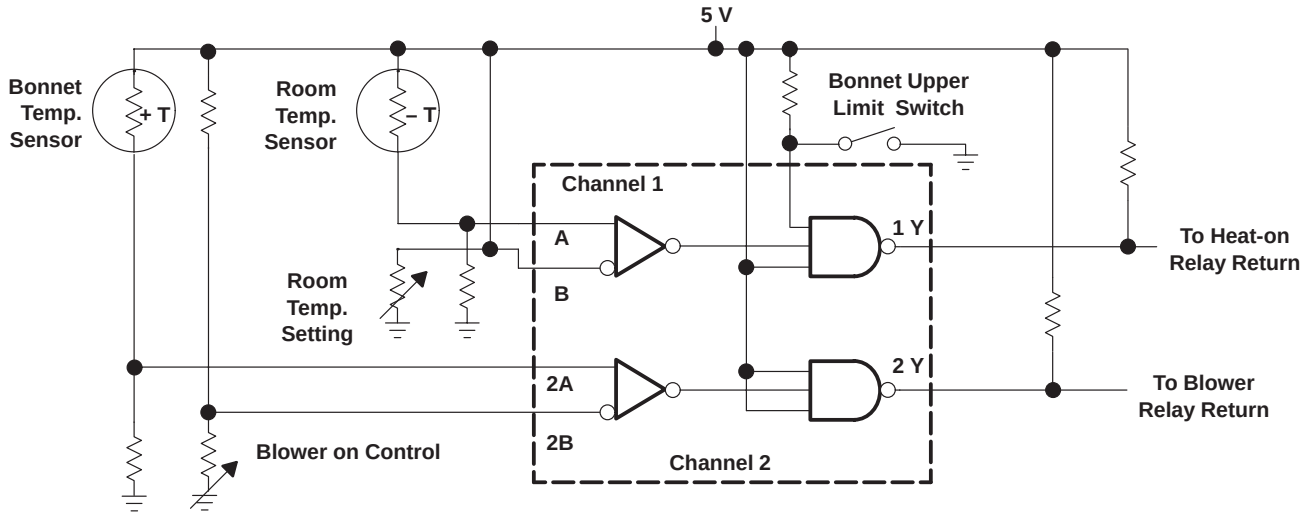


Figure 18. Furnace Control Using SN75108A

APPLICATION INFORMATION

repeaters for long lines

In some cases, the driven line may be so long that the noise level on the line reaches the common-mode limits or the attenuation becomes too large and results in poor reception. In such a case, a simple application of a receiver and a driver as repeaters [shown in Figure 19(a)] restores the signal level and allows an adequate signal level at the receiving end. If multichannel operation is desired, then proper gating for each channel must be sent through the repeater station using another repeater set as in Figure 19(b).

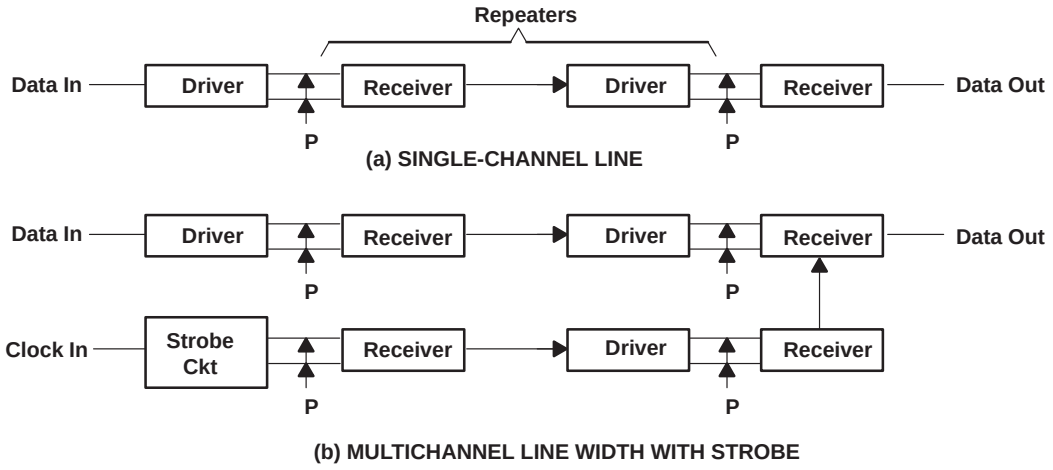


Figure 19. Receiver-Driver Repeaters

receiver as dual differential comparator

There are many applications for differential comparators, such as voltage comparison, threshold detection, controlled Schmitt triggering, and pulse-width control.

As a differential comparator, a ’107A or SN75108A can be connected to compare the noninverting input terminal with the inverting input as shown in Figure 20. The output is high or low, resulting from the A input being greater or less than the reference. The strobe inputs allow additional control over the circuit so that either output, or both, can be inhibited.

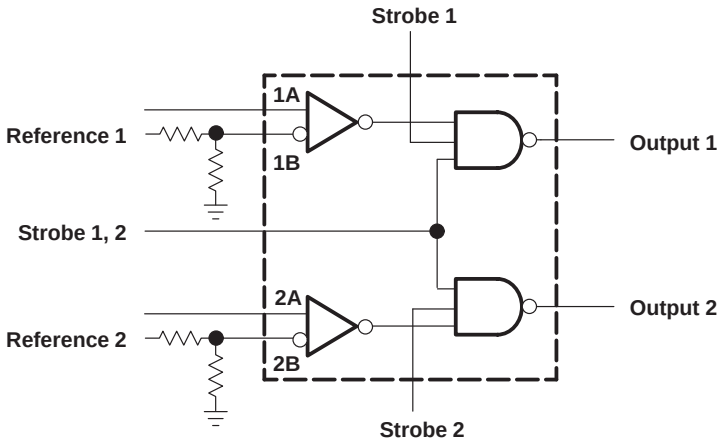
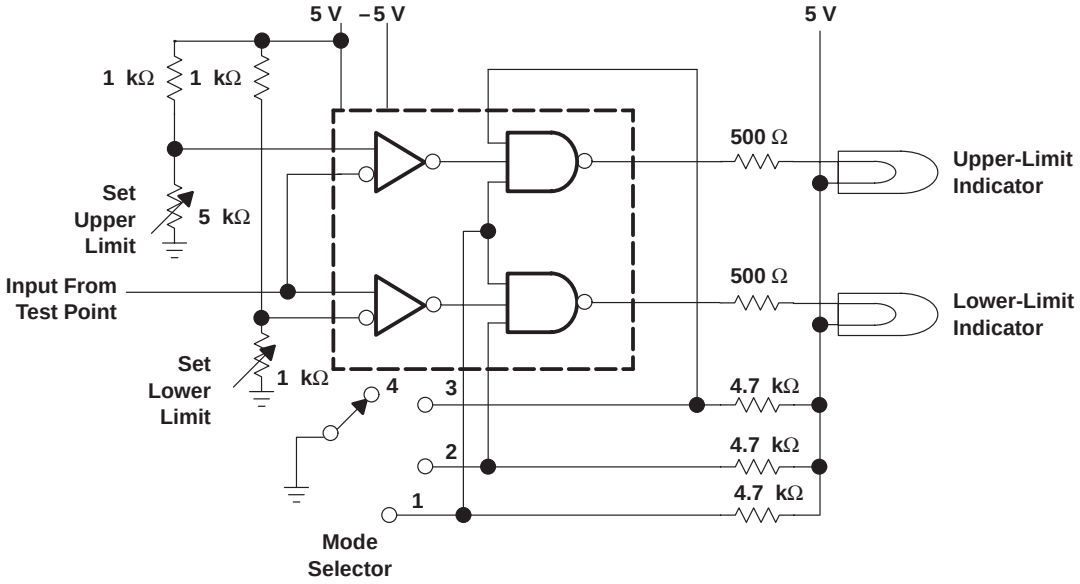


Figure 20. SN75107A Series Receiver as a Dual Differential Comparator

APPLICATION INFORMATION

window detector

The window detector circuit in Figure 21 has a large number of applications in test equipment and in determining upper limits, lower limits, or both at the same time, such as detecting whether a voltage or signal has exceeded its window limits. Illumination of the upper-limit (lower-limit) indicator shows that the input voltage is above (below) the selected upper (lower) limit. A mode selector is provided for selecting the desired test. For window detecting, the upper-and-lower-limits test position is used.



MODE SELECTOR LEGEND

POSITION	CONDITION
1	Off
2	Test for Upper Limit
3	Test for Lower Limit
4	Test for Upper and Lower Limits

Figure 21. Window Detector Using SN75108A

APPLICATION INFORMATION

temperature controller with zero-voltage switching

The circuit in Figure 22 switches an electric-resistive heater on or off by providing negative-going pulses to the gate of a triac during the time interval when the line voltage is passing through zero. The pulse generator is the 2N5447 and four diodes. This portion of the circuit provides negative-going pulses during the short time (approximately 100 μs) when the line voltage is near zero. These pulses are fed to the inverting input of one channel of the SN75108A. If the room temperature is below the desired level, the resistance of the thermistor is high and the noninverting input of channel 2 is above the reference level determined by the thermostat setting. This provides a high-level output from channel 2. This output is ANDed with the positive-going pulses from the output of channel 1, which are reinverted in the 2N5449.

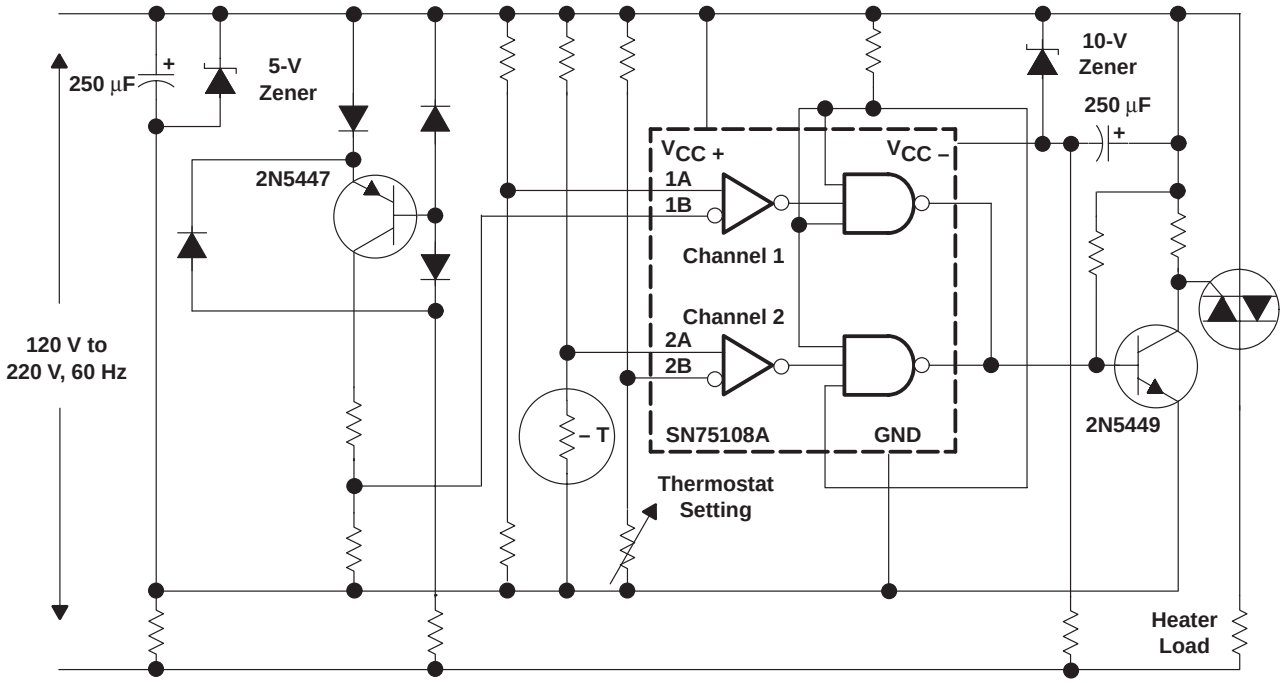


Figure 22. Zero-Voltage Switching Temperature Controller

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
5962-9690301Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
5962-9690301QCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	Level-NC-NC-NC
5962-9690301QDA	ACTIVE	CFP	W	14	1	TBD	A42 SNPB	Level-NC-NC-NC
JM38510/10401BCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	Level-NC-NC-NC
SN55107AJ	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	Level-NC-NC-NC
SN75107AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75107ADE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75107ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75107ADRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75107AN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN75107ANE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN75107ANSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75107ANSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75107BD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75107BDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75107BDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75107BDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75107BN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN75107BNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN75107BNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75107BNSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75108AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75108ADE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75108ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75108ADRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75108AN	OBSOLETE	PDIP	N	14		Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SNJ55107AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SNJ55107AJ	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	Level-NC-NC-NC
SNJ55107AW	ACTIVE	CFP	W	14	1	TBD	A42 SNPB	Level-NC-NC-NC

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

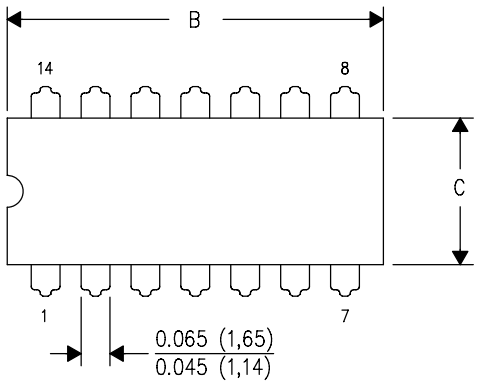
[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

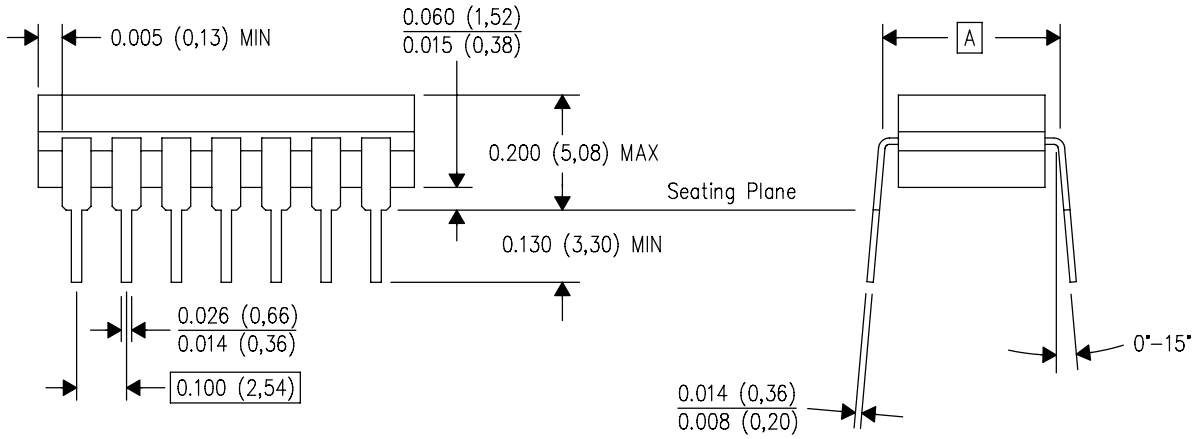
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



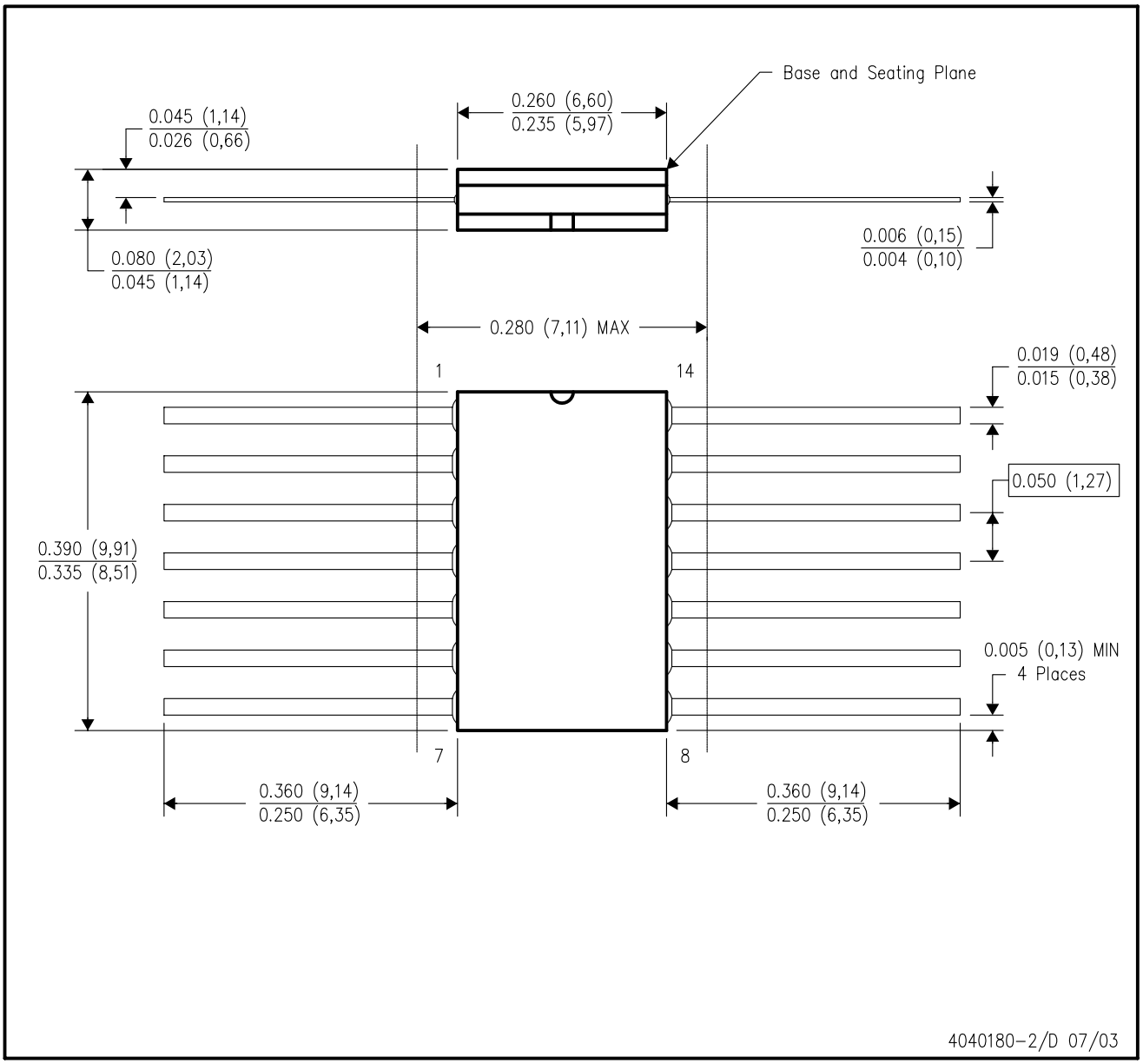
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

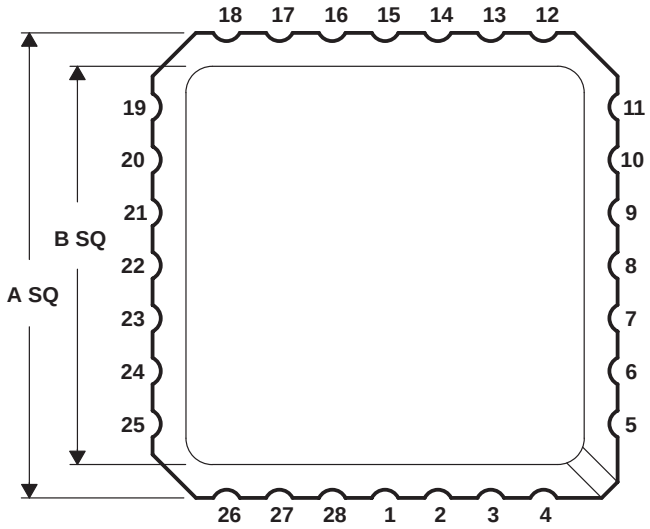
W (R–GDFP–F14) CERAMIC DUAL FLATPACK



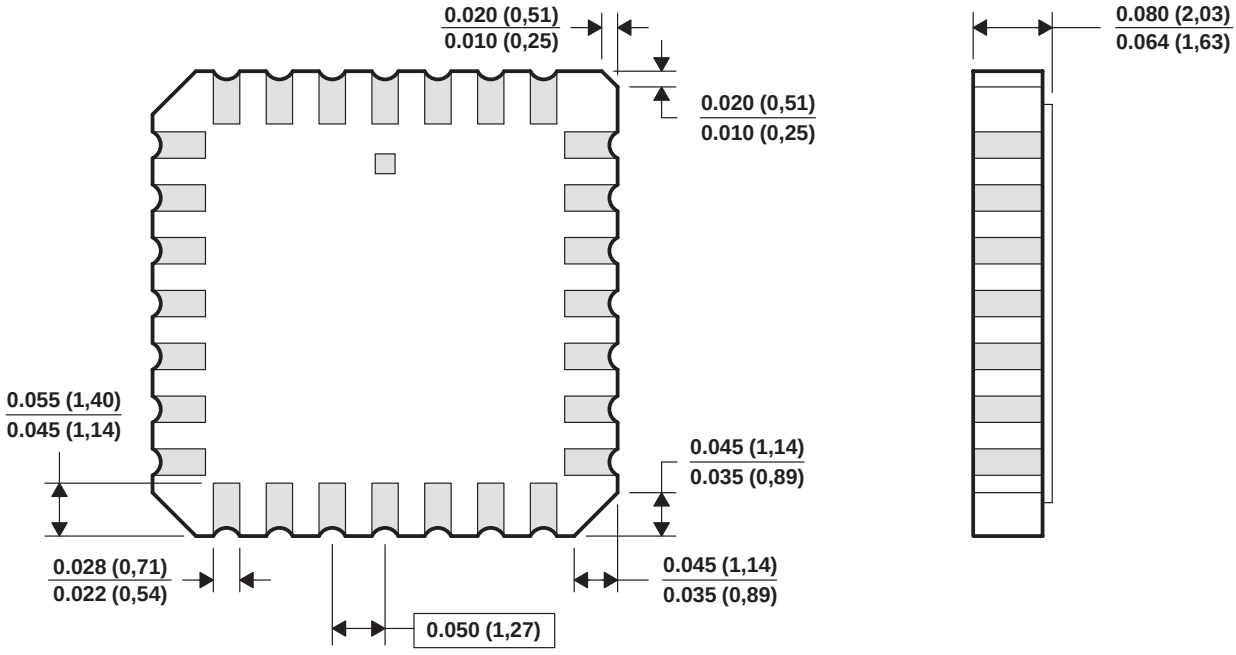
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14 and JEDEC MO–092AB

FK (S-CQCC-N)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



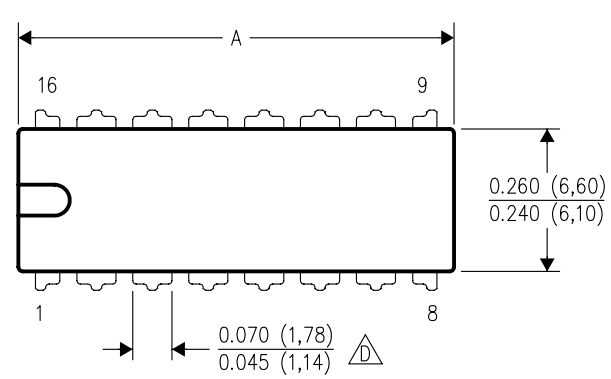
4040140/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

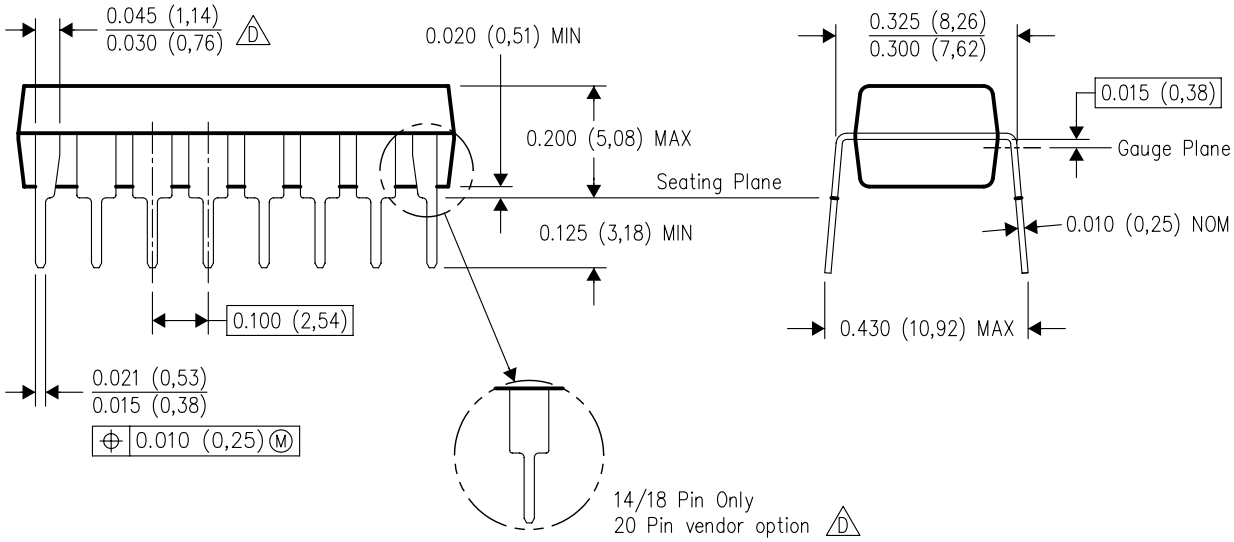
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.