

# SN55110A, SN75110A, SN75112 DUAL LINE DRIVERS

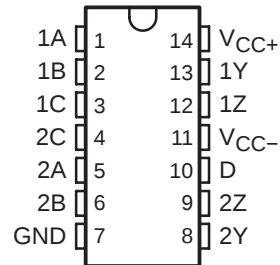
SLLS106G – DECEMBER 1975 – REVISED NOVEMBER 2004

- Improved Stability Over Supply Voltage and Temperature Ranges
- Constant-Current Outputs
- High Speed
- Standard Supply Voltages
- High Output Impedance
- High Common-Mode Output Voltage Range  
... -3 V to 10 V
- TTL-Input Compatibility
- Inhibitor Available for Driver Selection
- Glitch Free During Power Up/Power Down
- SN75112 and External Circuit Meets or Exceeds the Requirements of CCITT Recommendation V.35

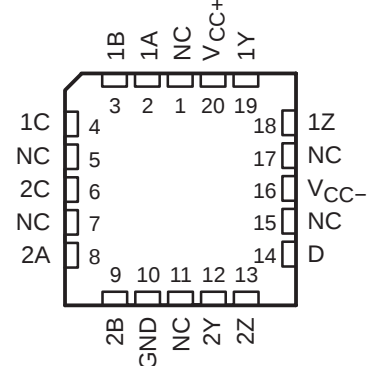
## description/ordering information

The SN55110A, SN75110A, and SN75112 dual line drivers have improved output current regulation with supply-voltage and temperature variations. In addition, the higher current of the SN75112 (27 mA) allows data to be transmitted over longer lines. These drivers offer optimum performance when used with the SN55107A, SN75107A, and SN75108A line receivers.

SN55110A ... J OR W PACKAGE  
SN75110A ... D, N, OR NS PACKAGE  
SN75112 ... D OR N PACKAGE  
(TOP VIEW)



SN55110A ... FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## ORDERING INFORMATION

| TA             | PACKAGE†  |              | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|-----------|--------------|-----------------------|------------------|
| 0°C to 70°C    | PDIP (N)  | Tube of 25   | SN75110AN             | SN75110AN        |
|                |           |              | SN75112N              | SN75112N         |
|                | SOIC (D)  | Tube of 50   | SN75110AD             | SN75110A         |
|                |           | Reel of 2500 | SN75110ADR            |                  |
|                |           | Tube of 50   | SN75112D              | SN75112          |
|                |           | Reel of 2500 | SN75112DR             |                  |
| -55°C to 125°C | SOP (NS)  | Reel of 2000 | SN75110ANSR           | SN75110A         |
|                | CDIP (J)  | Tube of 25   | SN55110AJ             | SN55110AJ        |
|                |           |              | SNJ55110AJ            | SNJ55110AJ       |
|                | CFP (W)   | Tube of 150  | SNJ55110AW            | SNJ55110AW       |
|                | LCCC (FK) | Tube of 55   | SNJ55110AFK           | SNJ55110AFK      |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# SN55110A, SN75110A, SN75112

## DUAL LINE DRIVERS

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### description/ordering information (continued)

These drivers feature independent channels with common voltage supply and ground terminals. The significant difference between the three drivers is in the output-current specification. The driver circuits feature a constant output current that is switched to either of two output terminals by the appropriate logic levels at the input terminals. The output current can be switched off (inhibited) by low logic levels on the enable inputs. The output current nominally is 12 mA for the '110A devices and is 27 mA for the SN75112.

The enable/inhibit feature is provided so the circuits can be used in party-line or data-bus applications. A strobe or inhibitor (enable D), common to both drivers, is included for increased driver-logic versatility. The output current in the inhibited mode,  $I_{O(off)}$ , is specified so that minimum line loading is induced when the driver is used in a party-line system with other drivers. The output impedance of the driver in the inhibited mode is very high. The output impedance of a transistor is biased to cutoff.

The driver outputs have a common-mode voltage range of  $-3\text{ V}$  to  $10\text{ V}$ , allowing common-mode voltage on the line without affecting driver performance.

All inputs are diode clamped and are designed to satisfy TTL-system requirements. The inputs are tested at  $2\text{ V}$  for high-logic-level input conditions and  $0.8\text{ V}$  for low-logic-level input conditions. These tests ensure  $400\text{-mV}$  noise margin when interfaced with TTL Series 54/74 devices.

The SN55110A is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN75110A and SN75112 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

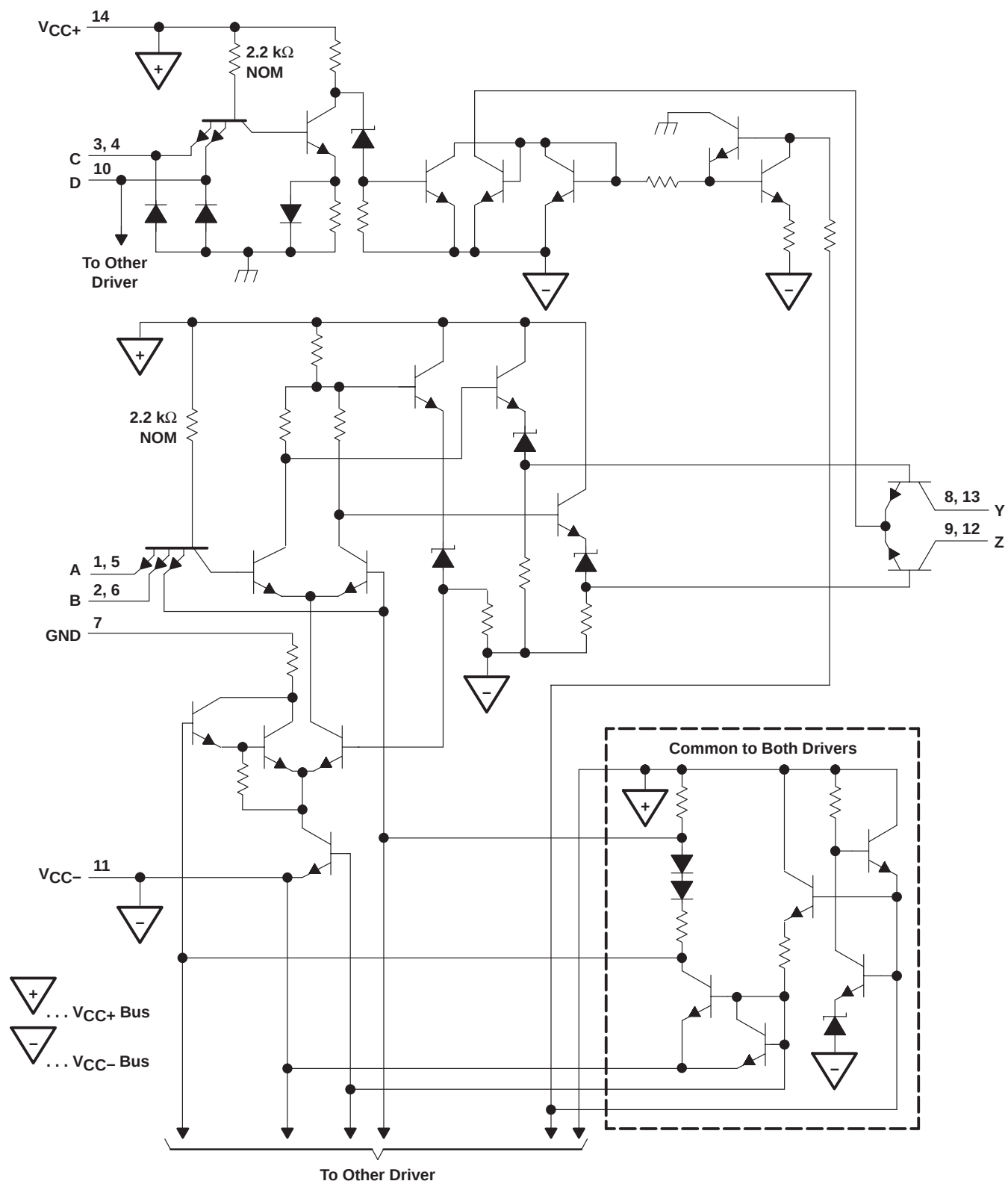
FUNCTION TABLE  
(each driver)

| LOGIC INPUTS |   | ENABLE INPUTS |   | OUTPUTS† |     |
|--------------|---|---------------|---|----------|-----|
| A            | B | C             | D | Y        | Z   |
| X            | X | L             | X | Off      | Off |
| X            | X | X             | L | Off      | Off |
| L            | X | H             | H | On       | Off |
| X            | L | H             | H | On       | Off |
| H            | H | H             | H | Off      | On  |

H = high level, L = low level, X = irrelevant

† When using only one channel of the line drivers, the other channel should be inhibited and/or have its outputs grounded.

## schematic (each driver)



Pin numbers shown are for the D, J, N, NS, and W packages.

# SN55110A, SN75110A, SN75112

## DUAL LINE DRIVERS

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### absolute maximum ratings over operating free-air temperature (unless otherwise noted)<sup>†</sup>

|                                                                              |                |
|------------------------------------------------------------------------------|----------------|
| Supply voltage: $V_{CC+}$ (see Note 1)                                       | 7 V            |
| $V_{CC-}$ (see Note 1)                                                       | –7 V           |
| Input voltage, $V_I$                                                         | 5.5 V          |
| Output voltage range, $V_O$                                                  | –5 V to 12 V   |
| Package thermal impedance, $\theta_{JA}$ (see Notes 2 and 3): D package      | 86°C/W         |
| N package                                                                    | 80°C/W         |
| NS package                                                                   | 76°C/W         |
| Package thermal impedance, $\theta_{JC}$ (see Notes 4 and 5): FK package     | 13.42°C/W      |
| J package                                                                    | 15.05°C/W      |
| W package                                                                    | 14.65°C/W      |
| Operating virtual junction temperature                                       | 150°C          |
| Case temperature for 60 seconds: FK package                                  | 260°C          |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or W package | 300°C          |
| Storage temperature range, $T_{stg}$                                         | –65°C to 150°C |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. Voltage values are with respect to network ground terminal.
  2. Maximum power dissipation is a function of  $T_J(\text{max})$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
  3. The package thermal impedance is calculated in accordance with JESD 51-7.
  4. Maximum power dissipation is a function of  $T_J(\text{max})$ ,  $\theta_{JC}$ , and  $T_C$ . The maximum allowable power dissipation at any allowable case temperature is  $P_D = (T_J(\text{max}) - T_C)/\theta_{JC}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
  5. The package thermal impedance is calculated in accordance with MIL-STD-883.

### recommended operating conditions (see Note 6)

|                                      | SN55110A |     |      | SN75110A<br>SN75112 |     |       | UNIT |
|--------------------------------------|----------|-----|------|---------------------|-----|-------|------|
|                                      | MIN      | NOM | MAX  | MIN                 | NOM | MAX   |      |
| $V_{CC+}$ Supply voltage             | 4.5      | 5   | 5.5  | 4.75                | 5   | 5.25  | V    |
| $V_{CC-}$ Supply voltage             | –4.5     | –5  | –5.5 | –4.75               | –5  | –5.25 | V    |
| Positive common-mode output voltage  | 0        |     | 10   | 0                   |     | 10    | V    |
| Negative common-mode output voltage  | 0        |     | –3   | 0                   |     | –3    | V    |
| $V_{IH}$ High-level input voltage    | 2        |     |      | 2                   |     |       | V    |
| $V_{IL}$ Low-level output voltage    |          |     | 0.8  |                     |     | 0.8   | V    |
| $T_A$ Operating free-air temperature | –55      |     | 125  | 0                   |     | 70    | °C   |

NOTE 6: When using only one channel of the line drivers, the other channel should be inhibited and/or have its outputs grounded.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER             |                                                            | TEST CONDITIONS <sup>†</sup>                                                      | SN55110A<br>SN75110A |                  |     | SN75112 |                  |     | UNIT |
|-----------------------|------------------------------------------------------------|-----------------------------------------------------------------------------------|----------------------|------------------|-----|---------|------------------|-----|------|
|                       |                                                            |                                                                                   | MIN                  | TYP <sup>‡</sup> | MAX | MIN     | TYP <sup>‡</sup> | MAX |      |
| V <sub>IK</sub>       | Input clamp voltage                                        | V <sub>CC±</sub> = MIN, I <sub>L</sub> = -12 mA                                   | -0.9                 | -1.5             |     | -0.9    | -1.5             |     | V    |
| I <sub>O(on)</sub>    | On-state output current                                    | V <sub>CC±</sub> = MAX, V <sub>O</sub> = 10 V                                     | 12                   | 15               |     | 27      | 40               |     | mA   |
|                       |                                                            | V <sub>CC</sub> = MIN to MAX, V <sub>O</sub> = -1 V to 1 V, T <sub>A</sub> = 25°C |                      |                  |     | 24      | 28               | 32  |      |
|                       |                                                            | V <sub>CC±</sub> = MIN, V <sub>O</sub> = -3 V                                     | 6.5                  | 12               |     | 15      | 27               |     |      |
| I <sub>O(off)</sub>   | Off-state output current                                   | V <sub>CC±</sub> = MIN, V <sub>O</sub> = 10 V                                     |                      |                  | 100 |         |                  | 100 | µA   |
| I <sub>I</sub>        | Input current at maximum input voltage                     | A, B, or C inputs                                                                 |                      |                  | 1   |         |                  | 1   | mA   |
|                       |                                                            | D input                                                                           |                      |                  | 2   |         |                  | 2   |      |
| I <sub>IH</sub>       | High-level input current                                   | A, B, or C inputs                                                                 |                      |                  | 40  |         |                  | 40  | µA   |
|                       |                                                            | D input                                                                           |                      |                  | 80  |         |                  | 80  |      |
| I <sub>IL</sub>       | Low-level input current                                    | A, B, or C inputs                                                                 |                      |                  | -3  |         |                  | -3  | mA   |
|                       |                                                            | D input                                                                           |                      |                  | -6  |         |                  | -6  |      |
| I <sub>CC+(on)</sub>  | Supply current from V <sub>CC</sub> with driver enabled    | V <sub>CC±</sub> = MAX, A and B inputs at 0.4 V, C and D inputs at 2 V            | 23                   | 35               |     | 25      | 40               |     | mA   |
| I <sub>CC-(on)</sub>  | Supply current from V <sub>CC-</sub> with driver enabled   | V <sub>CC±</sub> = MAX, A and B inputs at 0.4 V, C and D inputs at 2 V            | -34                  | -50              |     | -65     | -100             |     | mA   |
| I <sub>CC+(off)</sub> | Supply current from V <sub>CC-</sub> with driver inhibited | V <sub>CC±</sub> = MAX, A, B, C, and D inputs at 0.4 V                            | 21                   |                  |     | 30      |                  |     | mA   |
| I <sub>CC-(off)</sub> | Supply current from V <sub>CC±</sub> with driver inhibited | V <sub>CC±</sub> = MAX, A, B, C, and D inputs at 0.4 V                            | -17                  |                  |     | -32     |                  |     | mA   |

<sup>†</sup> For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.

<sup>‡</sup> All typical values are at V<sub>CC+</sub> = 5 V, V<sub>CC-</sub> = -5 V, T<sub>A</sub> = 25°C.

switching characteristics, V<sub>CC±</sub> = ±5 V, T<sub>A</sub> = 25°C (see Figure 1)

| PARAMETERS <sup>§</sup> | FROM<br>(INPUT) | TO<br>(OUTPUT) | TEST CONDITIONS                                |  | MIN | TYP | MAX | UNIT |
|-------------------------|-----------------|----------------|------------------------------------------------|--|-----|-----|-----|------|
| t <sub>PLH</sub>        | A or B          | Y or Z         | C <sub>L</sub> = 40 pF, R <sub>L</sub> = 50 Ω, |  |     | 9   | 15  | ns   |
| t <sub>PHL</sub>        |                 |                |                                                |  |     | 9   | 15  |      |
| t <sub>PLH</sub>        | C or D          | Y or Z         | C <sub>L</sub> = 40 pF, R <sub>L</sub> = 50 Ω, |  |     | 16  | 25  | ns   |
| t <sub>PHL</sub>        |                 |                |                                                |  |     | 13  | 25  |      |

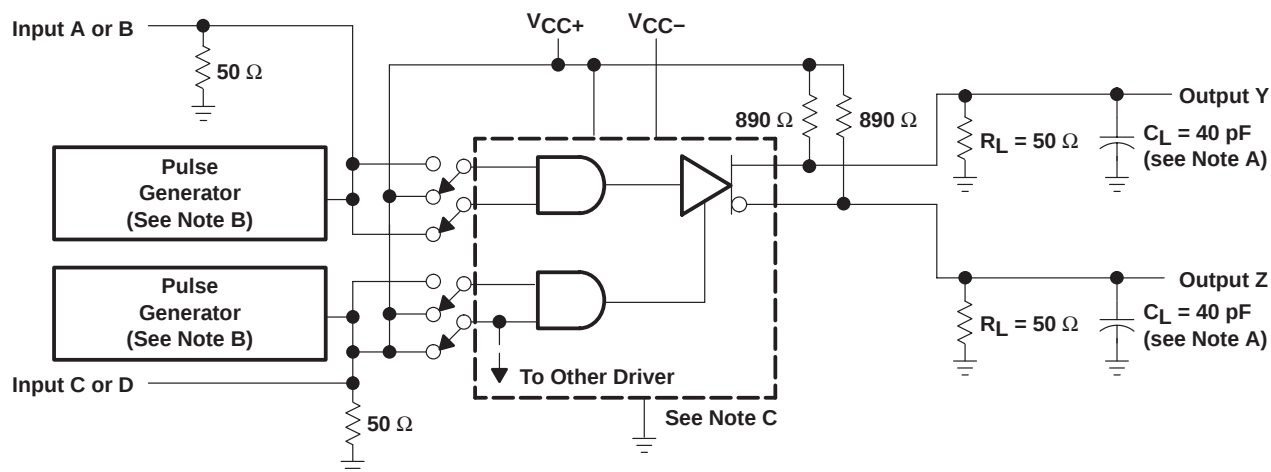
<sup>§</sup> t<sub>PLH</sub> = propagation delay time, low- to high-level output

t<sub>PHL</sub> = propagation delay time, high- to low-level output

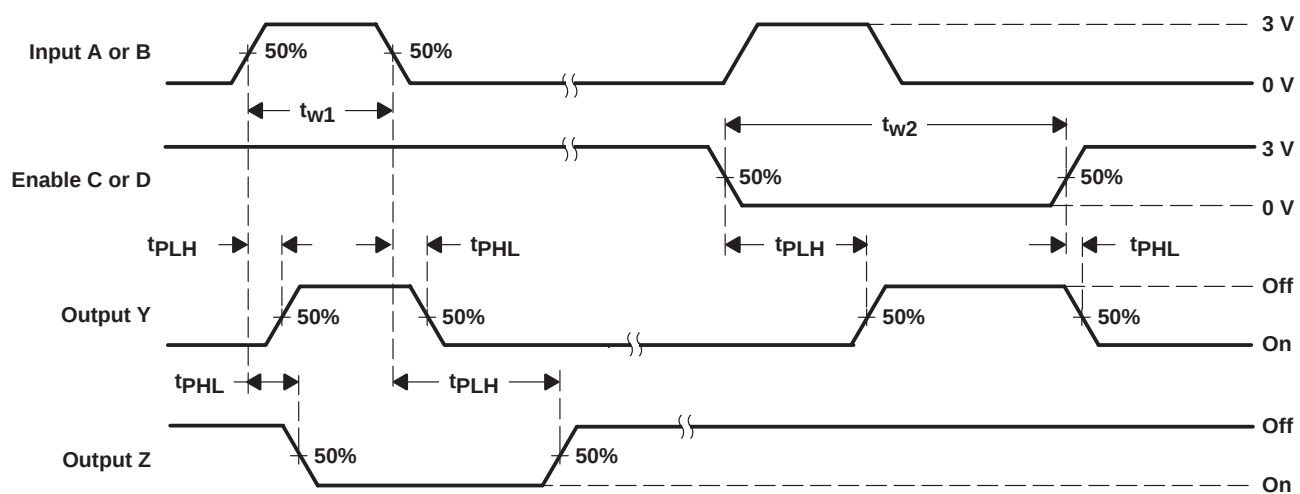
# SN55110A, SN75110A, SN75112 DUAL LINE DRIVERS

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## PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. The pulse generators have the following characteristics:  $Z_O = 50 \Omega$ ,  $t_r = t_f = 10 \pm 5 \text{ ns}$ ,  $t_{w1} = 500 \text{ ns}$ ,  $\text{PRR} \leq 1 \text{ MHz}$ ,  $t_{w2} = 1 \mu\text{s}$ ,  $\text{PRR} \leq 500 \text{ kHz}$ .
  - C. For simplicity, only one channel and the enable connections are shown.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

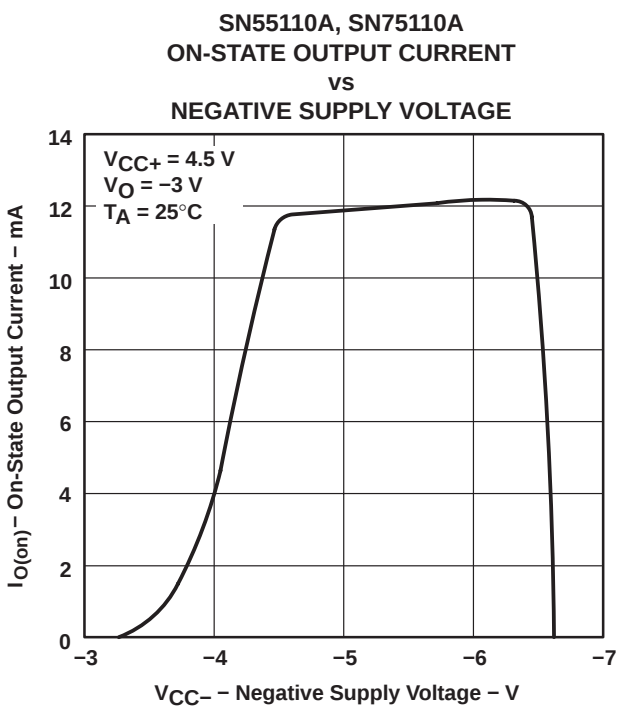


Figure 2

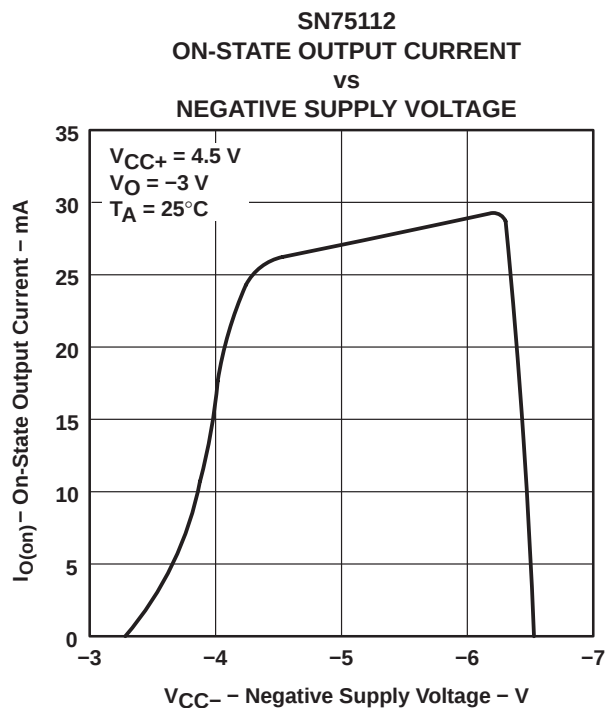


Figure 3

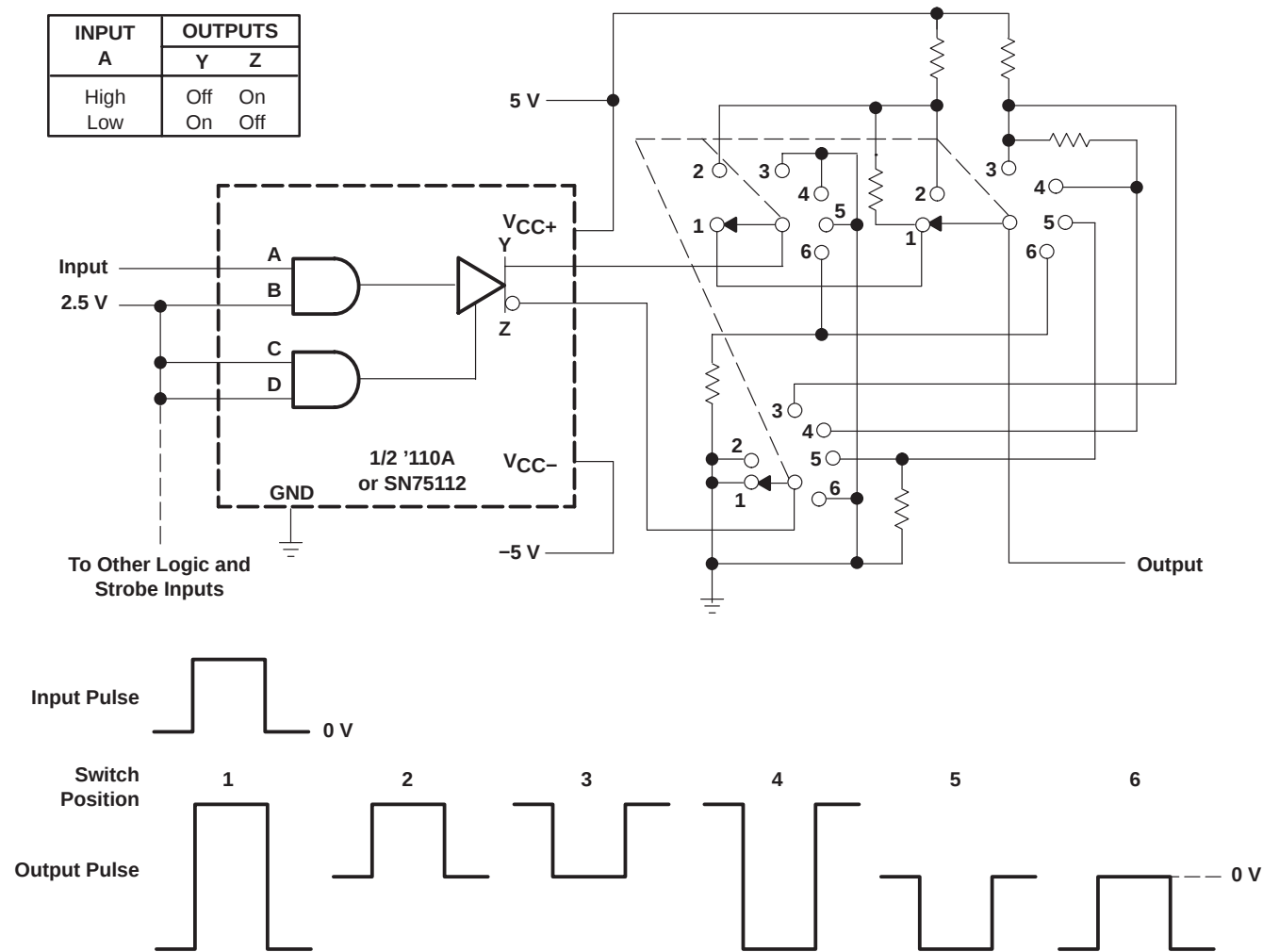
SN55110A, SN75110A, SN75112  
DUAL LINE DRIVERS

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APPLICATION INFORMATION

special pulse-control circuit

Figure 4 shows a circuit that can be used as a pulse-generator output or in many other testing applications.



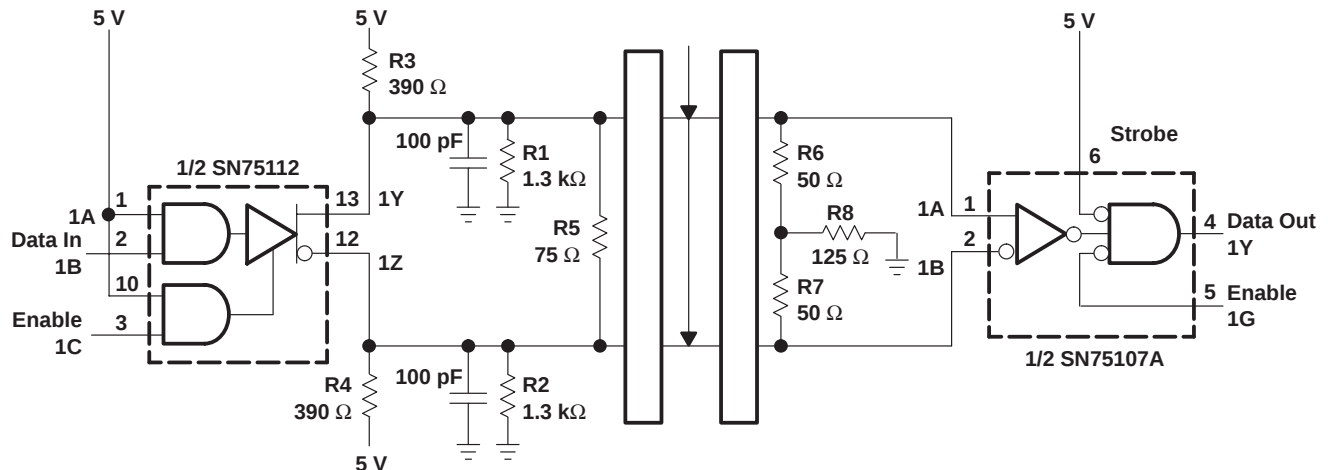
## using the SN75112 as a CCITT-recommended V.35 line driver

The SN75112 dual line driver, the SN75107A dual line receiver, and some external resistors can be used to implement the data-interchange circuit of CCITT recommendation V.35 (1976) modem specification. The circuit of one channel is shown in Figure 5 and meets the requirement of the interface as specified by Appendix 11 of CCITT V.35 and is summarized in Table 1 (V.35 has been replaced by ITU V.11).

### Table 1. CCITT V.35 Electrical Requirements

| GENERATOR                                    | MIN                        | MAX | UNIT     |
|----------------------------------------------|----------------------------|-----|----------|
| Source impedance, $Z_{\text{source}}$        | 50                         | 150 | $\Omega$ |
| Resistance to ground, R                      | 135                        | 165 | $\Omega$ |
| Differential output voltage, $V_{\text{OD}}$ | 440                        | 660 | mV       |
| 10% to 90% rise time, $t_r$                  | 40                         |     | ns       |
| or                                           | $0.01 \times ui^{\dagger}$ |     |          |
| Common-mode output voltage, $V_{\text{OC}}$  | -0.6                       | 0.6 | V        |
| LOAD (RECEIVER)                              | MIN                        | MAX | UNIT     |
| Input impedance, $Z_i$                       | 90                         | 110 | $\Omega$ |
| Resistance to ground, R                      | 135                        | 165 | $\Omega$ |

<sup>†</sup> ui = unit interval or minimum signal-element pulse duration



All resistors are 5%, 1/4 W.

**Figure 5. CCITT-Recommended V.35 Interface Using the SN75112 and SN75107A**

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup>    | Lead/<br>Ball Finish | MSL Peak Temp <sup>(3)</sup> | Samples<br>(Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|----------------------------|----------------------|------------------------------|-----------------------------|
| 5962-87547012A   | ACTIVE                | LCCC         | FK              | 20   | 1           | TBD                        | Call TI              | Call TI                      |                             |
| 5962-8754701CA   | ACTIVE                | CDIP         | J               | 14   | 1           | TBD                        | Call TI              | Call TI                      |                             |
| 5962-8754701DA   | ACTIVE                | CFP          | W               | 14   | 1           | TBD                        | Call TI              | Call TI                      |                             |
| SN55110AJ        | ACTIVE                | CDIP         | J               | 14   | 1           | TBD                        | A42                  | N / A for Pkg Type           |                             |
| SN75110AD        | ACTIVE                | SOIC         | D               | 14   | 50          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| SN75110ADE4      | ACTIVE                | SOIC         | D               | 14   | 50          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| SN75110ADG4      | ACTIVE                | SOIC         | D               | 14   | 50          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| SN75110ADR       | ACTIVE                | SOIC         | D               | 14   | 2500        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| SN75110ADRE4     | ACTIVE                | SOIC         | D               | 14   | 2500        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| SN75110ADRG4     | ACTIVE                | SOIC         | D               | 14   | 2500        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| SN75110AJ        | OBSOLETE              | CDIP         | J               | 14   |             | TBD                        | Call TI              | Call TI                      |                             |
| SN75110AN        | ACTIVE                | PDIP         | N               | 14   | 25          | Pb-Free (RoHS)             | CU NIPDAU            | N / A for Pkg Type           |                             |
| SN75110ANE4      | ACTIVE                | PDIP         | N               | 14   | 25          | Pb-Free (RoHS)             | CU NIPDAU            | N / A for Pkg Type           |                             |
| SN75110ANSR      | ACTIVE                | SO           | NS              | 14   | 2000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| SN75110ANSRE4    | ACTIVE                | SO           | NS              | 14   | 2000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| SN75110ANSRG4    | ACTIVE                | SO           | NS              | 14   | 2000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| SN75112D         | ACTIVE                | SOIC         | D               | 14   | 50          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| SN75112DE4       | ACTIVE                | SOIC         | D               | 14   | 50          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| SN75112DG4       | ACTIVE                | SOIC         | D               | 14   | 50          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| SN75112DR        | ACTIVE                | SOIC         | D               | 14   | 2500        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/ Ball Finish | MSL Peak Temp <sup>(3)</sup> | Samples (Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|-------------------|------------------------------|--------------------------|
| SN75112DRE4      | ACTIVE                | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU         | Level-1-260C-UNLIM           |                          |
| SN75112DRG4      | ACTIVE                | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU         | Level-1-260C-UNLIM           |                          |
| SN75112N         | ACTIVE                | PDIP         | N               | 14   | 25          | Pb-Free (RoHS)          | CU NIPDAU         | N / A for Pkg Type           |                          |
| SN75112NE4       | ACTIVE                | PDIP         | N               | 14   | 25          | Pb-Free (RoHS)          | CU NIPDAU         | N / A for Pkg Type           |                          |
| SNJ55110AFK      | ACTIVE                | LCCC         | FK              | 20   | 1           | TBD                     | POST-PLATE        | N / A for Pkg Type           |                          |
| SNJ55110AJ       | ACTIVE                | CDIP         | J               | 14   | 1           | TBD                     | A42               | N / A for Pkg Type           |                          |
| SNJ55110AW       | ACTIVE                | CFP          | W               | 14   | 1           | TBD                     | A42               | N / A for Pkg Type           |                          |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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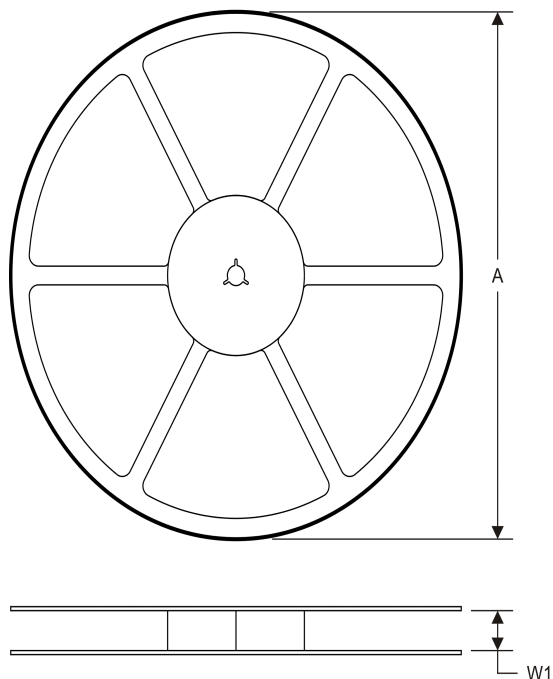
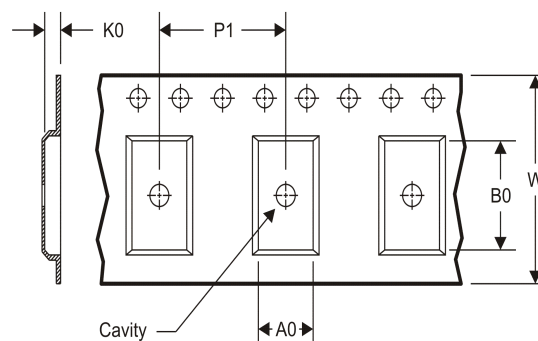
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**OTHER QUALIFIED VERSIONS OF SN55110A, SN75110A :**

- Catalog: [SN75110A](#)
- Military: [SN55110A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


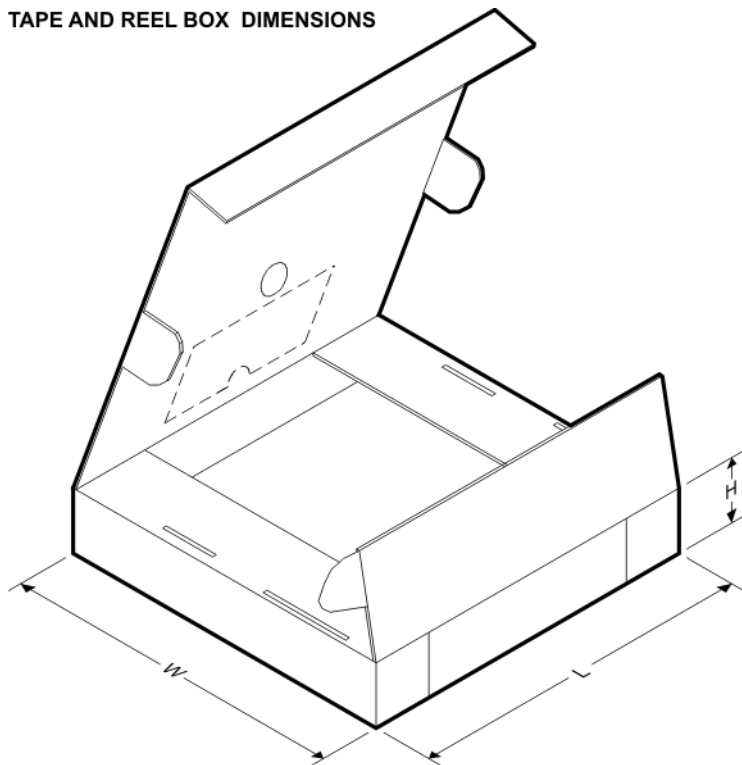
|    |                                                           |
|----|-----------------------------------------------------------|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN75110ADR  | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN75110ADR  | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN75110ANSR | SO           | NS              | 14   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |
| SN75112DR   | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



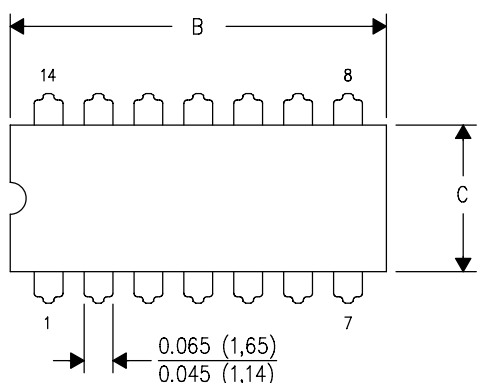
\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN75110ADR  | SOIC         | D               | 14   | 2500 | 333.2       | 345.9      | 28.6        |
| SN75110ADR  | SOIC         | D               | 14   | 2500 | 367.0       | 367.0      | 38.0        |
| SN75110ANSR | SO           | NS              | 14   | 2000 | 367.0       | 367.0      | 38.0        |
| SN75112DR   | SOIC         | D               | 14   | 2500 | 367.0       | 367.0      | 38.0        |

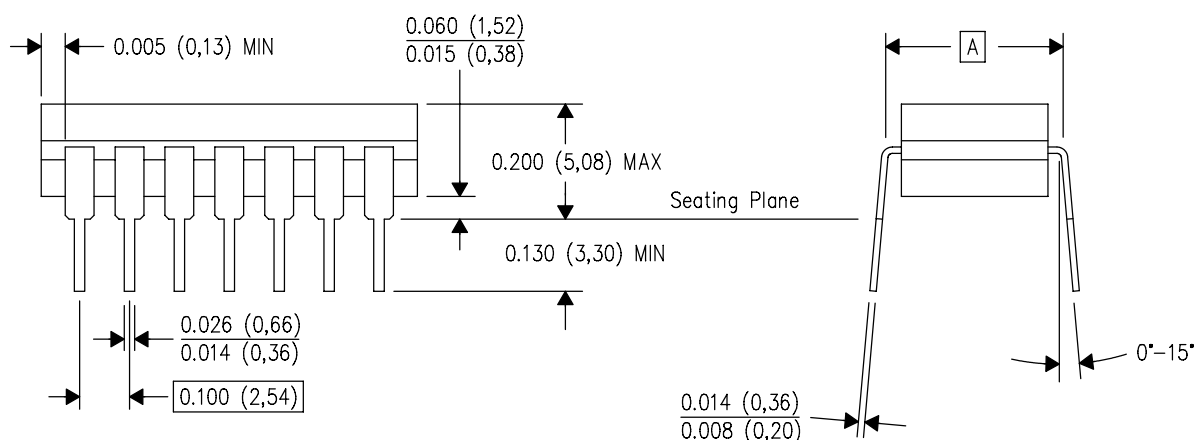
J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |

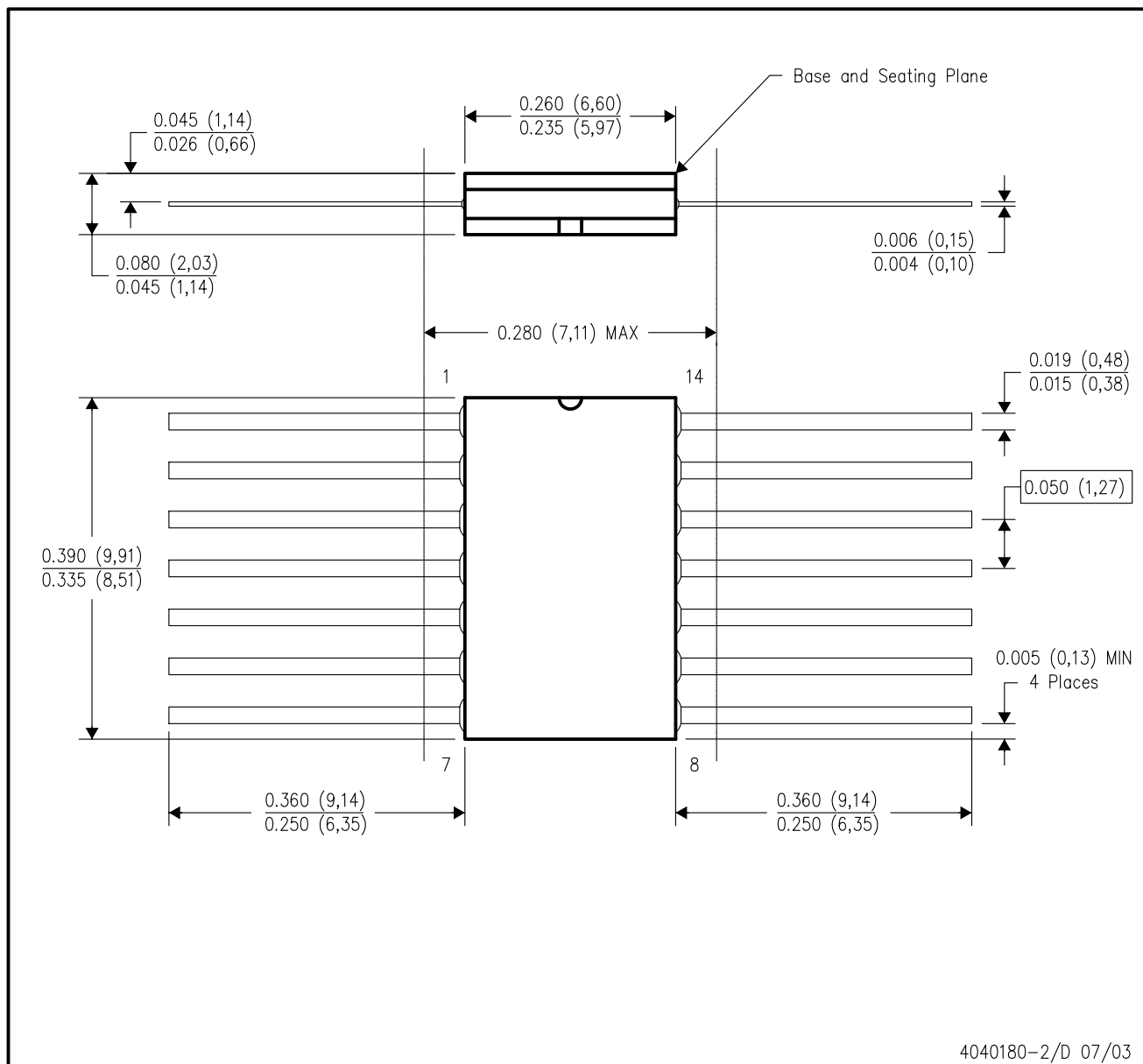


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK

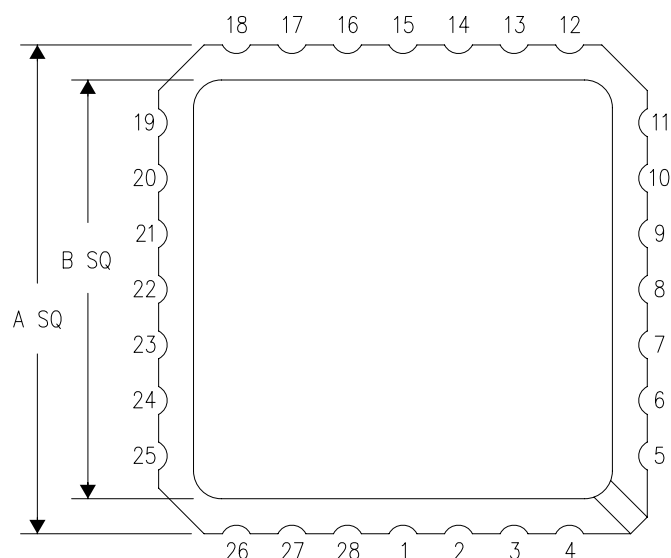


- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only.
  - Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

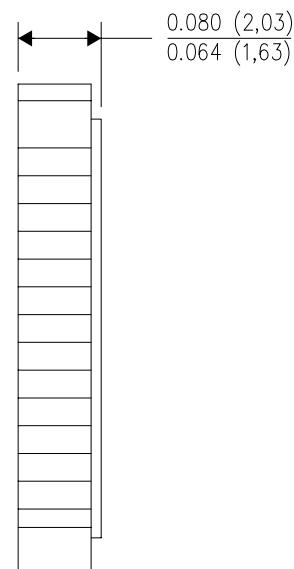
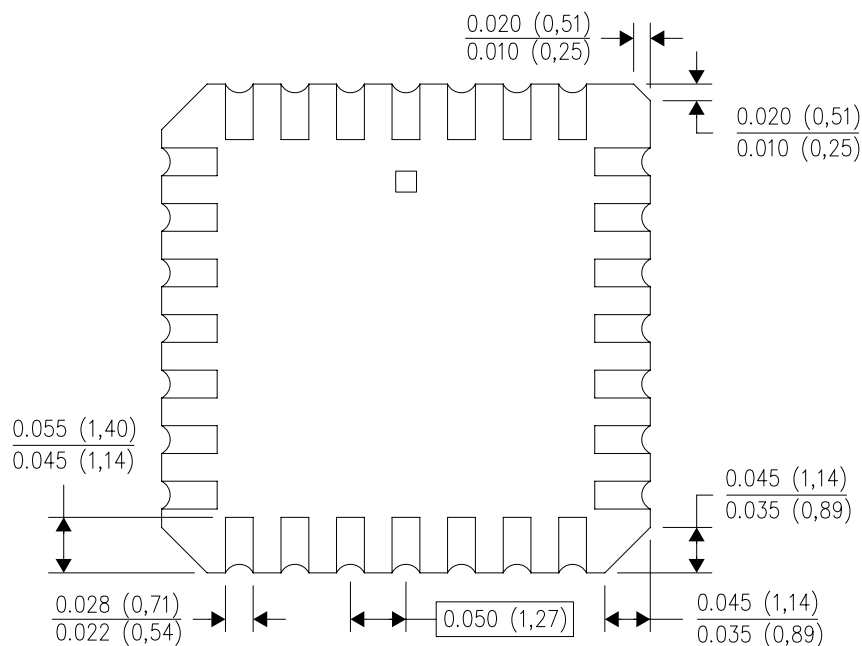
FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF<br>TERMINALS<br>** | A                |                  | B                |                  |
|---------------------------|------------------|------------------|------------------|------------------|
|                           | MIN              | MAX              | MIN              | MAX              |
| 20                        | 0.342<br>(8,69)  | 0.358<br>(9,09)  | 0.307<br>(7,80)  | 0.358<br>(9,09)  |
| 28                        | 0.442<br>(11,23) | 0.458<br>(11,63) | 0.406<br>(10,31) | 0.458<br>(11,63) |
| 44                        | 0.640<br>(16,26) | 0.660<br>(16,76) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 52                        | 0.740<br>(18,78) | 0.761<br>(19,32) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 68                        | 0.938<br>(23,83) | 0.962<br>(24,43) | 0.850<br>(21,6)  | 0.858<br>(21,8)  |
| 84                        | 1.141<br>(28,99) | 1.165<br>(29,59) | 1.047<br>(26,6)  | 1.063<br>(27,0)  |



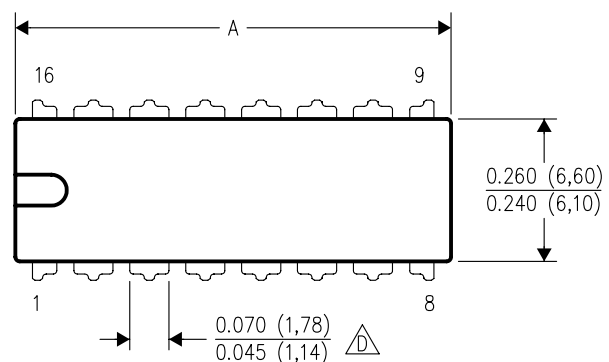
4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

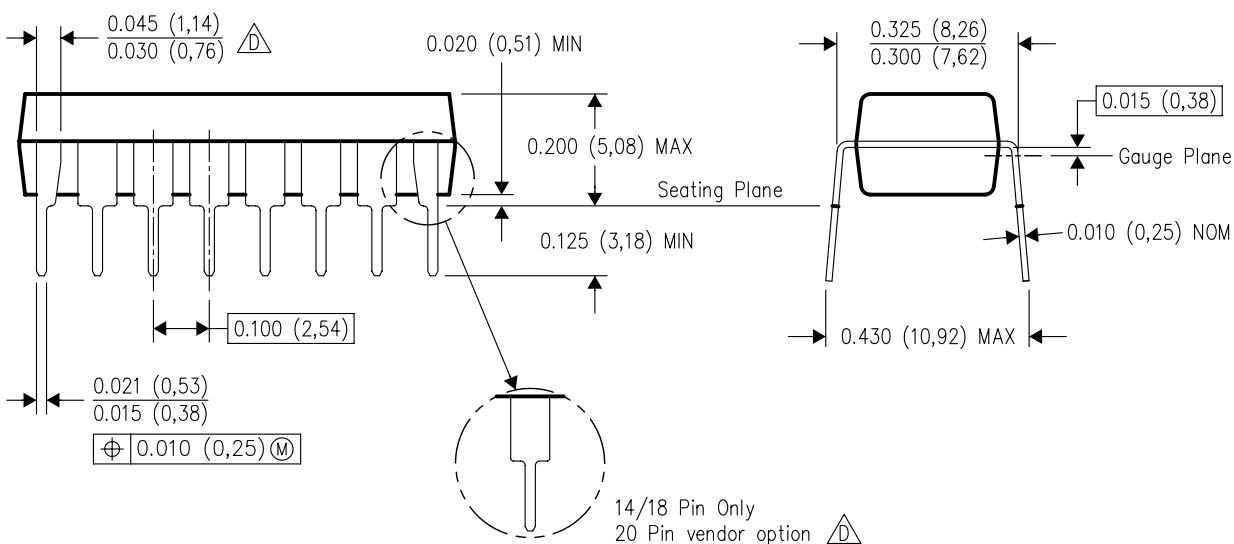
N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **<br>DIM      | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



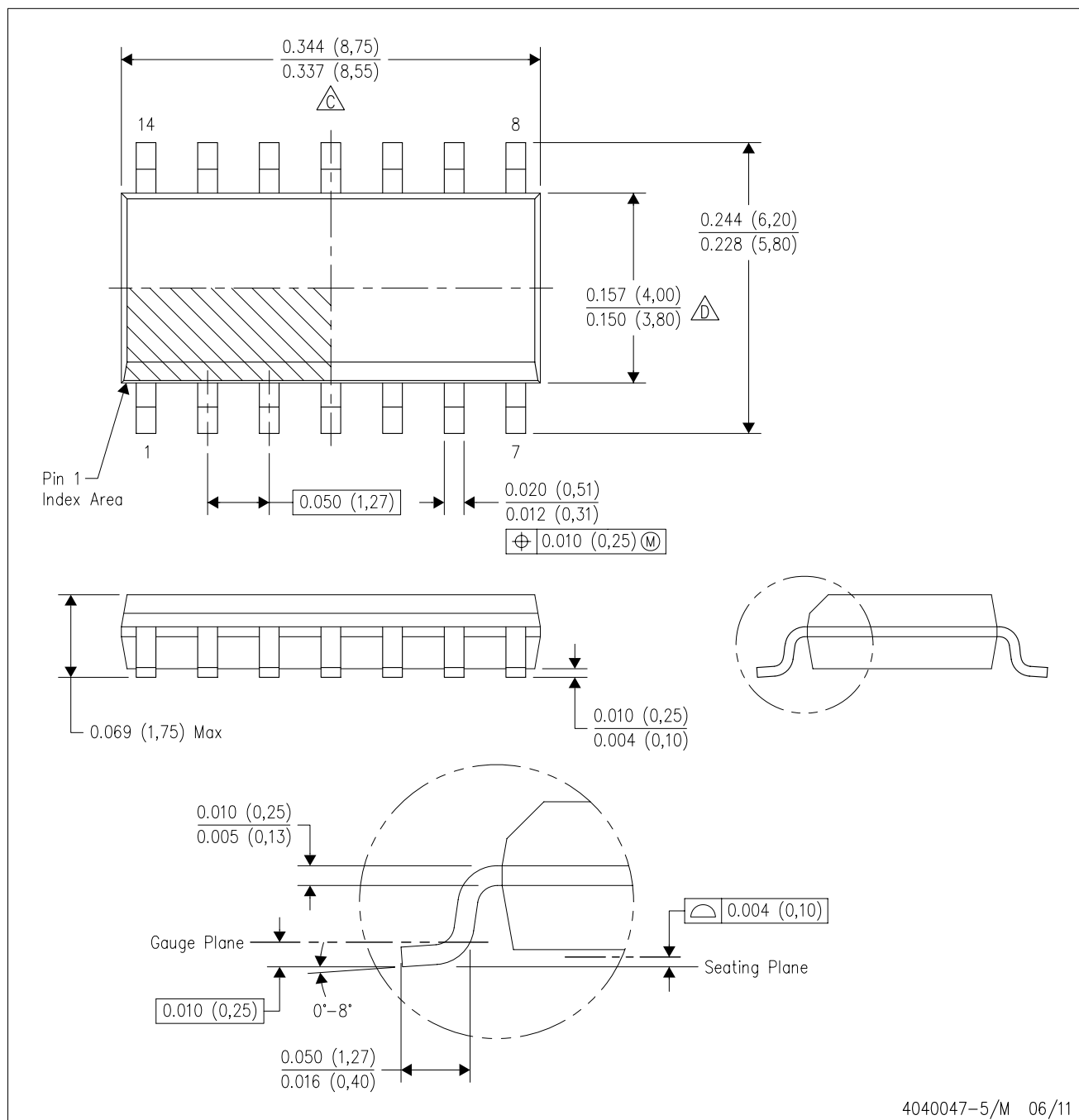
4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



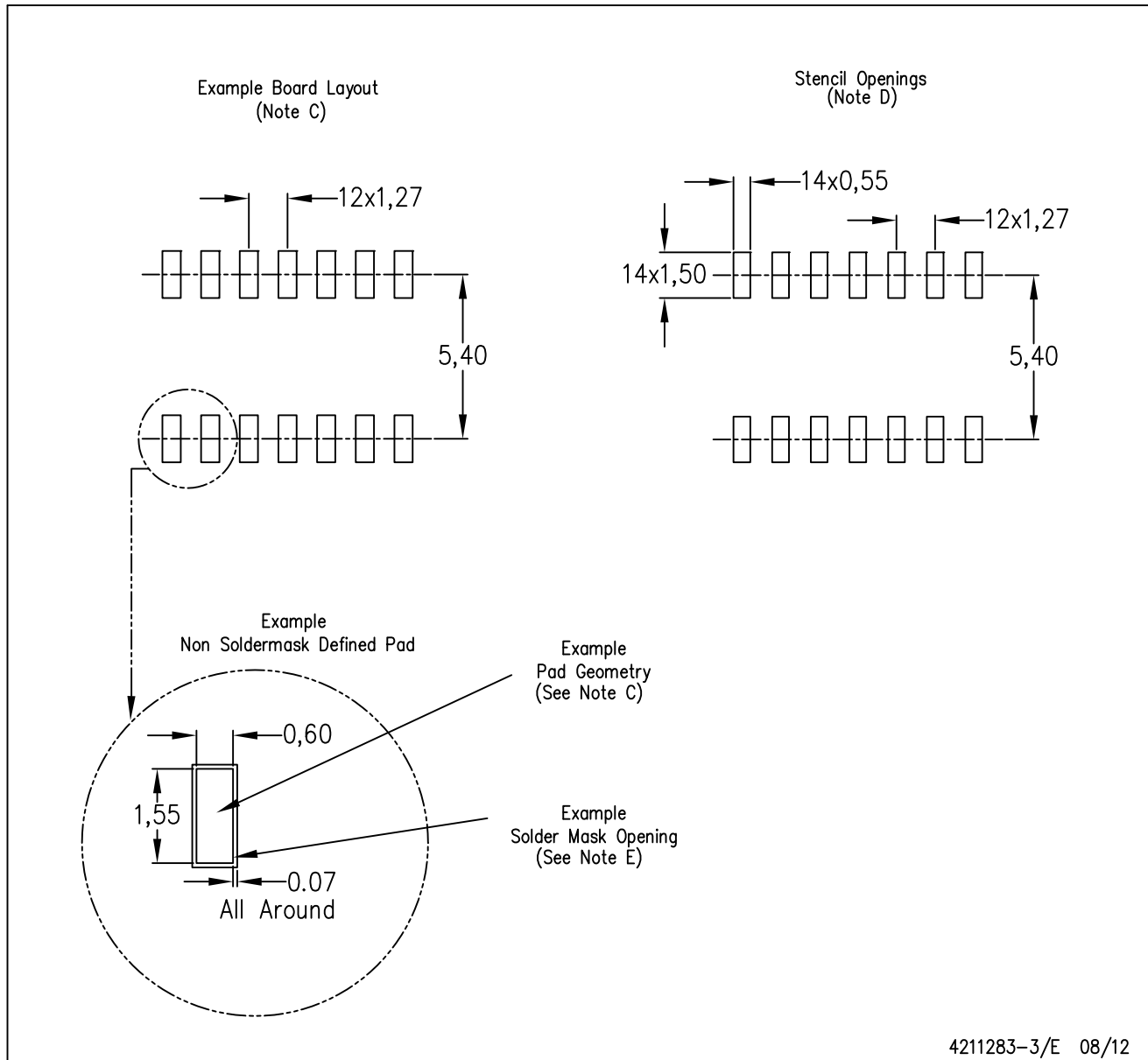
4040047-5/M 06/11

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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