

SN55182, SN75182 DUAL DIFFERENTIAL LINE RECEIVERS

SLLS092D – OCTOBER 1972 – REVISED APRIL 1998

- Single 5-V Supply
- Differential Line Operation
- Dual Channels
- TTL Compatibility
- ± 15 -V Common-Mode Input Voltage Range
- ± 15 -V Differential Input Voltage Range
- Individual Channel Strobes
- Built-In Optional Line-Termination Resistor
- Individual Frequency Response Controls
- Designed for Use With Dual Differential Drivers SN55183 and SN75183
- Designed to Be Interchangeable With National Semiconductor DS7820A and DS8820A

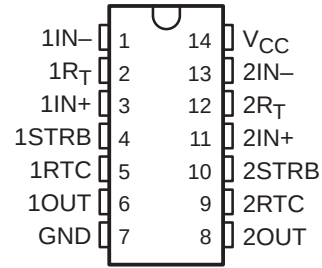
description

The SN55182 and SN75182 dual differential line receivers are designed to sense small differential signals in the presence of large common-mode noise. These devices give TTL-compatible output signals as a function of the polarity of the differential input voltage. The frequency response of each channel can be easily controlled by a single external capacitor to provide immunity to differential noise spikes. The output goes to a high level when the inputs are open circuited. A strobe input (STRB) is provided that, when in the low level, disables the receiver and forces the output to a high level.

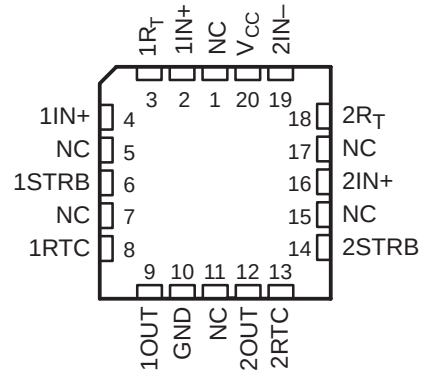
The receiver is of monolithic single-chip construction, and both halves of the dual circuits use common power-supply and ground terminals.

The SN55182 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN75182 is characterized for operation from 0°C to 70°C .

SN55182 . . . J OR W PACKAGE
SN75182 . . . N PACKAGE
(TOP VIEW)



SN55182 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

**THE SN55182 IS NOT RECOMMENDED
FOR NEW DESIGNS**

FUNCTION TABLE

INPUTS		OUTPUT OUT
STRB	V_{ID}	
L	X	H
H	H	H
H	L	L

H = $V_I \geq V_{IH}$ min or V_{ID} more positive than V_{TH} max
L = $V_I \leq V_{IL}$ max or V_{ID} more negative than V_{TL} max
X = irrelevant



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

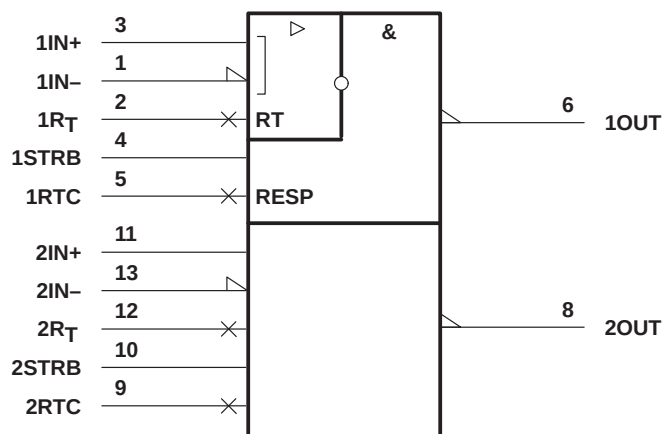
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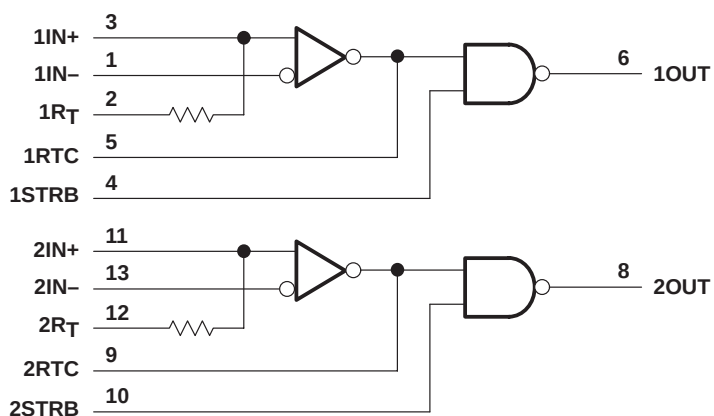
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the J, N, and W packages.

logic diagram (positive logic)

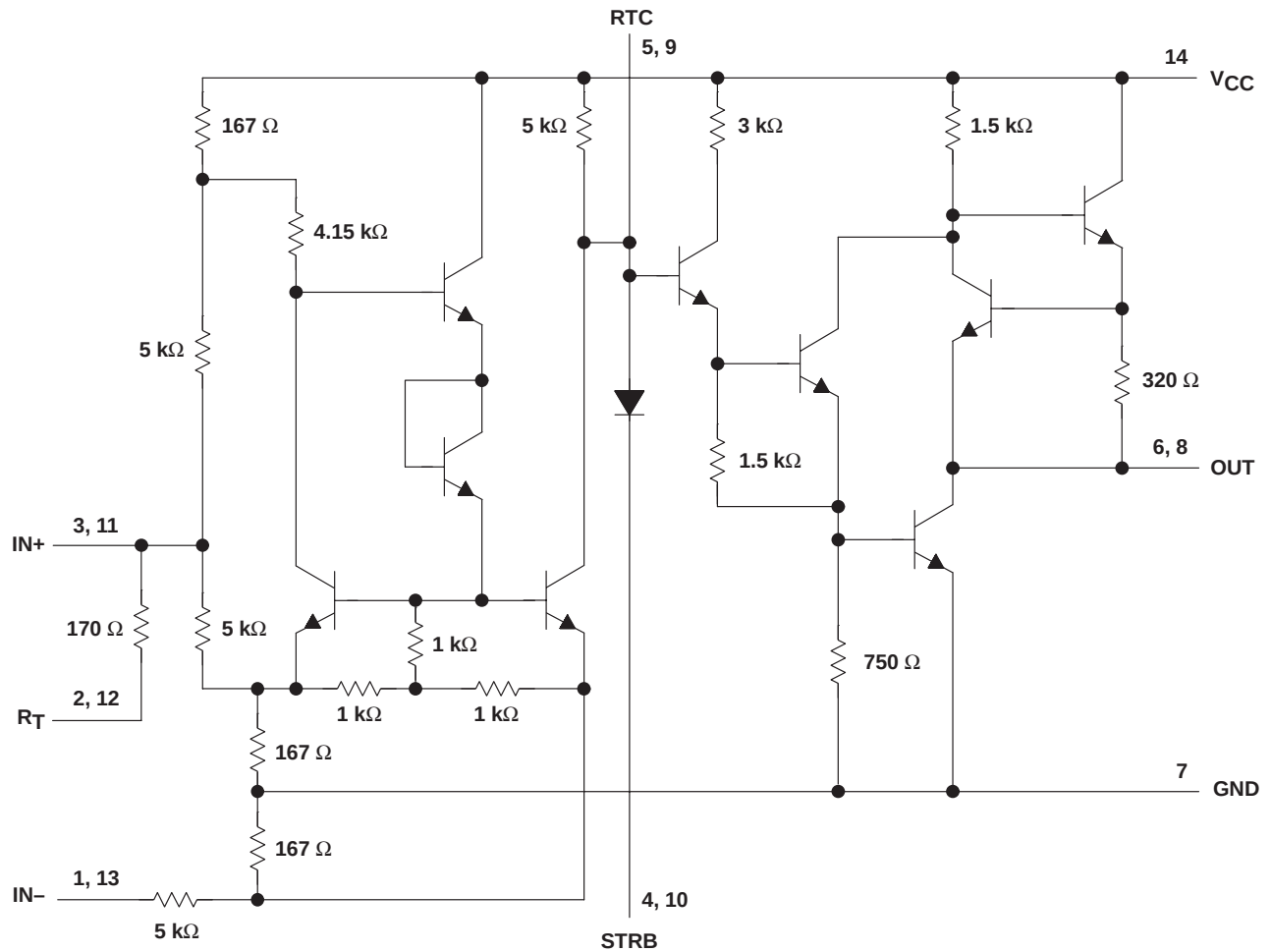


Pin numbers shown are for the J, N, and W packages.

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schematic (each receiver)



Resistor values shown are nominal.
Pin numbers shown are for the J, N, and W packages.

SN55182, SN75182

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC} (see Note 1)	8 V
Common-mode input voltage, V_{IC}	± 20 V
Differential input voltage, V_{ID} (see Note 2)	± 20 V
Strobe input voltage, $V_{I(STRB)}$	8 V
Output sink current	50 mA
Continuous total power dissipation	See Dissipation Rating Table
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or W package	300°C
Case temperature for 60 seconds, T_C : FK package	260°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltage values are at the noninverting terminal with respect to the inverting terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^{\circ}\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^{\circ}\text{C}$	$T_A = 70^{\circ}\text{C}$ POWER RATING	$T_A = 125^{\circ}\text{C}$ POWER RATING
FK [‡]	1375 mW	11.0 mW/ $^{\circ}\text{C}$	880 mW	275 mW
J [‡]	1375 mW	11.0 mW/ $^{\circ}\text{C}$	880 mW	275 mW
N	1150 mW	9.2 mW/ $^{\circ}\text{C}$	736 mW	—
W [‡]	1000 mW	8.0 mW/ $^{\circ}\text{C}$	640 mW	200 mW

[‡] In the FK, J, and W packages, SN55182 chips are alloy mounted.

recommended operating conditions

	SN55182			SN75182			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
Common-mode input voltage, V_{IC}			± 15			± 15	V
High-level strobe input voltage, $V_{IH(STRB)}$	2.1		5.5	2.1		5.5	V
Low-level strobe input voltage, $V_{IL(STRB)}$	0		0.9	0		0.9	V
High-level output current, I_{OH}			–400			–400	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	–55		125	0		70	$^{\circ}\text{C}$



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electrical characteristics over recommended ranges of V_{CC} , V_{IC} , and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS [†]		MIN	TYP [‡]	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	$V_O = 2.5\text{ V}$, $I_{OH} = -400\text{ }\mu\text{A}$	$V_{IC} = -3\text{ V to }3\text{ V}$ $V_{IC} = -15\text{ V to }15\text{ V}$		0.5 1		V
V_{IT-}	Negative-going input threshold voltage	$V_O = 0.4\text{ V}$, $I_{OL} = 16\text{ mA}$	$V_{IC} = -3\text{ V to }3\text{ V}$ $V_{IC} = -15\text{ V to }15\text{ V}$		-0.5 -1		V
V_{OH}	High-level output voltage	$V_{ID} = 1\text{ V}$, $V(\text{STRB}) = 2.1\text{ V}$, $I_{OH} = -400\text{ }\mu\text{A}$		2.5	4.2	5.5	V
		$V_{ID} = -1\text{ V}$, $V(\text{STRB}) = 0.4\text{ V}$, $I_{OH} = -400\text{ }\mu\text{A}$		2.5	4.2	5.5	
V_{OL}	Low-level output voltage	$V_{ID} = -1\text{ V}$, $V(\text{STRB}) = 2.1\text{ V}$, $I_{OL} = 16\text{ mA}$		0.25	0.4		V
I_I	Inverting input	$V_{IC} = 15\text{ V}$		3	4.2		mA
		$V_{IC} = 0$		0	-0.5		
		$V_{IC} = -15\text{ V}$		-3	-4.2		
	Noninverting input	$V_{IC} = 15\text{ V}$		5	7		
		$V_{IC} = 0$		-1	-1.4		
		$V_{IC} = -15\text{ V}$		-7	-9.8		
$I_{IH}(\text{STRB})$	High-level strobe input current	$V(\text{STRB}) = 5.5\text{ V}$			5		μA
$I_{IL}(\text{STRB})$	Low-level strobe input current	$V(\text{STRB}) = 0$		-1	-1.4		mA
r_i	Input resistance	Inverting input		3.6	5		k Ω
		Noninverting input		1.8	2.5		
	Line-terminating resistance	$T_A = 25^\circ\text{C}$		120	170	250	Ω
I_{OS}	Short-circuit output current	$V_{CC} = 5.5\text{ V}$, $V_O = 0$		-2.8	-4.5	-6.7	mA
I_{CC}	Supply current (average per receiver)	$V_{IC} = 15\text{ V}$, $V_{ID} = -1\text{ V}$		4.2	6		mA
		$V_{IC} = 0$, $V_{ID} = -0.5\text{ V}$		6.8	10.2		
		$V_{IC} = -15\text{ V}$, $V_{ID} = -1\text{ V}$		9.4	14		

[†] Unless otherwise noted, $V(\text{STRB}) \geq 2.1\text{ V}$ or open.

[‡] All typical values are at $V_{CC} = 5\text{ V}$, $V_{IC} = 0$, and $T_A = 25^\circ\text{C}$.

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

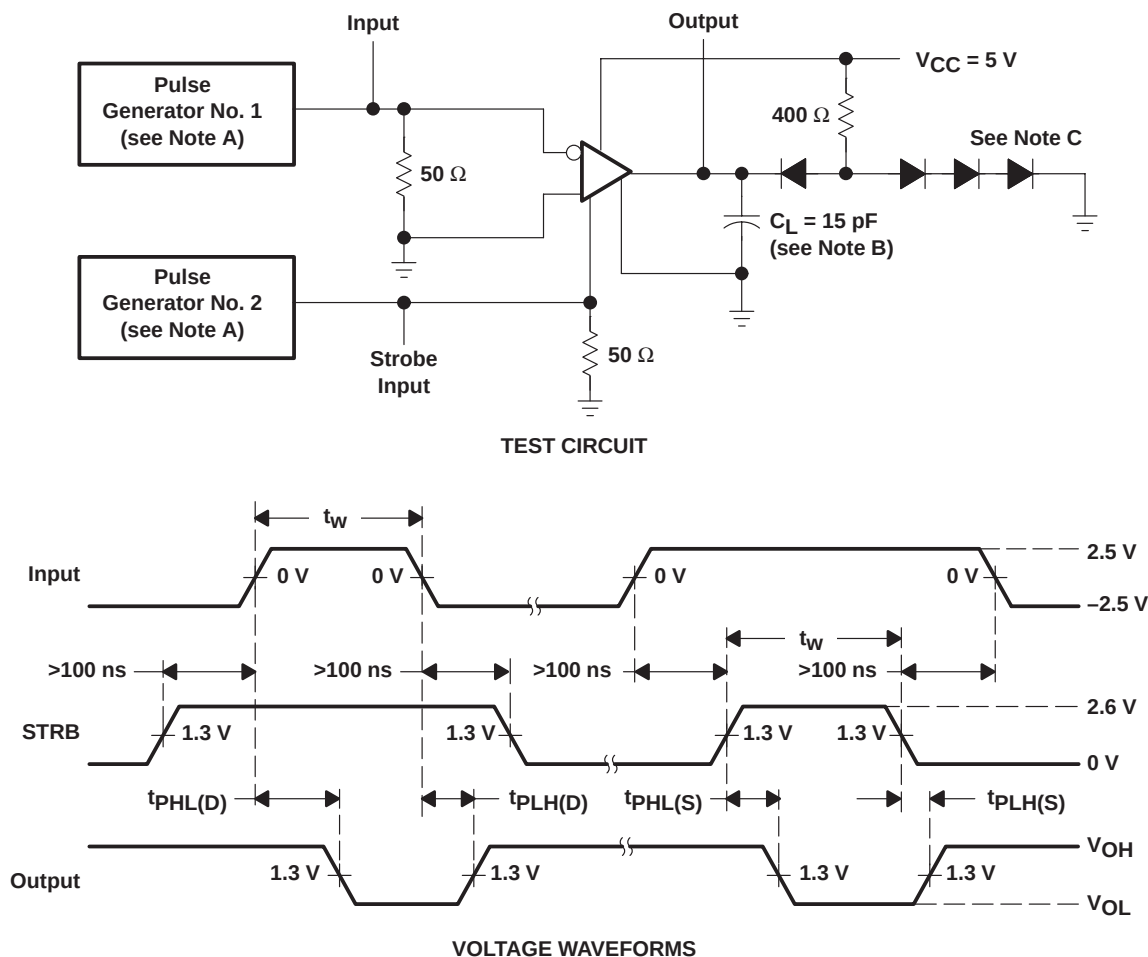
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{PLH}(\text{D})$	Propagation delay time, low- to high-level output from differential input	$R_L = 400\text{ }\Omega$, $C_L = 15\text{ pF}$	see Figure 1		18	40	ns
$t_{PHL}(\text{D})$	Propagation delay time, high- to low-level output from differential input	$R_L = 400\text{ }\Omega$, $C_L = 15\text{ pF}$	see Figure 1		31	45	ns
$t_{PLH}(\text{S})$	Propagation delay time, low- to high-level output from STRB input	$R_L = 400\text{ }\Omega$, $C_L = 15\text{ pF}$	see Figure 1		9	30	ns
$t_{PHL}(\text{S})$	Propagation delay time, high- to low-level output from STRB input	$R_L = 400\text{ }\Omega$, $C_L = 15\text{ pF}$	see Figure 1		15	25	ns



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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The pulse generators have the following characteristics: $Z_O = 50 \Omega$, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$, $t_W = 0.5 \pm 0.1 \mu\text{s}$, $\text{PRR} \leq 1 \text{ MHz}$.
 B. C_L includes probe and jig capacitance.
 C. All diodes are 1N3064 or equivalent.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS†

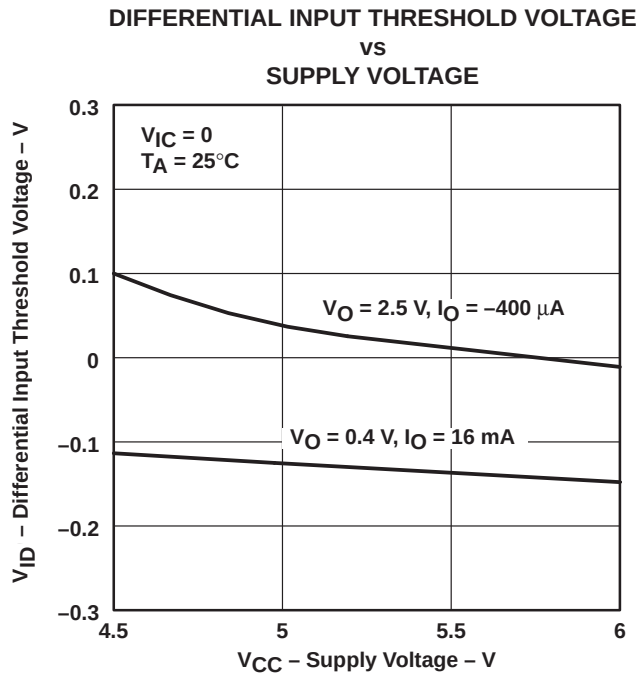


Figure 2

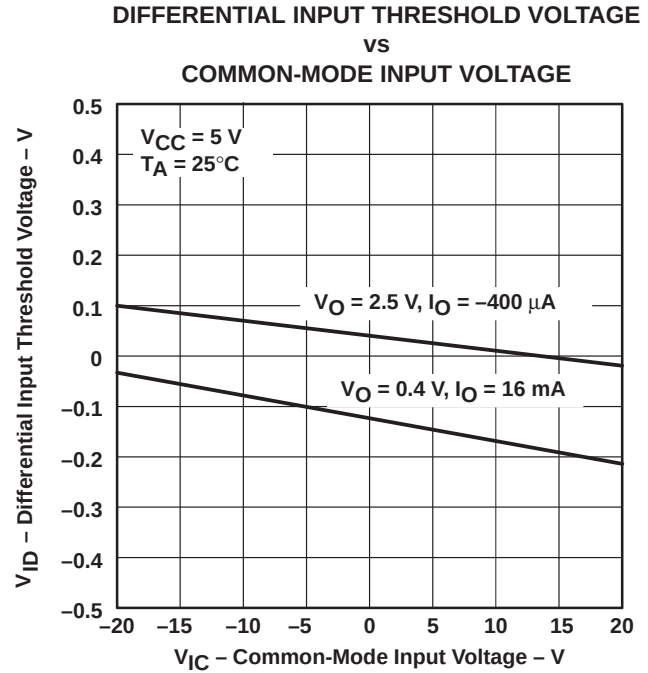


Figure 3

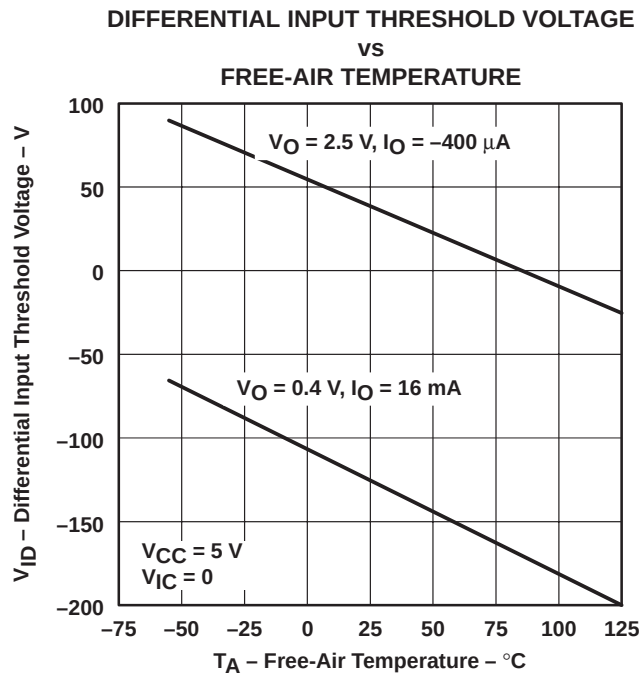


Figure 4

† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

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TYPICAL CHARACTERISTICS†

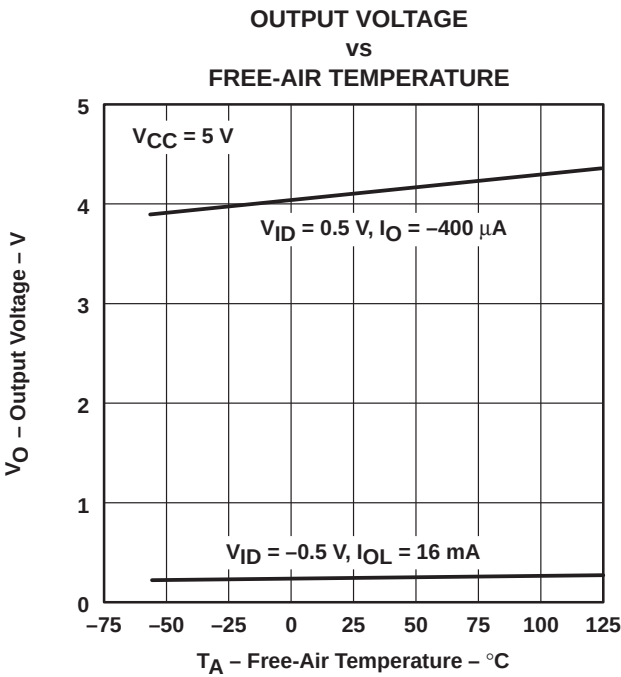


Figure 5

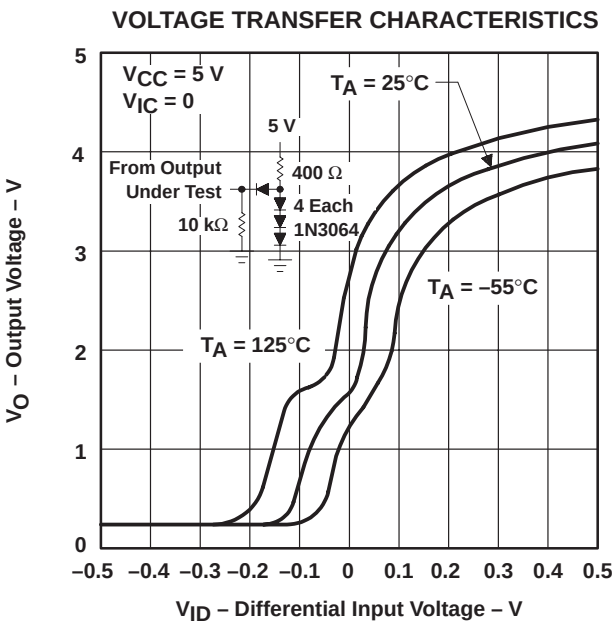


Figure 6

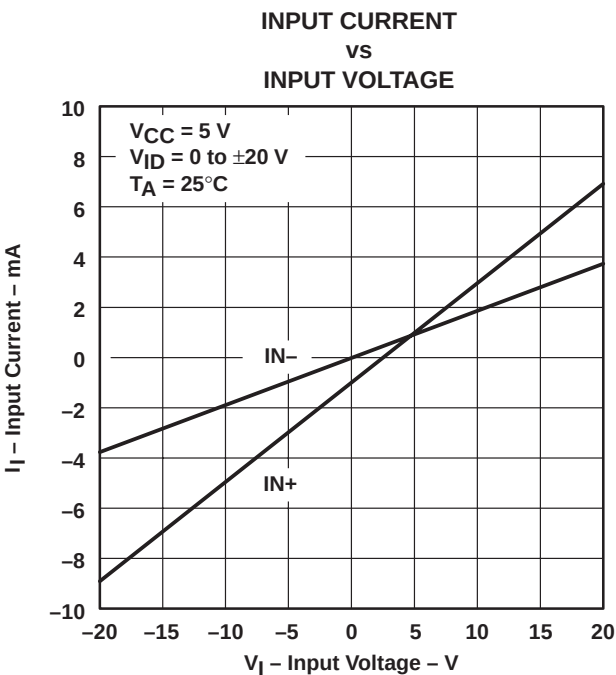


Figure 7

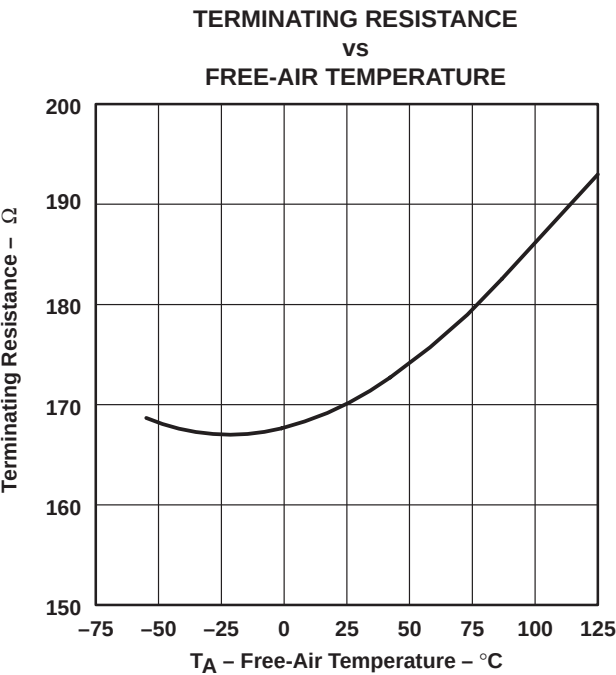


Figure 8

† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

TYPICAL CHARACTERISTICS†

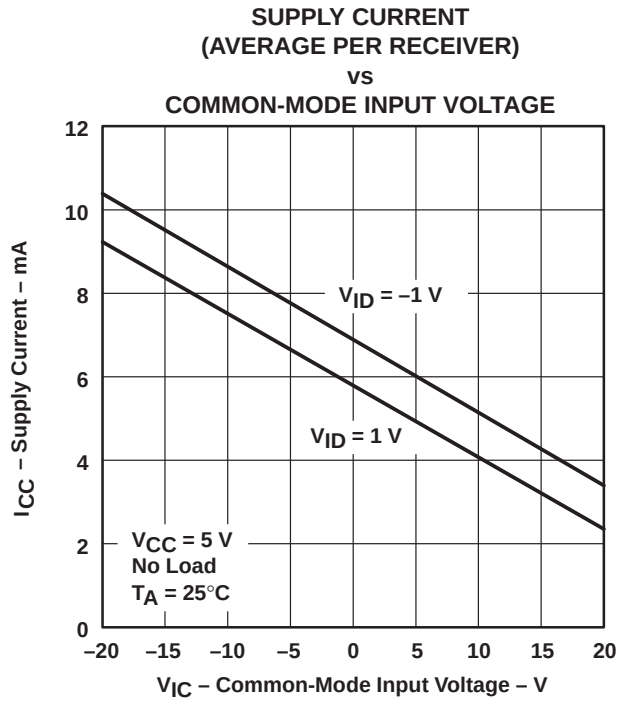


Figure 9

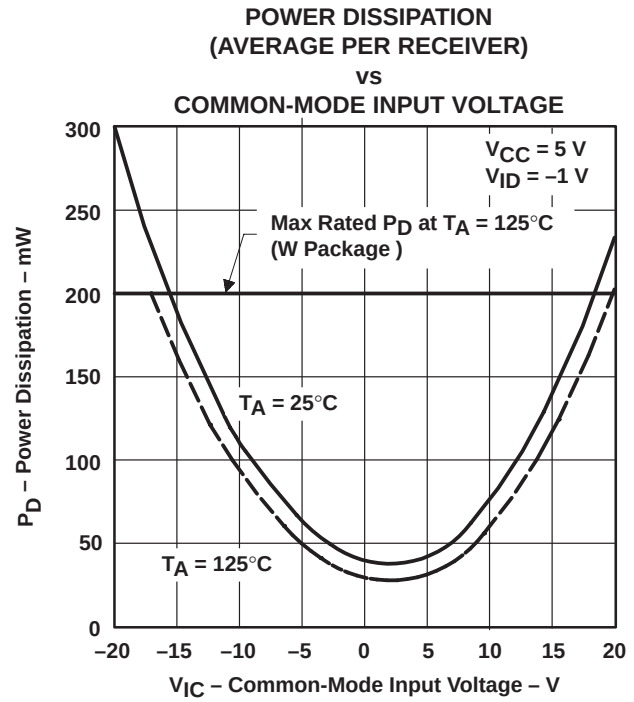


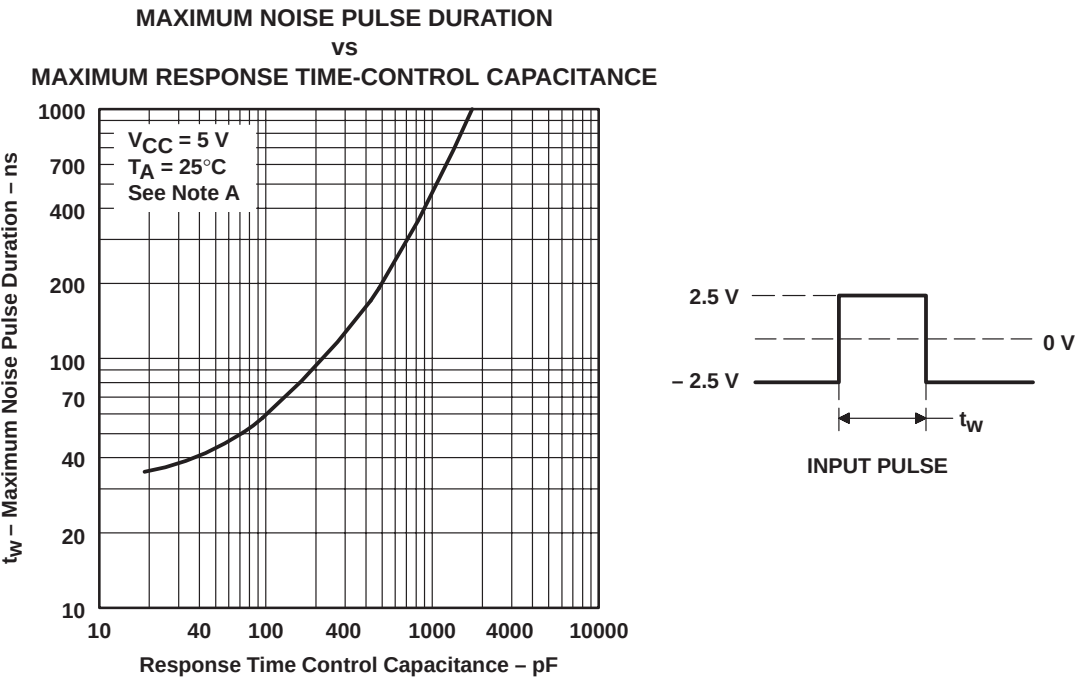
Figure 10

† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

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TYPICAL CHARACTERISTICS†



NOTE A: Figure 11 shows the maximum duration of the illustrated pulse that can be applied differently without the output changing from the low to high level.

Figure 11

† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

TYPICAL CHARACTERISTICS†

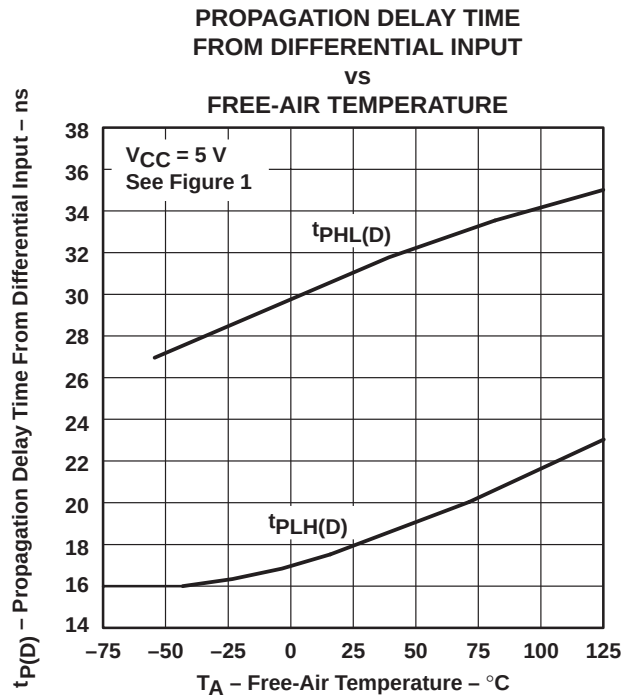


Figure 12

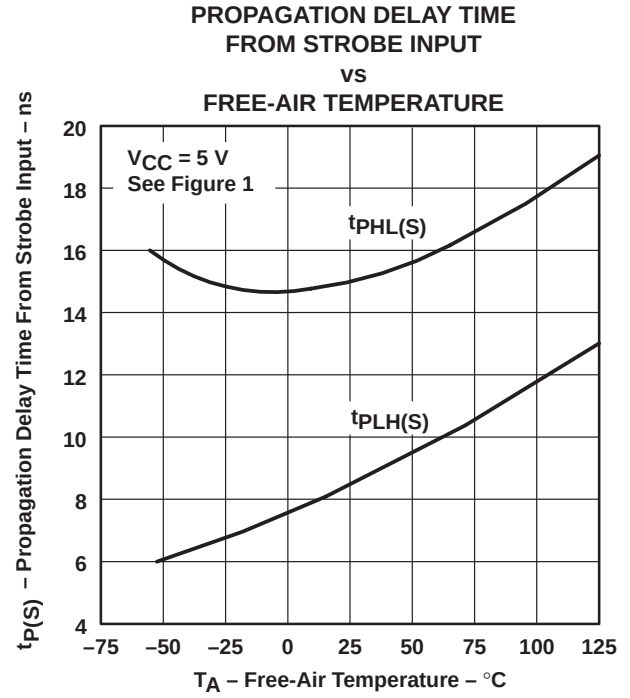


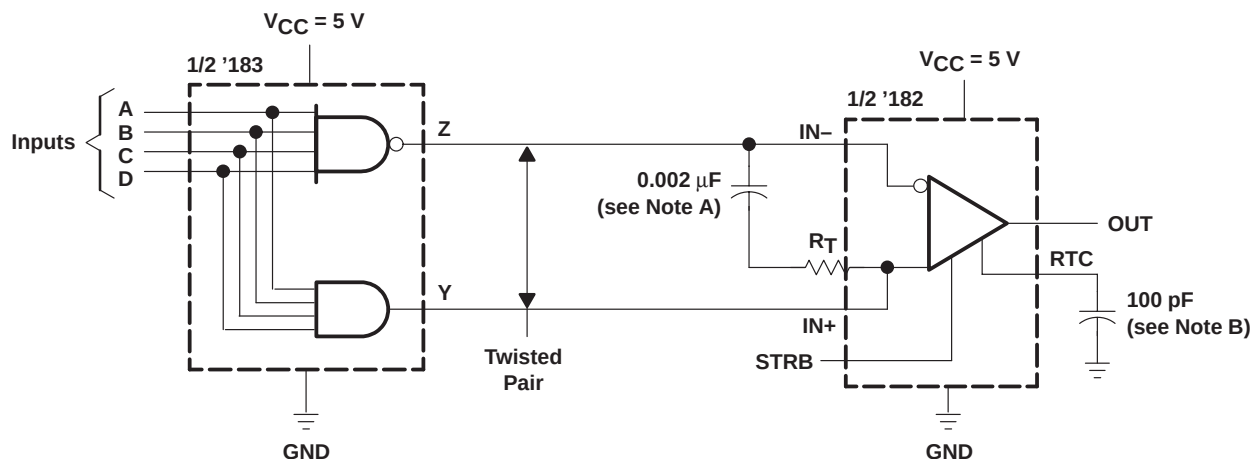
Figure 13

† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

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APPLICATION INFORMATION



NOTES: A. When the inputs are open circuited, the output is high. A capacitor may be used for dc isolation of the line-terminating resistor. At the frequency of operation, the impedance of the capacitor should be relatively small.

Example: let $f = 5 \text{ MHz}$
 $C = 0.002 \mu\text{F}$

$$Z_{(C)} = \frac{1}{2\pi f C} = \frac{1}{2\pi(5 \times 10^6)(0.002 \times 10^{-6})}$$

$$Z_{(C)} \approx 16\Omega$$

B. Use of a capacitor to control response time is optional.

Figure 14. Transmission of Digital Data Over Twisted-Pair Line

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
5962-7900801VCA	ACTIVE	CDIP	J	14	25	TBD	A42	N / A for Pkg Type	
5962-7900801VDA	ACTIVE	CFP	W	14	25	TBD	A42	N / A for Pkg Type	
SN55182J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	
SN75182D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN75182DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN75182DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN75182DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN75182DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN75182DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN75182N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN75182NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN75182NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN75182NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN75182NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SNJ55182FK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	
SNJ55182J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	
SNJ55182W	OBSOLETE	CFP	W	14		TBD	Call TI	Call TI	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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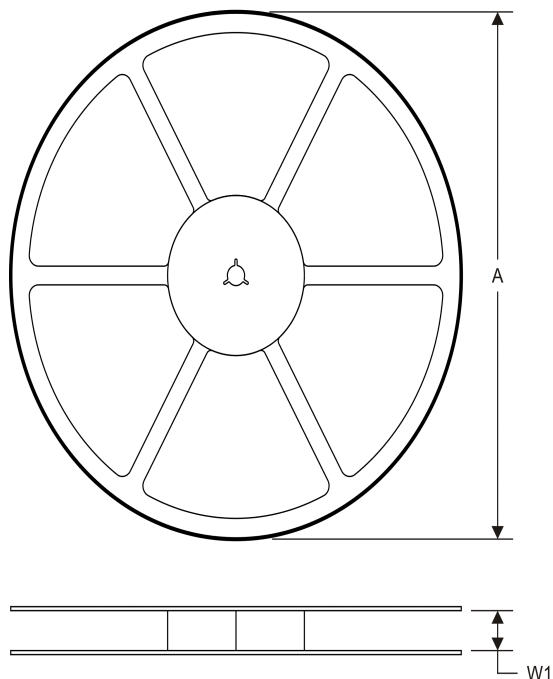
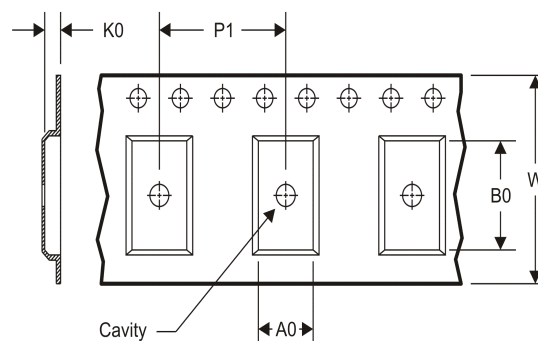
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OTHER QUALIFIED VERSIONS OF SN55182, SN55182-SP, SN75182 :

- Catalog: [SN75182](#), [SN55182](#)
- Military: [SN55182](#)
- Space: [SN55182-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


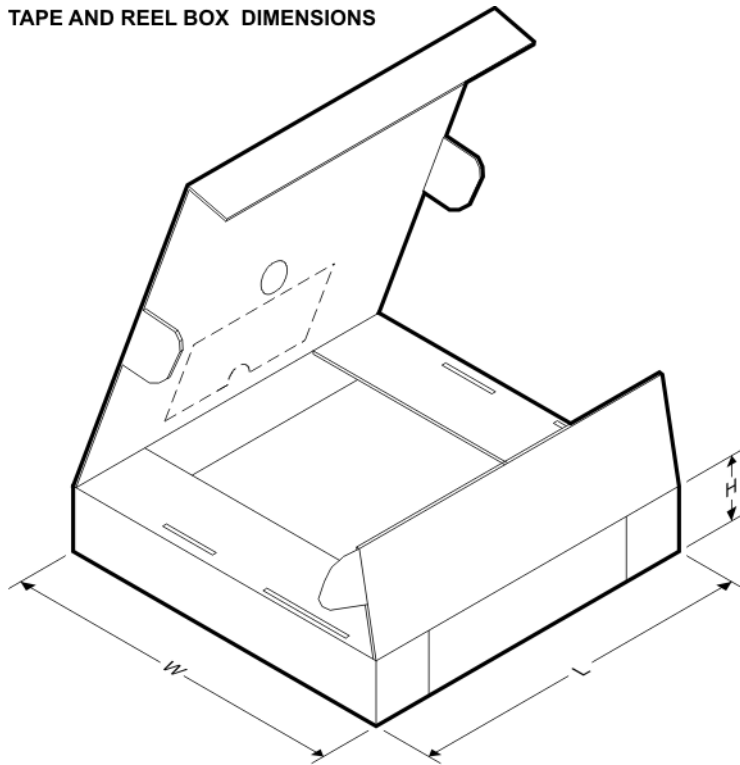
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75182DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN75182NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



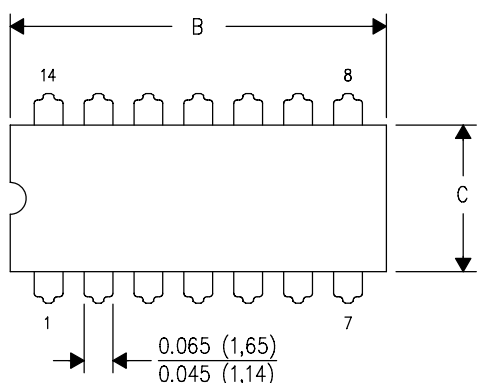
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75182DR	SOIC	D	14	2500	367.0	367.0	38.0
SN75182NSR	SO	NS	14	2000	367.0	367.0	38.0

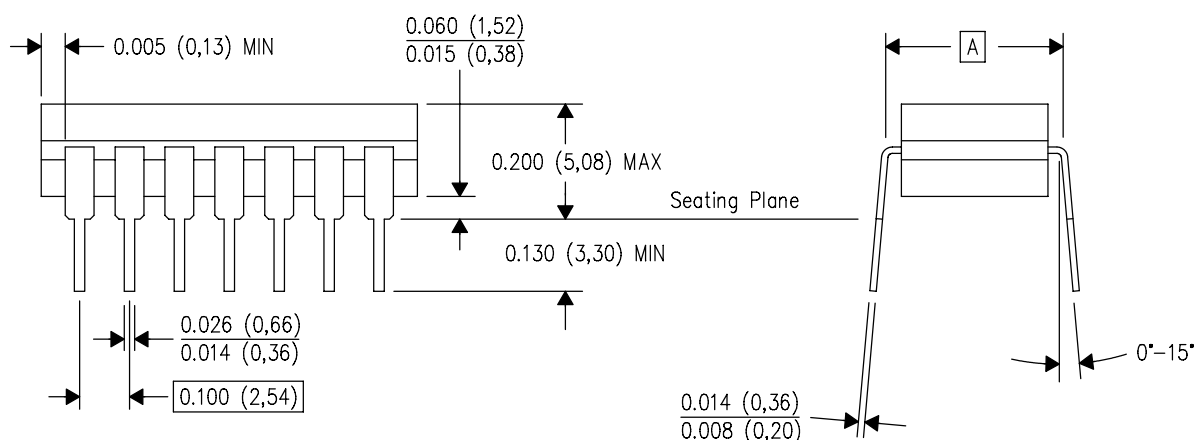
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

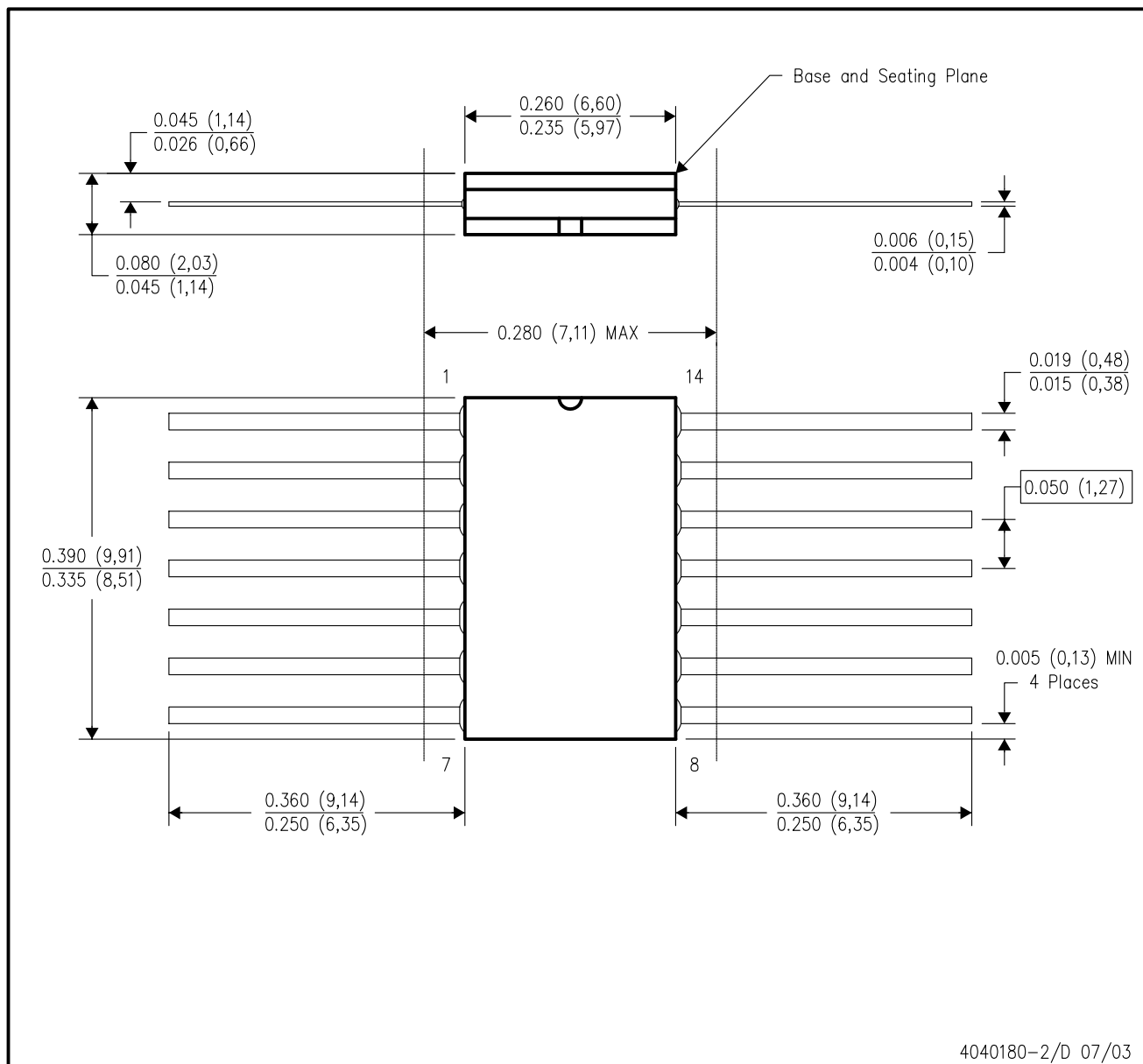


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK

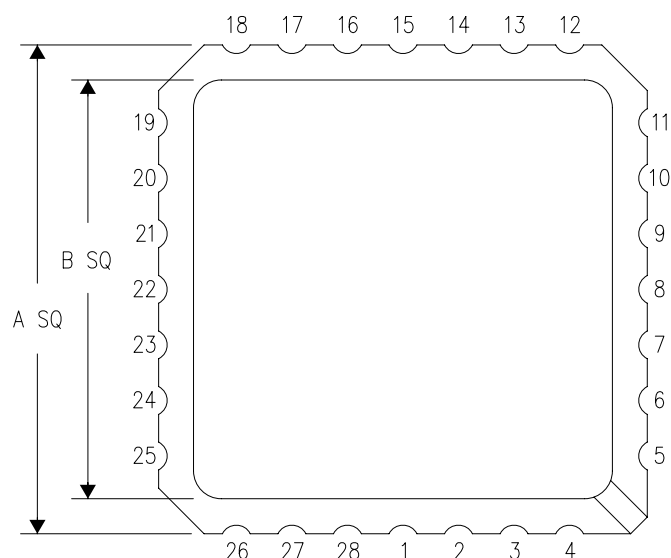


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

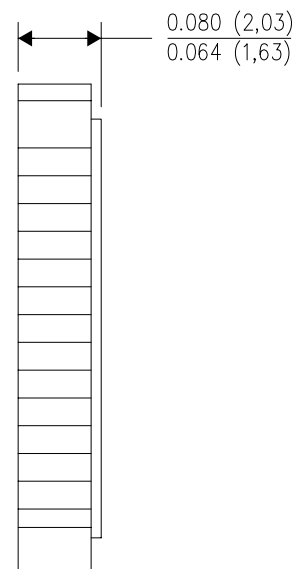
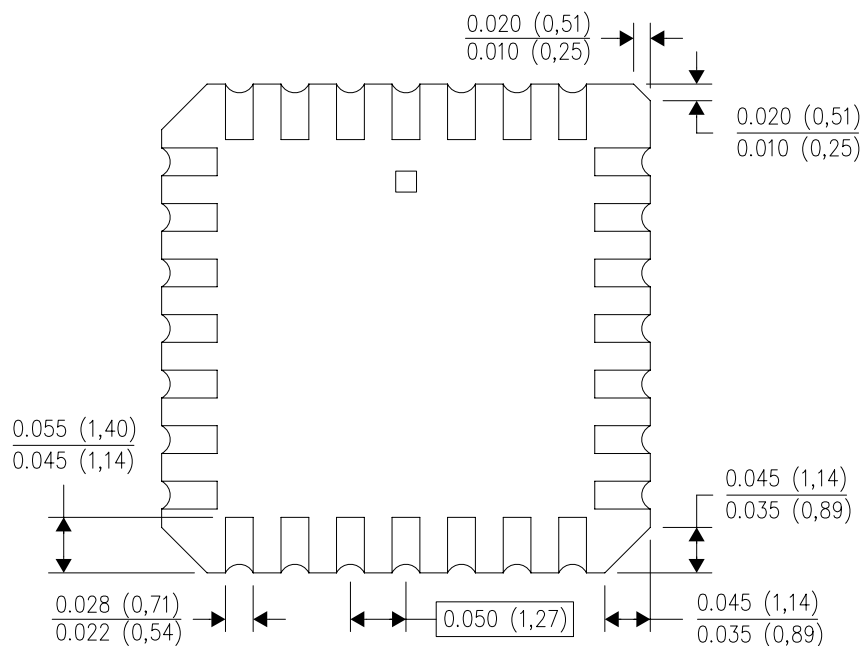
FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



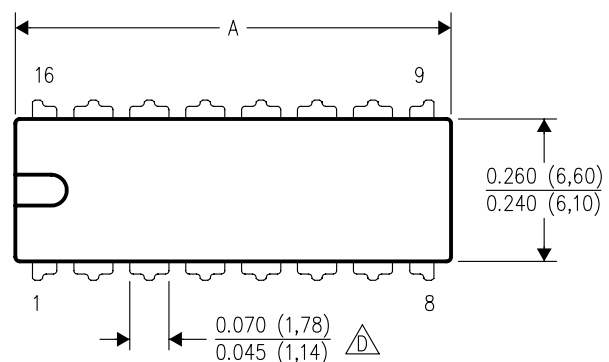
4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

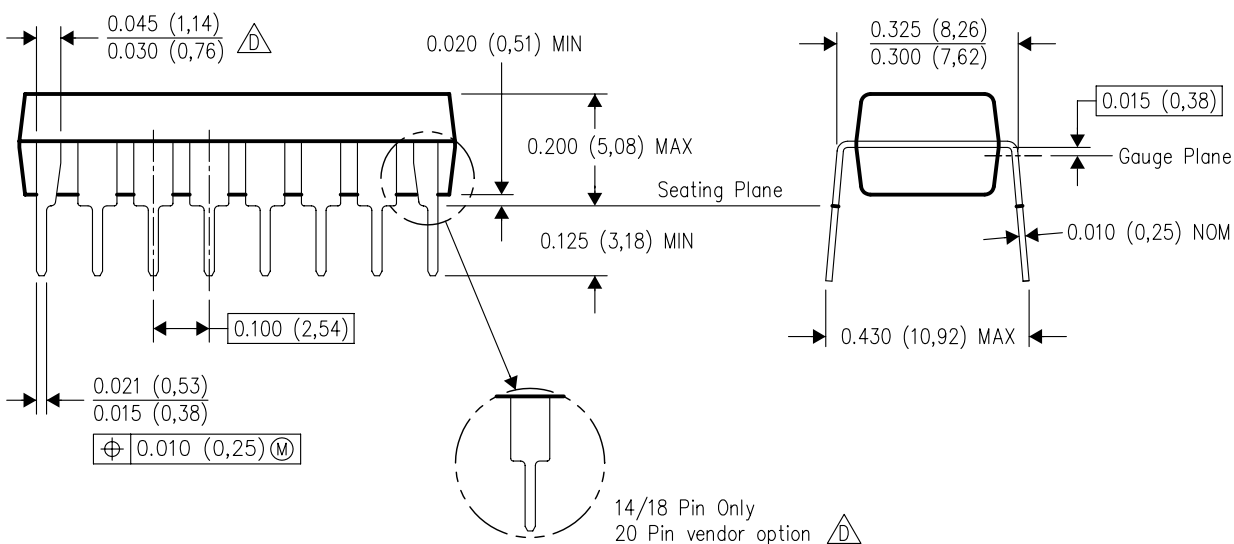
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



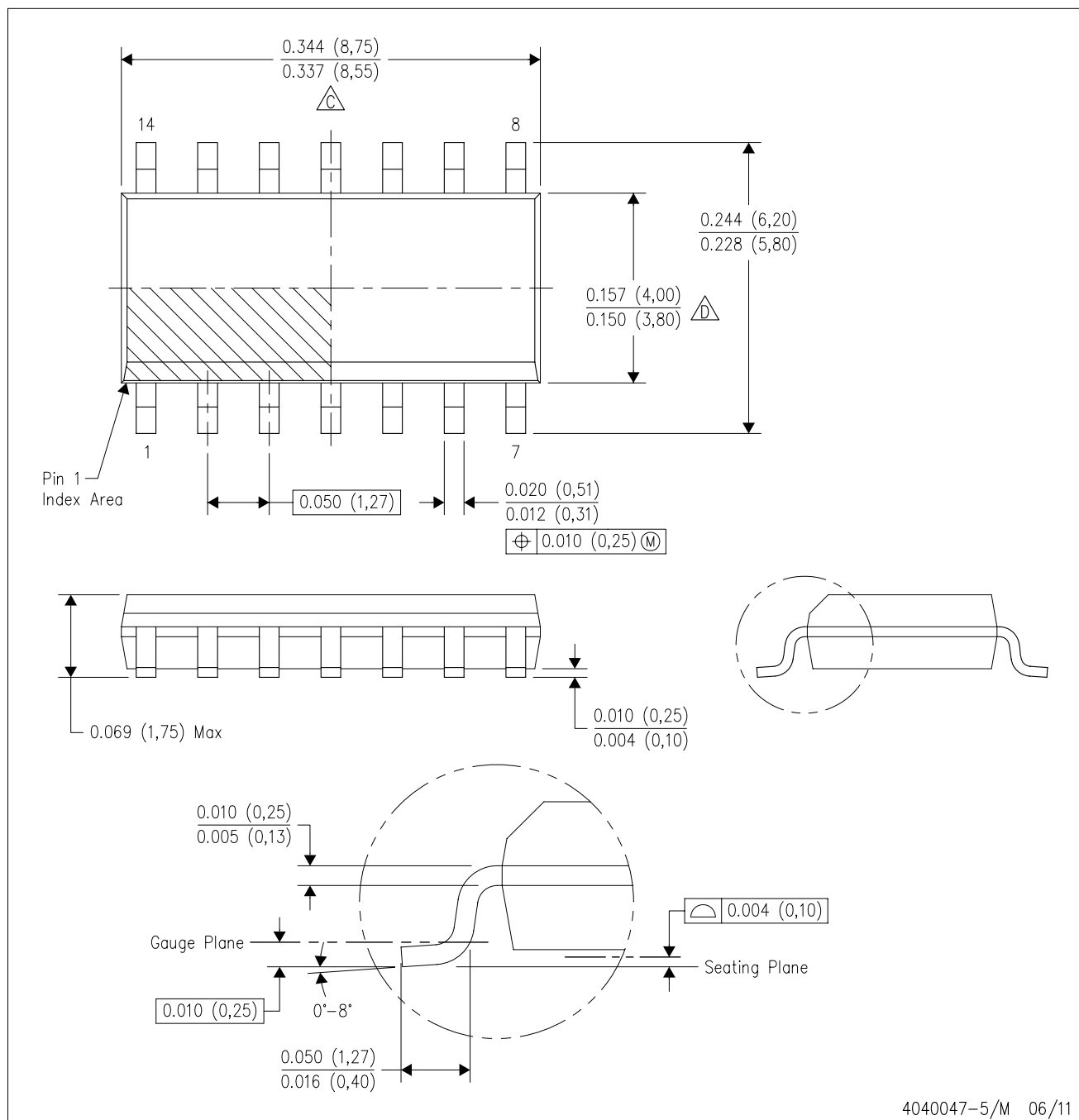
4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



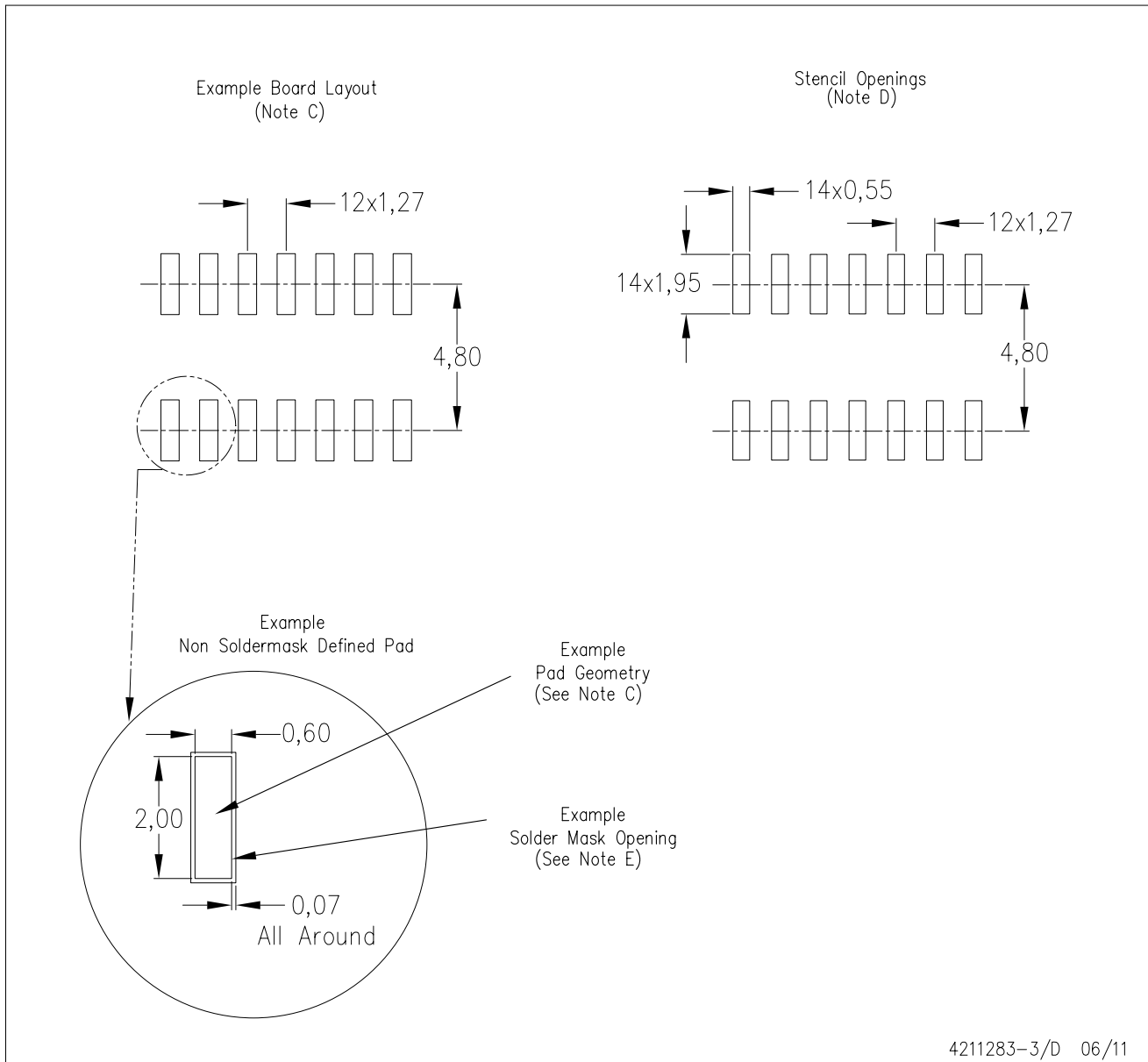
4040047-5/M 06/11

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



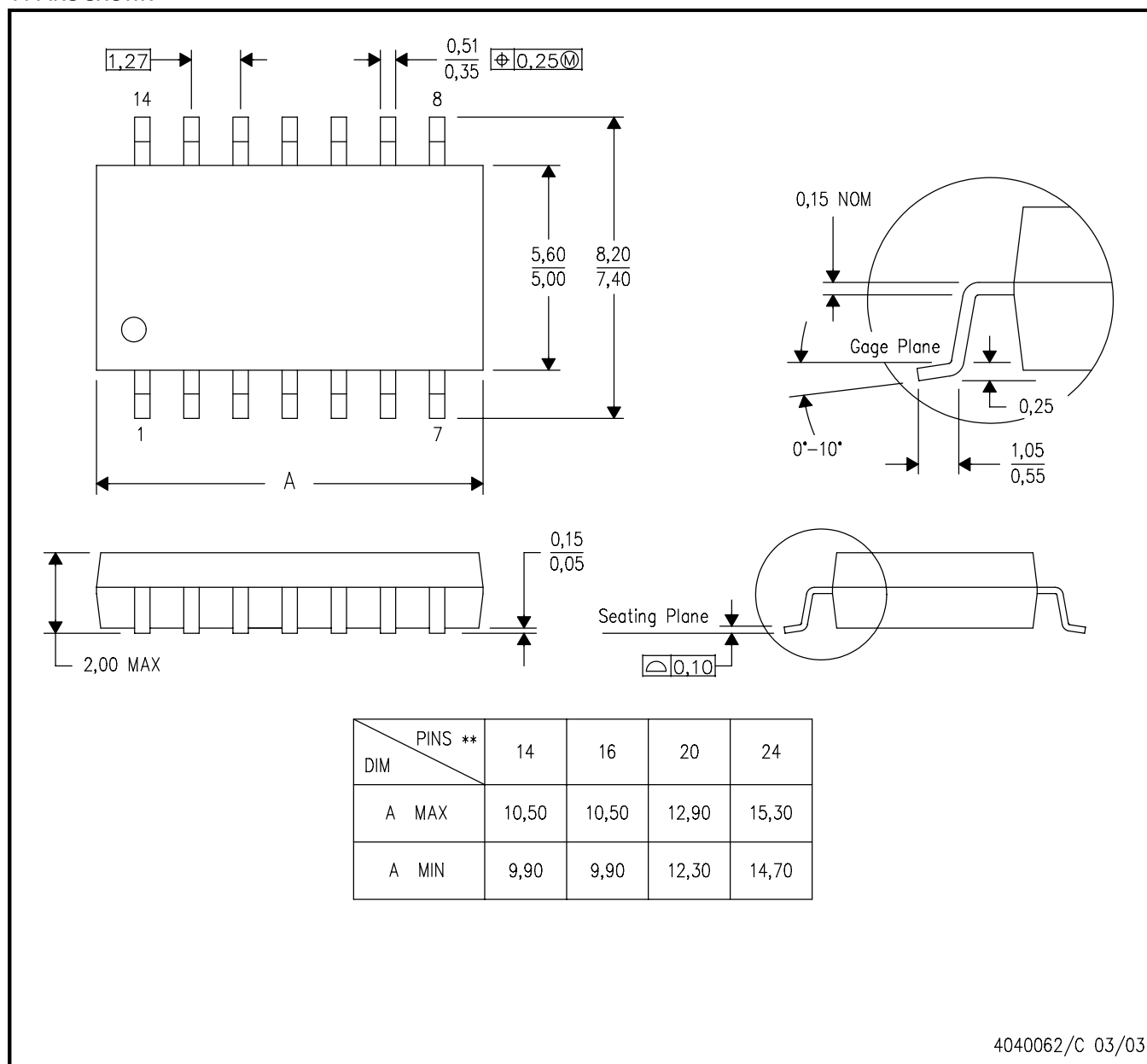
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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