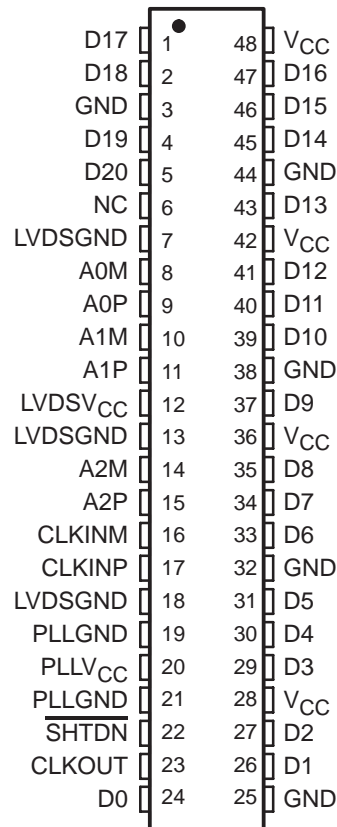


- **3:21 Data Channel Expansion at up to 178.5 Mbytes/s Throughput**
- **Suited for SVGA, XGA, or SXGA Display Data Transmission From Controller to Display With Very Low EMI**
- **Three Data Channels and Clock Low-Voltage Differential Channels In and 21 Data and Clock Low-Voltage TTL Channels Out**
- **Operates From a Single 3.3-V Supply and 250 mW (Typ)**
- **5-V Tolerant $\overline{\text{SHTDN}}$ Input**
- **ESD Protection Exceeds 4 kV on Bus Pins**
- **Packaged in Thin Shrink Small-Outline Package (TSSOP) With 20-Mil Terminal Pitch**
- **Consumes Less Than 1 mW When Disabled**
- **Wide Phase-Lock Input Frequency Range 31 MHz to 68 MHz**
- **No External Components Required for PLL**
- **Open-Circuit Receiver Fail-Safe Design**
- **Inputs Meet or Exceed the Requirements of ANSI EIA/TIA-644 Standard**
- **Improved Replacement for the National™ DS90C562**

DGG PACKAGE
(TOP VIEW)



description

NC – Not Connected

The SN75LVDS86 FlatLink receiver contains three serial-in 7-bit parallel-out shift registers, a 7× clock synthesizer, and four low-voltage differential signaling (LVDS) line receivers in a single integrated circuit. These functions allow receipt of synchronous data from a compatible transmitter, such as the SN75LVDS81, '83, '84, or '85, over four balanced-pair conductors, and expansion to 21 bits of single-ended low-voltage TTL (LVTTTL) synchronous data at a lower transfer rate.

When receiving, the high-speed LVDS data is received and loaded into registers at seven times (7×) the LVDS input clock (CLKIN) rate. The data is then unloaded to a 21-bit-wide LVTTTL parallel bus at the CLKIN rate. A phase-locked loop (PLL) clock synthesizer circuit generates a 7× clock for internal clocking and an output clock for the expanded data. The SN75LVDS86 presents valid data on the falling edge of the output clock (CLKOUT).

The SN75LVDS86 requires only four line-termination resistors for the differential inputs and little or no control. The data bus appears the same at the input to the transmitter and output of the receiver with the data transmission transparent to the user. The only possible user intervention is the use of the shutdown/clear ($\overline{\text{SHTDN}}$) active-low input to inhibit the clock and shut off the LVDS receivers for lower power consumption. A low level on this signal clears all internal registers to a low level.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

FlatLink is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2006, Texas Instruments Incorporated



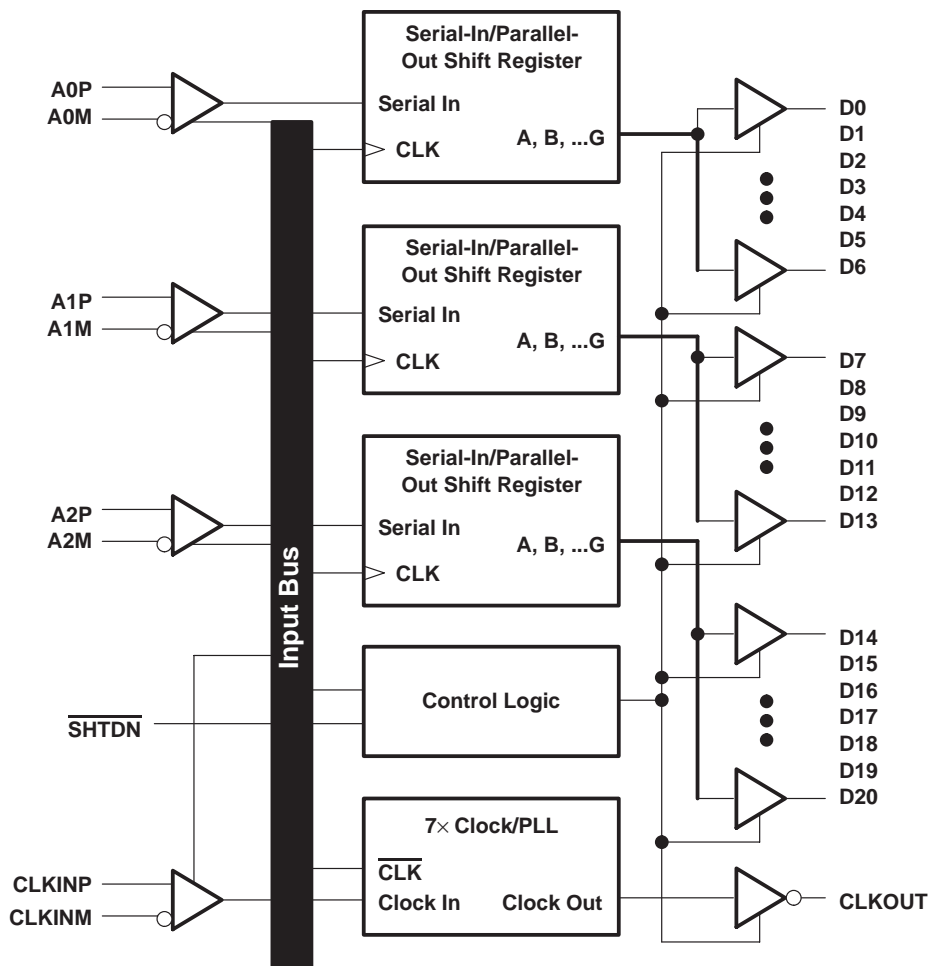
SN75LVDS86 FlatLink™ RECEIVER

SLLS268D – MARCH 1997 – REVISED JULY 2006

The LVDS receivers of the SN75LVDS86 include an open-circuit fail-safe design, such that when the inputs are not connected to an LVDS driver, the receiver outputs go to a low level. This occurs even when the line is differentially terminated at the receiver inputs.

The SN75LVDS86 is characterized for operation over ambient free-air temperatures of 0°C to 70°C.

functional block diagram



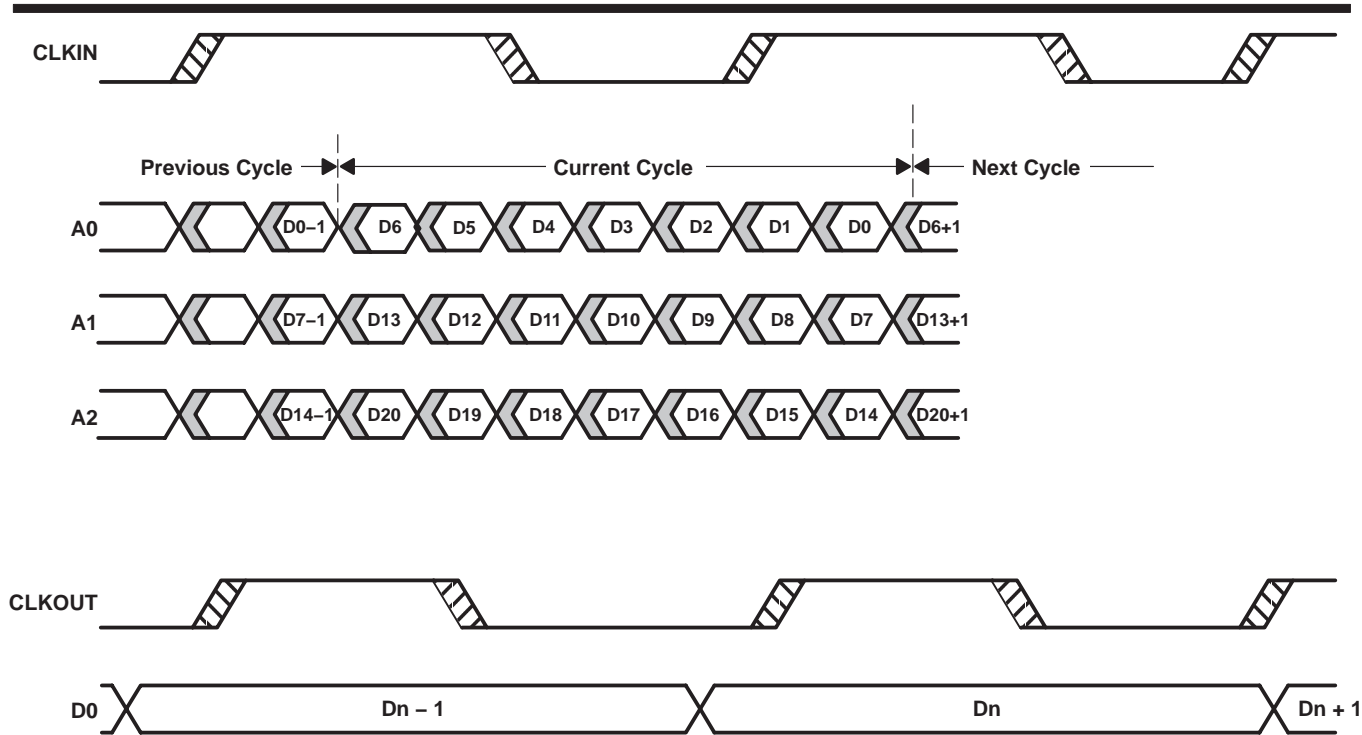
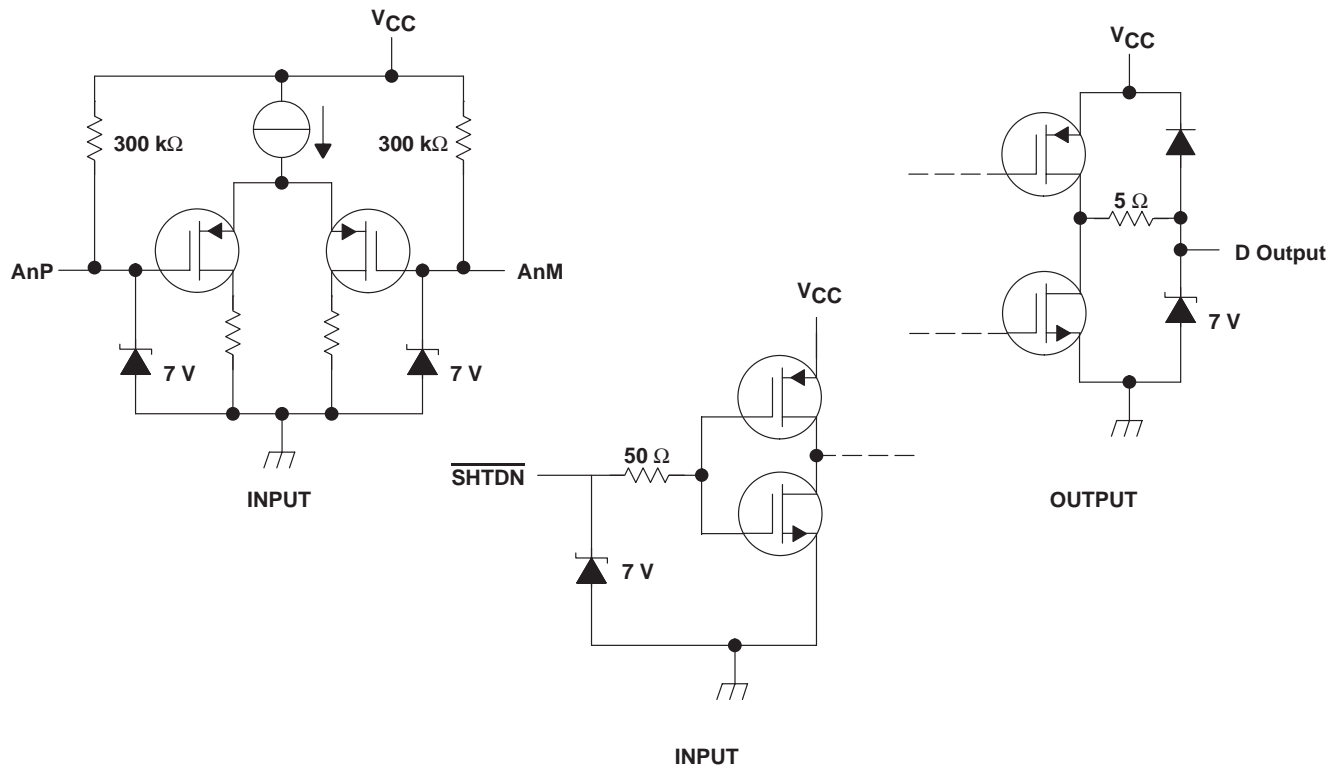


Figure 1. SN75LVDS86 Load and Shift Timing Sequences

equivalent input and output schematic diagrams



SN75LVDS86 FlatLink™ RECEIVER

SLLS268D – MARCH 1997 – REVISED JULY 2006

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|------------------------------|
| Supply voltage range, V_{CC} (see Note 1) | -0.5 V to 4 V |
| Output voltage range, V_O (Dxx terminals) | -0.5 V to $V_{CC} + 0.5$ V |
| Input voltage range, V_I : Any terminal except \overline{SHTDN} | -0.5 V to $V_{CC} + 0.5$ V |
| \overline{SHTDN} | -0.5 V to 5.5 V |
| Continuous total power dissipation | See Dissipation Rating Table |
| Storage temperature range, T_{stg} | -65°C to 150°C |
| Lead temperature 1,6 mm (1/16 in) from case for 10 s | 260°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND, unless otherwise noted.

DISSIPATION RATING TABLE

| PACKAGE | $T_A \leq 25^\circ\text{C}$ POWER RATING | DERATING FACTOR‡ ABOVE $T_A = 25^\circ\text{C}$ | $T_A = 70^\circ\text{C}$ POWER RATING |
|---------|---|--|--|
| DGG | 1316 mW | 13.1 mW/°C | 726 mW |

‡ This is the inverse of the junction-to-ambient thermal resistance when board mounted and with no air flow.

recommended operating conditions (see Figure 2)

| | MIN | NOM | MAX | UNIT |
|---|----------------------|----------------------------|-----|------|
| Supply voltage, V_{CC} | 3 | 3.3 | 3.6 | V |
| High-level input voltage, V_{IH} (\overline{SHTDN}) | 2 | | | V |
| Low-level input voltage, V_{IL} (\overline{SHTDN}) | | | 0.8 | V |
| Differential input voltage, $ V_{ID} $ | 0.1 | | 0.6 | V |
| Common-mode input voltage, V_{IC} (see Figure 2 and Figure 3) | $\frac{ V_{ID} }{2}$ | $2.4 - \frac{ V_{ID} }{2}$ | | V |
| | | $V_{CC} - 0.8$ | | |
| Operating free-air temperature, T_A | 0 | | 70 | °C |

timing requirements

| | MIN | NOM | MAX | UNIT |
|--|------|-------|------|------|
| t_c Cycle time, input clock§ | 14.7 | t_c | 32.4 | ns |
| t_{su1} Setup time, input (see Figure 7) | 600 | | | ps |
| t_{h1} Hold time, input (see Figure 7) | 600 | | | ps |

§ Parameter t_c is defined as the mean duration of a minimum of 32 000 clock cycles.



electrical characteristics over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|------------------|--|--|------|------|-----|------|
| V _{IT+} | Positive-going differential input threshold voltage | | | | 100 | mV |
| V _{IT-} | Negative-going differential input threshold voltage‡ | | -100 | | | mV |
| V _{OH} | High-level output voltage | I _{OH} = -4 mA | 2.4 | | | V |
| V _{OL} | Low-level output voltage | I _{OL} = 4 mA | | | 0.4 | V |
| I _{CC} | Quiescent current (average) | Disabled, All inputs open | | | 280 | μA |
| | | Enabled, AnP = 1 V, AnM = 1.4 V, t _C = 15.38 ns | | 58 | 72 | mA |
| | | Enabled, C _L = 8 pF, Grayscale pattern (see Figure 4), t _C = 15.38 ns | | 69 | | |
| | | Enabled, C _L = 8 pF, Worst-case pattern (see Figure 5), t _C = 15.38 ns | | 94 | | |
| I _{IH} | High-level input current ($\overline{\text{SHTDN}}$) | V _{IH} = V _{CC} | | | ±20 | μA |
| I _{IL} | Low-level input current ($\overline{\text{SHTDN}}$) | V _{IL} = 0 V | | | ±20 | μA |
| I _I | Input current (LVDS input terminals A and CLKIN) | 0 ≤ V _I ≤ 2.4 V | | | ±20 | μA |
| I _{OZ} | High-impedance output current | V _O = 0 or V _{CC} | | | ±10 | μA |

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for the negative-going input voltage threshold only.

switching characteristics over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|--------------------|--|---|-----|---------------------|-----|------|
| t _{su2} | Set up time, D0–D20 valid to CLKOUT↓ | C _L = 8 pF, See Figure 6 | 5 | | | ns |
| t _{h2} | Hold time, CLKOUT↓ to D0–D20 valid | C _L = 8 pF, See Figure 6 | 5 | | | ns |
| t _{RSKM} | Receiver input skew margin§ (see Figure 7) | t _C = 15.38 ns (±0.2%), Input clock jitter < 50 ps¶ | 490 | | | ps |
| t _d | Delay time, CLKIN↑ to CLKOUT↓ (see Figure 7) | t _C = 15.38 ns (±0.2%), C _L = 8 pF | | 3.7 | | ns |
| Δt _{C(o)} | Cycle time, change in output clock period# | t _C = 15.38 + 0.75 sin(2π500E3t) ± 0.05 ns, See Figure 8 | | ±80 | | ps |
| | | t _C = 15.38 + 0.75 sin(2π3E6t) ± 0.05 ns, See Figure 8 | | ±300 | | |
| t _{en} | Enable time, $\overline{\text{SHTDN}}$ ↑ to Dn valid | See Figure 9 | | 1 | | ms |
| t _{dis} | Disable time, $\overline{\text{SHTDN}}$ ↓ to off state | See Figure 10 | | 400 | | ns |
| t _t | Transition time, output (10% to 90% t _r or t _f) | C _L = 8 pF | | 3 | | ns |
| t _w | Pulse duration, output clock | | | 0.43 t _C | | ns |

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

§ The parameter t_{RSKM} is the timing margin available to the transmitter and interconnection skews and clock jitter. It is defined by $\frac{t_C}{14} - t_{su1}/t_{h1}$.

¶ |Input clock jitter| is the magnitude of the change in input clock period.

Δt_{C(o)} is the change in the output clock period from one cycle to the next cycle observed over 15 000 cycles.

PARAMETER MEASUREMENT INFORMATION

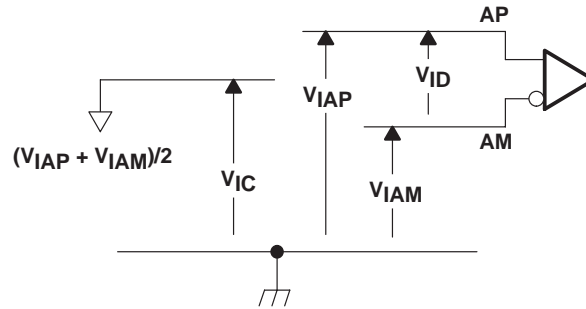


Figure 2. Voltage Definitions

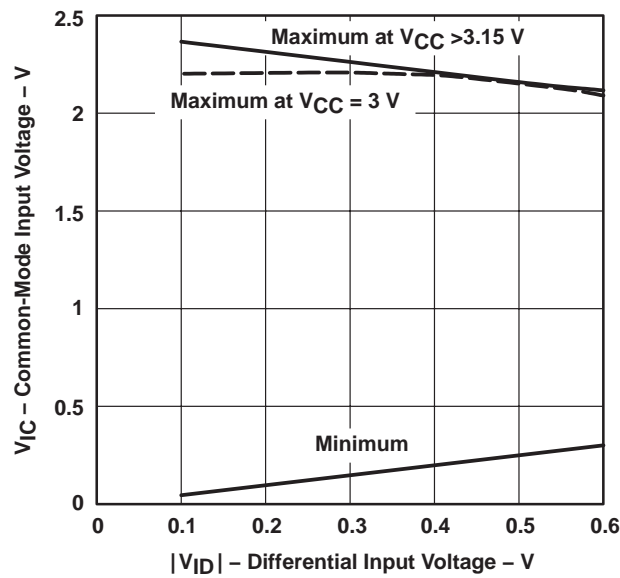
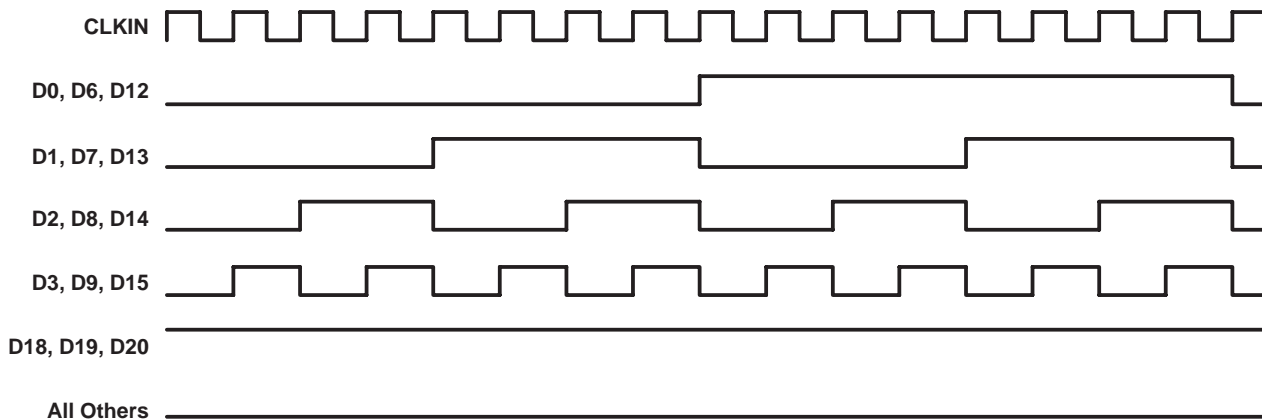


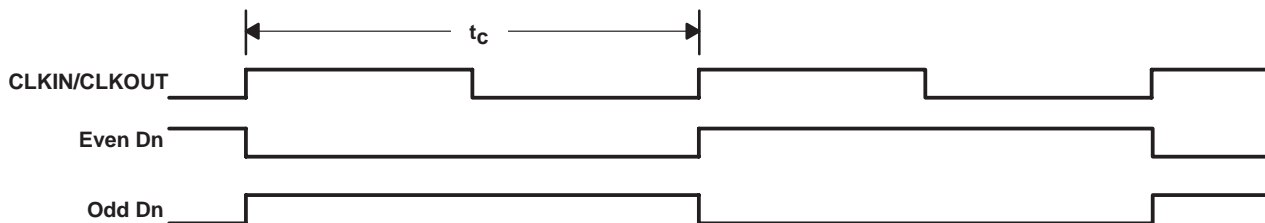
Figure 3. Common-Mode Input Voltage Vs Differential Input Voltage and V_{CC}

PARAMETER MEASUREMENT INFORMATION



NOTE A: The 16-grayscale test-pattern test device power consumption for a typical display pattern

Figure 4. 16-Grayscale Test Pattern



NOTE B: The worst-case test pattern produces nearly the maximum switching frequency for all of the LVTTTL outputs.

Figure 5. Worst-Case Test Pattern

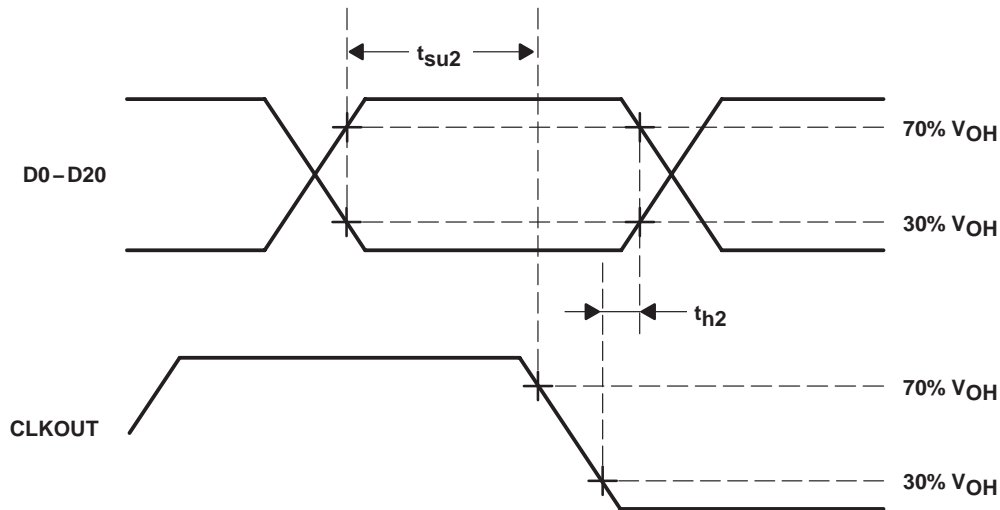
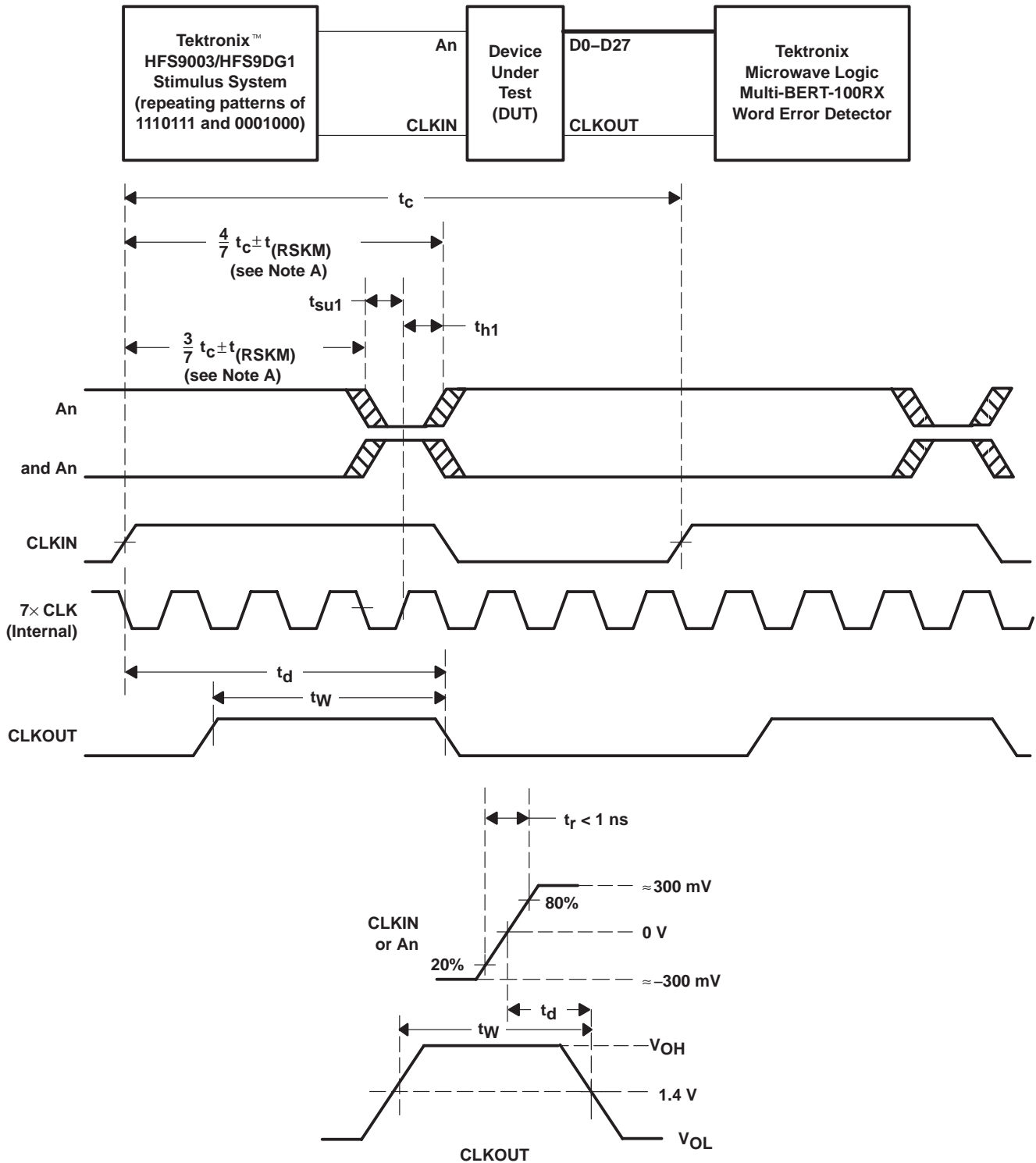


Figure 6. Setup and Hold Time

PARAMETER MEASUREMENT INFORMATION



NOTE A: $CLKIN$ is advanced or delayed with respect to data until errors are observed at the receiver outputs. The advance or delay is then reduced until there are no data errors observed. The magnitude of the advance or delay is $t_{(RSKM)}$.

Figure 7. Receiver Input Skew Margin, Setup/Hold Time, and Delay Timing

PARAMETER MEASUREMENT INFORMATION

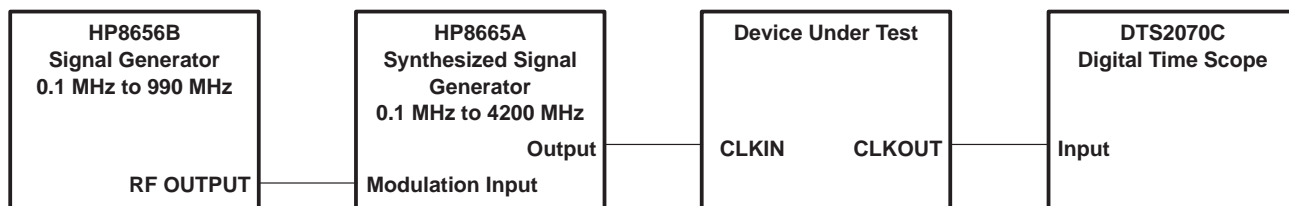
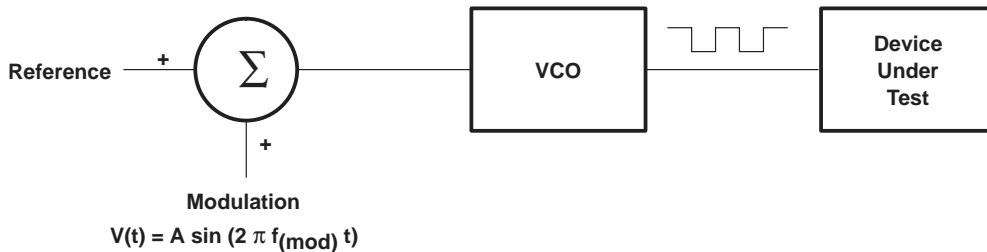


Figure 8. Output Clock Jitter Test Setup

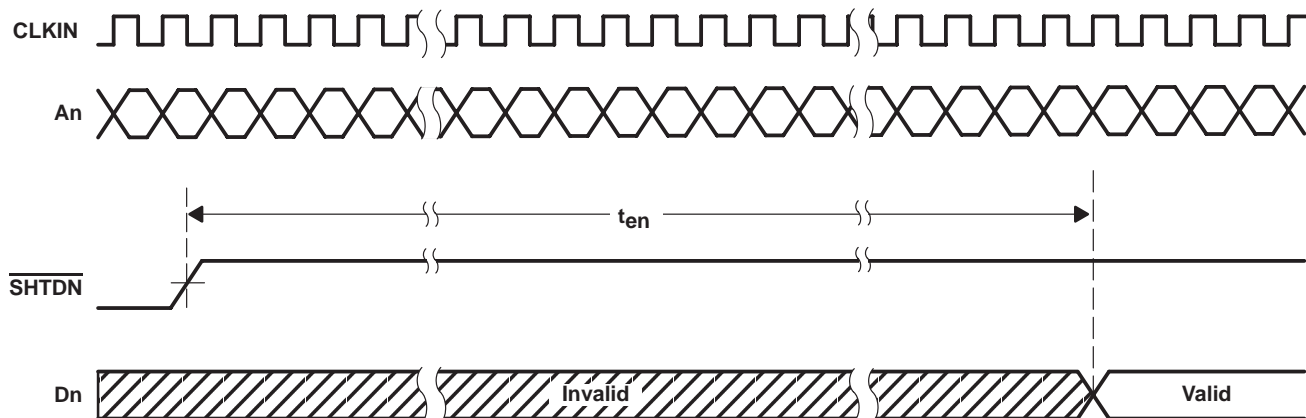


Figure 9. Enable Time

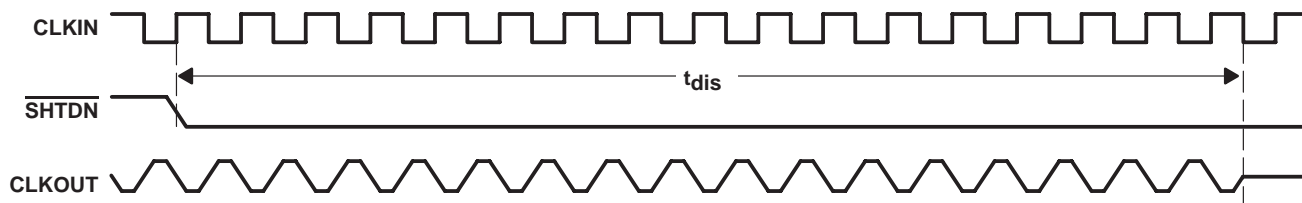


Figure 10. Disable Time

TYPICAL CHARACTERISTICS

**SUPPLY CURRENT
 vs
 CLOCK FREQUENCY**

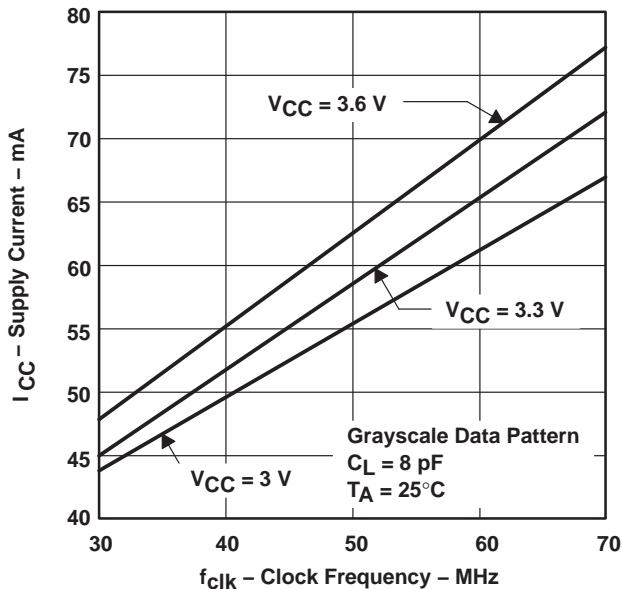


Figure 11. RMS Grayscale ICC vs Clock Frequency

**ZERO-TO-PEAK OUTPUT JITTER
 vs
 MODULATION FREQUENCY**

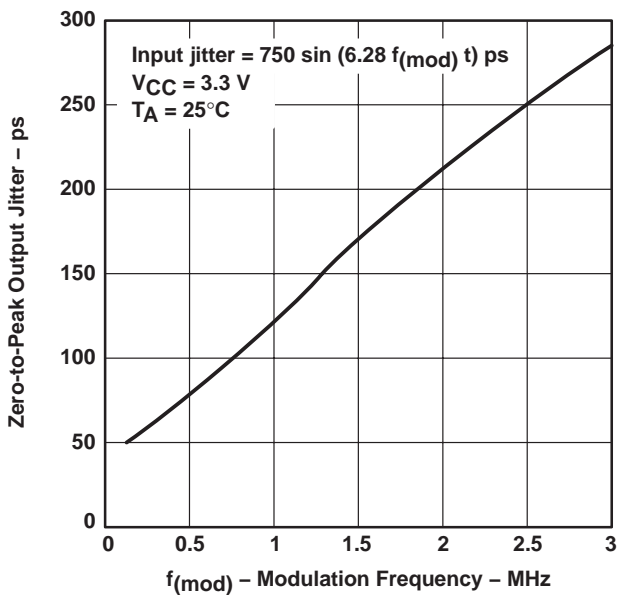
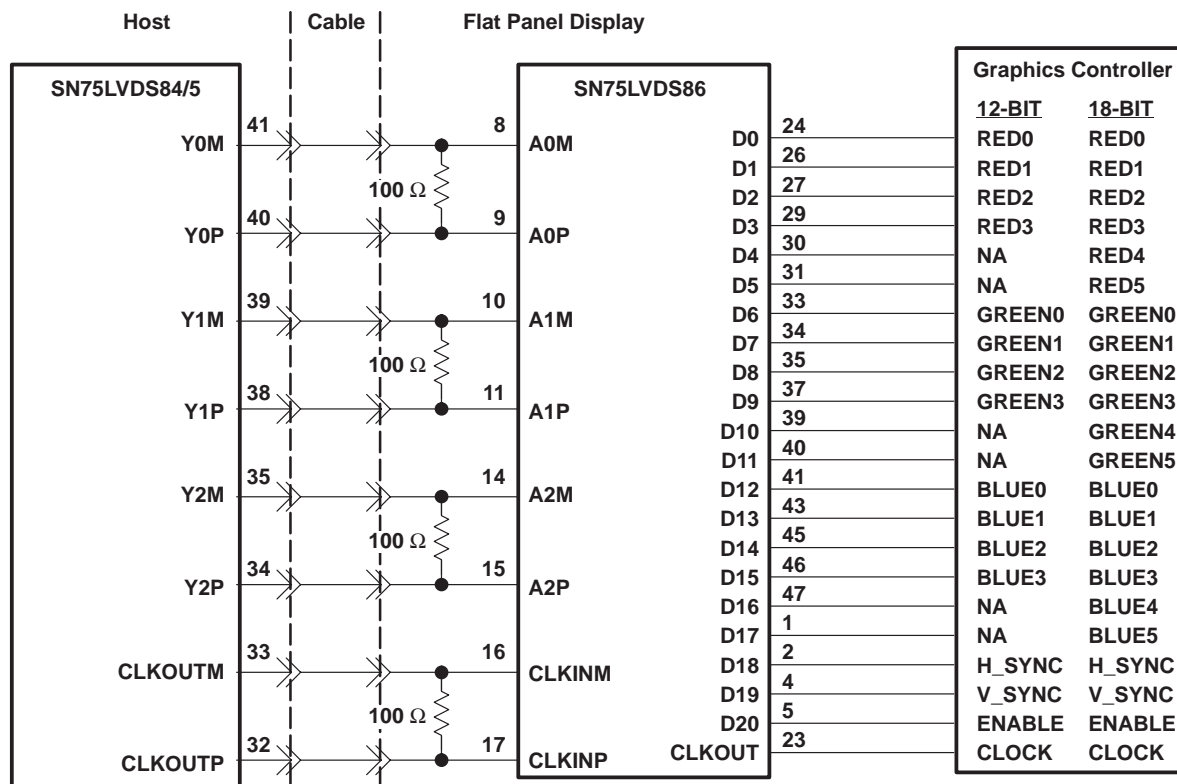


Figure 12. Typical FlatLink™ PLL Characteristics

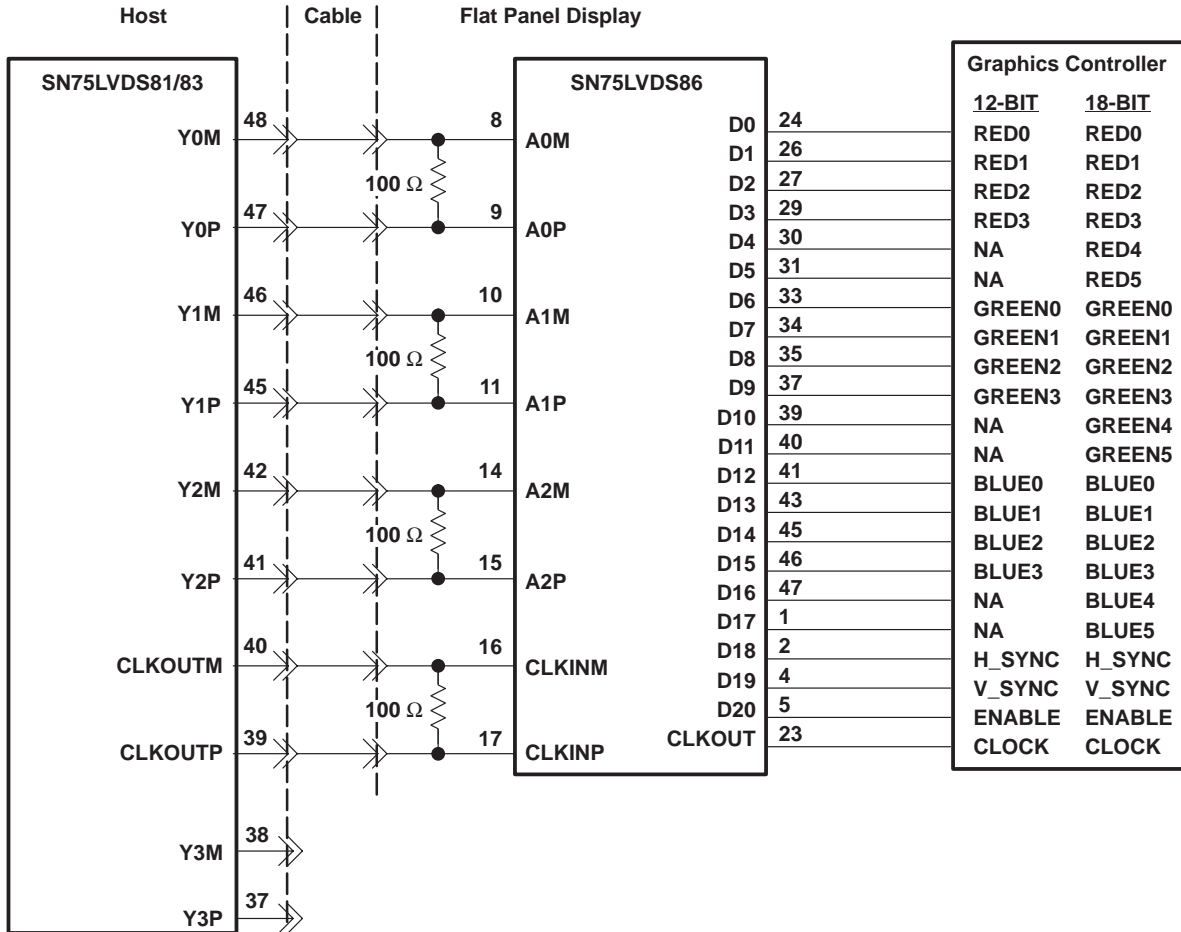
APPLICATION INFORMATION



NOTES: A. The four 100-Ω terminating resistors are recommended to be 0603 types.
 B. NA – not applicable, these unused inputs should be left open.

Figure 13. 18-Bit Color Host to Flat Panel Display Application

APPLICATION INFORMATION



NOTES: A. The four 100-Ω terminating resistors are recommended to be 0603 types.
 B. NA – not applicable, these unused inputs should be left open.

Figure 14. 24-Bit Color Host to 18-Bit Color LCD Panel Display Application†

† See the *FlatLink™ Designer's Guide* (SLLA012) for more application information.

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN75LVDS86DGG | ACTIVE | TSSOP | DGG | 48 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| SN75LVDS86DGGG4 | ACTIVE | TSSOP | DGG | 48 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| SN75LVDS86DGGGR | ACTIVE | TSSOP | DGG | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| SN75LVDS86DGGRG4 | ACTIVE | TSSOP | DGG | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

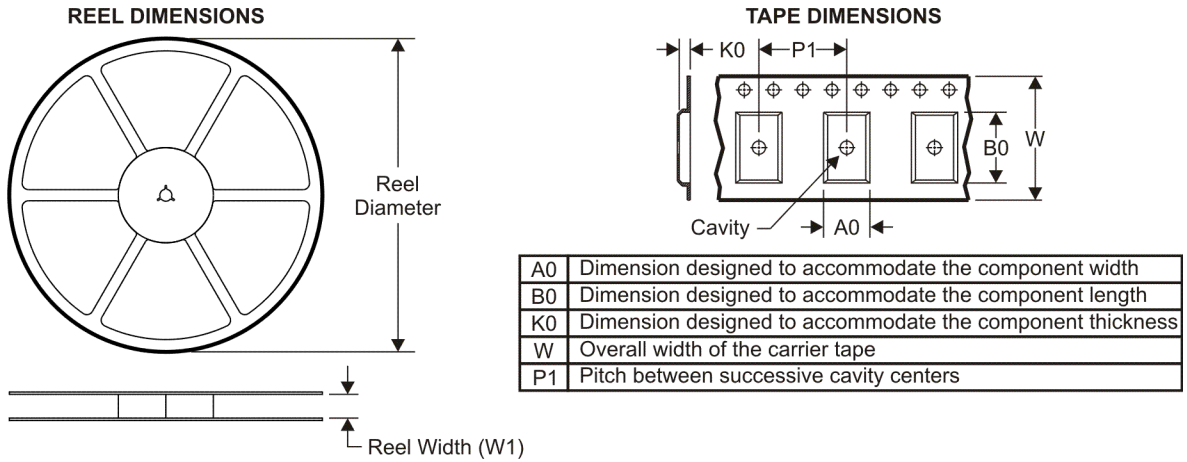
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN75LVDS86DGGR | TSSOP | DGG | 48 | 2000 | 330.0 | 24.4 | 8.6 | 15.8 | 1.8 | 12.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN75LVDS86DGGR | TSSOP | DGG | 48 | 2000 | 346.0 | 346.0 | 41.0 |

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

| | |
|-----------------------------|--|
| Amplifiers | amplifier.ti.com |
| Data Converters | dataconverter.ti.com |
| DSP | dsp.ti.com |
| Clocks and Timers | www.ti.com/clocks |
| Interface | interface.ti.com |
| Logic | logic.ti.com |
| Power Mgmt | power.ti.com |
| Microcontrollers | microcontroller.ti.com |
| RFID | www.ti-rfid.com |
| RF/IF and ZigBee® Solutions | www.ti.com/lprf |

Applications

| | |
|--------------------|--|
| Audio | www.ti.com/audio |
| Automotive | www.ti.com/automotive |
| Broadband | www.ti.com/broadband |
| Digital Control | www.ti.com/digitalcontrol |
| Medical | www.ti.com/medical |
| Military | www.ti.com/military |
| Optical Networking | www.ti.com/opticalnetwork |
| Security | www.ti.com/security |
| Telephony | www.ti.com/telephony |
| Video & Imaging | www.ti.com/video |
| Wireless | www.ti.com/wireless |

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2008, Texas Instruments Incorporated