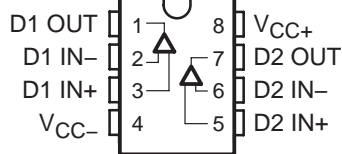


THS6052, THS6053 175 mA, ± 12 V ADSL CPE LINE DRIVERS

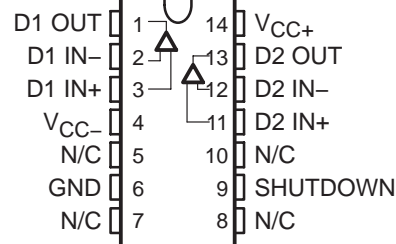
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- **Remote Terminal ADSL Line Driver**
 - Ideal for Both Full Rate ADSL and G.Lite
 - Compatible With 1:1 Transformer Ratio
- **Low 2.7 pA/ $\sqrt{\text{Hz}}$ Noninverting Current Noise**
 - Reduces Noise Feedback Through Hybrid Into Downstream Channel
- **Wide Supply Voltage Range ± 5 V to ± 15 V**
 - Ideal for ± 12 -V Operation
- **Wide Output Swing**
 - 42 Vpp Differential Output Voltage, $R_L = 200 \Omega$, ± 12 -V Supply
- **High Output Current**
 - 175 mA (typ)
- **High Speed**
 - 110 MHz (-3 dB, $G=8$, ± 12 V)
 - 1500 V/ μs Slew Rate ($G = 8$, ± 12 V)
- **Low Distortion, Single-Ended, $G = 8$**
 - -83 dBc (250 kHz, 2 Vpp, 100- Ω load)
- **Low Power Shutdown (THS6053)**
 - 300- μA Total Standby Current
- **Thermal Shutdown and Short Circuit Protection**
- **Standard SOIC, SOIC PowerPAD, and TSSOP PowerPAD™ Package**
- **Evaluation Module Available**

THS6052
SOIC (D) AND
SOIC PowerPAD™ (DDA) PACKAGE
(TOP VIEW)

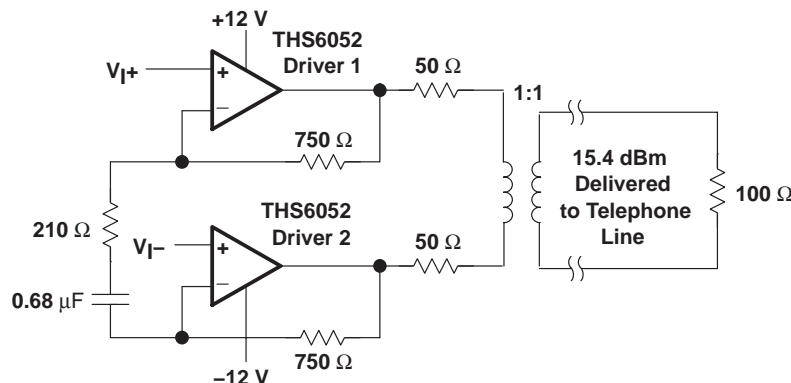


THS6053
SOIC (D) AND
TSSOP PowerPAD™ (PWP) PACKAGE
(TOP VIEW)



description

The THS6052/3 is a high-speed line driver ideal for driving signals from the remote terminal to the central office in asymmetrical digital subscriber line (ADSL) applications. It can operate from ± 12 -V supply voltages while drawing only 5.2 mA of supply current per channel. It offers low -83 dBc total harmonic distortion driving a 100- Ω load (2 Vpp). The THS6052/3 offers a high 42-Vpp differential output swing across a 200- Ω load from a ± 12 -V supply. The THS6053 features a low-power shutdown mode, consuming only 300 μA quiescent current per channel. The THS6052/3 is packaged in a standard SOIC, SOIC PowerPAD™, and TSSOP PowerPAD™ packages.



RELATED PRODUCTS

DEVICE	DESCRIPTION
THS6042/3	350-mA, ± 12 V ADSL CPE line driver
THS6092/3	275-mA, +12 V ADSL CPE line driver
OPA2677	380-mA, +12 V ADSL CPE line driver
THS6062	Low noise ADSL receiver



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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THS6052, THS6053 175 mA, ±12 V ADSL CPE LINE DRIVERS

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AVAILABLE OPTION

T _A	PACKAGED DEVICE				EVALUATION MODULES
	SOIC-8 (D)	SOIC-8 PowerPAD (DDA)	SOIC-14 (D)	TSSOP-14 (PWP)	
0°C to 70°C	THS6052CD	THS6052CDDA	THS6053CD	THS6053CPWP	THS6052EVM THS6053EVM
-40°C to 85°C	THS6052ID	THS6052IDDA	THS6053ID	THS6053IPWP	—

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V _{CC+} to V _{CC-}	33 V
Input voltage	± V _{CC}
Output current (see Note 1)	275 mA
Differential input voltage	± 4 V
Maximum junction temperature	150°C
Total power dissipation at (or below) 25°C free-air temperature	See Dissipation Ratings Table
Operating free-air temperature, T _A : Commercial	0°C to 70°C
Industrial	-40°C to 85°C
Storage temperature, T _{stg} : Commercial	-65°C to 125°C
Industrial	-65°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The THS6052 and THS6053 may incorporate a PowerPAD™ on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipating plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI technical brief SLMA002 for more information about utilizing the PowerPAD™ thermally enhanced package.

DISSIPATION RATING TABLE

PACKAGE	θ _{JA}	θ _{JC}	T _A = 25°C T _J = 150°C POWER RATING
D-8	95°C/W‡	38.3°C/W‡	1.32 W
DDA	45.8°C/W‡	9.2°C/W‡	2.73 W
D-14	66.6°C/W‡	26.9°C/W‡	1.88 W
PWP	37.5°C/W	1.4°C/W	3.3 W

‡ This data was taken using the JEDEC proposed high-K test PCB. For the JEDEC low-K test PCB, the θ_{JA} is 168°C/W for the D-8 package and 122.3°C/W for the D-14 package.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V _{CC+} to V _{CC-}	Dual supply	±5		±15	V
	Single supply	10		30	
Operating free-air temperature, T _A	C-suffix	0		70	°C
	I-suffix	-40		85	



electrical characteristics over recommended operating free-air temperature range, $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 12\text{ V}$, $R_{FEEDBACK} = 750\ \Omega$, $R_L = 100\ \Omega$ (unless otherwise noted)

dynamic performance

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
BW	Small-signal bandwidth (–3 dB)	$R_L = 50\ \Omega$	G= 1, $R_F = 1\ \text{k}\Omega$	$V_{CC} = \pm 5\ \text{V}$	110		MHz
				$V_{CC} = \pm 12\ \text{V}$	120		
			G= 2, $R_F = 680\ \Omega$	100			
				G= 8, $R_F = 330\ \Omega$	$V_{CC} = \pm 5\ \text{V}, \pm 12\ \text{V}$		
		$R_L = 100\ \Omega$	G= 1, $R_F = 1\ \text{k}\Omega$		$V_{CC} = \pm 5\ \text{V}$	150	
				$V_{CC} = \pm 12\ \text{V}$	170		
			G= 2, $R_F = 680\ \Omega$	135			
				G= 8, $R_F = 330\ \Omega$	$V_{CC} = \pm 5\ \text{V}, \pm 12\ \text{V}$		
SR	Slew rate (see Note 2), G=8	$V_O = 4\ \text{V}_{PP}$	$V_{CC} = \pm 5\ \text{V}$		$V_{CC} = \pm 5\ \text{V}$	650	
			$V_{CC} = \pm 12\ \text{V}$	$V_{CC} = \pm 12\ \text{V}$	850		
			$V_{CC} = \pm 15\ \text{V}$	$V_{CC} = \pm 15\ \text{V}$	950		
		$V_O = 16\ \text{V}_{PP}$	$V_{CC} = \pm 12\ \text{V}$	$V_{CC} = \pm 12\ \text{V}$	1500		
			$V_{CC} = \pm 15\ \text{V}$	$V_{CC} = \pm 15\ \text{V}$	1700		
				$V_{CC} = \pm 15\ \text{V}$	$V_{CC} = \pm 15\ \text{V}$	1700	

NOTE 2: Slew rate is defined from the 25% to the 75% output levels.

noise/distortion performance

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
THD	Total harmonic distortion (single-ended configuration)	Gain = 8, $R_L = 100\ \Omega$, $V_{CC} = \pm 12\ \text{V}$, $f = 250\ \text{kHz}$	$V_O(pp) = 2\ \text{V}$	–83		dBc	
			$V_O(pp) = 16\ \text{V}$	–78			
		Gain = 8, $R_L = 50\ \Omega$, $V_{CC} = \pm 5\ \text{V}$, $f = 250\ \text{kHz}$	$V_O(pp) = 2\ \text{V}$	–74			
			$V_O(pp) = 6\ \text{V}$	–72			
V_n	Input voltage noise	$V_{CC} = \pm 5\ \text{V}$, $f = 10\ \text{kHz}$, $\pm 12\ \text{V}$		2.1		nV/ $\sqrt{\text{Hz}}$	
I_n	Input current noise	+Input	$f = 10\ \text{kHz}$, $V_{CC} = \pm 5\ \text{V}$, $V_{CC} = \pm 12\ \text{V}$, $V_{CC} = \pm 15\ \text{V}$	2.7		pA/ $\sqrt{\text{Hz}}$	
		–Input		10.7			
X_T	Crosstalk	$f = 250\ \text{kHz}$, G = 2, $R_L = 100\ \Omega$	$V_{CC} = \pm 12\ \text{V}$, $R_L = 100\ \Omega$	$V_O = 2\ \text{V}_{p-p}$	–79		dBc
		$f = 250\ \text{kHz}$, G = 2, $R_L = 50\ \Omega$	$V_{CC} = \pm 5\ \text{V}$, $R_L = 50\ \Omega$	$V_O = 2\ \text{V}_{p-p}$	–71		

THS6052, THS6053

175 mA, ± 12 V ADSL CPE LINE DRIVERS

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electrical characteristics over recommended operating free-air temperature range, $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 12$ V, $R_{FEEDBACK} = 750\ \Omega$, $R_L = 100\ \Omega$ (unless otherwise noted) (continued)

dc performance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OS}	Input offset voltage	$V_{CC} = \pm 12$ V, $V_{CC} = \pm 6$ V	$T_A = 25^\circ\text{C}$	5	10	mV
			$T_A = \text{full range}$		15	
	Differential offset voltage		$T_A = 25^\circ\text{C}$	3	6	
			$T_A = \text{full range}$		8	
Offset drift		$T_A = \text{full range}$		30	$\mu\text{V}/^\circ\text{C}$	
I _{IB}	– Input bias current	$V_{CC} = \pm 12$ V, $V_{CC} = \pm 6$ V	$T_A = 25^\circ\text{C}$	5	10	μA
			$T_A = \text{full range}$		12	
	+ Input bias current		$T_A = 25^\circ\text{C}$	2	5	
			$T_A = \text{full range}$		6	
	Differential input bias current		$T_A = 25^\circ\text{C}$	5	10	
$T_A = \text{full range}$			12			
Z _{OL}	Open loop transimpedance	$V_{CC} = \pm 12$ V, $V_{CC} = \pm 6$ V	$R_L = 1\ \text{k}\Omega$,	1		M Ω

input characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{ICR}	Input common-mode voltage range	$V_{CC} = \pm 12$ V	± 9.7	± 10.1		V
		$V_{CC} = \pm 6$ V	± 3.8	± 4.2		
CMRR	Common-mode rejection ratio	$V_{CC} = \pm 12$ V, $V_{CC} = \pm 6$ V	$T_A = 25^\circ\text{C}$	59	66	dB
			$T_A = \text{full range}$	57		
R _I	Input resistance	+ Input		1.5		M Ω
		– Input		15		Ω
C _I	Input capacitance			2		pF

output characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _O	Output voltage swing	$R_L = 50\ \Omega$, $V_{CC} = \pm 6$ V		± 4.2	± 4.6	V
			Single ended			
		$R_L = 100\ \Omega$	$V_{CC} = \pm 12$ V	± 10.1	± 10.5	
		$V_{CC} = \pm 6$ V	± 4.4	± 4.8		
I _O	Output current	$R_L = 25\ \Omega$, $V_{CC} = \pm 12$ V	150	175	mA	
		$R_L = 10\ \Omega$, $V_{CC} = \pm 6$ V	150	175		
I _{SC}	Short-circuit current	$R_L = 0\ \Omega$, $V_{CC} = \pm 12$ V		250		mA
	Output resistance	Open loop		14		Ω



THS6052, THS6053

175 mA, ±12 V ADSL CPE LINE DRIVERS

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electrical characteristics over recommended operating free-air temperature range, $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 12\text{ V}$, $R_{FEEDBACK} = 750\ \Omega$, $R_L = 100\ \Omega$ (unless otherwise noted) (continued)

power supply

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{CC}	Operating range	Dual supply		±4.5		±16.5	V
		Single supply		9		33	
I_{CC}	Quiescent current (each driver)	$V_{CC} = \pm 12\text{ V}$	$T_A = 25^\circ\text{C}$		5.2	7	mA
			$T_A = \text{full range}$			8	
		$V_{CC} = \pm 6\text{ V}$	$T_A = 25^\circ\text{C}$		4.5	6.5	
			$T_A = \text{full range}$			7.5	
PSRR	Power supply rejection ratio	$V_{CC} = \pm 12\text{ V}$	$T_A = 25^\circ\text{C}$	-64	-62		dB
			$T_A = \text{full range}$		-61	-	
		$V_{CC} = \pm 6\text{ V}$	$T_A = 25^\circ\text{C}$	-60	-70		
			$T_A = \text{full range}$		-58		

shutdown characteristics (THS6053 only)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{IL}(\text{SHDN})$	Shutdown pin voltage for power up	$V_{CC} = \pm 6\text{ V}, \pm 12\text{ V}$ GND = 0 V, (GND Pin as Reference)				0.8	V
$V_{IH}(\text{SHDN})$	Shutdown pin voltage for power down	$V_{CC} = \pm 6\text{ V}, \pm 12\text{ V}$, GND = 0 V, (GND Pin as Reference)		2			V
$I_{CC}(\text{SHDN})$	Total quiescent current when in shutdown state	$V_{GND} = 0\text{ V}$, $V_{CC} = \pm 6\text{ V}, \pm 12\text{ V}$			0.3	0.7	mA
t_{DIS}	Disable time (see Note 3)	$V_{CC} = \pm 12\text{ V}$			0.1		μs
t_{EN}	Enable time (see Note 3)	$V_{CC} = \pm 12\text{ V}$			0.4		μs
$I_{IL}(\text{SHDN})$	Shutdown pin input bias current for power up	$V_{CC} = \pm 6\text{ V}, \pm 12\text{ V}$			40	100	μA
$I_{IH}(\text{SHDN})$	Shutdown pin input bias current for power down	$V_{CC} = \pm 6\text{ V}, \pm 12\text{ V}$, $V(\text{SHDN}) = 3.3\text{ V}$			50	100	μA

NOTE 3: Disable/enable time is defined as the time from when the shutdown signal is applied to the SHDN pin to when the supply current has reached half of its final value.



THS6052, THS6053 175 mA, ± 12 V ADSL CPE LINE DRIVERS

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APPLICATION INFORMATION

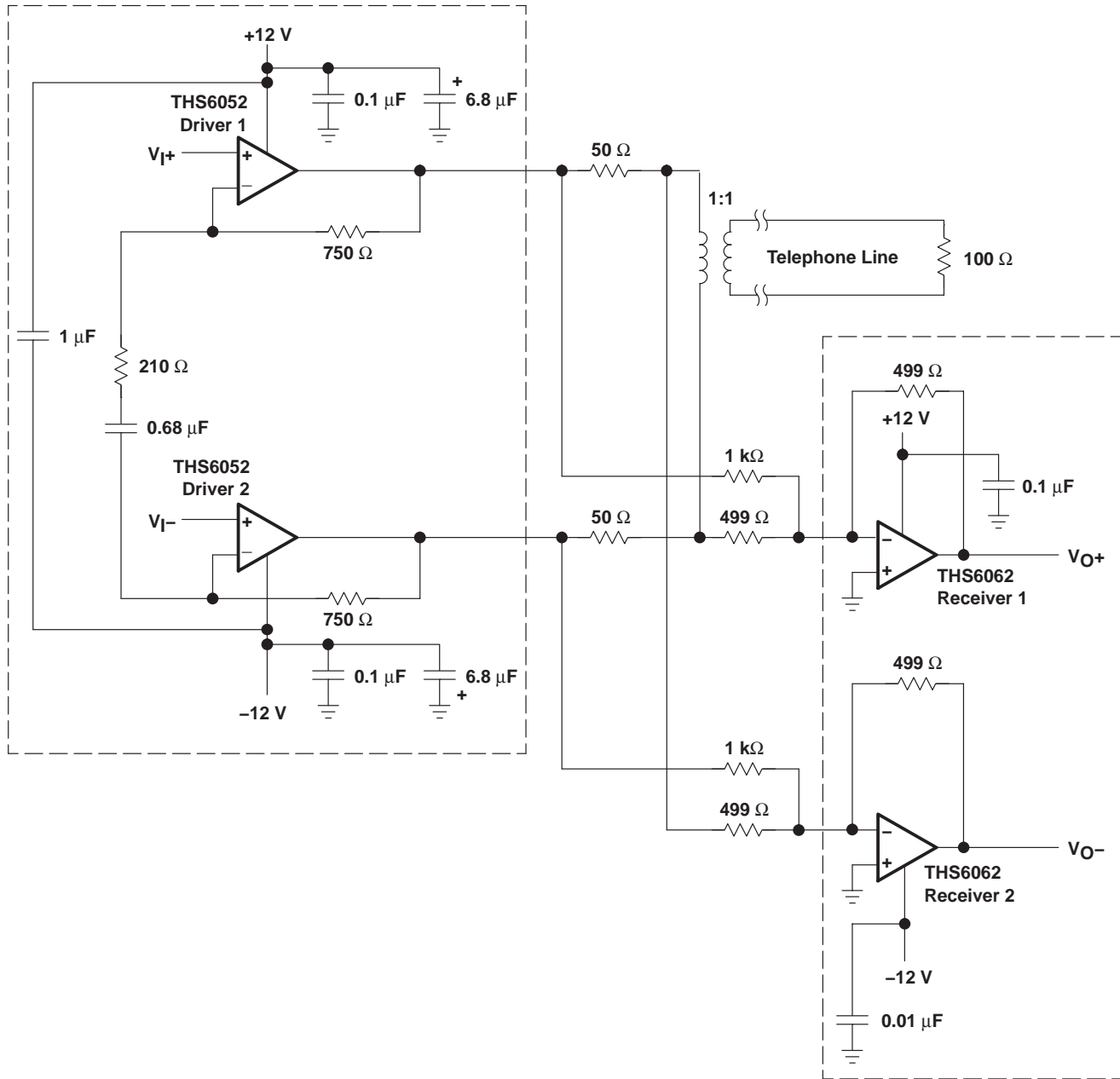


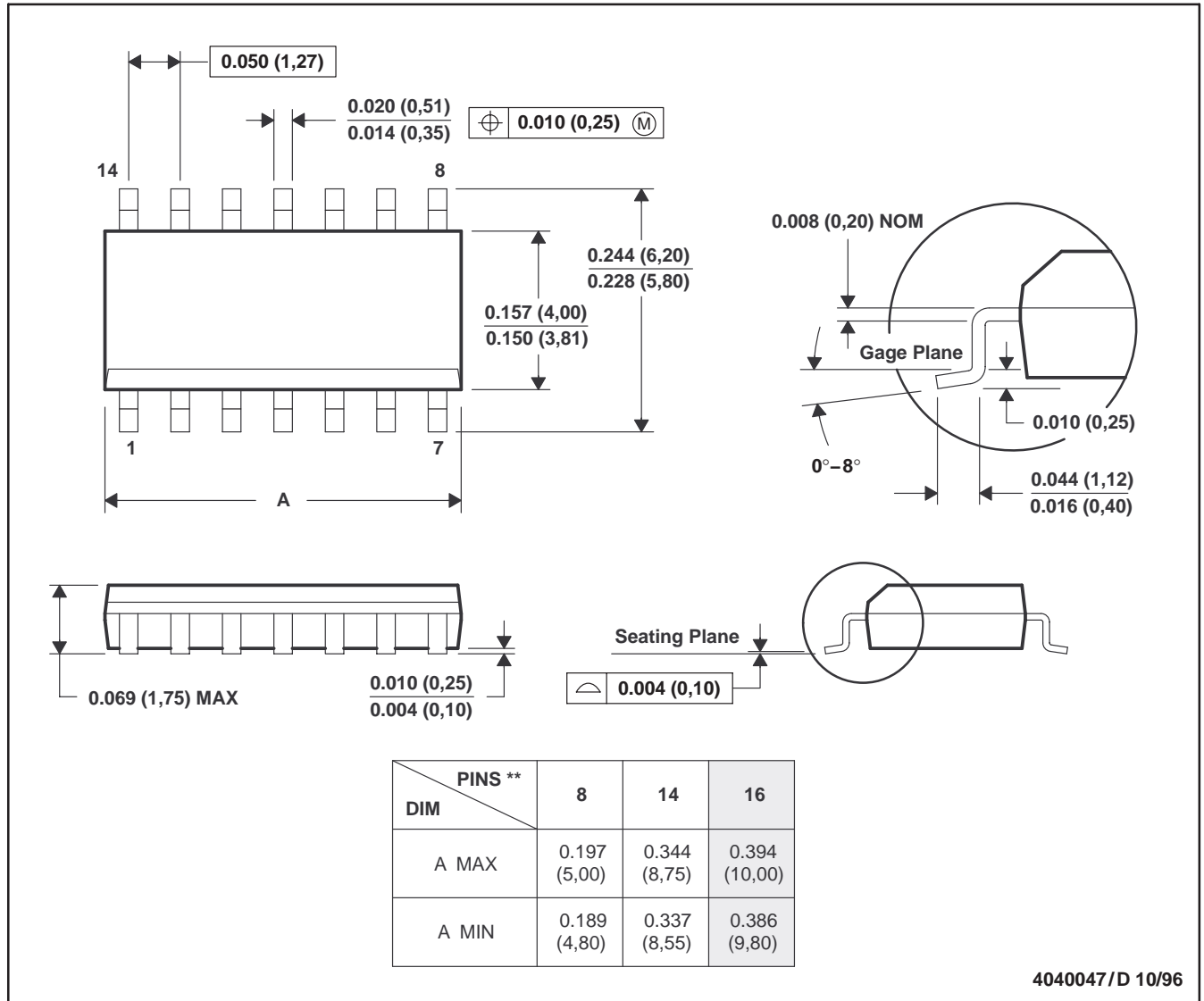
Figure 1. THS6052 ADSL Application With 1:1 Transformer Ratio

MECHANICAL DATA

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

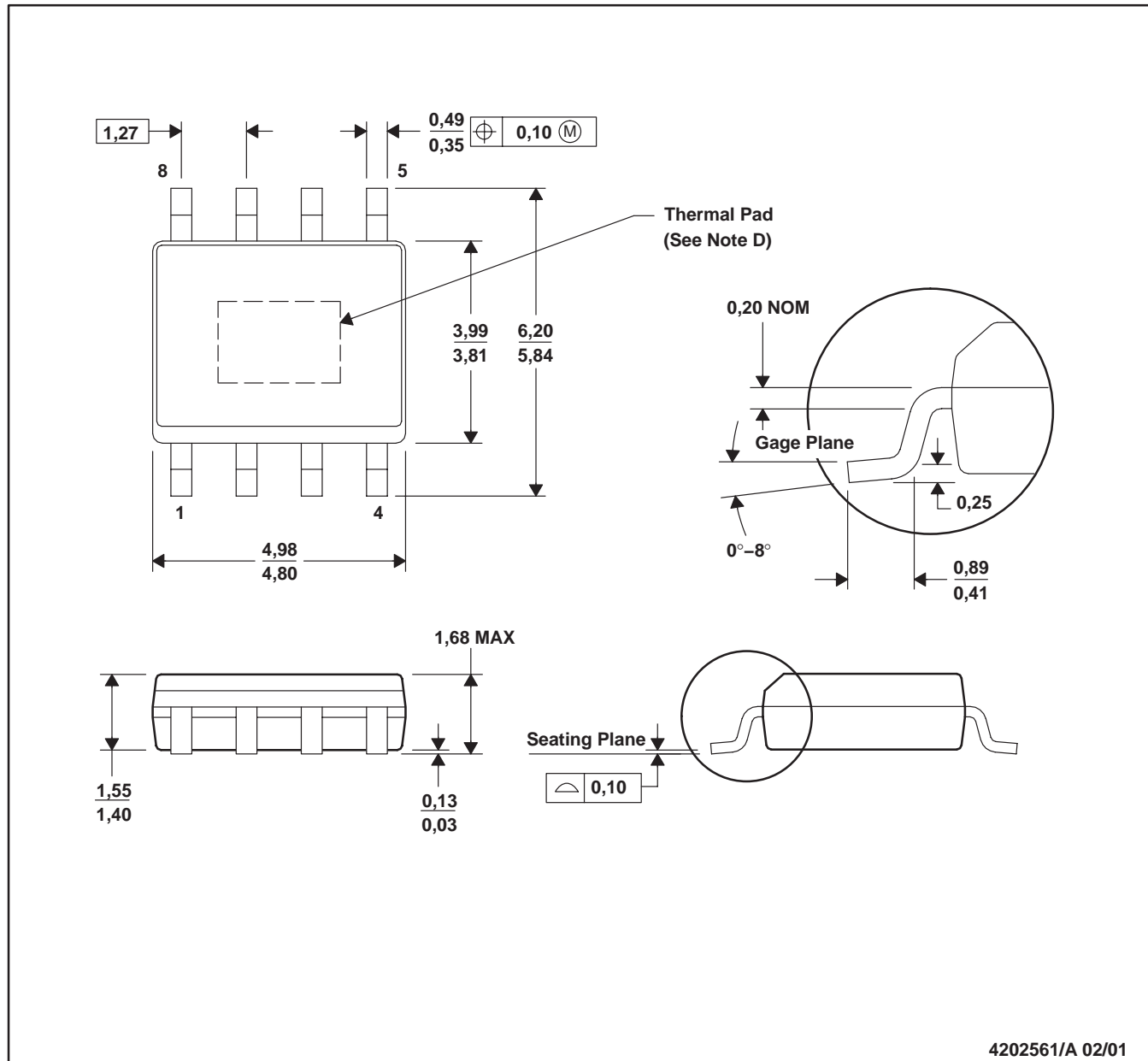
THS6052, THS6053 175 mA, ±12 V ADSL CPE LINE DRIVERS

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MECHANICAL DATA

DDA (S-PDSO-G8)

Power PAD™ PLASTIC SMALL-OUTLINE



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.

PowerPAD is a trademark of Texas Instruments.



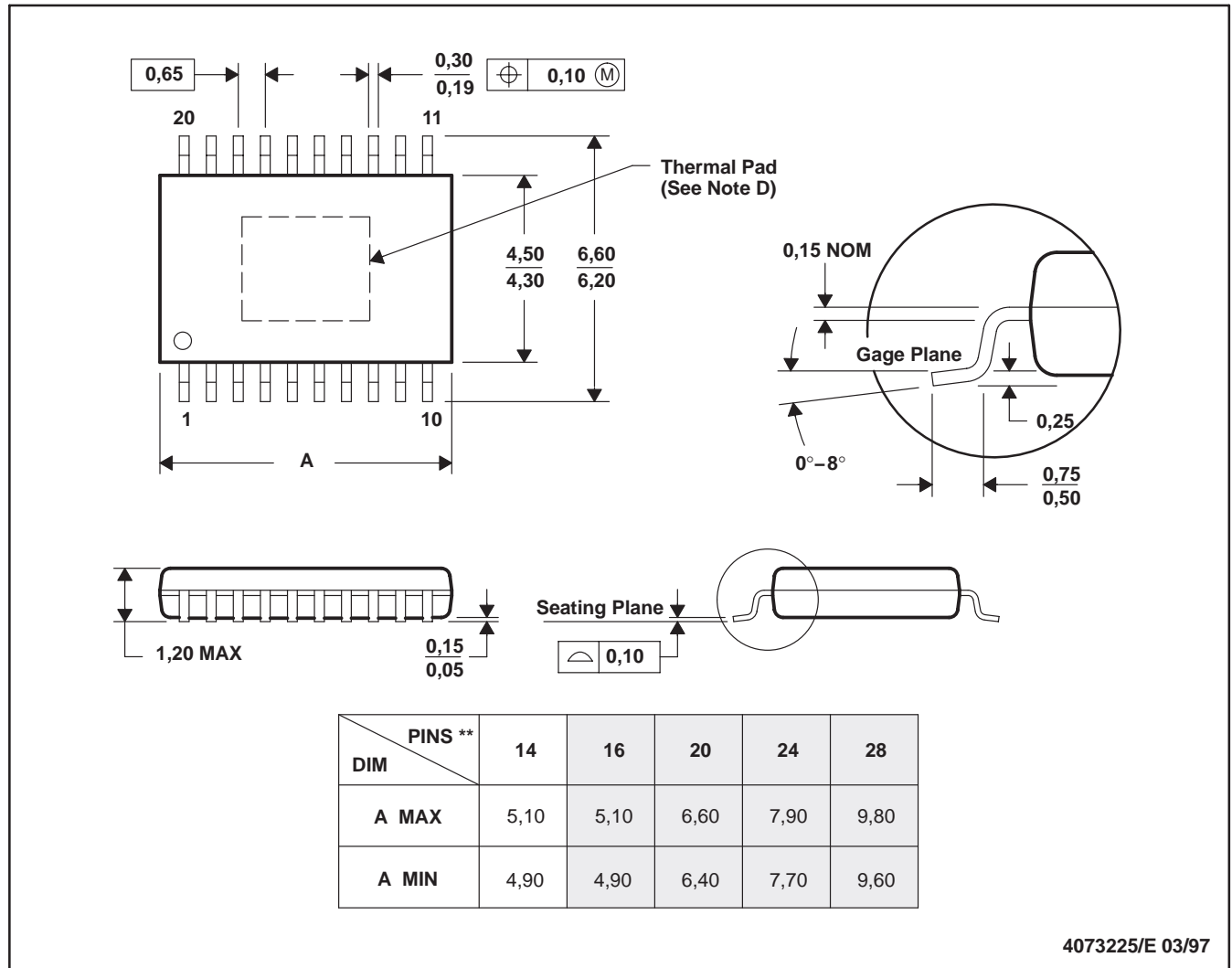
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MECHANICAL INFORMATION

PWP (R-PDSO-G**)

PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE

20-PIN SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusions.
 D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
 E. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
THS6052CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS6052CDDA	ACTIVE	SO Power PAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM
THS6052CDDAG3	ACTIVE	SO Power PAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM
THS6052CDDAR	ACTIVE	SO Power PAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM
THS6052CDDARG3	ACTIVE	SO Power PAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM
THS6052CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS6052CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS6052CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS6052ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS6052IDDA	ACTIVE	SO Power PAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM
THS6052IDDAG3	ACTIVE	SO Power PAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM
THS6052IDDAR	ACTIVE	SO Power PAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM
THS6052IDDARG3	ACTIVE	SO Power PAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM
THS6052IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS6052IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS6052IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS6053CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS6053CDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS6053CDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS6053CDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS6053CPWP	ACTIVE	HTSSOP	PWP	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS6053CPWPG4	ACTIVE	HTSSOP	PWP	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
						no Sb/Br)		
THS6053CPWPR	ACTIVE	HTSSOP	PWP	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS6053CPWPRG4	ACTIVE	HTSSOP	PWP	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS6053ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS6053IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS6053IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS6053IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS6053IPWP	ACTIVE	HTSSOP	PWP	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS6053IPWPG4	ACTIVE	HTSSOP	PWP	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS6053IPWPR	ACTIVE	HTSSOP	PWP	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS6053IPWPRG4	ACTIVE	HTSSOP	PWP	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



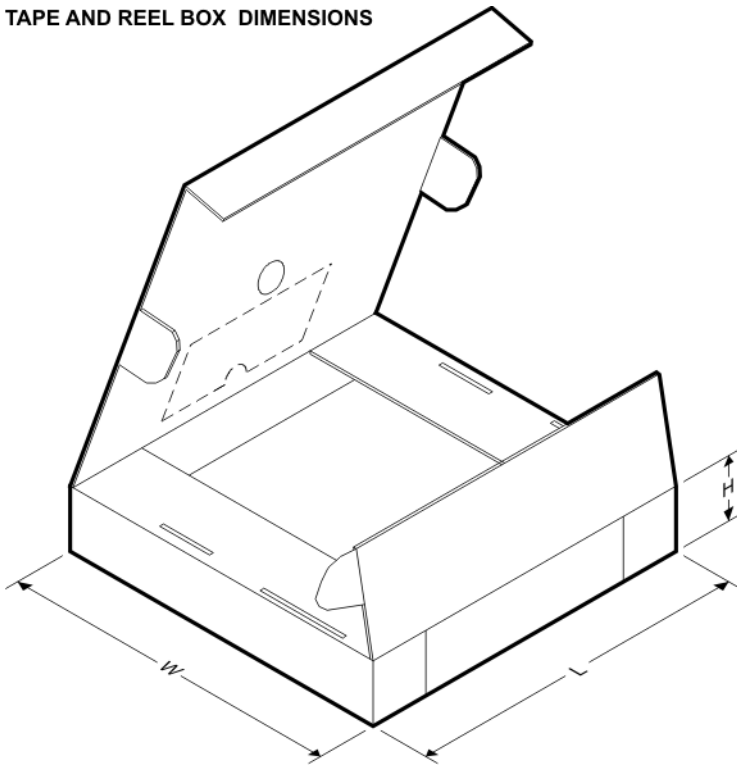
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS6052CDDAR	SO Power PAD	DDA	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS6052CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS6052IDDAR	SO Power PAD	DDA	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS6052IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS6053CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
THS6053CPWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.67	5.4	1.6	8.0	12.0	Q1
THS6053IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
THS6053IPWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.67	5.4	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

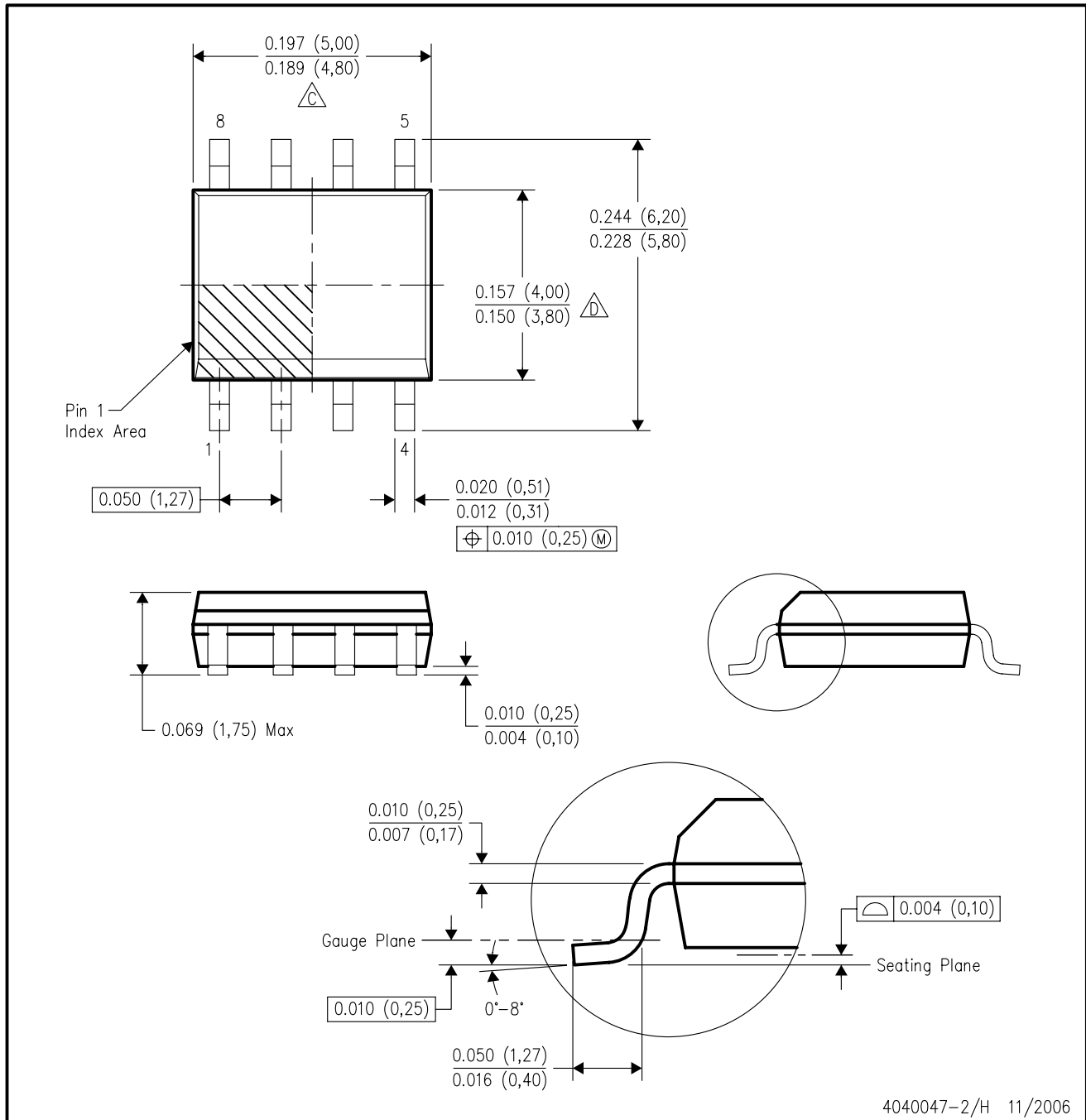


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS6052CDDAR	SO PowerPAD	DDA	8	2500	346.0	346.0	29.0
THS6052CDR	SOIC	D	8	2500	346.0	346.0	29.0
THS6052IDDAR	SO PowerPAD	DDA	8	2500	346.0	346.0	29.0
THS6052IDR	SOIC	D	8	2500	346.0	346.0	29.0
THS6053CDR	SOIC	D	14	2500	346.0	346.0	33.0
THS6053CPWPR	HTSSOP	PWP	14	2000	346.0	346.0	29.0
THS6053IDR	SOIC	D	14	2500	346.0	346.0	33.0
THS6053IPWPR	HTSSOP	PWP	14	2000	346.0	346.0	29.0

D (R-PDSO-G8)

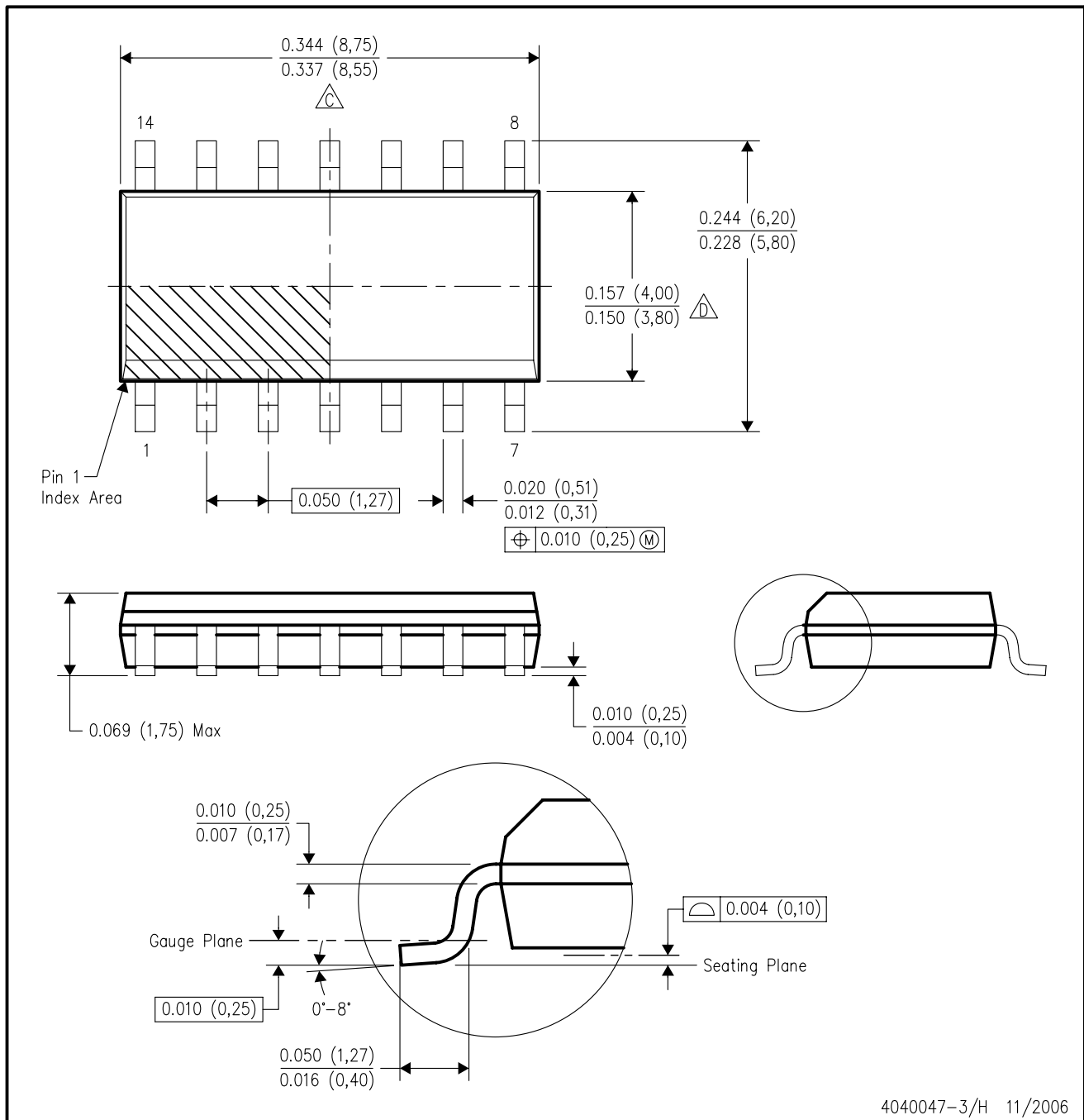
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G14)

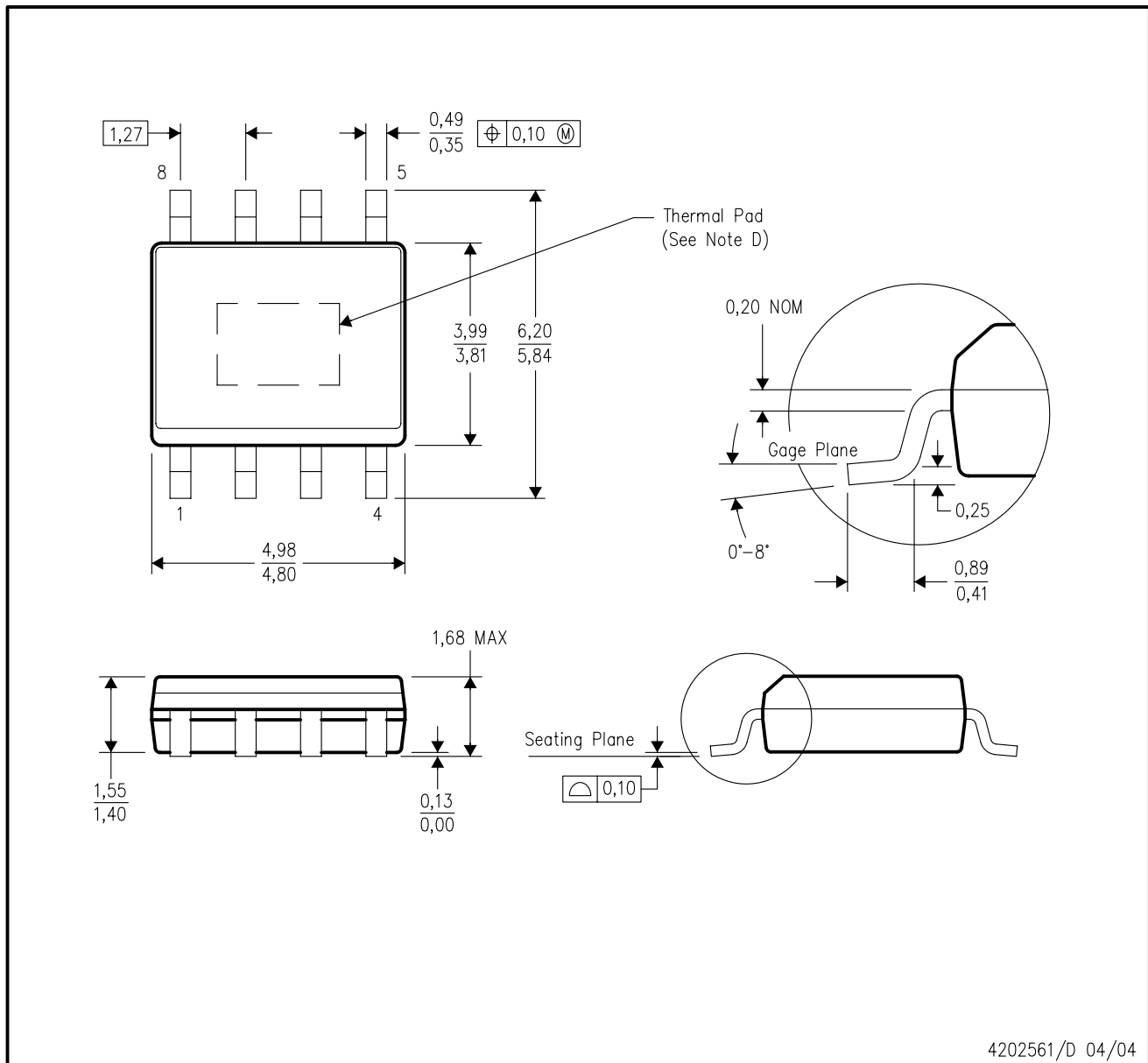
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AB.

DDA (R-PDSO-G8)

PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.

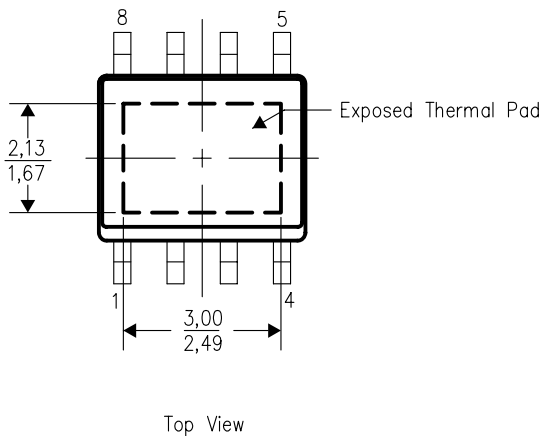
PowerPAD is a trademark of Texas Instruments.

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

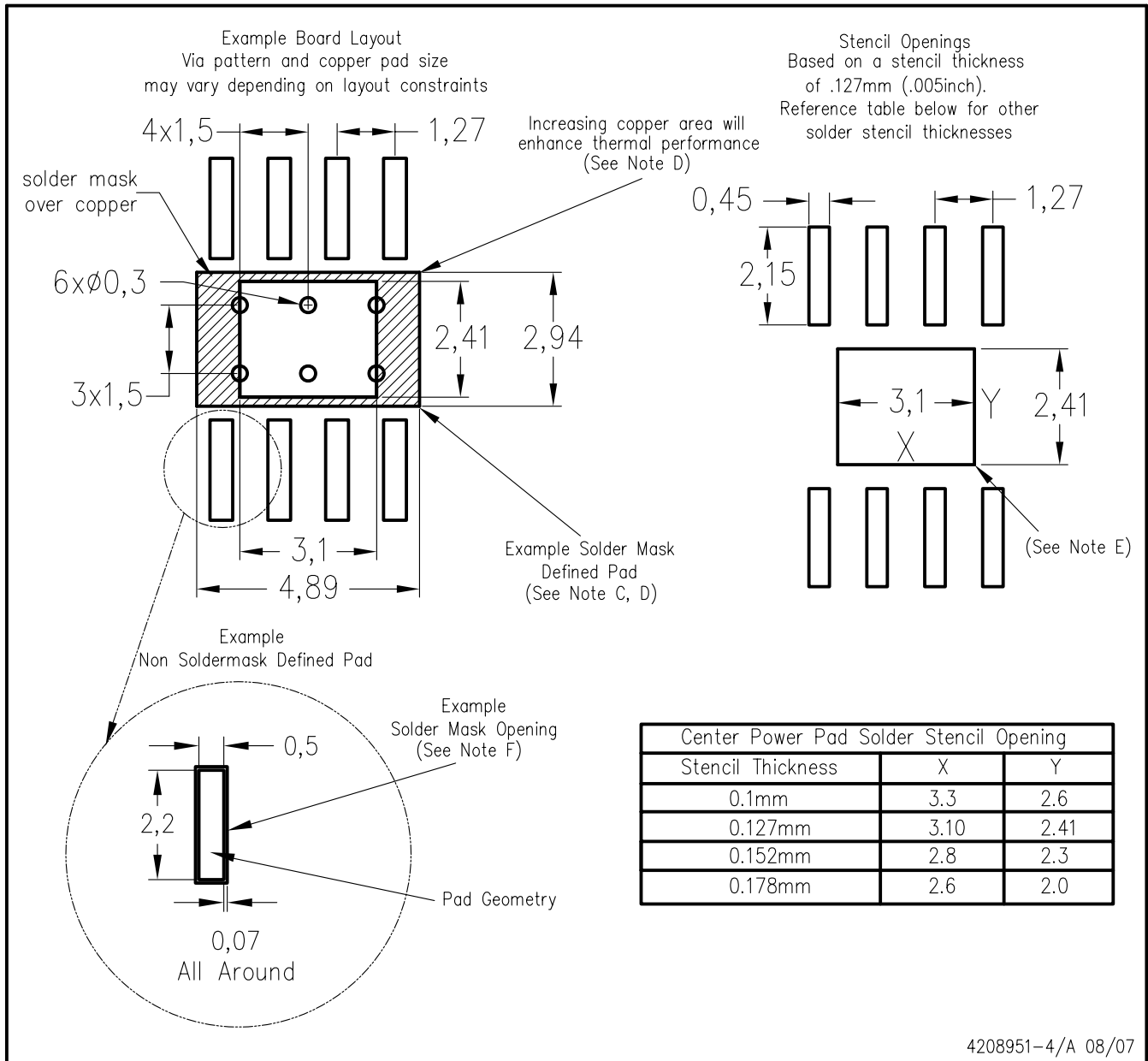
The exposed thermal pad dimensions for this package are shown in the following illustration.



NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DDA (R-PDSO-G8) PowerPAD™



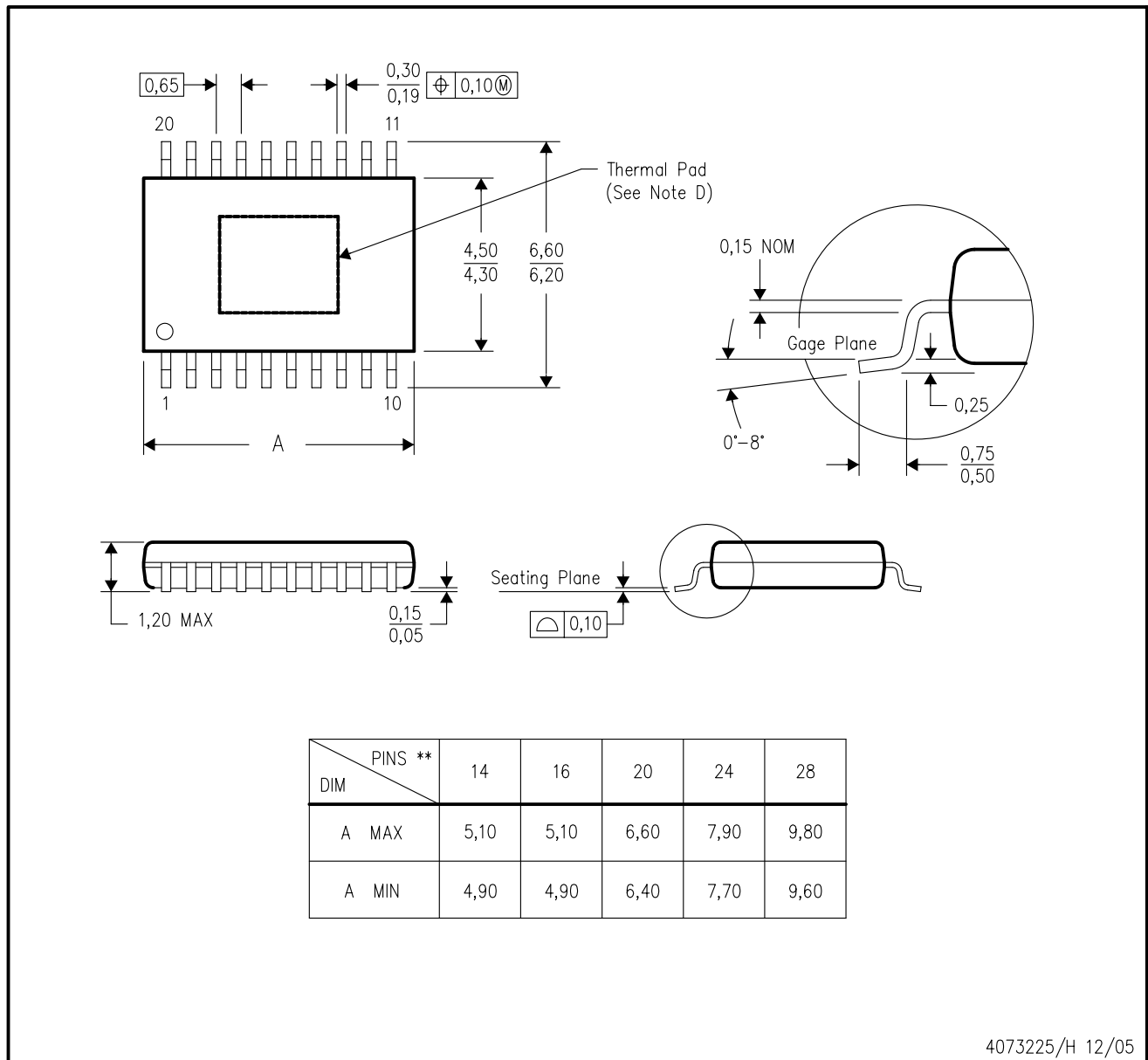
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.

PWP (R-PDSO-G**)

PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE

20 PIN SHOWN



4073225/H 12/05

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - E. Falls within JEDEC MO-153

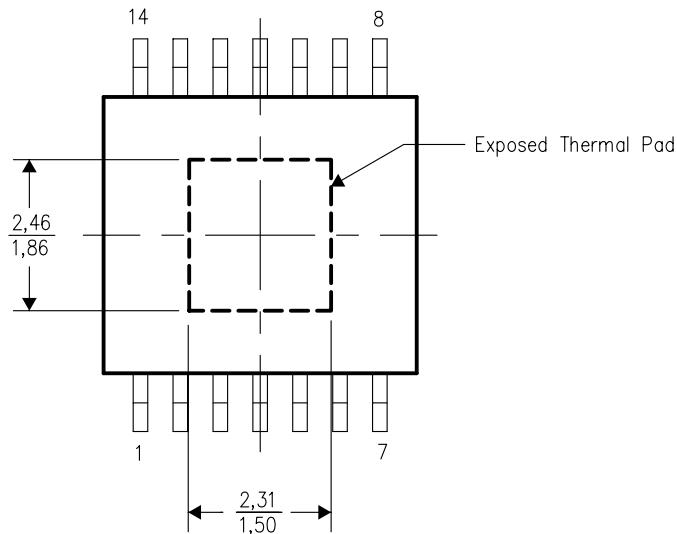
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THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

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The exposed thermal pad dimensions for this package are shown in the following illustration.

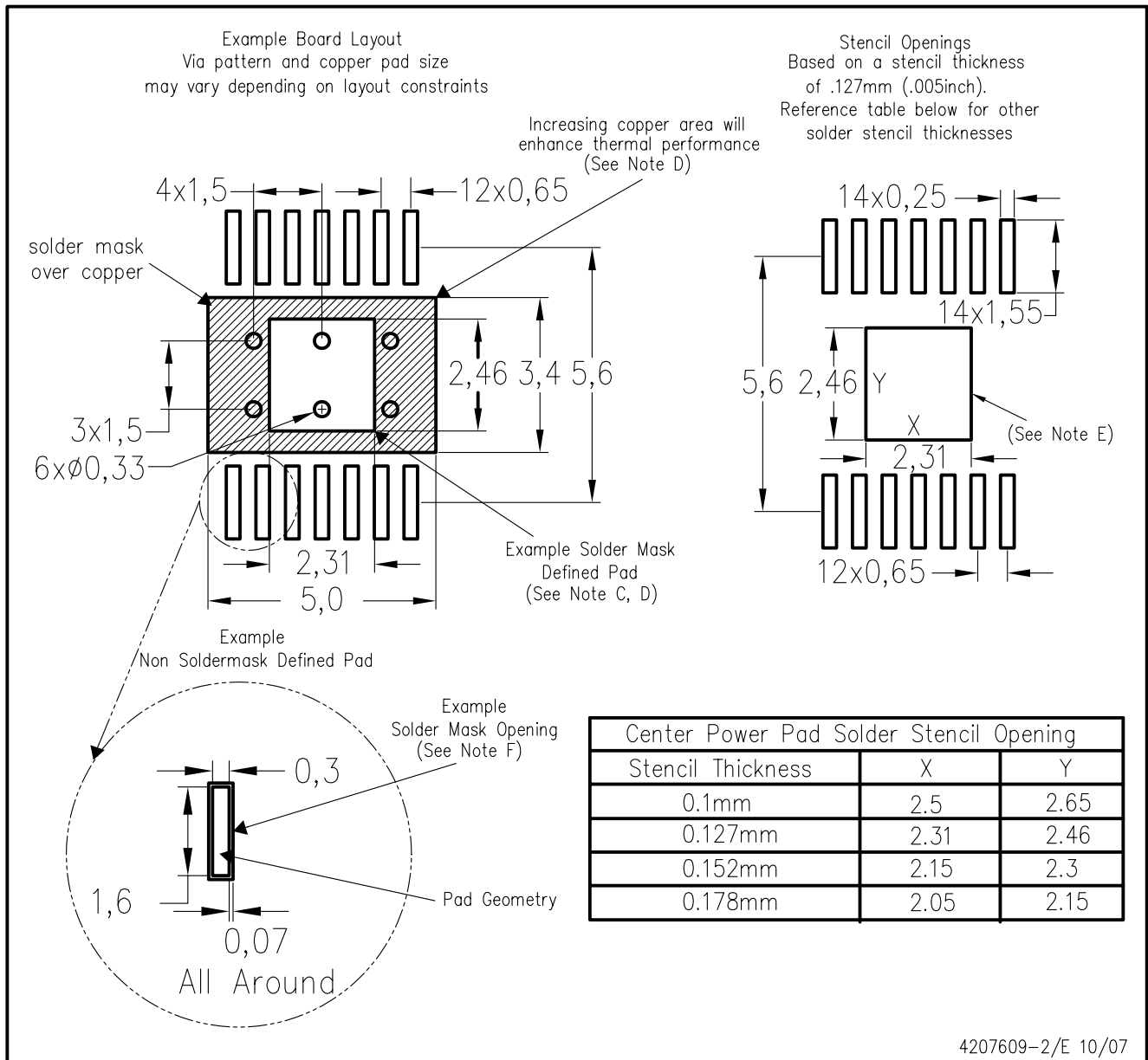


Top View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

PWP (R-PDSO-G14) PowerPAD™



4207609-2/E 10/07

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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