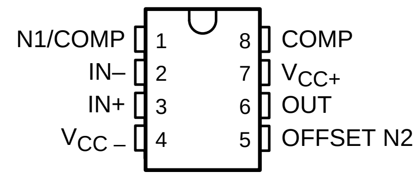
- **Low Power Consumption**
- **Wide Common-Mode and Differential Voltage Ranges**
- **Low Input-Bias and Offset Currents**
- **Output Short-Circuit Protection**
- **Low Total Harmonic Distortion . . . 0.003% Typ**
- **Low Noise . . . V_n = 18 nV/√Hz Typ at f = 1 kHz**
- **High Input Impedance . . . JFET Input Stage**
- **Common-Mode Input Voltage Range Includes V_{CC+}**
- **Latch-Up-Free Operation**
- **High Slew Rate . . . 13 V/µs Typ**

D PACKAGE
(TOP VIEW)



description

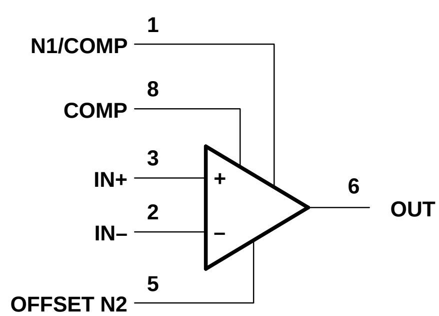
The JFET-input TL070 operational amplifier is designed as the lower-noise version of the TL080 amplifier with low input-bias and offset currents and fast slew rate. The low harmonic distortion and low noise make the TL070 ideally suited for high-fidelity and audio-preamplifier applications. This amplifier features JFET inputs (for high input impedance) coupled with bipolar output stages integrated on a single monolithic chip.

The TL070I device is characterized for operation from –40°C to 85°C.

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGE SMALL OUTLINE (D)
–40°C to 85°C	10 mV	TL070ID

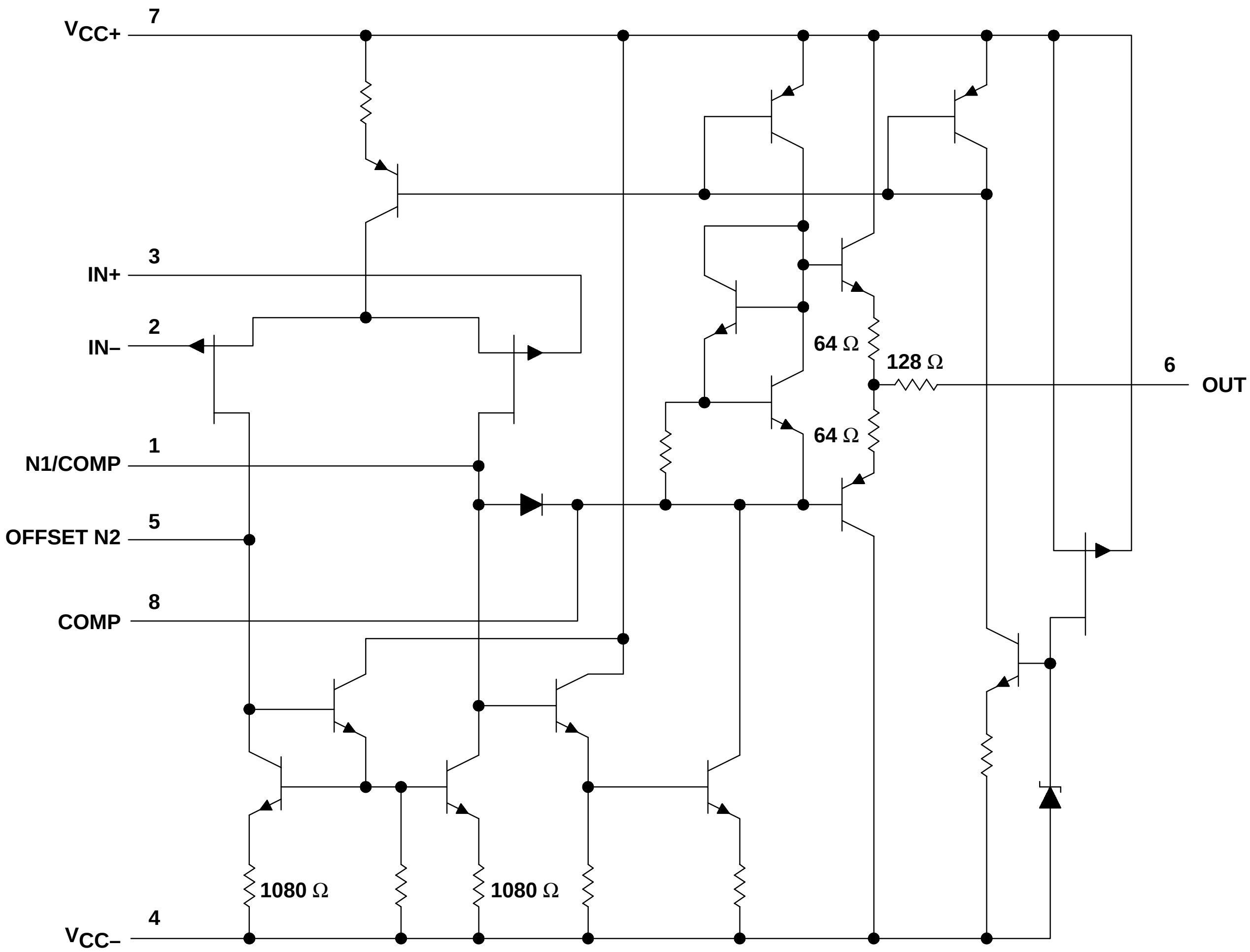
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

schematic



All component values shown are nominal.

COMPONENT COUNT†	
Transistors	13
Diodes	2
Resistors	10
epi-FET	1
JFET	2

† Includes all bias and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1)		18 V
Supply voltage, V_{CC-}		–18 V
Differential input voltage, V_{ID} (see Note 2)		±30 V
Input voltage, V_I (see Notes 1 and 3)		±15 V
Duration of short-circuit current (see Note 4)		Unlimited
Package thermal impedance, θ_{JA} (see Note 5):	D package	97°C/W
	PW package	149°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260°C
Storage temperature range, T_{stg}		–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN–.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

electrical characteristics, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	25°C		3	10	mV
			Full range			13	
$\alpha_{V_{IO}}$	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω	Full range		18		μV/°C
I_{IO}	Input offset current	V_O = 0	25°C		5	100	pA
			Full range			10	nA
I_{IB}	Input bias current‡	V_O = 0	25°C		65	200	pA
			Full range			20	nA
V_{ICR}	Common-mode input voltage range		25°C	±11	–12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±12	±13.5		V
		R_L ≥ 10 kΩ	Full range	±12			
		R_L ≥ 2 kΩ		±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 2 kΩ	25°C	25	200		V/mV
			Full range	15			
B_1	Unity-gain bandwidth		25°C		3		MHz
r_i	Input resistance		25°C		10^{12}		W
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min, V_O = 0, R_S = 50 Ω	25°C	70	100		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±9 V to ±15 V, V_O = 0, R_S = 50 Ω	25°C	70	100		dB
I_{CC}	Supply current	V_O = 0, No load	25°C		1.4	2.5	mA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100	25°C		120		dB

† All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified. Full range for T_A is –40°C to 85°C.
‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 5. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, See Figure 1		8	13		V/μs
t_r	Rise-time overshoot factor	V_I = 20 mV, R_L = 2 kΩ, C_L = 100 pF, See Figure 1			0.1		μs
					20		%
V_n	Equivalent input noise voltage	R_S = 20 Ω	f = 1 kHz		18		nV/$\sqrt{Hz}$
			f = 10 Hz to 10 kHz		4		μV
I_n	Equivalent input noise current	R_S = 20 Ω,	f = 1 kHz		0.01		pA/$\sqrt{Hz}$
THD	Total harmonic distortion	$V_{O(rms)}$ = 10 V, R_S ≤ 1 kΩ, R_L ≥ 2 kΩ,	f = 1 kHz		0.003		%

APPLICATION INFORMATION

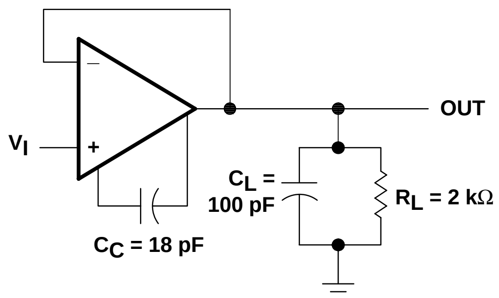


Figure 1. Unity-Gain Amplifier

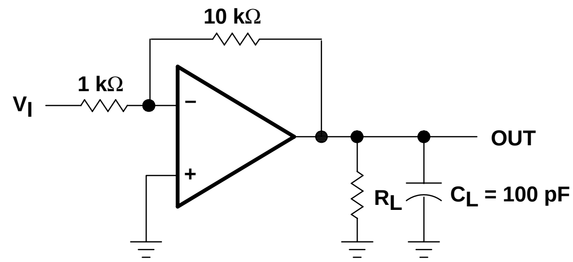


Figure 2. Gain-of-10 Inverting Amplifier

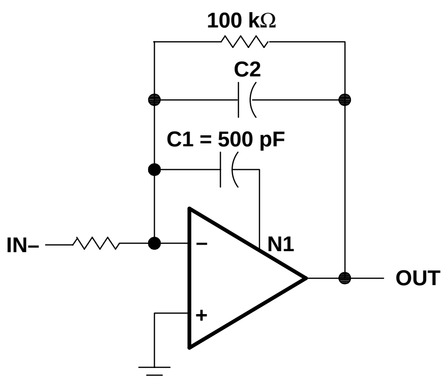


Figure 3. Feed-Forward Compensation

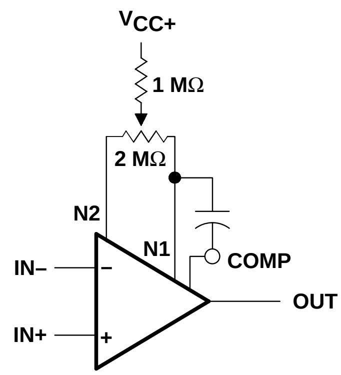


Figure 4. Input Offset Voltage Null Circuit

TYPICAL CHARACTERISTICS

Table of Graphs

	FIGURE
Input bias current vs Free-air temperature	5
Maximum peak output voltage vs Frequency	6, 7, 8
Maximum peak output voltage vs Free-air temperature	9
Maximum peak output voltage vs Load resistance	10
Maximum peak output voltage vs Supply voltage	11
Large-signal differential voltage amplification vs Free-air temperature	12
Differential voltage amplification vs Frequency with feed-forward compensation	13
Large-signal differential voltage amplification and phase shift vs Frequency	14
Normalized unity-gain bandwidth and phase shift vs Free-air temperature	15
Common-mode rejection ratio vs Free-air temperature	16
Supply current vs Supply voltage	17
Supply current vs Free-air temperature	18
Total power dissipated vs Free-air temperature	19
Normalized slew rate vs Free-air temperature	20
Equivalent input noise voltage vs Frequency	21
Total harmonic distortion vs Frequency	22
Voltage-follower large-signal pulse response	23
Output voltage vs Elapsed time	24

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

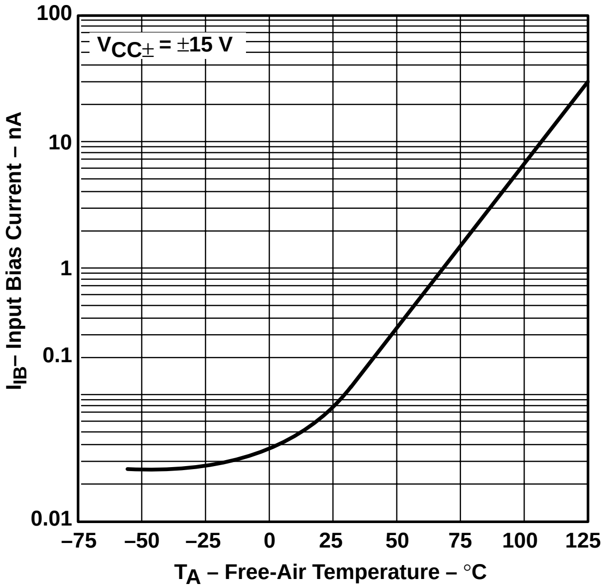


Figure 5

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

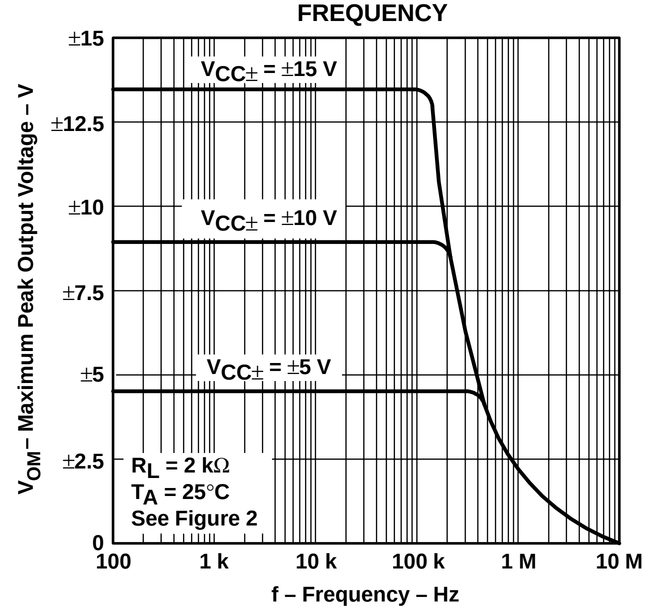


Figure 6

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

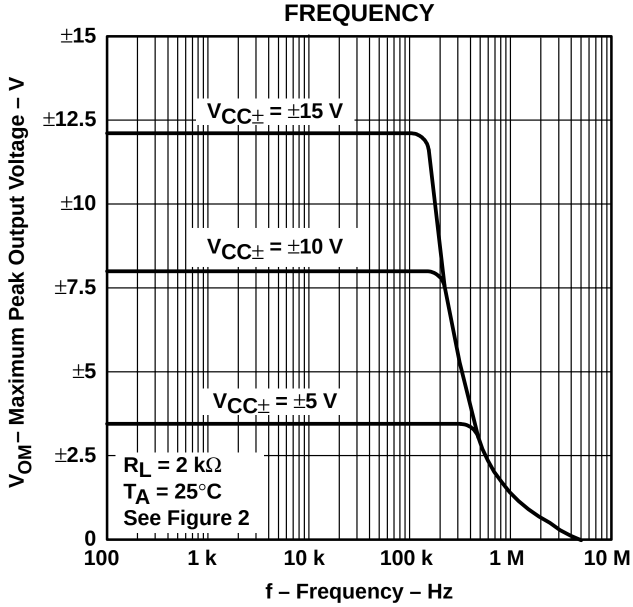


Figure 7

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

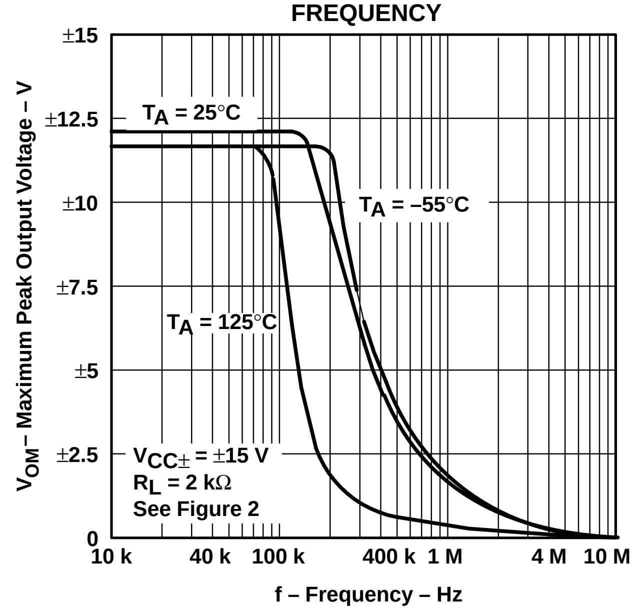


Figure 8

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. An 18-pF compensation capacitor is used.

TYPICAL CHARACTERISTICS†

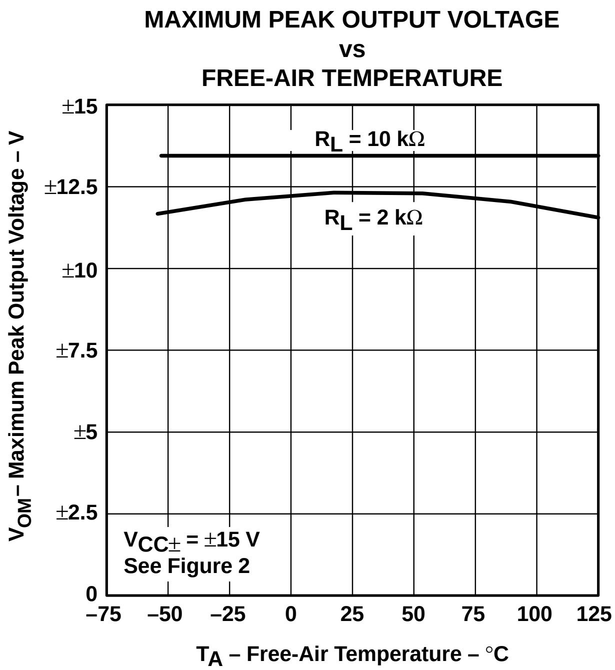


Figure 9

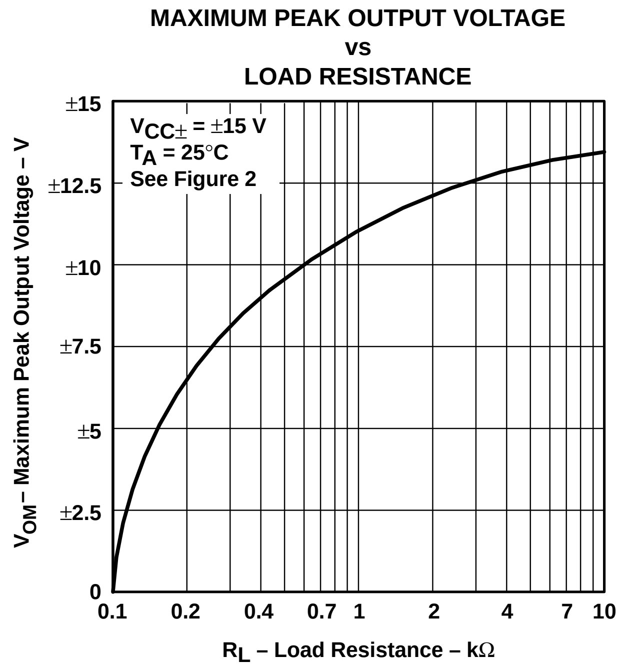


Figure 10

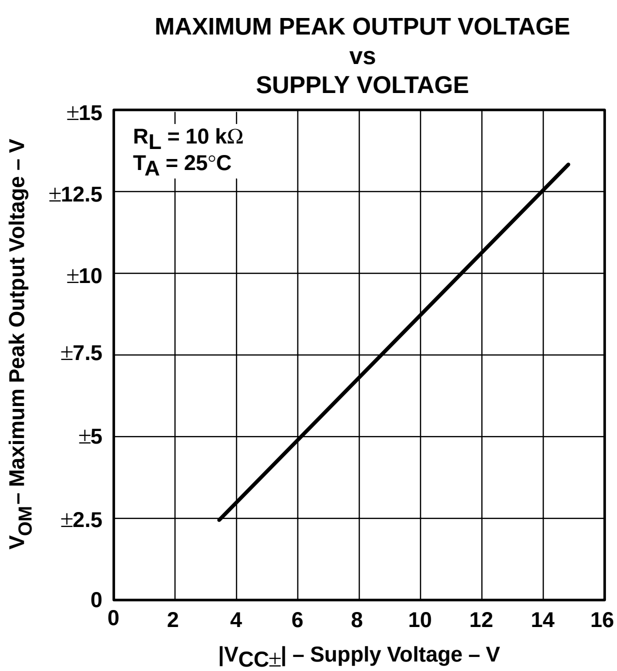


Figure 11

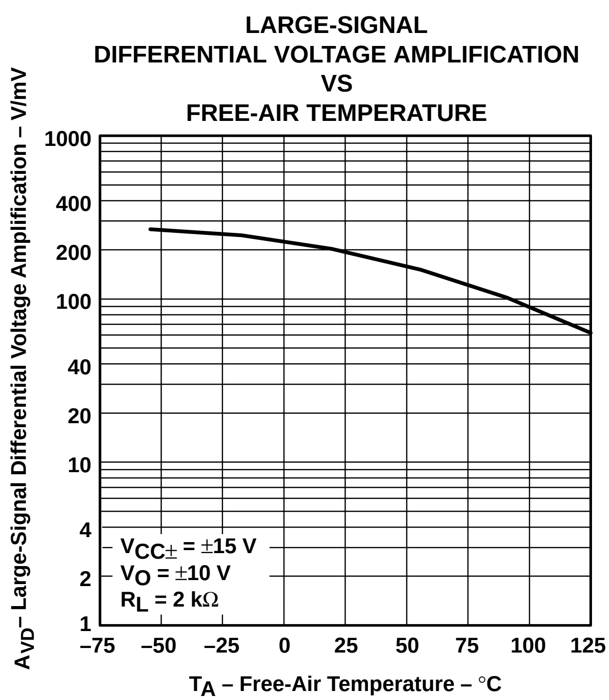


Figure 12

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. An 18-pF compensation capacitor is used.

TYPICAL CHARACTERISTICS†

DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY WITH FEED-FORWARD COMPENSATION

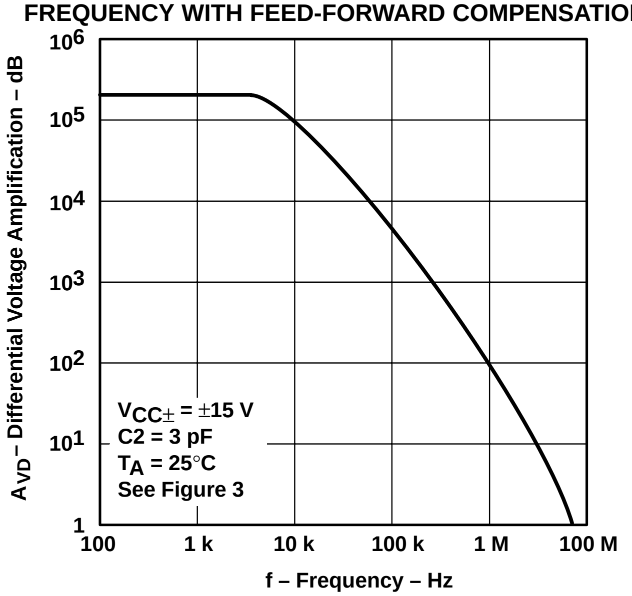


Figure 13

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

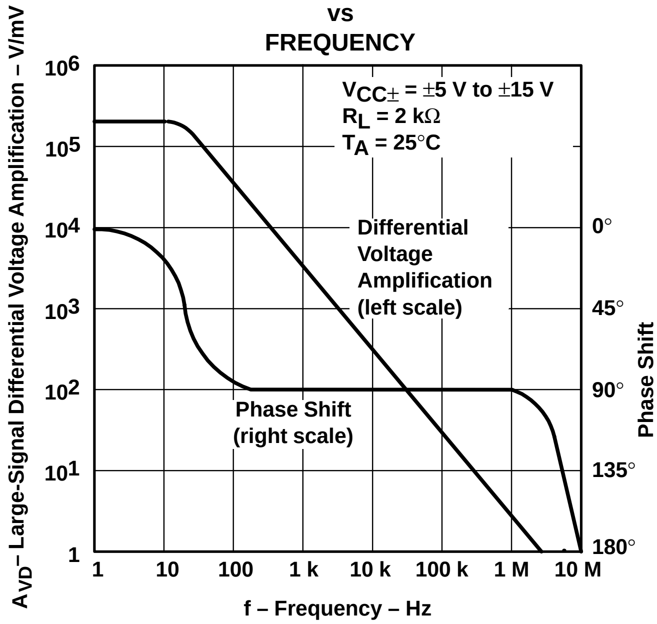


Figure 14

NORMALIZED UNITY-GAIN BANDWIDTH AND PHASE SHIFT vs FREE-AIR TEMPERATURE

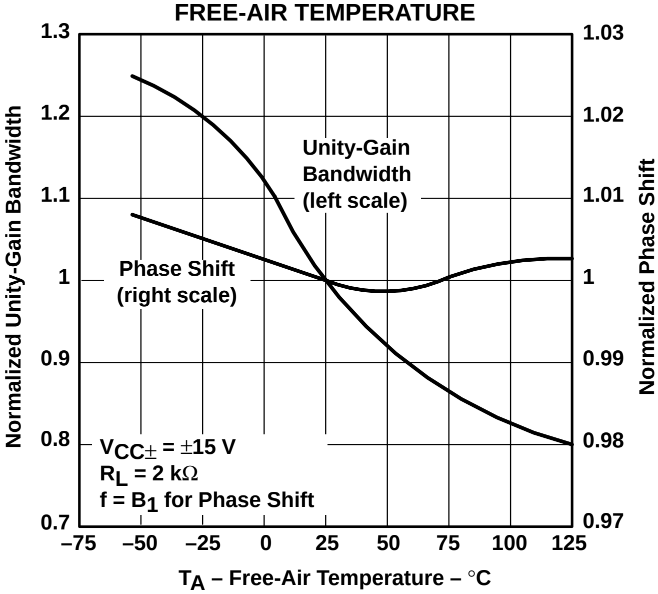


Figure 15

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

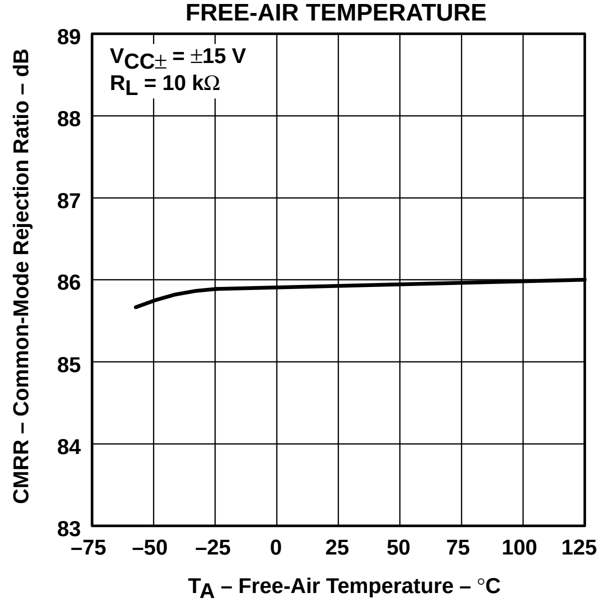


Figure 16

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. An 18-pF compensation capacitor is used.

TYPICAL CHARACTERISTICS†

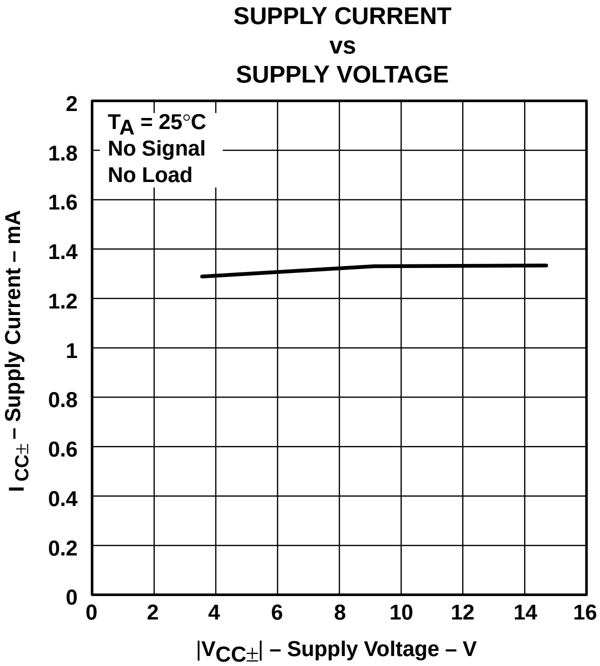


Figure 17

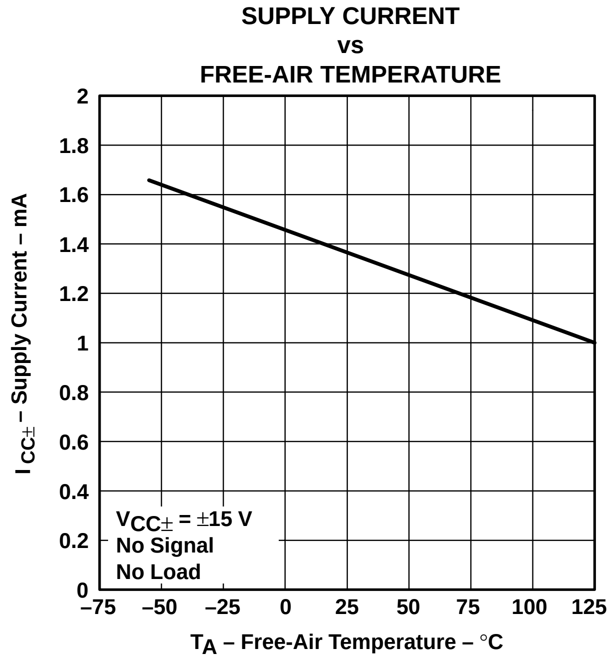


Figure 18

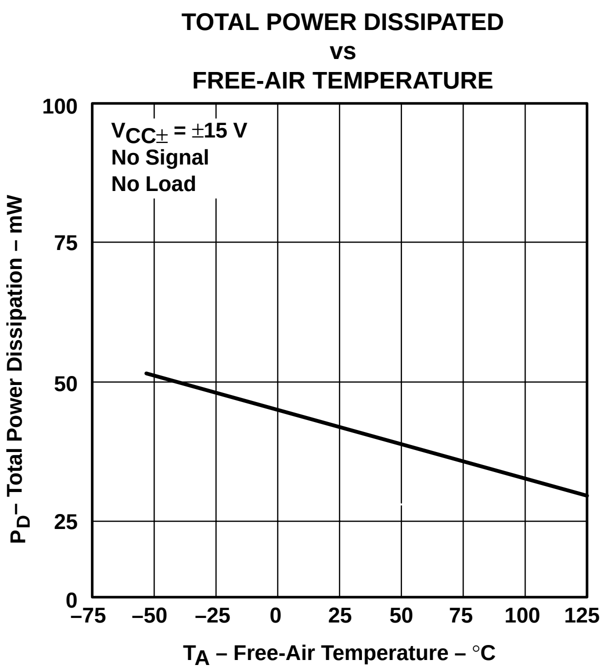


Figure 19

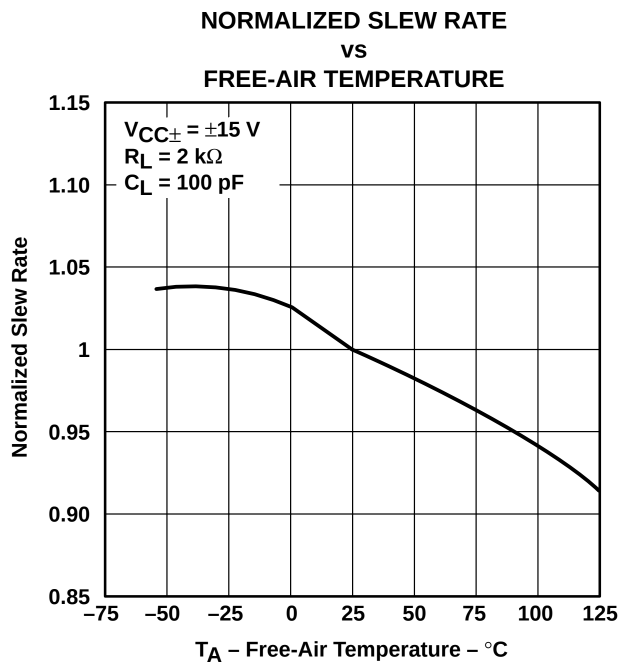


Figure 20

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. An 18-pF compensation capacitor is used.

TYPICAL CHARACTERISTICS

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

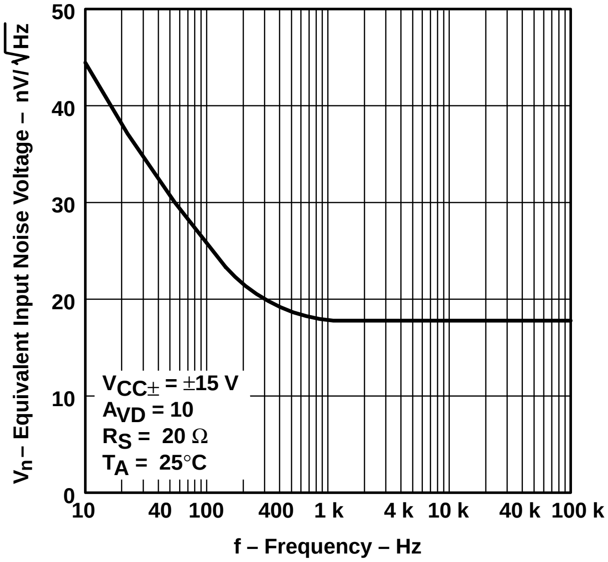


Figure 21

TOTAL HARMONIC DISTORTION vs FREQUENCY

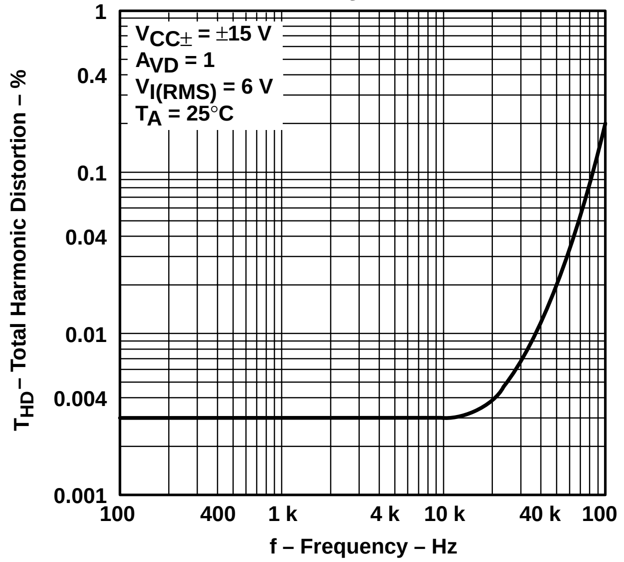


Figure 22

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

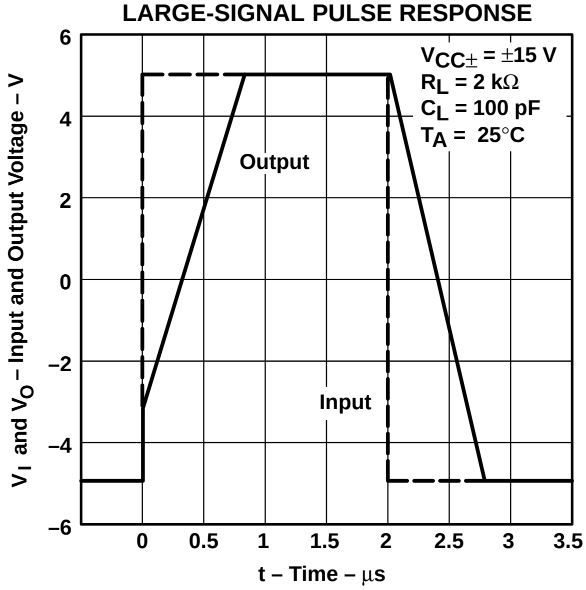


Figure 23

OUTPUT VOLTAGE vs ELAPSED TIME

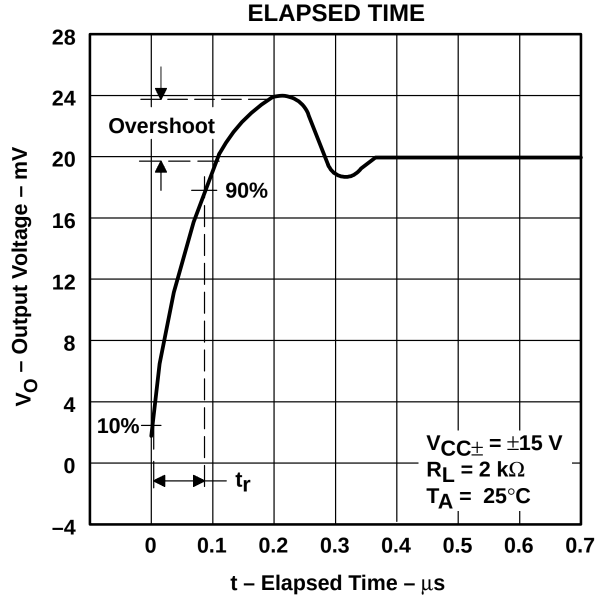


Figure 24

APPLICATION INFORMATION

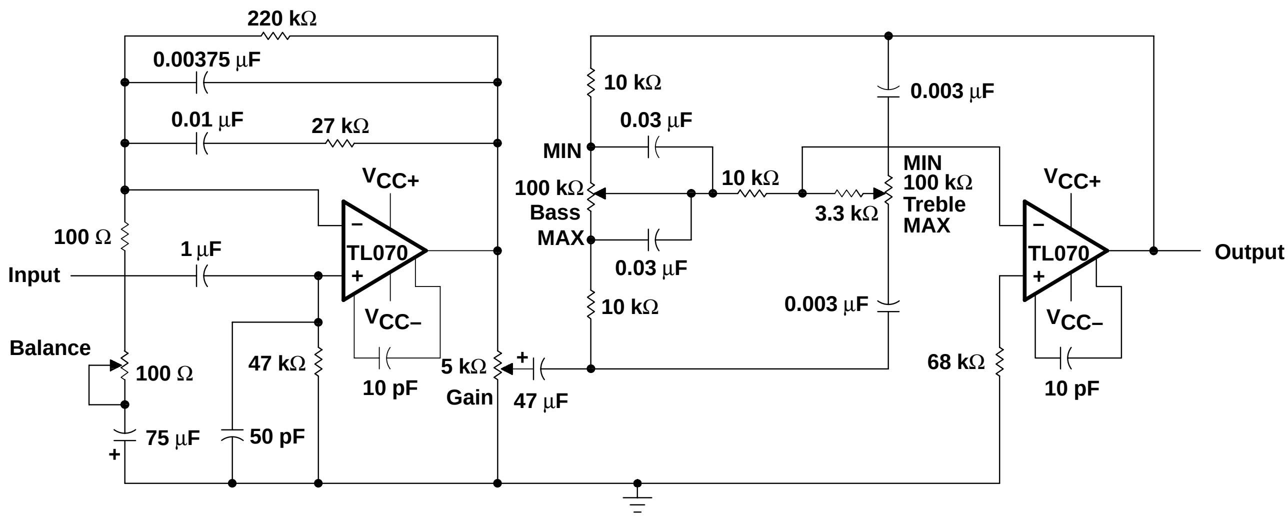


Figure 25. IC Preamplifier

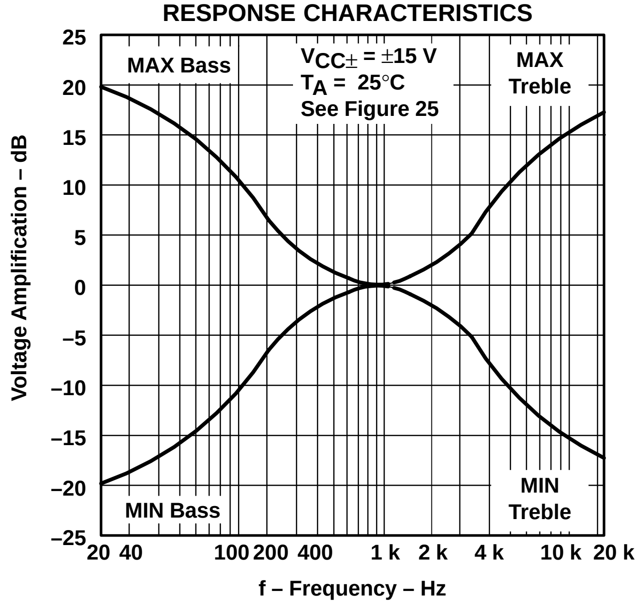


Figure 26

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		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TL070CD	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
TL070CP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
TL070IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL070IDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL070IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL070IP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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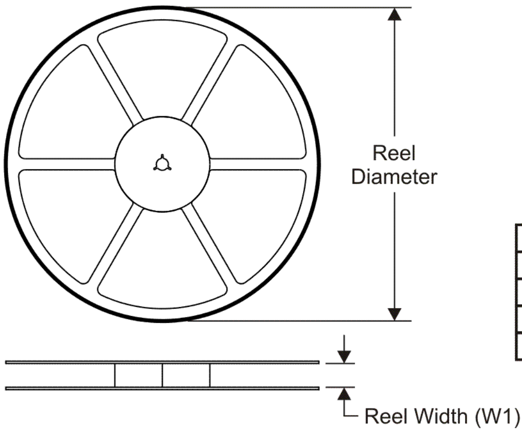
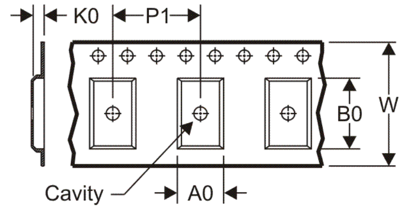
PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

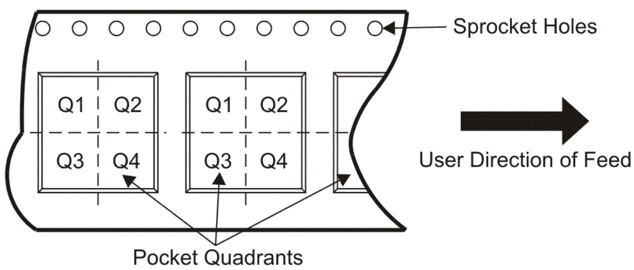


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

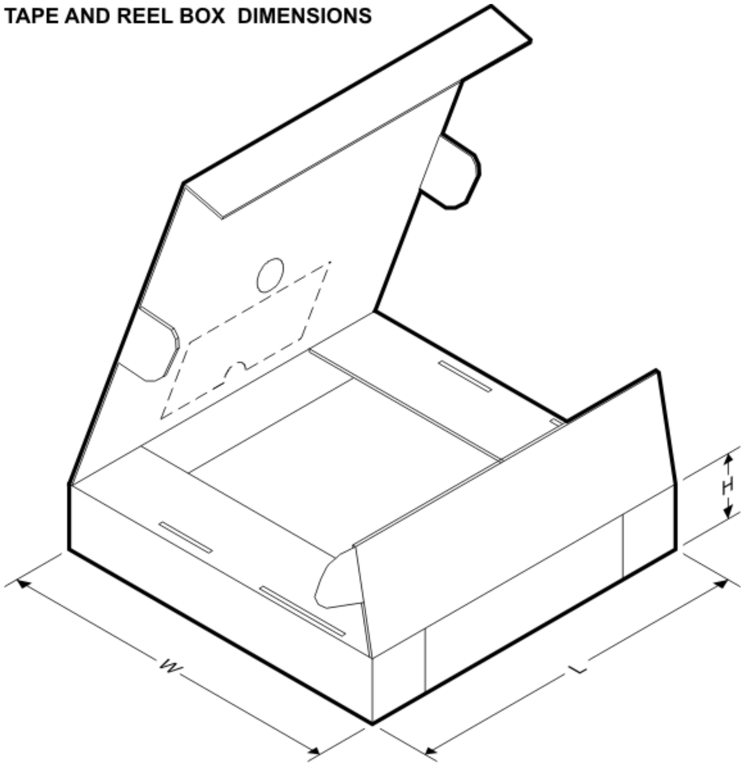
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL070IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

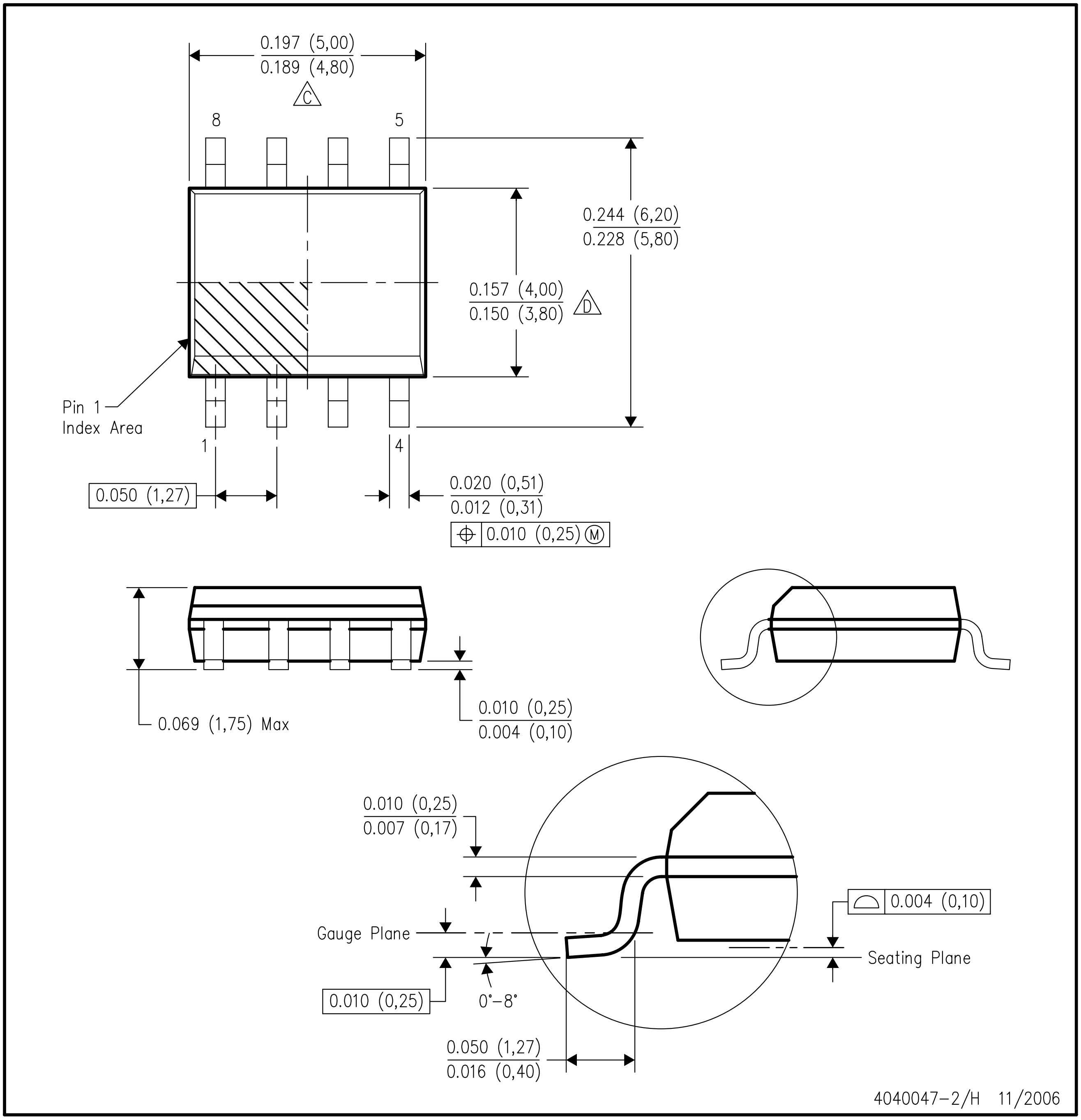
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

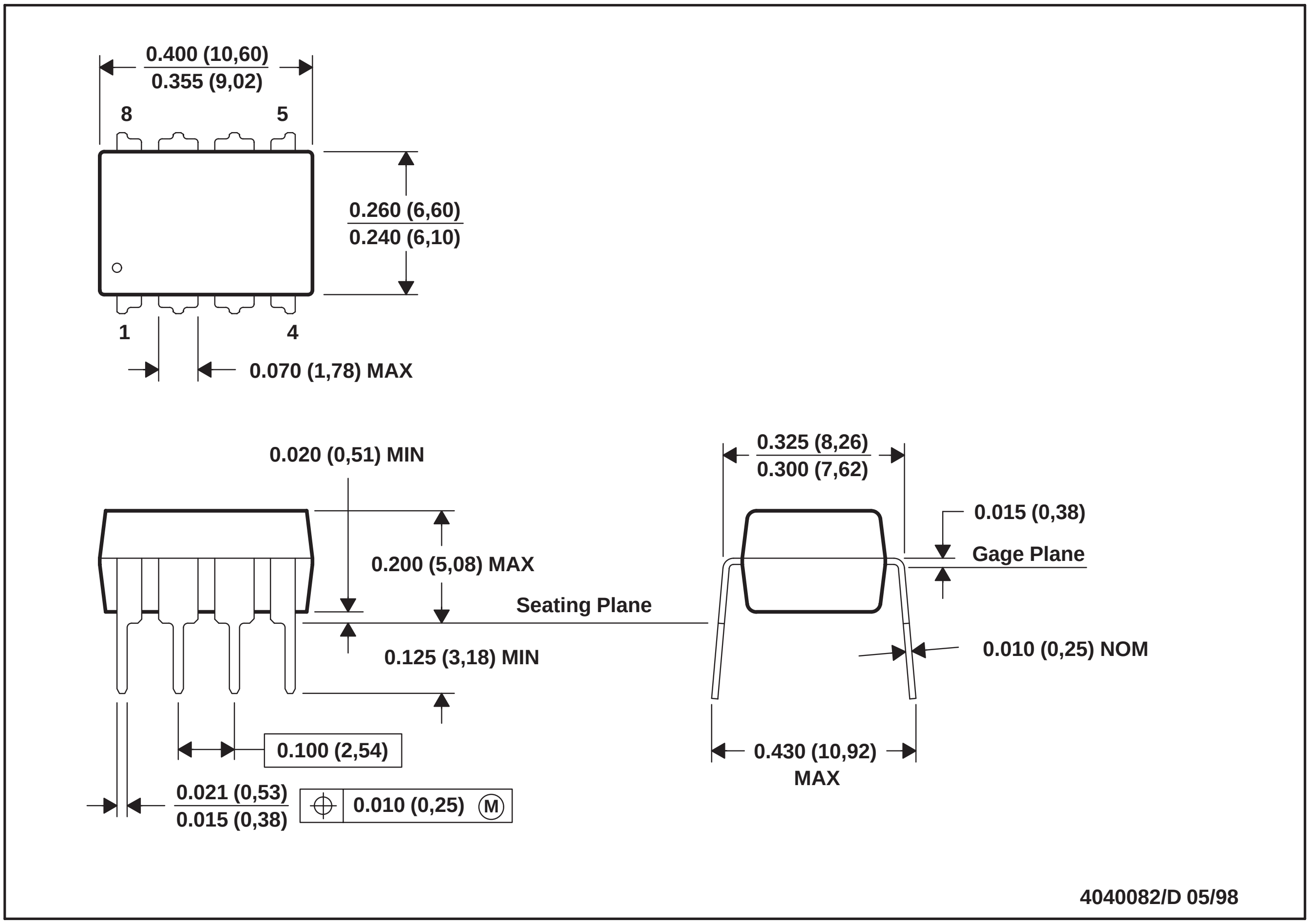
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL070IDR	SOIC	D	8	2500	340.5	338.1	20.6

D (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AA.

P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

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