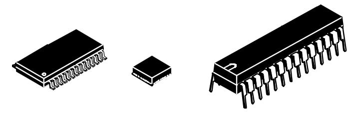


PWP RHB NT

16 CHANNEL LED DRIVER WITH DOT CORRECTION AND GRAYSCALE PWM CONTROL

FEATURES

- **16 Channels**
- **12 bit (4096 Steps) Grayscale PWM Control**
- **Dot Correction**
  - **– 6 bit (64 Steps)**
  - **– Storable in Integrated EEPROM**
- **Drive Capability (Constant Current Sink)**
  - **– 0 mA to 60 mA (V_{CC} < 3.6 V)**
  - **– 0 mA to 120 mA (V_{CC} > 3.6 V)**
- **LED Power Supply Voltage up to 17 V**
- **V_{CC} = 3.0 V to 5.5 V**
- **Serial Data Interface**
- **Controlled In-Rush Current**
- **30-MHz Data Transfer Rate**
- **CMOS Level I/O**
- **Error Information**
  - **– LOD: LED Open Detection**
  - **– TEF: Thermal Error Flag**

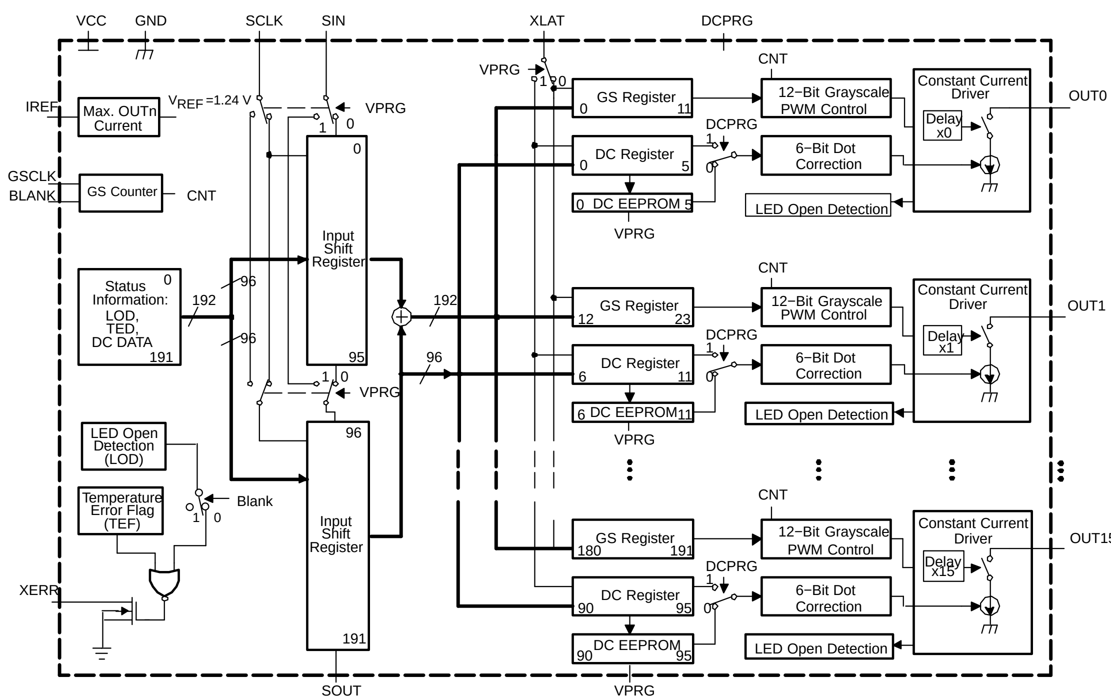
APPLICATIONS

- **Monocolor, Multicolor, Fullcolor LED Displays**
- **LED Signboards**
- **Display Backlighting**

DESCRIPTION

The TLC5940 is a 16-channel constant-current sink LED driver. Each channel has an individually adjustable 4096-step grayscale PWM brightness control and a 64-step constant-current sink (dot correction). The dot correction adjusts the brightness variations between LED channels and other LED drivers. The dot correction data is stored in an integrated EEPROM. Both grayscale control and dot correction are accessible via a serial interface. A single external resistor sets the maximum current value of all 16 channels.

The TLC5940 features two error information circuits. The LED open detection (LOD) indicates a broken or disconnected LED at an output terminal. The thermal error flag (TEF) indicates an overtemperature condition.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPad is a trademark of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	PACKAGE	PART NUMBER
-20°C to 85°C	28-pin HTSSOP Powerpad™	TLC5940PWP
-20°C to 85°C	32-pin 5 mm x 5 mm QFN	TLC5940RHB
-20°C to 85°C	28-pin PDIP	TLC5940NT

ABSOLUTE MAXIMUM RATINGS.

over operating free-air temperature range (unless otherwise noted)(1)

			UNIT
V_I	Input voltage range(2)	VCC	- 0.3 V to 6 V
I_O	Output current (dc)		130 mA
V_I	Input voltage range	$V_{(BLANK)}$, $V_{(DCPRG)}$, $V_{(SCLK)}$, $V_{(XLAT)}$	-0.3 V to V_{CC} +0.3 V
V_O	Output voltage range	$V_{(SOUT)}$, $V_{(XERR)}$	-0.3 V to V_{CC} +0.3 V
		$V_{(OUT0)}$ to $V_{(OUT15)}$	-0.3 V to 18 V
	EEPROM program range	$V_{(PRG)}$	-0.3 V to 24 V
	EEPROM write cycles		50
	ESD rating	HBM (JEDEC JESD22-A114, Human Body Model)	2 kV
		CBM (JEDEC JESD22-C101, Charged Device Model)	500 V
T_{stg}	Storage temperature range		-55 °C to 150°C
T_A	Operating ambient temperature range		-20°C to 85°C
	Package thermal impedance(3)	HTSSOP (PWP)(4)	31.58°C/W
		QFN (RHB)	35.9°C/W
		PDIP (NP)	48°C/W

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.
(4) With PowerPad soldered on PCB with 2 oz. trace of copper. See SLMA002 for further information.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
DC Characteristics						
V_{CC}	Supply Voltage		3		5.5	V
V_O	Voltage applied to output (OUT0 - OUT15)				17	V
V_{IH}	High-level input voltage		0.8 V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage		GND		0.2 V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 5 V at SOUT			-1	mA
I_{OL}	Low-level output current	V_{CC} = 5 V at SOUT, XERR			1	mA
I_{OLC}	Constant output current	OUT0 to OUT15, V_{CC} < 3.6 V			60	mA
		OUT0 to OUT15, V_{CC} > 3.6 V			120	mA
$V_{(PRG)}$	EEPROM program voltage		20	22	23	V
T_A	Operating free-air temperature range		-20		85	°C
AC Characteristics V_{CC} = 3 V to 5.5 V, T_A = -40°C to 85°C (unless otherwise noted)						
$f_{(SCLK)}$	Data shift clock frequency	SCLK			30	MHz
$f_{(GSCLK)}$	Grayscale clock frequency	GSCLK			30	MHz
t_{wh0}/t_{wl0}	SCLK pulse duration	SCLK = H/L (1)	16			ns
t_{wh1}/t_{wl1}	GSCLK pulse duration	GSCLK = H/L (2)	16			ns
t_{wh2}	XLAT pulse duration	XLAT = H (3)	20			ns
t_{wh3}	BLANK pulse duration	BLANK = H (2)	20			ns
t_{su0}	Setup time	SIN - SCLK (3)	10			ns
t_{su1}		SCLK - XLAT (3)	10			ns
t_{su2}		VPRG - SCLK (4)	10			ns
t_{su3}		VPRG - XLAT (4)	10			ns
t_{su4}		BLANK - GSCLK (2)	10			ns
t_{su5}		VPRG - DCPRG	1			ms
t_{h0}	Hold Time	SCLK - SIN (3)	10			ns
t_{h1}		XLAT - SCLK (3)	10			ns
t_{h2}		SCLK - VPRG (4)	10			ns
t_{h3}		XLAT - VPRG (4)	10			ns
t_{h4}		BLANK - GSCLK (2)	10			ns
t_{h5}		DCPRG - VPRG	1			ms
t_{prog}		Programming time for EEPROM	20			ms

(1) See Figure 6
(2) See Figure 11
(3) See Figure 9
(4) See Figure 3

DISSIPATION RATINGS

PACKAGE	POWER RATING T_A < 25°C	DERATING FACTOR ABOVE T_A = 25°C	POWER RATING T_A = 70°C	POWER RATING T_A = 85°C
28-pin HTSSOP with PowerPad™ (1)	3958 mW	31.67 mW/°C	2533 mW	2058 mW
32-pin QFN (1)	3482 mW	27.86 mW/°C	2228 mW	1811 mW
28-pin PDIP	2456 mW	19.65 mW/°C	1572 mW	1277 mW

(1) The PowerPAD is soldered to the PCB with a 2 oz.copper trace. See SLMA002 for further information.

ELECTRICAL CHARACTERISTICS

V_{CC} = 3 V to 5.5 V, T_A = -20°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = -1 mA, SOUT	V_{CC} - 0.5			V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA, SOUT			0.5	V
I_I	Input current	V_I = V_{CC} or GND, BLANK, DCPRG, GSCLK, SCLK, SIN, XLAT,VPRG	-1		1	mA
I_{CC}	Supply current	No data transfer, all output OFF, V_O = 1 V, $R_{(IREF)}$ = 10 kΩ		0.9	6	mA
		No data transfer, all output OFF, V_O = 1 V, $R_{(IREF)}$ = 1.3 kΩ		5.2	12	
		Data transfer 30 MHz, all output ON, V_O = 1 V, $R_{(IREF)}$ = 1.3 kΩ		16	25	
		Data transfer 30 MHz, all output ON, V_O = 1 V, $R_{(IREF)}$ = 640 Ω		30	60	
$I_{O(LC)}$	Constant output current	All output ON, V_O = 1 V, $R_{(IREF)}$ = 640 Ω	56	61	66	mA
I_{lkg}	Leakage output current	All output OFF, V_O = 15 V, $R_{(IREF)}$ = 640 Ω , OUT0 to OUT15			0.1	µA
$\Delta I_{O(LC0)}$	Constant current error	All output ON, V_O = 1 V, $R_{(IREF)}$ = 640 Ω, OUT0 to OUT15		±1	±4	%
		All output ON, V_O = 1 V, $R_{(IREF)}$ = 320 Ω, OUT0 to OUT15		±1	±6	%
$\Delta I_{O(LC1)}$		device to device, averaged current from OUT0 to OUT15,$R_{(IREF)}$ = 1920 Ω (20mA)		-2, +0.4	±4	%
$\Delta I_{O(LC2)}$		device to device, averaged current from OUT0 to OUT15,$R_{(IREF)}$ = 480 Ω (80mA)		-2.7, +2	±4	%
$\Delta I_{O(LC3)}$	Power supply rejection ratio, PSRR	All output ON, V_O = 1 V, $R_{(IREF)}$ = 640 Ω OUT0 to OUT15		±1	±4	%/V
		All output ON, V_O = 1 V, $R_{(IREF)}$ = 320 Ω , OUT0 to OUT15		±1	±6	%/V
$\Delta I_{O(LC4)}$	Load regulation	All output ON, V_O = 1 V to 3 V, $R_{(IREF)}$ = 640 Ω, OUT0 to OUT15		±2	±6	%/V
		All output ON, V_O = 1 V to 3 V, $R_{(IREF)}$ = 320 Ω, OUT0 to OUT15		±2	±8	%/V
$T_{(TEF)}$	Thermal error flag threshold	Junction temperature(1)	150		170	°C
$V_{(LED)}$	LED open detection threshold			0.3	0.4V	V
$V_{(IREF)}$	Reference voltage output	$R_{I(REF)}$ = 640 Ω	1.20	1.24	1.28	V

(1) Not tested. Specified by design

SWITCHING CHARACTERISTICS

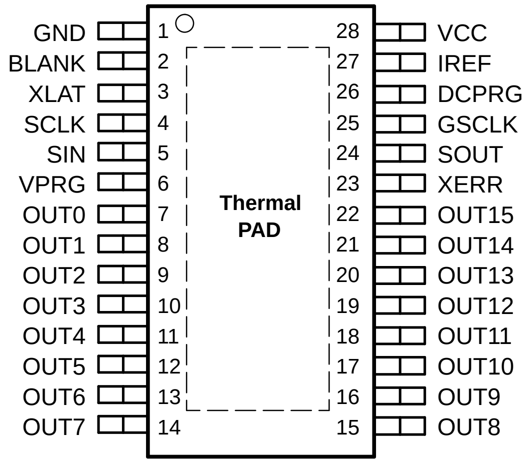
V_{CC} = 3 V to 5.5 V, T_A = -20°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{r0}	Rise time	SOUT			16	ns
t_{r1}		OUTn, V_{CC} = 5 V, T_A = 60°C, DCx = 3F		10	30	
t_{f0}	Fall time	SOUT			16	ns
t_{f1}		OUTn, V_{CC} = 5 V, T_A = 60°C, DCx = 3F		10	30	
t_{pd0}	Propagation delay time	SCLK - SOUT (1)			30	ns
t_{pd1}		DCPRG - OUT0			30	ns
t_{pd2}		BLANK - OUT0 (2)			60	ns
t_{pd3}		OUTn - XERR (2)			1000	ns
t_{pd4}		GSCLK - OUT0 (2)			60	ns
t_{pd5}		XLAT - I_{OUT} (dot correction)			1000	ns
t_d	Output delay time	OUTn - OUT(n+1) (2)		20	30	ns

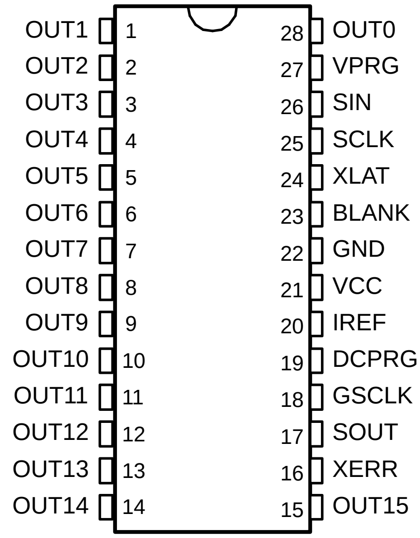
(1) See Figure 9
(2) See Figure 11

DEVICE INFORMATION

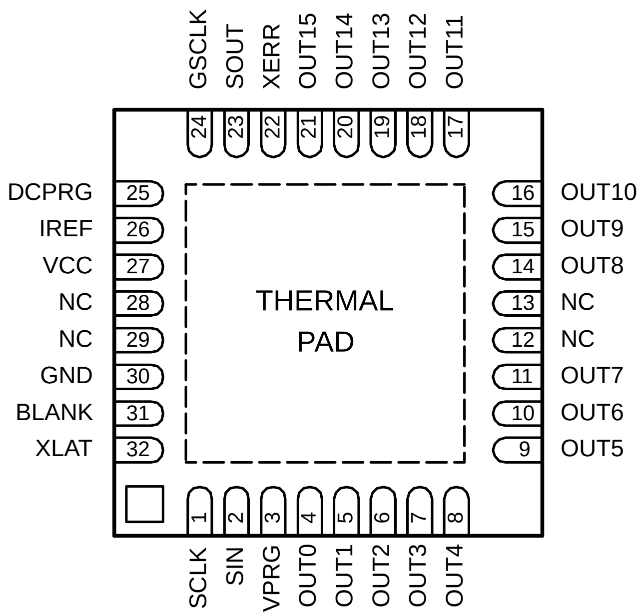
PWP PACKAGE
(TOP VIEW)



NT PACKAGE
(TOP VIEW)



RHB PACKAGE
(TOP VIEW)



NC − No internal connection

TERMINAL FUNCTION

TERMINAL				I/O	DESCRIPTION
	DIP	PWP	RHB		
NAME	NO.	NO.	NO.		
BLANK	23	2	31	I	Blank all outputs. When BLANK = H, all OUTn outputs are forced OFF. GS counter is also reset. When BLANK = L, OUTn are controlled by grayscale PWM control.
DCPRG	19	26	25	I	Switch DC data input. When DCPRG = L, DC is connected to EEPROM. When DCPRG = H, DC is connected to the DC register. DCPRG is also controls EEPROM writing, when VPRG = $V_{(PRG)}$
GND	22	1	30	G	Ground
GSCLK	18	25	24	I	Reference clock for grayscale PWM control
IREF	20	27	26	I	Reference current terminal
NC	-	-	12, 13, 28, 29		No connection
OUT0	28	7	4	O	Constant current output
OUT1	1	8	5	O	Constant current output
OUT2	2	9	6	O	Constant current output
OUT3	3	10	7	O	Constant current output
OUT4	4	11	8	O	Constant current output
OUT5	5	12	9	O	Constant current output
OUT6	6	13	10	O	Constant current output
OUT7	7	14	11	O	Constant current output
OUT8	8	15	14	O	Constant current output
OUT9	9	16	15	O	Constant current output
OUT10	10	17	16	O	Constant current output
OUT11	11	18	17	O	Constant current output
OUT12	12	19	18	O	Constant current output
OUT13	13	20	19	O	Constant current output
OUT14	14	21	20	O	Constant current output
OUT15	15	22	21	O	Constant current output
SCLK	25	4	1	I	Serial data shift clock
SIN	26	5	2	I	Serial data input
SOUT	17	24	23	O	Serial data output
VCC	21	28	27	I	Power supply voltage
VPRG	27	6	3	I	Multifunction input pin. When VPRG = GND, the device is in GS mode. When VPRG = V_{CC}, the device is in DC mode. When VPRG = $V_{(PRG)}$, DC register data can programmed into DC EEPROM with DCPRG=HIGH.
XERR	16	23	22	O	Error output. XERR is an open-drain terminal. XERR goes L when LOD or TEF is detected.
XLAT	24	3	32	I	Data latch. Note that the internal connections are switched by VPRG. At XLAT↑ (VPRG = GND), GS register gets new data. At XLAT↑ (VPRG = V_{CC}), DC register gets new data.

PARAMETER MEASUREMENT INFORMATION

PIN EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

Resistor values are equivalent resistances and not tested.

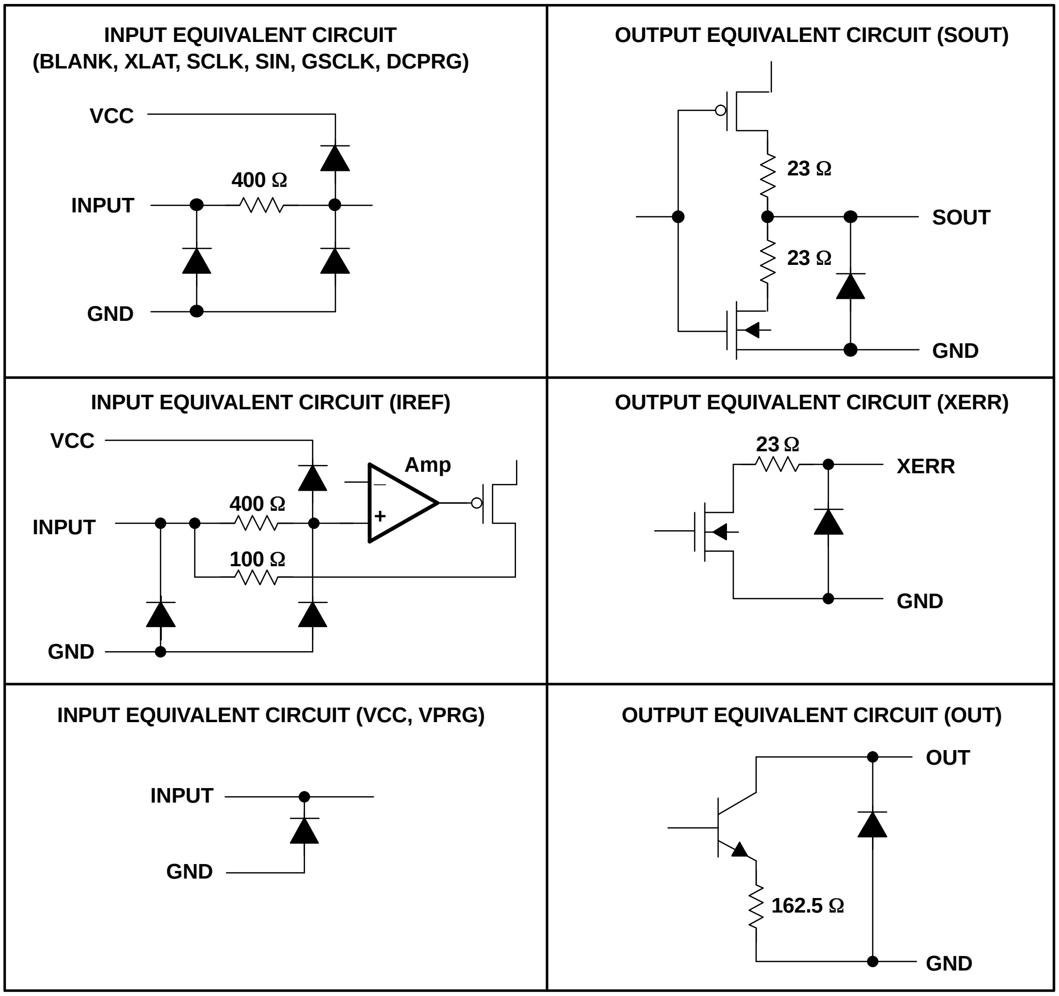


Figure 1. Input and Output Equivalent Circuits

PARAMETER MEASUREMENT INFORMATION (continued)

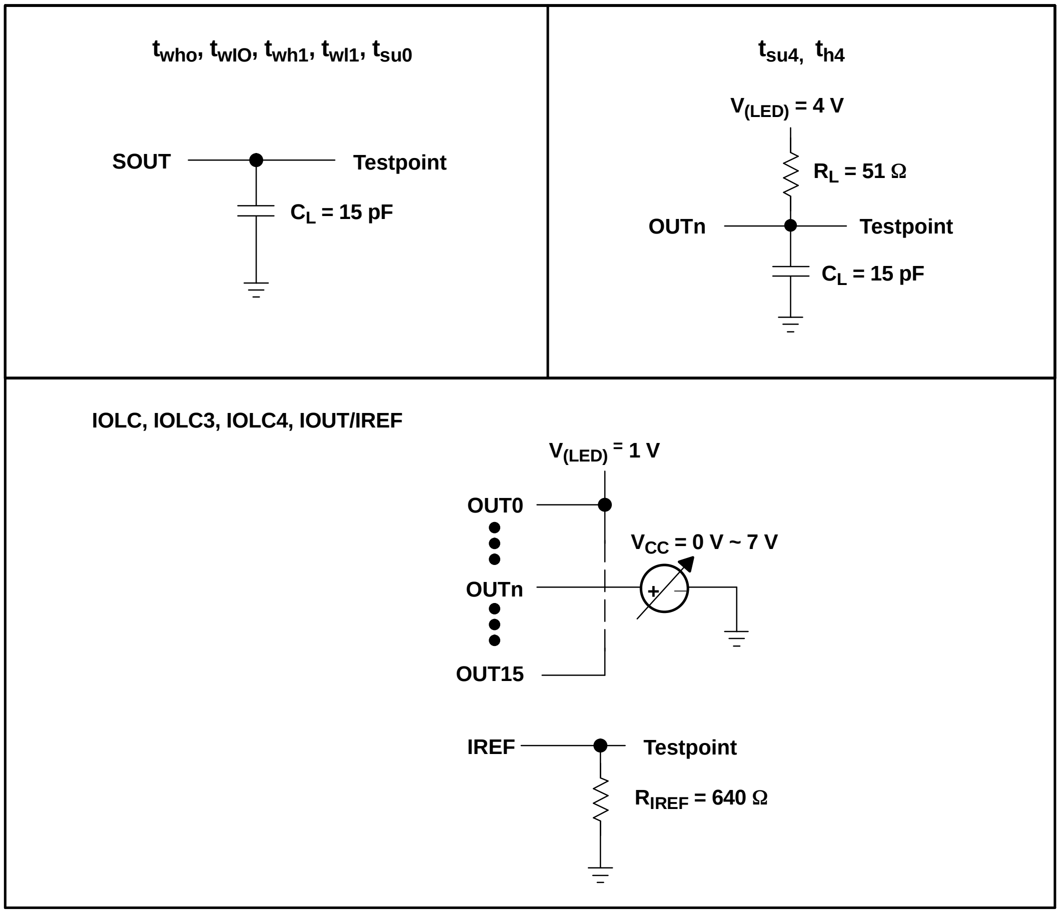


Figure 2. Parameter Measurement Circuits

PRINCIPLES OF OPERATION

SERIAL INTERFACE

The TLC5940 includes a flexible serial interface, which can be connected to microcontrollers or digital signal processors in various ways. Only 3 pins are needed to input data into the device. The rising edge of SCLK signal shifts the data from the SIN pin to the internal register. After all data is clocked in, a rising edge of XLAT latches the serial data to the internal registers. All data are clocked in with the MSB first. Multiple TLC5940 devices can be cascaded by connecting the SOUT pin of one device with the SIN pin of the following device. The SOUT pin can also be connected to the controller to receive status information from TLC5940. The serial data format is 96-bit or 192-bit wide, depending on programming mode of the device.

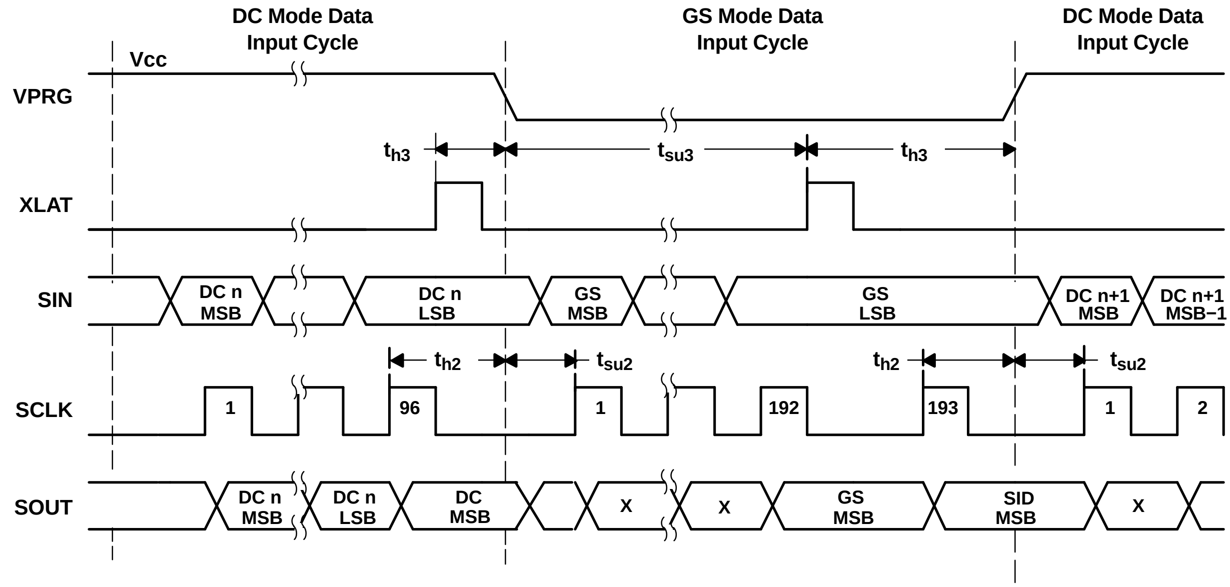


Figure 3. Serial Data Input Timing Chart

ERROR INFORMATION OUTPUT

The open-drain output XERR is used to report both of the TLC5940 error flags, TEF and LOD. During normal operating conditions, the internal transistor connected to the XERR pin is turned off. The voltage on XERR is pulled up to V_{CC} through an external pullup resistor. If TEF or LOD is detected, the internal transistor is turned on, and XERR is pulled to GND. Since XERR is an open-drain output, multiple ICs can be OR'ed together and pulled up to V_{CC} with a single pullup resistor. This reduces the number of signals needed to report a system error (see Figure 12).

To differentiate LOD and TEF signal from XERR pin, LOD can be masked out with BLANK = HIGH.

Table 1. XERR Truth Table

ERROR CONDITION		ERROR INFORMATION		SIGNALS	
TEMPERATURE	OUNTn VOLTAGE	TEF	LOD	BLANK	XERR
$T_J < T_{(TEF)}$	Don't Care	L	X	H	H
$T_J > T_{(TEF)}$	Don't Care	H	X		L
$T_J < T_{(TEF)}$	OUTn > $V_{(LED)}$	L	L	L	H
	OUTn < $V_{(LED)}$	L	H		L
$T_J > T_{(TEF)}$	OUTn > $V_{(LED)}$	H	L		L
	OUTn < $V_{(LED)}$	H	H		L

TEF: THERMAL ERROR FLAG

The TLC5940 provides a temperature error flag (TEF) circuit to indicate an overtemperature condition of the IC. If the junction temperature exceeds the threshold temperature (160°C typical), the TEF circuit trips and pulls XERR to ground. TEF status can also be read out from the TLC5940 status register.

LOD: LED OPEN DETECTION

The TLC5940 provides an LED open-detection circuit (LOD). This circuit reports an error if any one of the 16 LEDs is open or disconnected from the circuit. The LOD circuit trips when the following two conditions are met simultaneously:

1. BLANK is set to LOW
2. When the voltage at OUTn is less than $V_{(LED)}$ of 0.3 V (typical) (Note: the voltage at each OUTn is sampled 1 µs after being turned on).

The LOD circuit also pulls XERR to GND when tripped. The LOD status of each channel can also be read out from the TLC5940 status information data (SID) in GS data input cycle.

DELAY BETWEEN OUTPUTS

The TLC5940 has graduated delay circuits between outputs. These circuits can be found in the constant current driver block of the device (see functional block diagram). The fixed-delay time is 20 ns (typical), OUT0 has no delay, OUT1 has 20 ns delay, and OUT2 has 40 ns delay, etc. These delays prevent large inrush currents which reduces the bypass capacitors when the outputs turn on.

OUTPUT ENABLE

All OUTn channels of TLC5940 can switched off with one signal. When BLANK is set to high, all OUTn are disabled, regardless of logic operations of the device. The grayscale counter is also reset. When BLANK is set to low, all OUTn work under normal conditions.

Table 2. BLANK Signal Truth Table

BLANK	OUT0 - OUT15
LOW	Normal condition
HIGH	Disabled

SETTING MAXIMUM CHANNEL CURRENT

The maximum output current per channel is programmed by a single resistor, $R_{(IREF)}$, which is placed between IREF pin and GND pin. The voltage on IREF is set by an internal band gap $V_{(IREF)}$ with a typical value of 1.24 V. The maximum channel current is equivalent to the current flowing through $R_{(IREF)}$ multiplied by a factor of 31.5. The maximum output current can be calculated by Equation 1:

$$I_{max} = \frac{V_{(IREF)}}{R_{(IREF)}} \times 31.5 \tag{1}$$

where:

$V_{(IREF)}$ = 1.24 V

$R_{(IREF)}$ = User selected external resistor.

Figure 4 shows the maximum output current I_O versus $R_{(IREF)}$. $R_{(IREF)}$ is the value of the resistor between IREF terminal to GND, and I_O is the constant output current of OUT0 to OUT15.

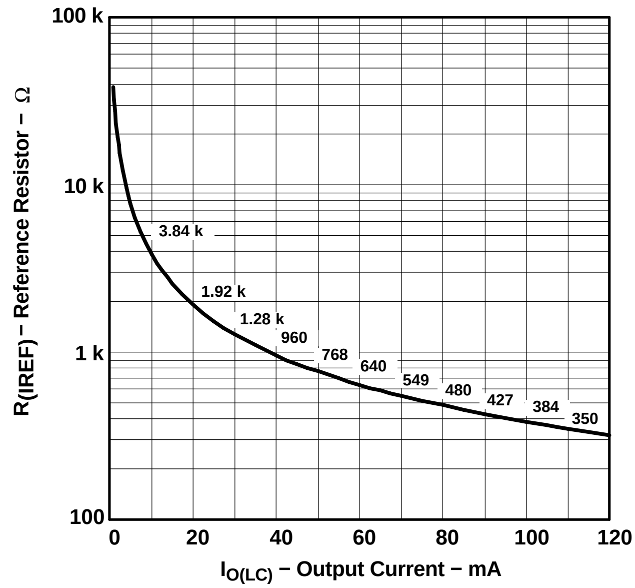


Figure 4. Output Current vs $I_{(REF)}$ Resistor

OPERATING MODES

The TLC5940 has different operating modes depending on the signals VPRG and DCPRG. Table 3 shows the available operating modes. The TLC5940 GS operating mode (see Figure 9) and shift register values are not defined after power up. One solution to solve this is to set dot correction data after TLC5940 power up and switch back to GS PWM mode. The other solution is to overflow the input shift register with 193 bits of dummy data and latch it while TLC5940 is in GS PWM mode.

Table 3. TLC5940 Operating Modes Truth Table

SIGNAL		INPUT SHIFT REGISTER	MODE	DC VALUE
DCPRG	VCPRG			
L	GND	192 bit	Grayscale PWM Mode	EEPROM
H				DC Register
L	V_{CC}	96 bit	Dot Correction Data Input Mode	EEPROM
H				DC Register
L	$V_{(PRG)}$	X	EEPROM Programming Mode	EEPROM
H				Write dc register value to EEPROM

SETTING DOT CORRECTION

The TLC5940 has the capability to fine adjust the output current of each channel OUT0 to OUT15 independently. This is also called dot correction. This feature is used to adjust the brightness deviations of LEDs connected to the output channels OUT0 to OUT15. Each of the 16 channels can be programmed with a 6-bit word. The channel output can be adjusted in 64 steps from 0% to 100% of the maximum output current I_{max}. Equation 2 determines the output current for each output n:

$$I_{OUTn} = I_{max} \times \frac{DCn}{63} \tag{2}$$

where:

I_{max} = the maximum programmable output current for each output.

DCn = the programmed dot correction value for output n (DCn = 0 to 63).

n = 0 to 15

Dot correction data are entered for all channels at the same time. The complete dot correction data format consists of 16 x 6-bit words, which forms a 96-bit wide serial data packet. The channel data is put one after another. All data is clocked in with MSB first. Figure 5 shows the DC data format.

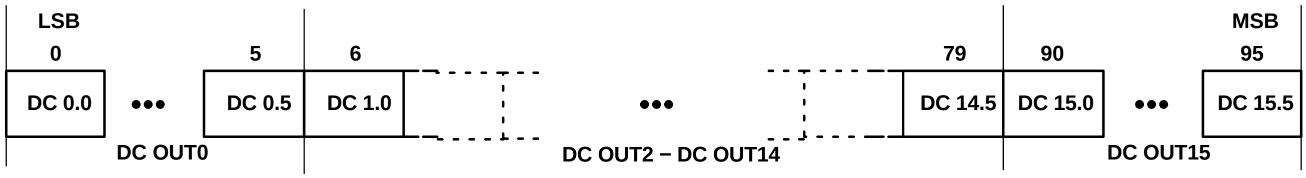


Figure 5. Dot Correction Data Packet Format

To input data into the dot correction register, VPRG must be set to V_{CC}. The internal input shift register is then set to 96-bit width. After all serial data are clocked in, a rising edge of XLAT is used to latch the data into the dot correction register. Figure 6 shows the dc data input timing chart.

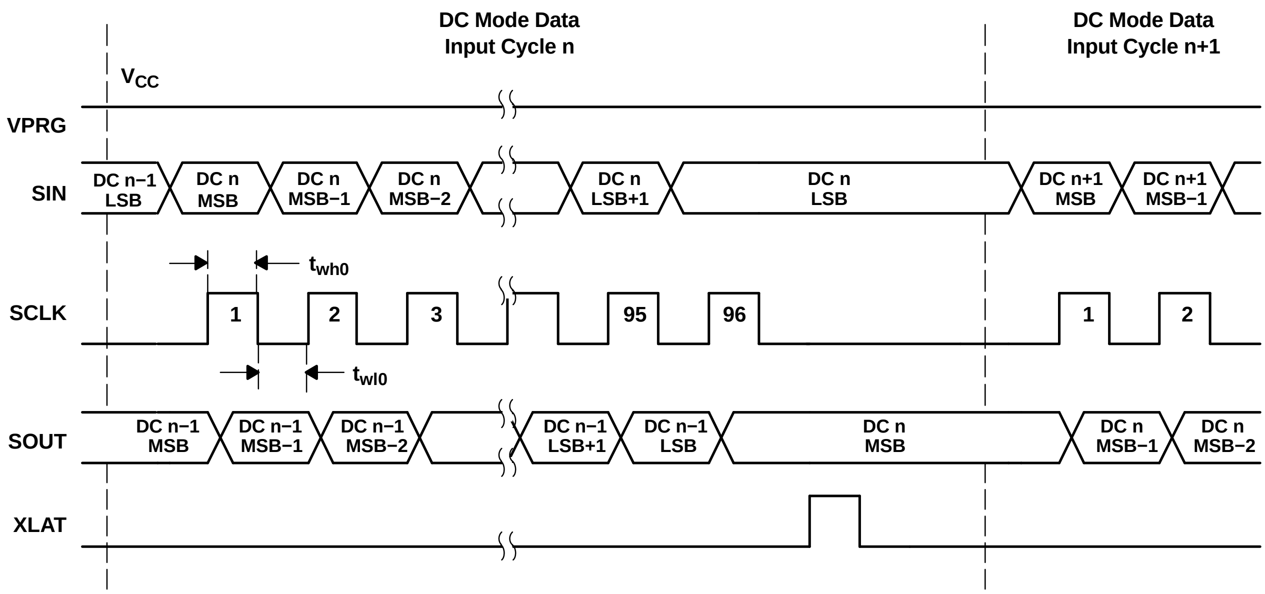


Figure 6. Dot Correction Data Input Timing Chart

The TLC5940 has also an EEPROM to store dot correction data. To store data from the dot correction register to EEPROM, DCPRG is set to high after applying V_{PRG} to VPRG pin. Figure 7 shows the EEPROM programming timings.

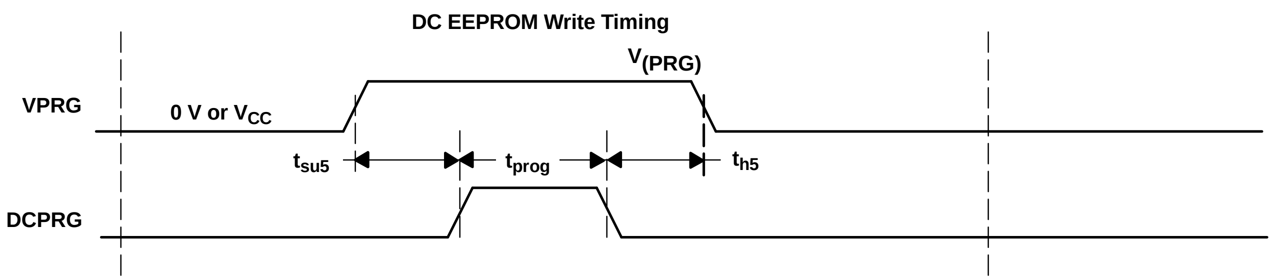


Figure 7. EEPROM Programming Timing Chart

SETTING GRAYSCALE

The TLC5940 can adjust the brightness of each channel OUTn using a PWM control scheme. The use of 12-bit per channel results in 4096 different brightness steps, respective 0% to 100% brightness. Equation 3 determines the brightness level for each output n:

$$\text{Brightness in \%} = \frac{GSn}{4095} \times 100 \tag{3}$$

where:

GSn = the programmed grayscale value for output n (GSn = 0 to 4095)

n = 0 to 15

Grayscale data for all OUTn

The input shift register enters grayscale data into grayscale register for all channels simultaneously. The complete grayscale data format consists of 16 x 12 bit words, which forms a 192-bit wide data packet (see Figure 8). The data packet must be clocked in with the MSB first.

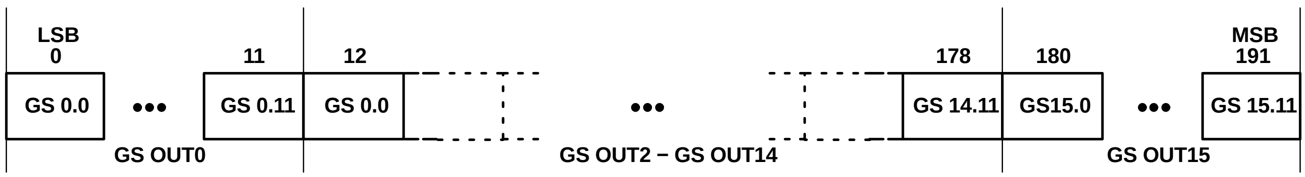


Figure 8. Grayscale Data Packet Format

When VPRG is set to GND, TLC5940 enters the grayscale data input mode. The device switches the input shift register to 192-bit width. After all data is clocked in, a rising edge of XLAT signal latches the data into the grayscale register (see Figure 9). The first GS data input cycle after dot correction requires an additional SCLK pulse after the XLAT signal to complete the grayscale update cycle. All GS data in the input shift register is replaced with status information data (SID) after latching into grayscale register.

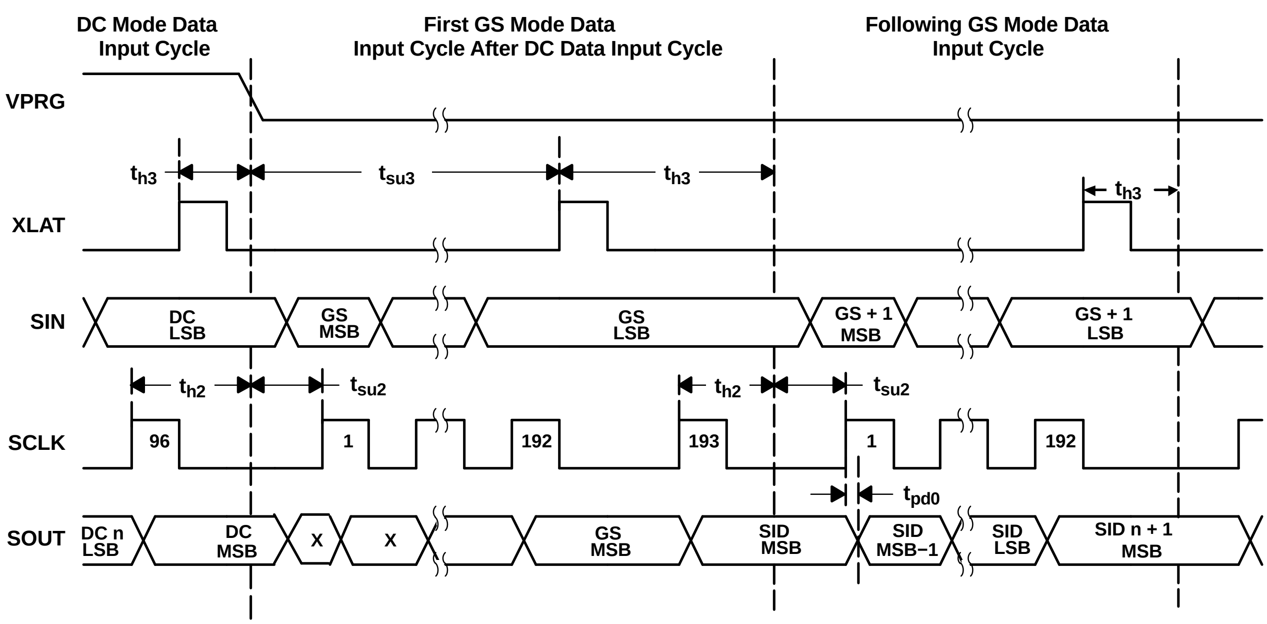


Figure 9. Grayscale Data Input Timing Chart

STATUS INFORMATION OUTPUT

The TLC5940 does have a status information register, which can be accessed in grayscale mode (VPRG = GND). After the XLAT signal latches the data into GS register the input shift register data will be replaced with status information data (SID) of the device (see Figure 9). LOD, TEF and dot correction EEPROM data (DCPRG=LOW) or dot correction register data (DCPRG=HIGH) can be read out at the SOUT pin. The status information data packet is 192-bit wide. Bit 176 - bit 191 contains the LOD status of each channel. Bit 175 contains the TEF status. If DCPRG is low, bit 72 - bit 167 contains the value of the dot correction EEPROM. If DCPRG is high, bit 72 - bit 167 contains the data of the dot correction register. The remaining bits are reserved. The complete status information data packet is shown in Figure 10.

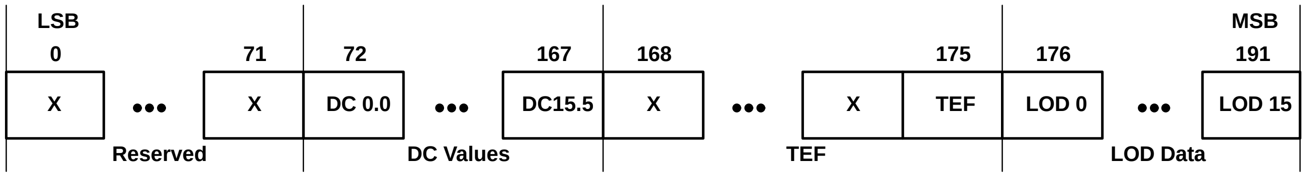


Figure 10. Status Information Data Packet Format

GRAYSCALE PWM OPERATION

The grayscale PWM cycle starts with the falling edge of BLANK. The first GSCLK pulse after BLANK increases the grayscale counter by one and switches on all OUTn with grayscale value not zero. Each following rising edge of GSCLK increases the grayscale counter by one. The TLC5940 compares the grayscale value of each output OUTn with the grayscale counter value. All OUTn with grayscale values equal to counter values are switched off. A BLANK=H signal after 4096 GSCLK pulses resets the grayscale counter to zero and completes the grayscale PWM cycle (see Figure 11).

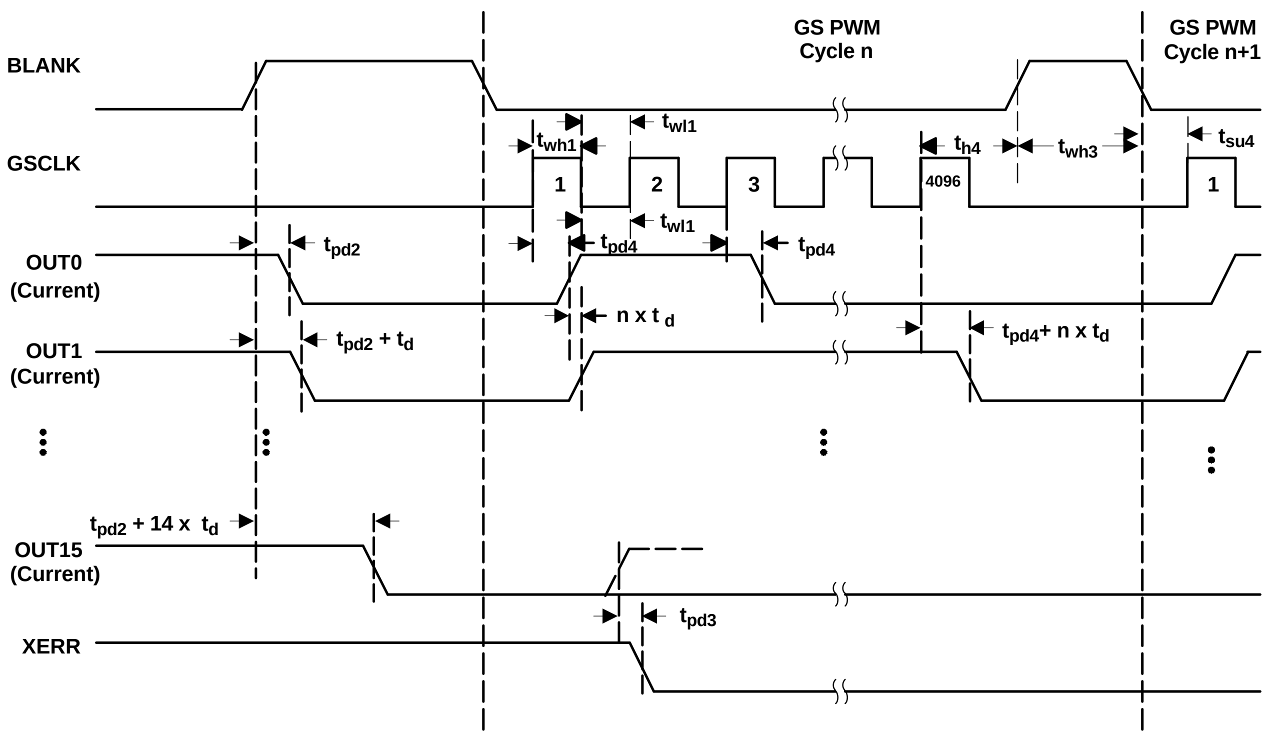


Figure 11. Grayscale PWM Cycle Timing Chart

SERIAL DATA TRANSFER RATE

Figure 12 shows a cascading connection of *n* TLC5940 devices connected to a controller, building a basic module of an LED display system. The maximum number of cascading TLC5940 devices depends on the application system and is in the range of 40 devices. Equation 4 calculates the minimum frequency needed:

$$f_{(GSCLK)} = 4096 \times f_{(update)}$$

$$f_{(SCLK)} = 193 \times f_{(update)} \times n \qquad (4)$$

where:

$f_{(GSCLK)}$: minimum frequency needed for GSCLK

$f_{(SCLK)}$: minimum frequency needed for SCLK and SIN

$f_{(update)}$: update rate of whole cascading system

n: number cascaded of TLC5940 device

Application Example

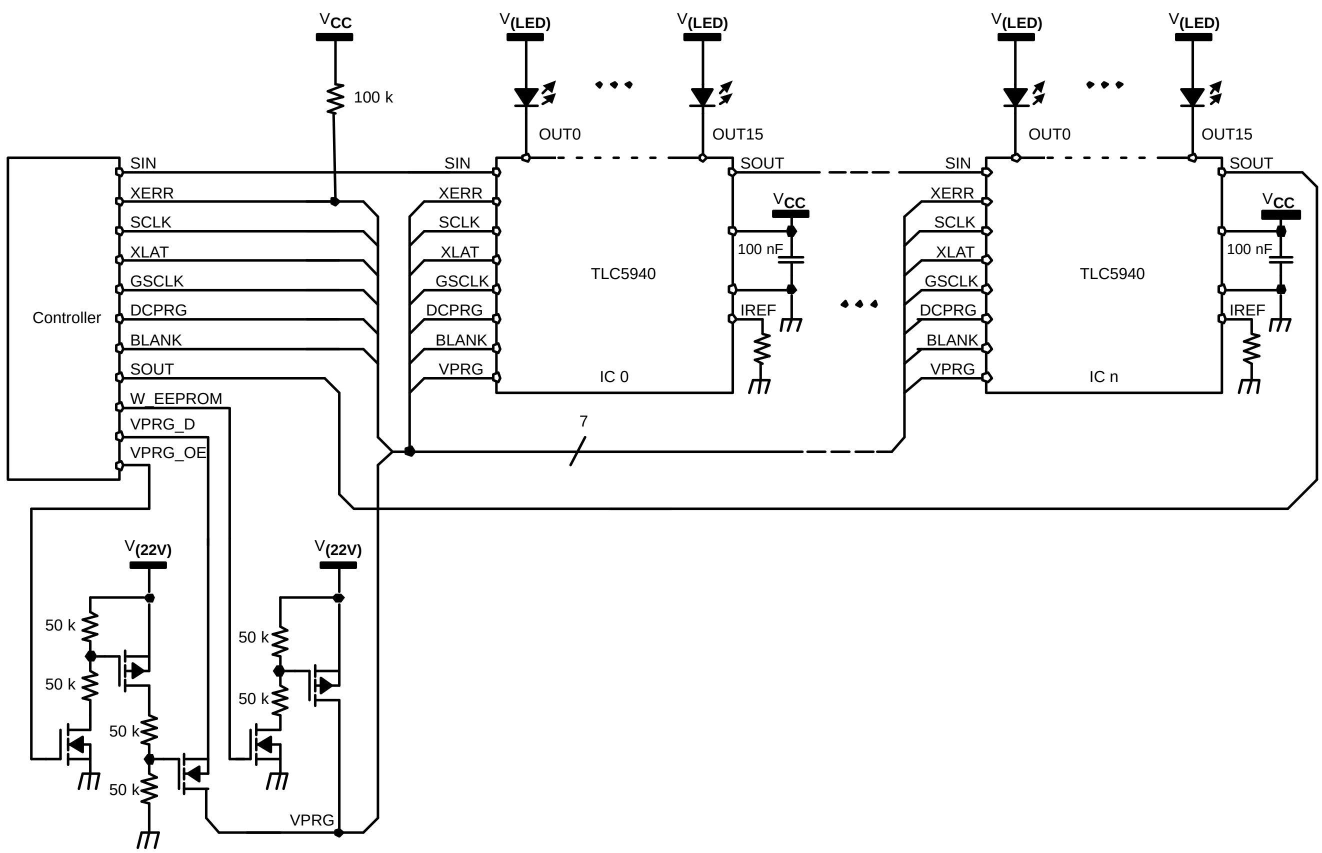
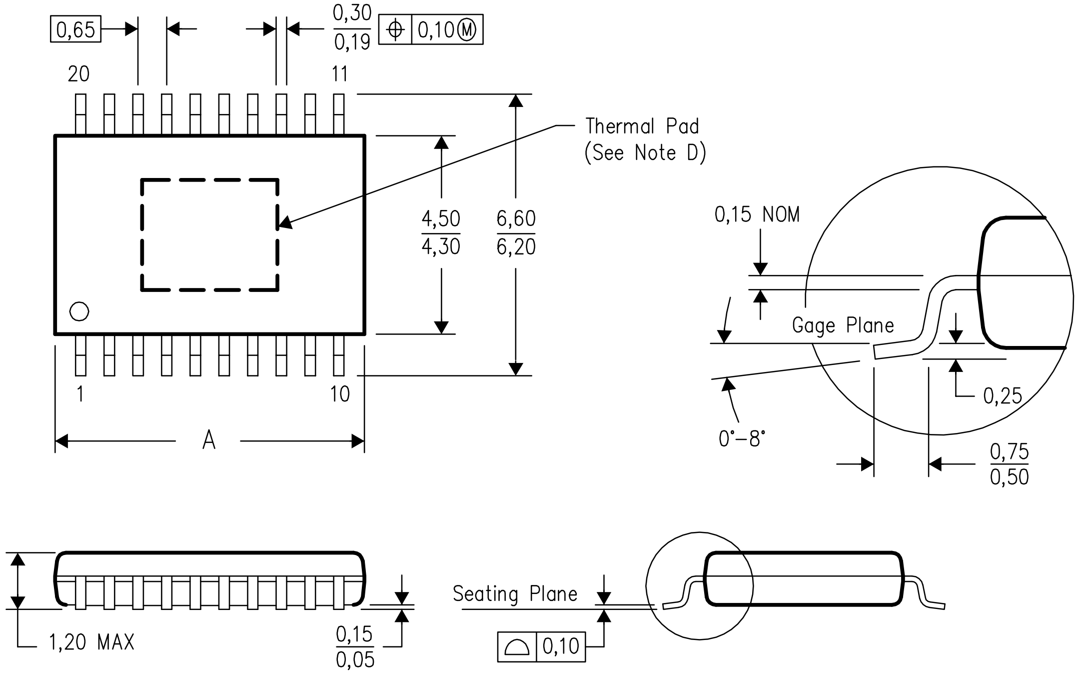


Figure 12. Cascading Devices

PWP (R-PDSO-G**) PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE

20 PIN SHOWN



PINS ** / DIM	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

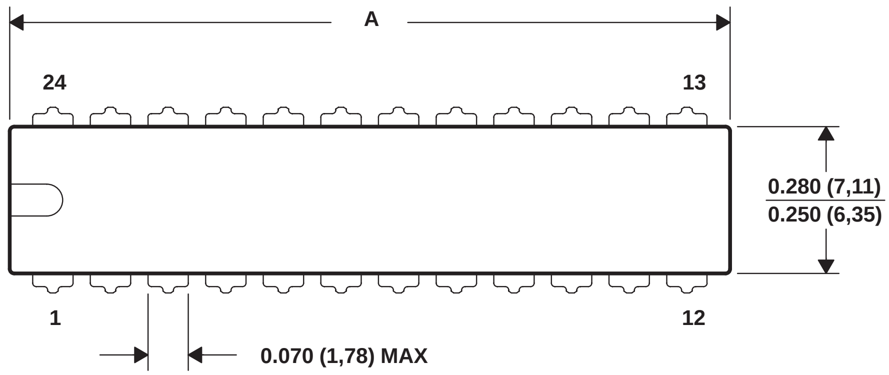
4073225/G 08/03

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusions.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
- E. Falls within JEDEC MO-153

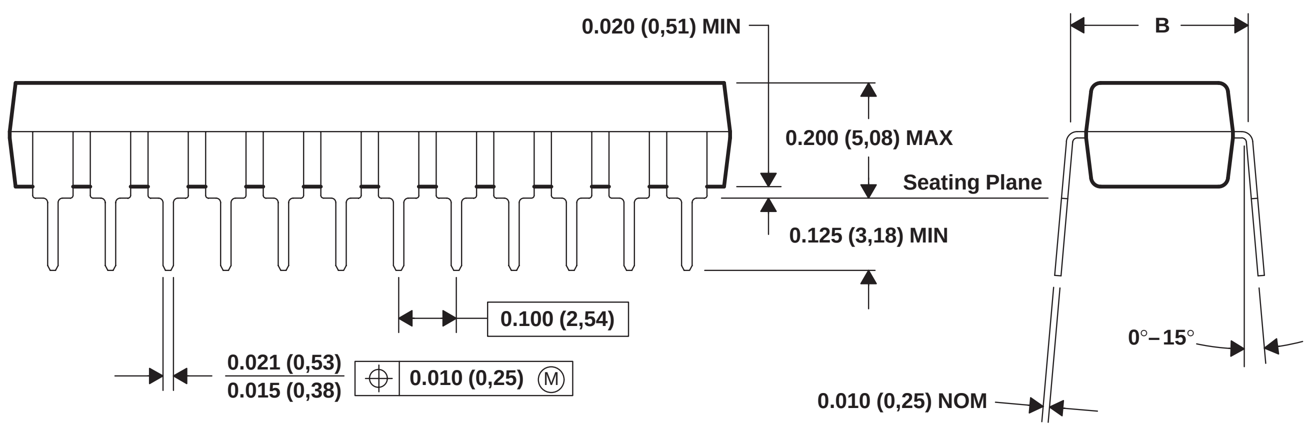
PowerPAD is a trademark of Texas Instruments.

NT (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

24 PINS SHOWN



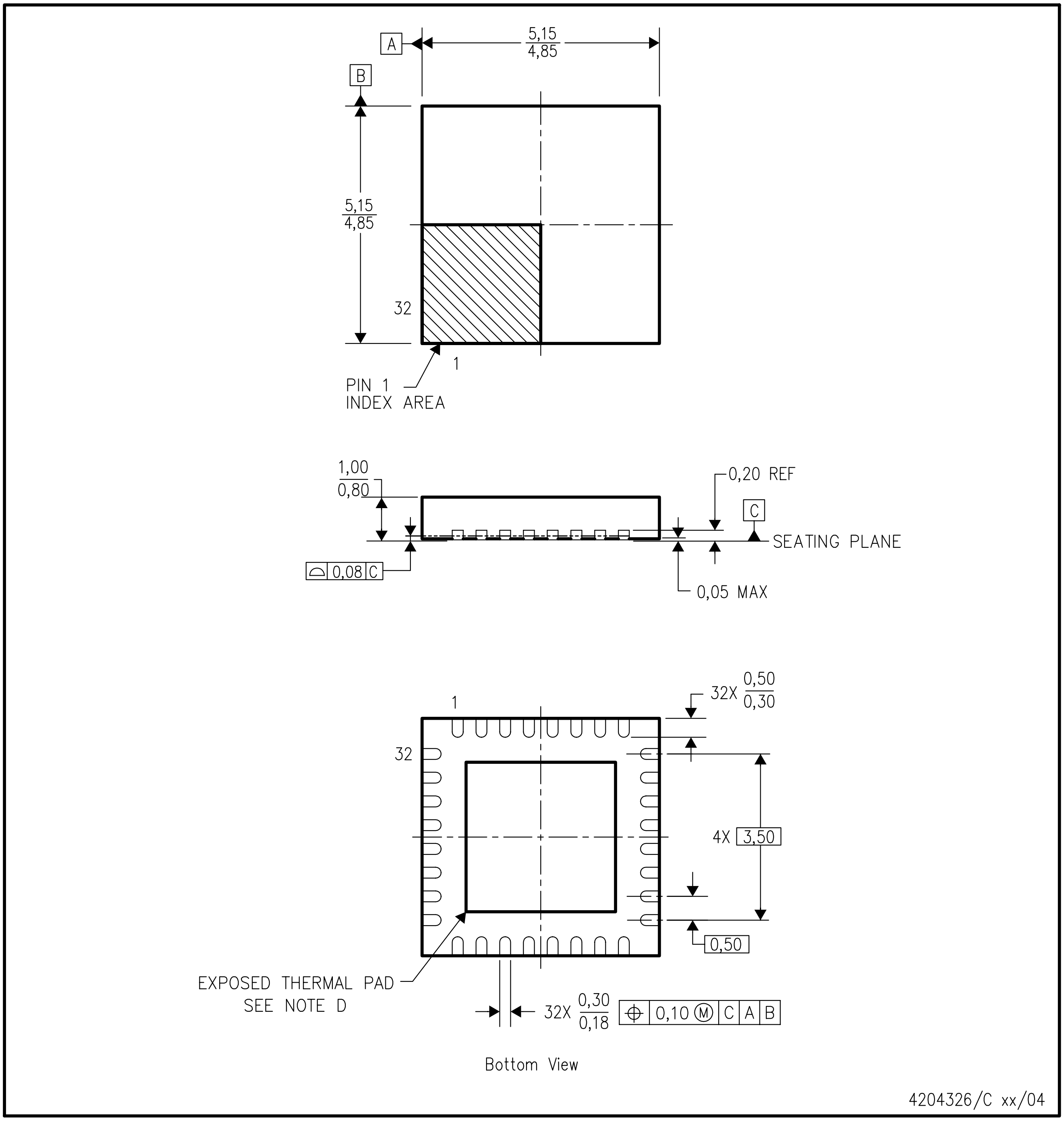
PINS ** / DIM	24	28
A MAX	1.260 (32,04)	1.425 (36,20)
A MIN	1.230 (31,24)	1.385 (35,18)
B MAX	0.310 (7,87)	0.315 (8,00)
B MIN	0.290 (7,37)	0.295 (7,49)



4040050/B 04/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

RHB (S-PQFP-N32) PLASTIC QUAD FLATPACK



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) Package configuration.
- D The Package thermal pad must be soldered to the board for thermal and mechanical performance. See product data sheet for details regarding the exposed thermal pad dimensions.
- E. Falls within JEDEC MO-220.