Micropower Supply Voltage Supervisors

Check for Samples: TLC7701, TLC7725, TLC7703 , TLC7733, TLC7705

FEATURES

- **Power-On Reset Generator**
- **Automatic Reset Generation After Voltage Drop**
- **Precision Voltage Sensor**
- **Temperature-Compensated Voltage Reference**
- **Programmable Delay Time by External Capacitor**
- **Supply Voltage Range . . . 2 V to 6 V**
- **Defined RESET Output from V_{DD} ≥ 1 V**
- **Power-Down Control Support for Static RAM With Battery Backup**
- **Maximum Supply Current of 16 µA**
- **Power Saving Totem-Pole Outputs**
- **Temperature Range . . . Up to –55°C to 125°C**

APPLICATIONS

- **Medical Imaging**

DESCRIPTION

The TLC77xx family of micropower supply voltage supervisors provide reset control, primarily in microcomputer and microprocessor systems.

During power-on, $\overline{\text{RESET}}$ is asserted when V_{DD} reaches 1 V. After minimum V_{DD} (≥2 V) is established, the circuit monitors SENSE voltage and keeps the reset outputs active as long as SENSE voltage ($V_{I(SENSE)}$) remains below the threshold voltage. An internal timer delays return of the output to the inactive state to ensure proper system reset. The delay time, t_d, is determined by an external capacitor:

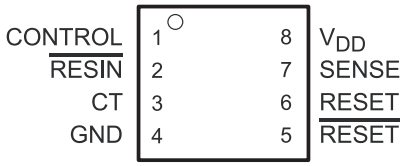
$$t_d = 2.1 \times 10^4 \times C_T$$

Where

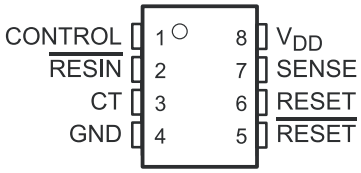
C_T is in farads

t_d is in seconds

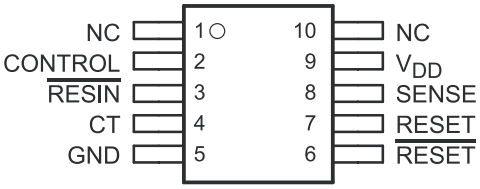
DRB PACKAGE
(TOP VIEW)



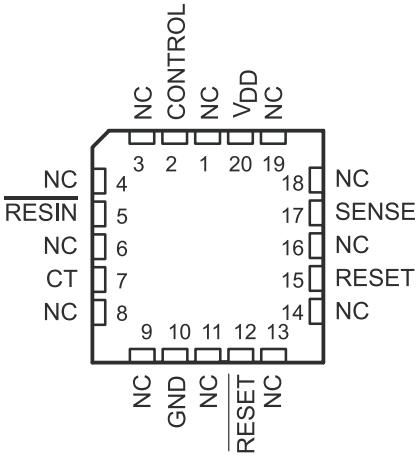
D, JG, P OR PW PACKAGE
(TOP VIEW)



U PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



Except for the TLC7701, which can be customized with two external resistors, each supervisor has a fixed sense threshold voltage set by an internal voltage divider. When SENSE voltage drops below the threshold voltage, the outputs become active and stay in that state until SENSE voltage returns above threshold voltage and the delay time, t_d, has expired.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

In addition to the power-on-reset and undervoltage-supervisor function, the TLC77xx adds power-down control support for static RAM. When CONTROL is tied to GND, RESET will act as active high. The voltage monitor contains additional logic intended for control of static memories with battery backup during power failure. By driving the chip select ($\overline{CS}$) of the memory circuit with the RESET output of the TLC77xx and with the CONTROL driven by the memory bank select signal ($\overline{CSH1}$) of the microprocessor (see Figure 10), the memory circuit is automatically disabled during a power loss. (In this application the TLC77xx power has to be supplied by the battery.)

The TLC77xxI is characterized for operation over a temperature range of –40°C to 85°C; the TLC77xxQ is characterized for operation over a temperature range of –40°C to 125°C; and the TLC77xxM is characterized for operation over the full Military temperature range of –55°C to 125°C.

The 3x3 mm DRB package is also available as a non-magnetic package for medical imaging application.

AVAILABLE OPTIONS

T_A	THRESHOLD VOLTAGE (V)	PACKAGED DEVICES						
		SMALL OUTLINE (D)(1)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	CERAMIC DUAL FLATPACK (U)	PLASTIC DIP (P)	THIN SHRINK SMALL OUTLINE (PW)(2)	SMALL OUTLINE NO LEAD (DRB)
–40°C to 85°C	1.1	TCLC7701ID	—	—	—	TCLC7701IP	TCLC7701IPWR	—
	2.25	TLC7725ID	—	—	—	TLC7725IP	TLC7725IPWR	—
	2.63	TLC7703ID	—	—	—	TLC7703IP	TLC7703IPWR	—
	2.93	TLC7733ID	—	—	—	TLC7733IP	TLC7733IPWR	—
	4.55	TLC7705ID	—	—	—	TLC7705IP	TLC7705IPWR	—
	1.1	TLC7701IDBR	—	—	—	—	—	TLC7701IDRBT-NM
–40°C to 125°C	1.1	TLC7701QD	—	—	—	TLC7701QP	TLC7701QPWR	—
	2.25	TLC7725QD	—	—	—	TLC7725QP	TLC7725QPWR	—
	2.63	TLC7703QD	—	—	—	TLC7703QP	TLC7703QPWR	—
	2.93	TLC7733QD	—	—	—	TLC7733QP	TLC7733QPWR	—
	4.55	TLC7705QD	—	—	—	TLC7705QP	TLC7705QPWR	—
–55°C to 125°C	2.93	—	—	—	—	—	—	—
	4.55	—	—	—	—	—	—	—

(1) The D package is available taped and reeled. Add the suffix R to the device type when ordering (e.g., TLC7705QDR).
(2) The PW package is only available left-end taped and reeled (indicated by the R suffix on the device type; e.g., TLC7705QPWR).

Table 1. FUNCTION TABLE

CONTROL	$\overline{RESIN}$	$V_{I(SENSE)} > V_{IT+}$	RESET	$\overline{RESET}$
L	L	False	H	L
L	L	True	H	L
L	H	False	H	L
L	H	True	L(1)	H(1)
H	L	False	H	L
H	L	True	H	L
H	H	False	H	L
H	H	True	H	H(1)

(1) RESET and $\overline{RESET}$ states shown are valid for $t > t_d$.

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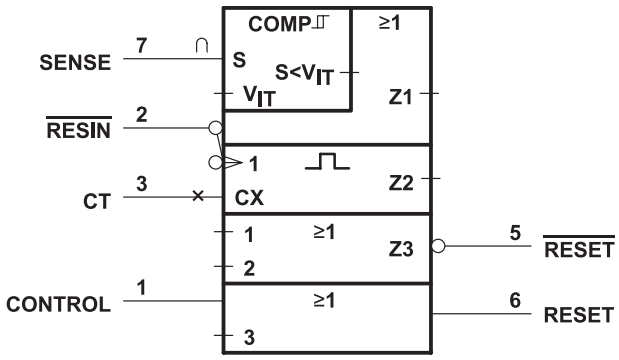
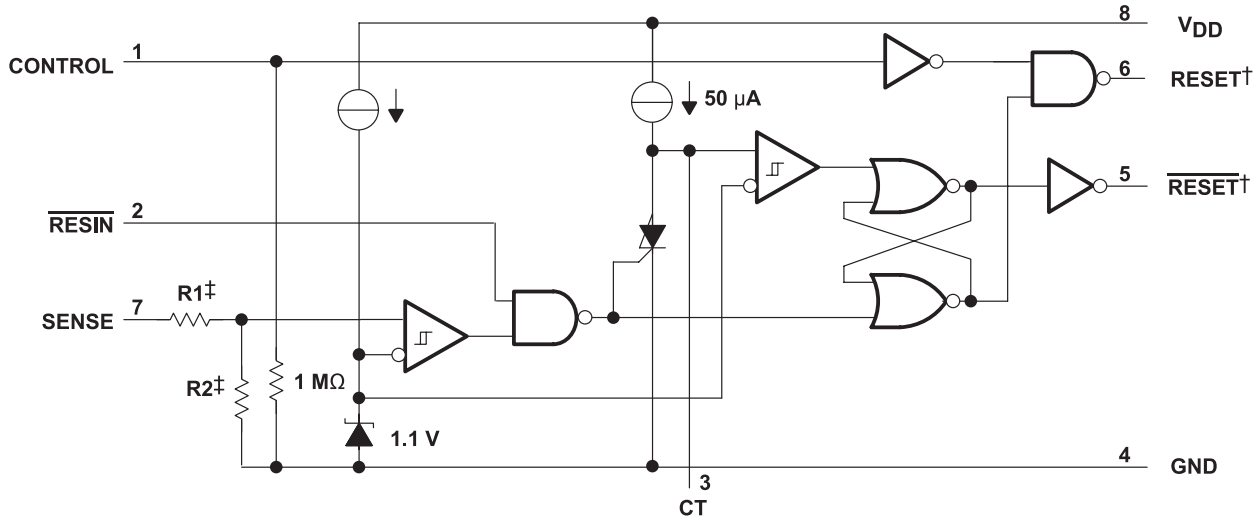
LOGIC SYMBOL



(1) This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

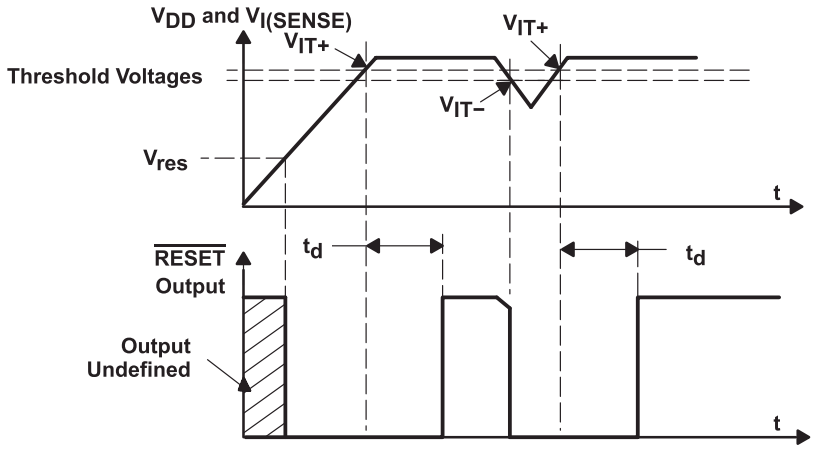
FUNCTIONAL BLOCK DIAGRAM



† Outputs are totem-pole configuration. External pullup or pulldown resistors are not required.
‡ Nominal values:

	R1 (Typ)	R2 (Typ)
TLC7701	0	∞
TLC7725	600 kΩ	600 kΩ
TLC7703	698 kΩ	502 kΩ
TLC7733	750 kΩ	450 kΩ
TLC7705	910 kΩ	290 kΩ

TIMING DIAGRAM



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ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			VALUE	UNIT
V_{DD}	Supply voltage(2)		7	V
	Input voltage range, CONTROL, RESIN, SENSE(2)		–0.3 to 7	V
I_{OL}	Maximum low output current		10	mA
I_{OH}	Maximum high output current,		–10	mA
I_{IK}	Input clamp current, (VI < 0 or VI > VDD)		±10	mA
I_{OK}	Output clamp current, (VO 0 or VO > VDD)		±10	mA
	Continuous total power dissipation		See Dissipation Rating Table	
T_A	Operating free-air temperature range	TL77xxI	–40 to 84	°C
		TL77xxQ	–40 to 125	°C
		TL77xxM	–55 to 125	°C
T_{stg}	Storage temperature range		–65 to 150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.

DISSIPATION RATINGS

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	377 mW	145 mW
DRB				
FK	1375 mW	11.0 mW/°C	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	546 mW	210 mW
P	1000 mW	8.0 mW/°C	520 mW	200 mW
PW	525 mW	4.2 mW/°C	273 mW	105 mW
U	700 mW	5.5 mW/°C	370 mW	150 mW

RECOMMENDED OPERATING CONDITIONS

at specified temperature range

			MIN	MAX	UNIT
V_{DD}	Supply voltage		2	6	V
V_I	Input voltage		0	V_{DD}	V
V_{IH}	High-level input voltage at $\overline{\text{RESIN}}$ and CONTROL(1)		$0.7\times V_{DD}$		V
V_{IL}	Low-level input voltage at $\overline{\text{RESIN}}$ and CONTROL(1)			$0.2\times V_{DD}$	V
I_{OH}	High-level output current			–2	mA
I_{OL}	Low-level output current			2	mA
Δt/ΔV	input transition rise and fall rate at $\overline{\text{RESIN}}$ and CONTROL			100	ns/ V
T_A	Operating free-air temperature range	TLC77xxI	–40	85	°C
		TLC77xxQ	–40	125	
		TLC77xxM	–55	125	

(1) To ensure a low supply current, V_{IL} should be kept <0.3 V and $V_{IH} > V_{DD}$ –0.3 V.

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ELECTRICAL CHARACTERISTICS

over recommended operating conditions(1) (unless otherwise noted)

PARAMETER				TEST CONDITIONS	TLC77xx			UNIT
					MIN	TYP	MAX	
V_{OH}	High-level output voltage	I_{OH} = –20 µA		V_{DD} = 2 V	1.8			V
				V_{DD} = 2.7 V	2.5			
				V_{DD} = 4.5 V	4.3			
		I_{OH} = 2 –mA		V_{DD} = 4.5 V	3.7			
V_{OL}	Low-Level output voltage	I_{OL} = 20 µA		V_{DD} = 2 V			0.2	V
				V_{DD} = 2.7 V			0.2	
				V_{DD} = 4.5 V			0.2	
		I_{OL} = 2 mA		V_{DD} = 4.5 V			0.5	
$V_{IT–}$	Negative-going input threshold voltage, SENSE(2)		TCLC7701	V_{DD} = 2 V to 6 V	1.04	1.1	1.16	mV
			TLC7725		2.18	2.25	2.32	
			TLC7703		2.56	2.63	2.70	
			TLC7733		2.86	2.93	3	
			TLC7705		4.47	4.55	4.63	
V_{hus}	Hysteresis voltage, SENSE		TCLC7701	V_{DD} = 2 V to 6 V		30		mV
			TLC7725			70		
			TLC7703					
			TLC7733					
			TLC7705					
V_{res}	Power-up reset voltage(3)			I_{OL} = 20 µA			1	V
I_I	Input current	$\overline{RESIN}$		V_I = 0 V to V_{DD}			2	µA
		CONTROL		V_I = V_{DD}		7	15	
		SENSE		V_I = 5 V		5	10	
		SENSE, TLC7701 only		V_I = 5 V			2	
I_{DD}	Supply current			$\overline{RESIN}$ = V_{DD}, SENSE = V_{DD} ≥ V_{IT}max + 0.2 V, CONTROL = 0 V, Outputs open		9	16	µA
$I_{DD(d)}$	Supply current during t_d			VDD = 5 V, V_{CT} = 0, $\overline{RESIN}$ = V_{DD}, SENSE = V_{DD}, CONTROL = 0 V, Outputs open		120	150	µA
C_I	Input capacitance, SENSE			V_I = 0 V to V_{DD}		50		pF

(1) All characteristics are measured with C_T = 0.1 µF.
(2) To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 mF) should be connected near the supply terminals.
(3) The lowest supply voltage at which $\overline{RESET}$ becomes active. The symbol V_{res} is not currently listed within EIA or JEDEC standards for semiconductor symbology. Rise time of V_{DD}≥ 15 µs/V.

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ELECTRICAL CHARACTERISTICS

over recommended operating conditions(1) (unless otherwise noted)

PARAMETER			TEST CONDITIONS		TLC77xxM			UNIT
					MIN	TYP(2)	MAX	
V_{OH}	High-level output voltage	I_{OH} = –20 µA	V_{DD} = 2 V	T_A = 25°C	1.8			V
				T_A = –55°C to 125°C	1.7			
			V_{DD} = 2.7 V	T_A = 25°C	2.5			V
				T_A = –55°C to 125°C	2.3			
			V_{DD} = 4.5 V	T_A = 25°C	4.3			V
				T_A = –55°C to 125°C	4.2			
		I_{OH} = –2 µA	V_{DD} = 4.5 V	T_A = 25°C	3.7			V
				T_A = –55°C to 125°C	3.6			
V_{OL}	Low-level output voltage	I_{OL} = –20 µA	V_{DD} = 2 V	T_A = 25°C			0.2	V
				T_A = –55°C to 125°C			0.2	
			V_{DD} = 2.7 V	T_A = 25°C			0.2	V
				T_A = –55°C to 125°C			0.2	
			V_{DD} = 4.5 V	T_A = 25°C			0.2	V
				T_A = –55°C to 125°C			0.2	
		I_{OL} = 2 mA	V_{DD} = 4.5 V	T_A = 25°C			0.5	V
				T_A = –55°C to 125°C			0.5	
V_{IT-}	Negative-going input threshold voltage, SENSE (3)	TLC7733	V_{DD} = 2 V to 6 V		2.86	2.93	3.1	V
		TLC7705			4.3	4.5	4.8	
V_{hys}	Hysteresis voltage, SENSE		V_{DD} = 2 V to 6 V			70		mV
V_{res}	Power-up reset voltage(2)		I_{OL} = 20 µA				1	V
I_I	Input current	$\overline{RESIN}$	V_I = 0 V to V_{DD}				2	µA
		CONTROL	V_I = V_{DD}			7	15	
		SENSE	V_I = 5 V			5	10	
		SENSE, TLC7701 only	V_I = 5 V				2	
I_{DD}	Supply current		$\overline{RESIN}$ = VDD, SENSE = $V_{DD} \geq V_{IT}$max + 0.2 V, CONTROL = 0 V, Outputs open			9	16	µA
$I_{DD(d)}$	Supply current during t_d	TLC7733	V_{CT} = 0 , $\overline{RESIN}$ = V_{DD}, CONTROL = 0 V, SENSE = V_{DD}, Outputs open	V_{DD} = 3.3 V			250	µA
		TLC7705		V_{DD} = 5 V		120	150	
C_I	Input capacitance, SENSE		V_I = 0 V to V_{DD}			50		pF

(1) All characteristics are measured with C_T = 0.1 µF.
(2) Typical values apply at T_A = 25°C.
(3) To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 mF) should be connected near the supply terminals.

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SWITCHING CHARACTERISTICS

at V_{DD} = 5 V, R_L = 2 kΩ, C_L = 50 pF, T_A = 25°C (unless otherwise noted)

PARAMETER		MEASURED		TEST CONDITIONS	TLC77xx			UNIT
		FROM (INPUT)	TO (OUTPUT)		MIN	TYP	MAX	
t_d	Delay time	$V_{I(SENSE)} \geq V_{IT+}$	RESET and $\overline{\text{RESET}}$	$\overline{\text{RESIN}}$ = 0.7 × V_{DD}, CONTROL = 0.2 × V_{DD}, C_T = 100 nF, T_A = Full range, See timing diagram	1.1	2.1	4.2	ms
t_{PLH}	Propagation delay time, low-to-high-level output	SENSE	$\overline{\text{RESET}}$	V_{IH} = V_{IT+}max + 0.2 V, V_{IL} = V_{IT-}min – 0.2 V, $\overline{\text{RESIN}}$ = 0.7 × V_{DD}, CONTROL = 0.2 × V_{DD}, CT = NC(1)			20	µs
t_{PHL}	Propagation delay time, high-to-low-level output						5	
t_{PLH}	Propagation delay time, low-to-high-level output		RESET				5	
t_{PHL}	Propagation delay time, high-to-low-level output						20	
t_{PLH}	Propagation delay time, low-to-high-level output	$\overline{\text{RESIN}}$	$\overline{\text{RESET}}$	V_{IH} = 0.7 × V_{DD}, V_{IL} = 0.2 × V_{DD}, SENSE = V_{IT+}max + 0.2 V, CONTROL = 0.2 × V_{DD}, CT = NC(1)			20	µs
t_{PHL}	Propagation delay time, high-to-low-level output						40	ns
t_{PLH}	Propagation delay time, low-to-high-level output		RESET				45	ns
t_{PHL}	Propagation delay time, high-to-low-level output						20	µs
t_{PLH}	Propagation delay time, low-to-high-level output	CONTROL	RESET	V_{IH} = 0.7 × V_{DD}, V_{IL} = 0.2 × V_{DD}, SENSE = V_{IT+}max + 0.2 V, RESIN = 0.7 × V_{DD}, CT = NC(1)			38	ns
t_{PHL}	Propagation delay time, high-to-low-level output						38	ns
	Low-level minimum pulse duration to switch RESET and $\overline{\text{RESET}}$	SENSE		V_{IH} = V_{IT+}max + 0.2 V, V_{IL} = V_{IT-}min –0.2 V,				
		$\overline{\text{RESIN}}$		V_{IL} = 0.2 × V_{DD}, V_{IH} = 0.7 × V_{DD}				
t_r	Rise time		RESET and $\overline{\text{RESET}}$	10% to 90%				
t_f	Fall time			90% to 10%				

(1) NC = No capacitor, and includes up to 100-pF probe and jig capacitance.

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SWITCHING CHARACTERISTICS

at V_{DD} = 5 V, R_L = 2 kΩ, C_L = 50 pF, T_A = 25°C (unless otherwise noted)

PARAMETER		MEASURED		TEST CONDITIONS	T_A	TLC77xxM			UNIT
		FROM (INPUT)	TO (OUTPUT)			MIN	TYP	MAX	
t_d	Delay time	$V_{I(SENSE)} \geq V_{IT+}$	RESET and $\overline{\text{RESET}}$	RESIN = 2.7 V, CONTROL = 0.4 V, C_T = 100 nF, See timing diagram	Full range	1.1	2.1	4.2	ms
t_{PLH}	Propagation delay time, low-to-high-level output	SENSE	$\overline{\text{RESET}}$	$V_{IH} = V_{IT+}$max + 0.2 V, $V_{IL} = V_{IT-min}$ - 0.2 V, $\overline{\text{RESIN}}$ = 2.7 V, CONTROL = 0.4 V, CT = NC(1)	25°C			20	µs
					Full range			24	
			RESET		25°C			5	µs
					Full range			7	
t_{PHL}	Propagation delay time, high-to-low-level output	SENSE	$\overline{\text{RESET}}$	$V_{IH} = V_{IT+}$max + 0.2 V, $V_{IL} = V_{IT-min}$ - 0.2 V, $\overline{\text{RESIN}}$ = 2.7 V, CONTROL = 0.4 V, CT = NC(1)	25°C			5	µs
					Full range			7	
			RESET		25°C			20	µs
					Full range			24	
t_{PLH}	Propagation delay time, low-to-high-level output	$\overline{\text{RESIN}}$	$\overline{\text{RESET}}$	V_{IH} = 2.7 V, V_{IL} = 0.4 V, SENSE = V_{IT+}max + 0.2 V, CONTROL = 0.4 V, CT = NC(1)	25°C			20	µs
					Full range			24	
			RESET		25°C			45	ns
					Full range			65	
t_{PHL}	Propagation delay time, high-to-low-level output	$\overline{\text{RESIN}}$	$\overline{\text{RESET}}$	V_{IH} = 2.7 V, V_{IL} = 0.4 V, SENSE = V_{IT+}max + 0.2 V, CONTROL = 0.4 V, CT = NC(1)	25°C			40	ns
					Full range			60	
			RESET		25°C			20	µs
					Full range			24	
t_{PLH}	Propagation delay time, low-to-high-level output	CONTROL	RESET	V_{IH} = 2.7 V, V_{IL} = 0.4 V, SENSE = V_{IT+}max + 0.2 V, $\overline{\text{RESIN}}$ = 2.7 V, CT = NC(1)	25°C			38	ns
					Full range			58	
t_{PHL}	Propagation delay time, high-to-low-level output				25°C			38	ns
					Full Range			58	
	Low-level minimum pulse duration	SENSE		$V_{IH} = V_{IT+}$max + 0.2 V, $V_{IL} = V_{IT-min}$ - 0.2 V	Full range	3			µs
		$\overline{\text{RESIN}}$		V_{IL} = 0.4 V, V_{IH} = 2.7 V		1			
t_r	Rise time		RESET and $\overline{\text{RESET}}$	10% to 90%	Full range		8		ns/V
t_f	Fall time			90% to 10%			4		

(1) NC = No capacitor, and includes up to 100-pF probe and jig capacitance.

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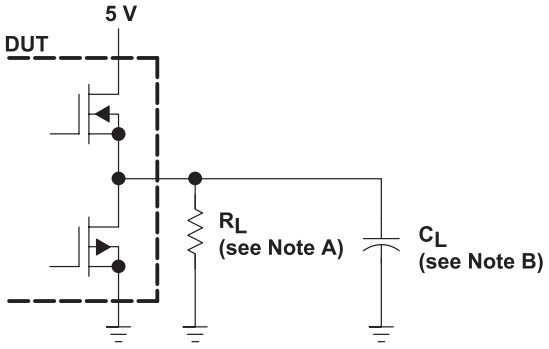
PARAMETER MEASUREMENT INFORMATION



NOTES: A. For switching characteristics, R_L = 2 kΩ.
B. C_L = 50 pF includes jig and probe capacitance.

Figure 1. RESET and $\overline{\text{RESET}}$ Output Configurations

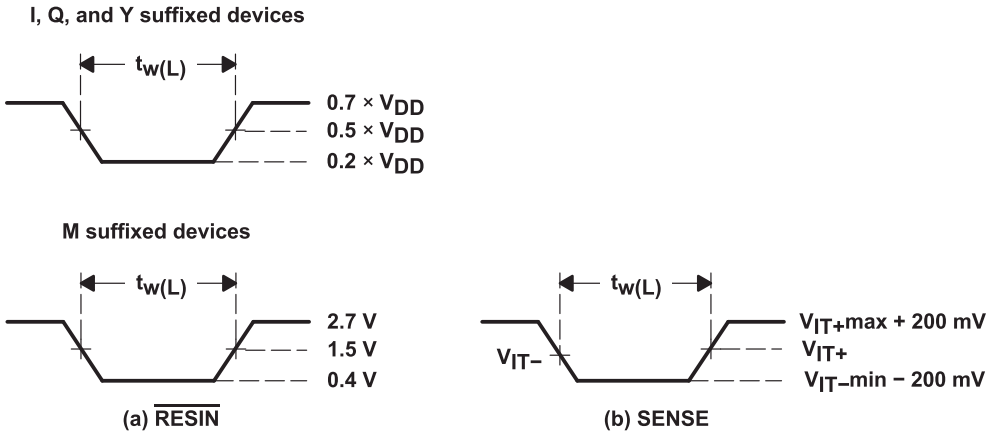


Figure 2. Input Pulse Definition Waveforms

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TYPICAL CHARACTERISTICS

NORMALIZED INPUT THRESHOLD VOLTAGE vs TEMPERATURE

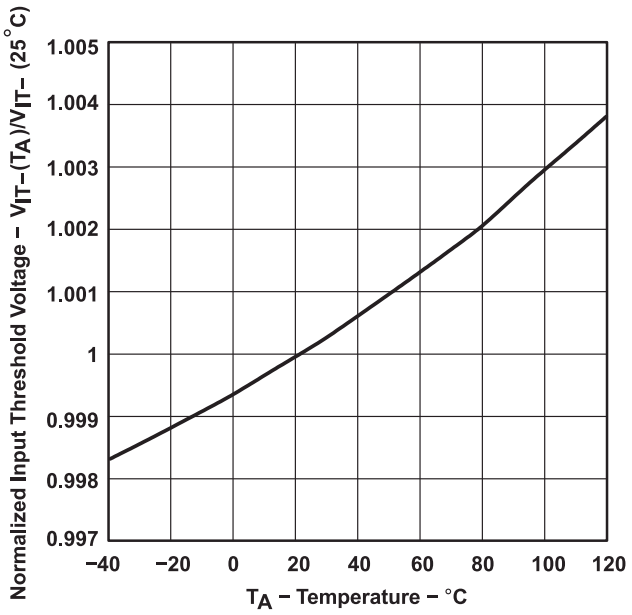

Figure 3.

SUPPLY CURRENT vs SUPPLY VOLTAGE

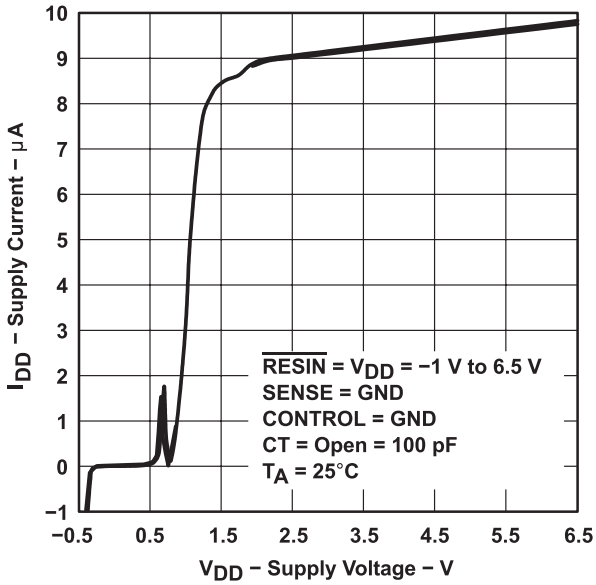

Figure 4.

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

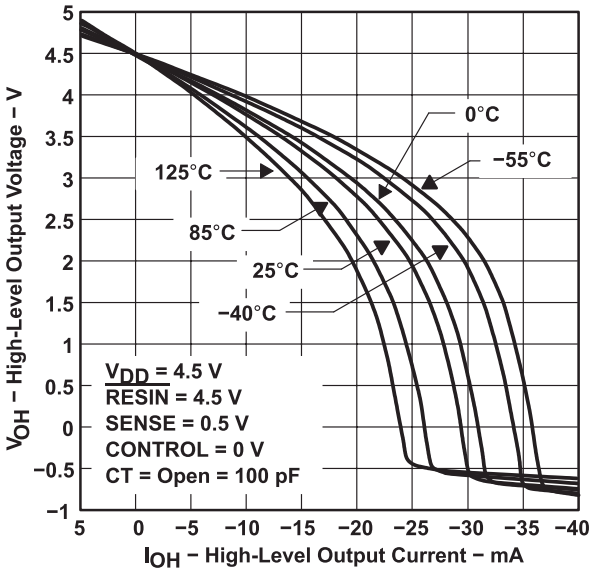

Figure 5.

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

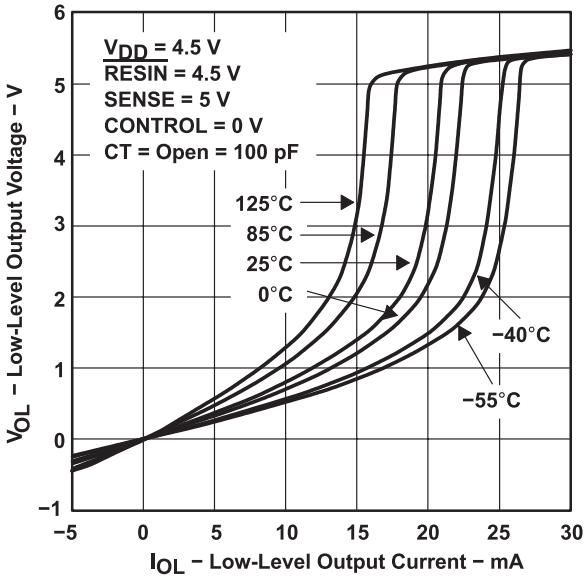

Figure 6.

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TYPICAL CHARACTERISTICS (continued)

INPUT CURRENT vs INPUT VOLTAGE AT SENSE

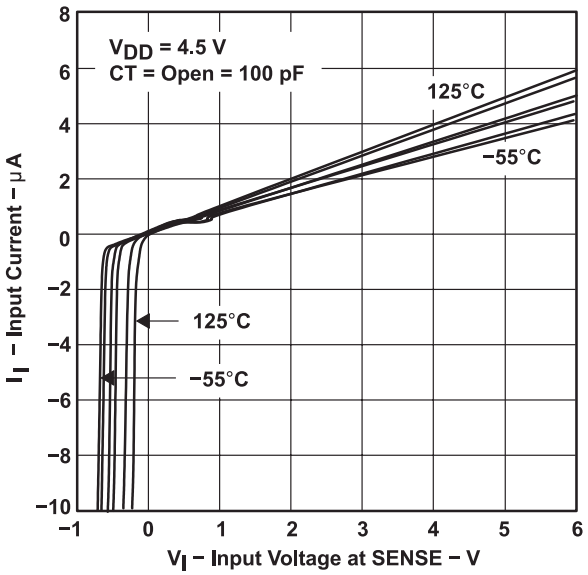

Figure 7.

MINIMUM PULSE DURATION AT SENSE vs SENSE THRESHOLD OVERDRIVE

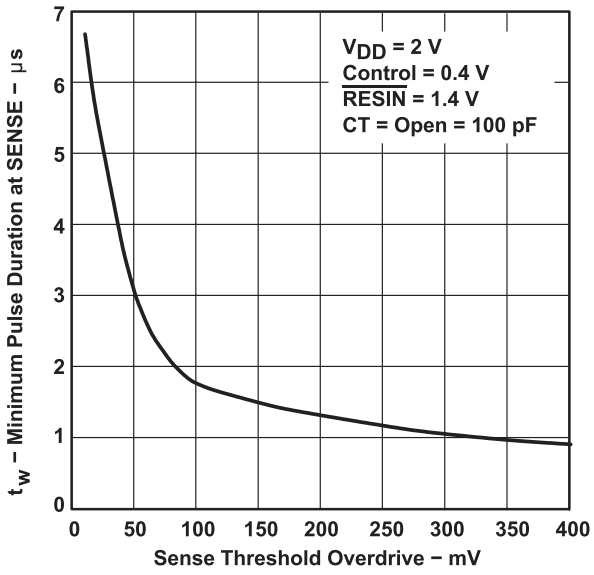

Figure 8.

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APPLICATION INFORMATION

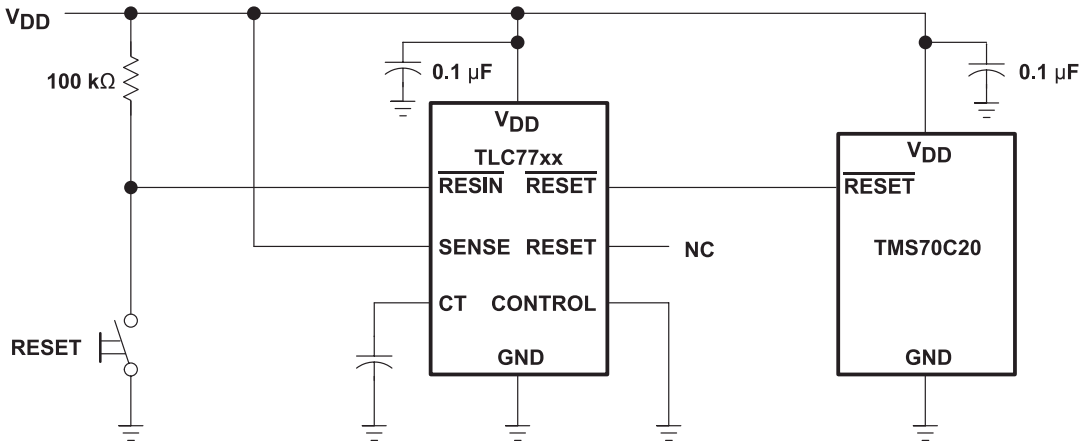

Figure 9. Reset Controller in a Microcomputer System

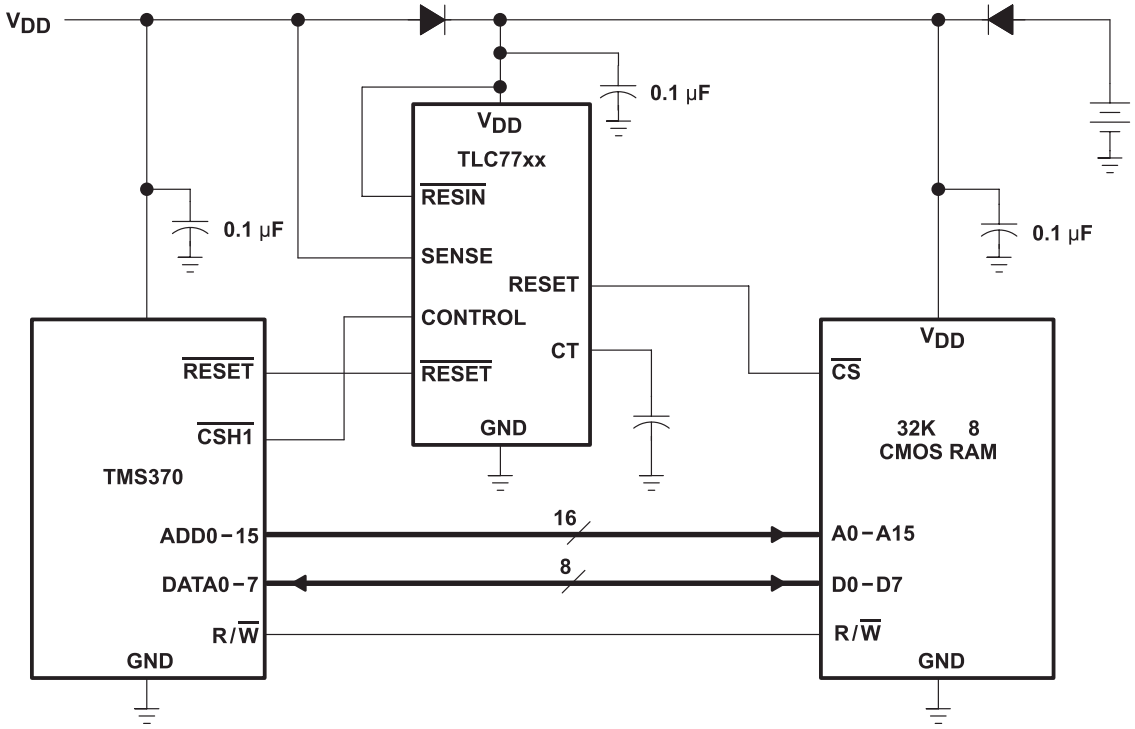

Figure 10. Data Retention During Power Down Using Static CMOS RAMs

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Changes from Revision L (February 2003) to Revision M **Page**

- Updated the DRB package Pin Out dimensions and Ordering Information. 1

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
5962-9750901Q2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-9750901QPA	ACTIVE	CDIP	JG	8	1	TBD	Call TI	Call TI	
5962-9751301Q2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-9751301QHA	ACTIVE	CFP	U	10	1	TBD	Call TI	Call TI	
5962-9751301QPA	ACTIVE	CDIP	JG	8	1	TBD	Call TI	Call TI	
TLC7701ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7701IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7701IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7701IDRBT-NM	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	
TLC7701IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7701IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC7701IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC7701IPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7701IPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7701IPWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI	
TLC7701IPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7701IPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7701QD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7701QDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7701QDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TLC7701QDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7701QP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC7701QPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC7701QPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7701QPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7701QPWLE	PREVIEW	TSSOP	PW	8		TBD	Call TI	Call TI	
TLC7701QPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7701QPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7703ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7703IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7703IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7703IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7703IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC7703IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC7703IPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7703IPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7703IPWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI	
TLC7703IPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7703IPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7703QD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TLC7703QDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7703QP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC7703QPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC7703QPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7703QPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7705ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7705IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7705IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7705IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7705IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC7705IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC7705IPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7705IPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7705IPWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI	
TLC7705IPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7705IPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7705MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
TLC7705MJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	
TLC7705MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	
TLC7705MUB	ACTIVE	CFP	U	10	1	TBD	A42	N / A for Pkg Type	
TLC7705QD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7705QDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TLC7705QDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7705QDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7705QP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC7705QPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC7705QPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7705QPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7705QPWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI	
TLC7705QPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7705QPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7725ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7725IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7725IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7725IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7725IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC7725IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC7725IPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7725IPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7725IPWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI	
TLC7725IPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7725IPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TLC7725QD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7725QDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7725QDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7725QDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7725QP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC7725QPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC7725QPWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI	
TLC7725QPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7725QPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7733ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7733IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7733IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7733IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7733IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC7733IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC7733IPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7733IPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7733IPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7733IPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7733MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
TLC7733MJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TLC7733MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	
TLC7733QD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7733QDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7733QDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7733QDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7733QP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC7733QPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC7733QPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7733QPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7733QPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7733QPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLC7701, TLC7705, TLC7705M, TLC7733, TLC7733M :

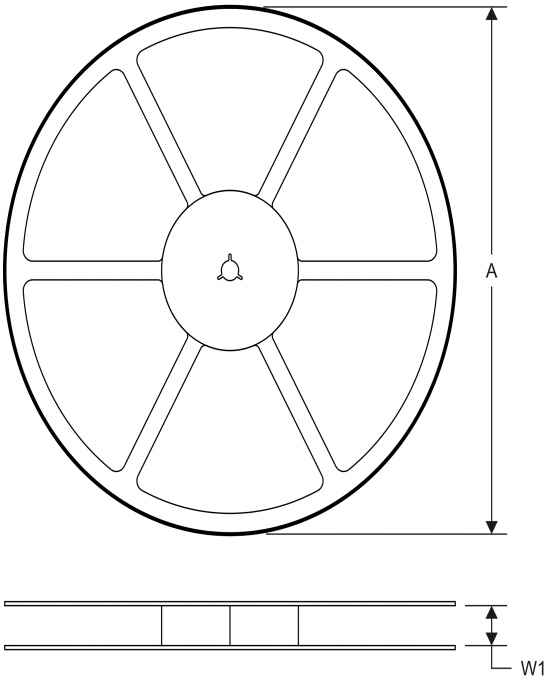
- Catalog: TLC7705, TLC7733
- Automotive: TLC7701-Q1, TLC7705-Q1, TLC7705-Q1, TLC7733-Q1, TLC7733-Q1
- Enhanced Product: TLC7701-EP, TLC7705-EP, TLC7705-EP, TLC7733-EP, TLC7733-EP
- Military: TLC7705M, TLC7733M

NOTE: Qualified Version Definitions:

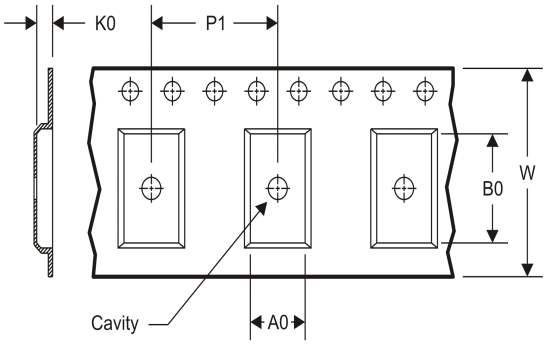
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

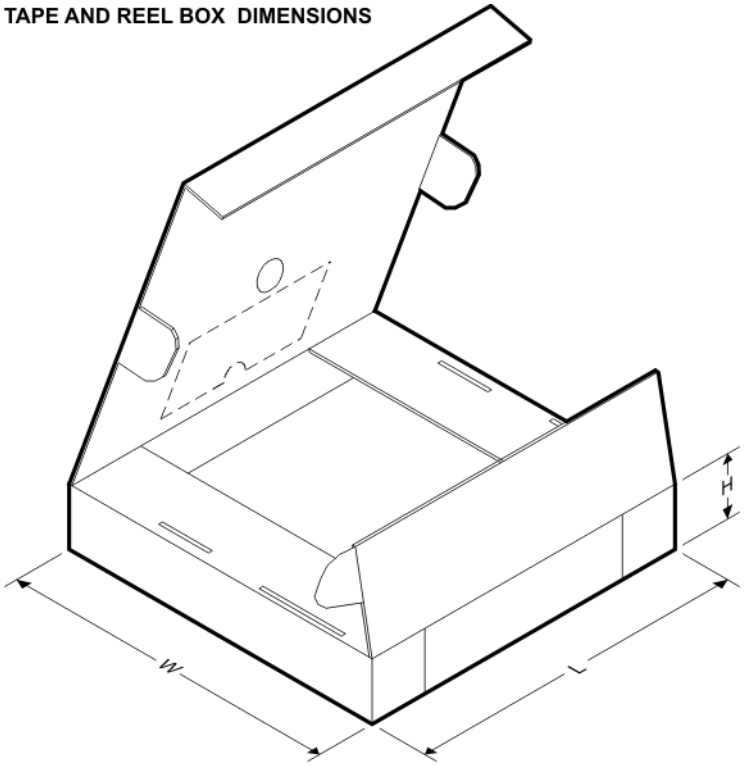
TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC7701IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC7701IDRBT-NM	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLC7701IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC7701QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC7701QPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC7703IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC7703IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC7705IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC7705IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC7705QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC7705QPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC7725IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC7725IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC7725QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC7725QPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC7733IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC7733IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC7733IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC7733QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC7733QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC7733QPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



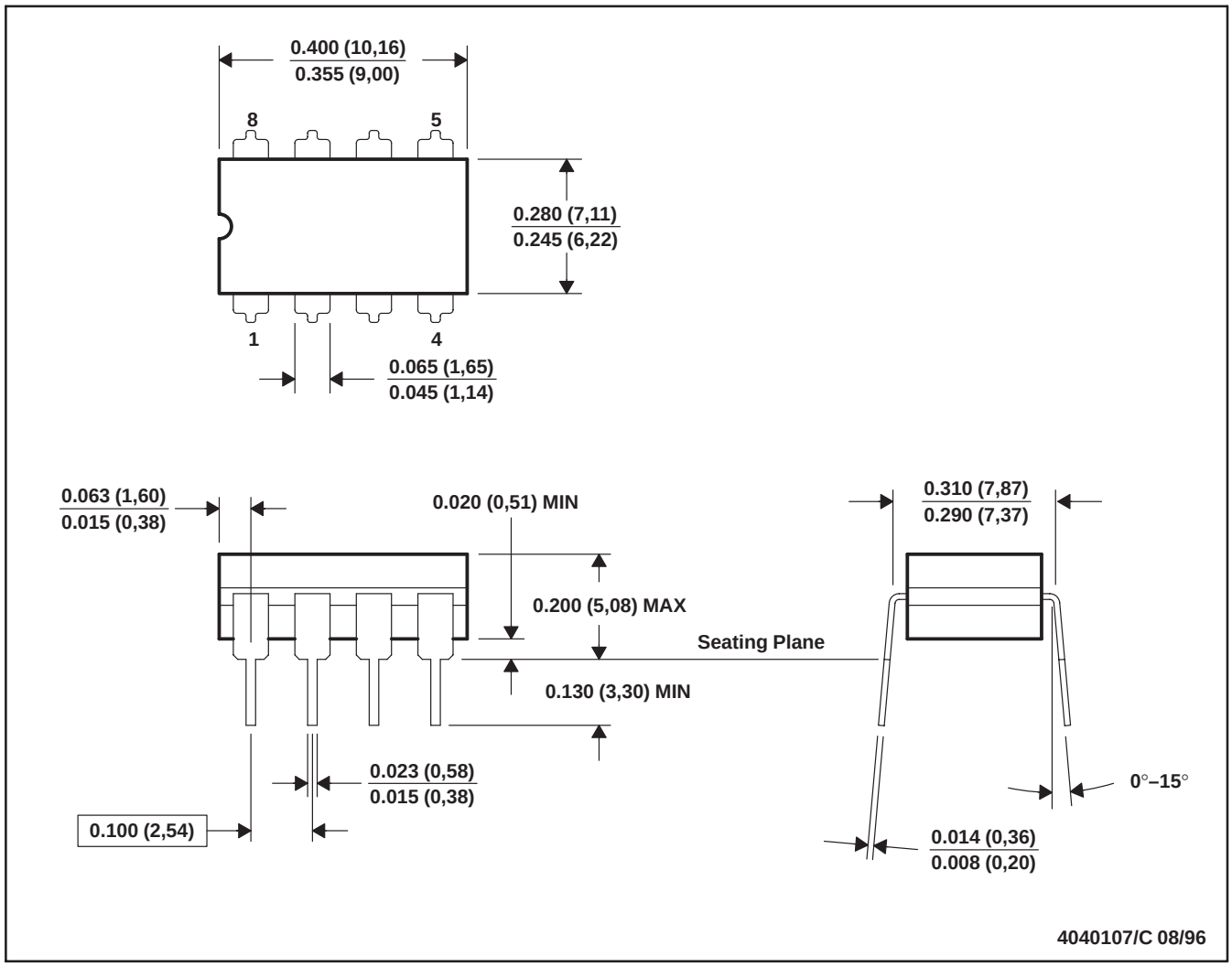
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC7701IDR	SOIC	D	8	2500	367.0	367.0	35.0
TLC7701IDRBT-NM	SON	DRB	8	250	210.0	185.0	35.0
TLC7701IPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TLC7701QDR	SOIC	D	8	2500	367.0	367.0	35.0
TLC7701QPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TLC7703IDR	SOIC	D	8	2500	367.0	367.0	35.0
TLC7703IPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TLC7705IDR	SOIC	D	8	2500	367.0	367.0	35.0
TLC7705IPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TLC7705QDR	SOIC	D	8	2500	367.0	367.0	35.0
TLC7705QPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TLC7725IDR	SOIC	D	8	2500	367.0	367.0	35.0
TLC7725IPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TLC7725QDR	SOIC	D	8	2500	367.0	367.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC7725QPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TLC7733IDR	SOIC	D	8	2500	367.0	367.0	35.0
TLC7733IDR	SOIC	D	8	2500	367.0	367.0	35.0
TLC7733IPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TLC7733QDR	SOIC	D	8	2500	367.0	367.0	35.0
TLC7733QDR	SOIC	D	8	2500	367.0	367.0	35.0
TLC7733QPWR	TSSOP	PW	8	2000	367.0	367.0	35.0

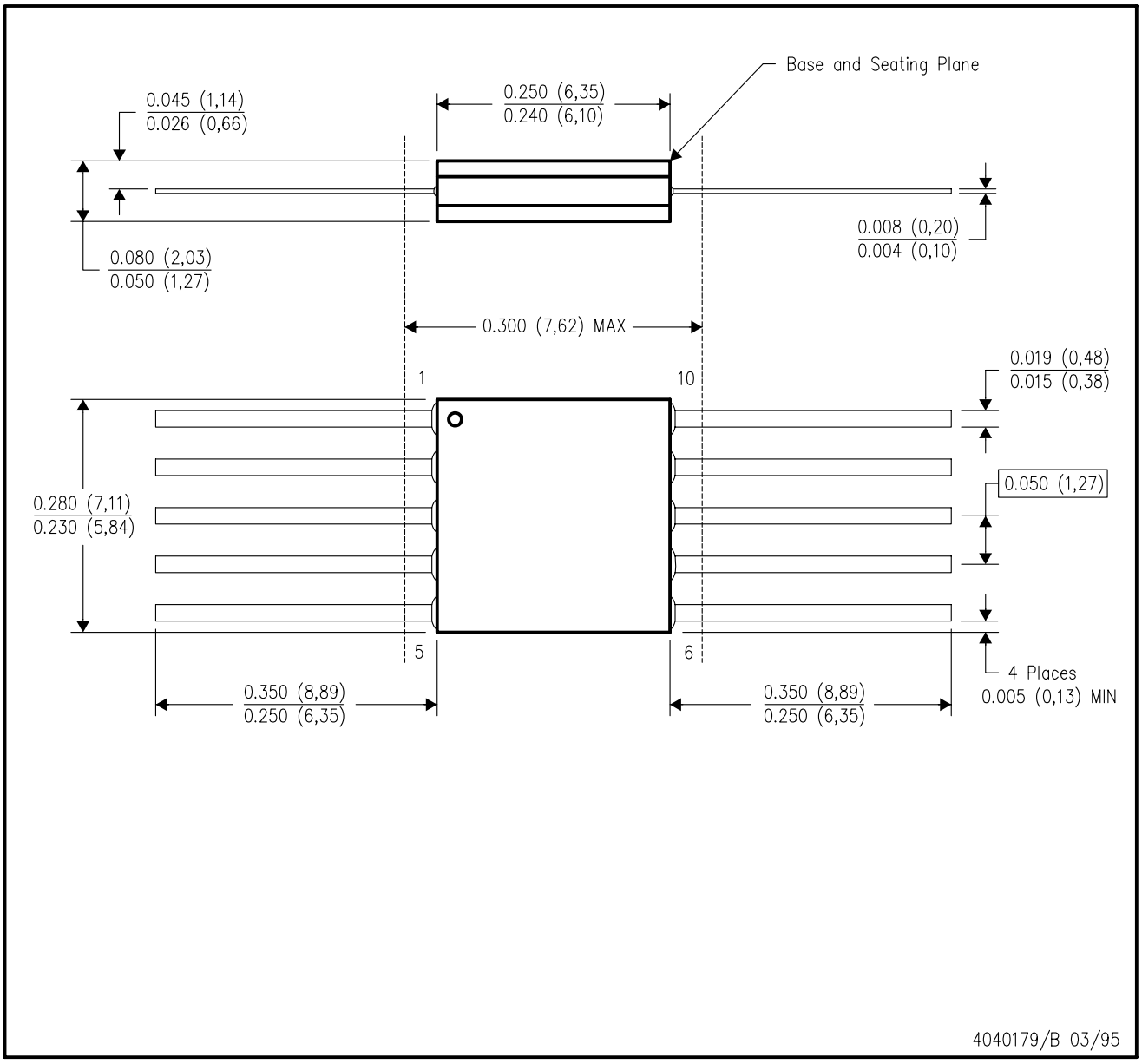
MCER001A – JANUARY 1995 – REVISED JANUARY 1997

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

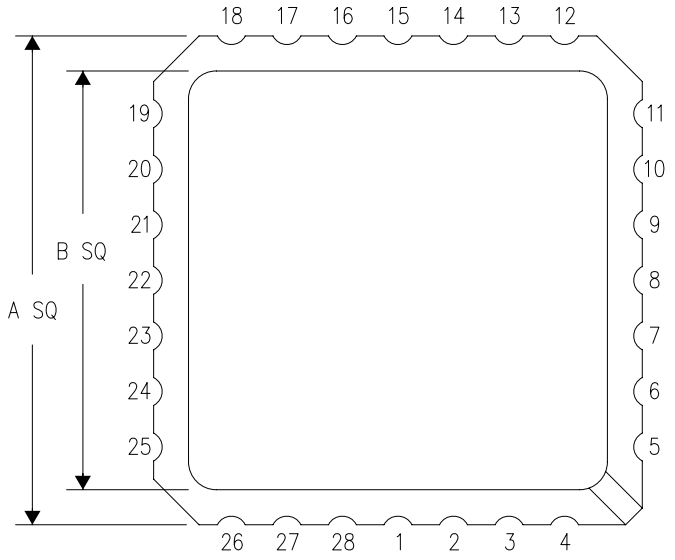
U (S–GDFP–F10) CERAMIC DUAL FLATPACK



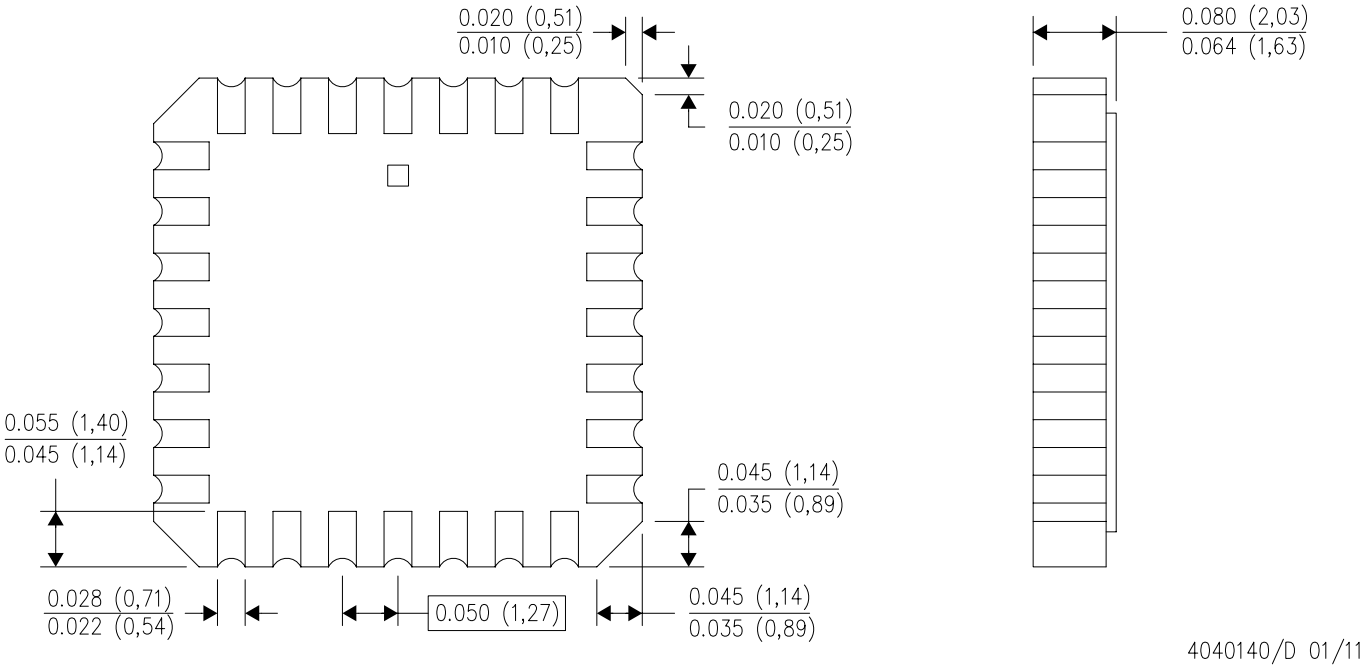
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F10 and JEDEC MO–092AA

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



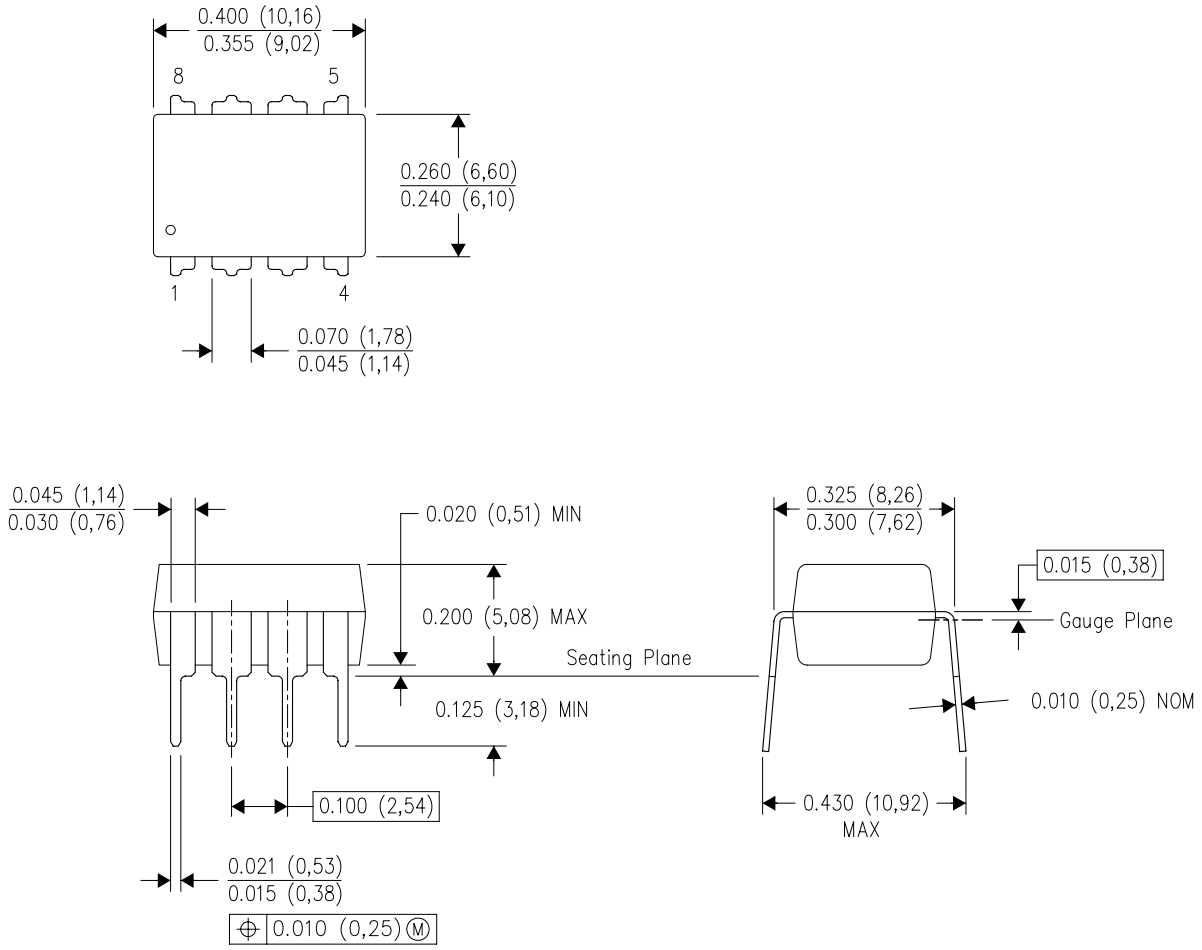
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

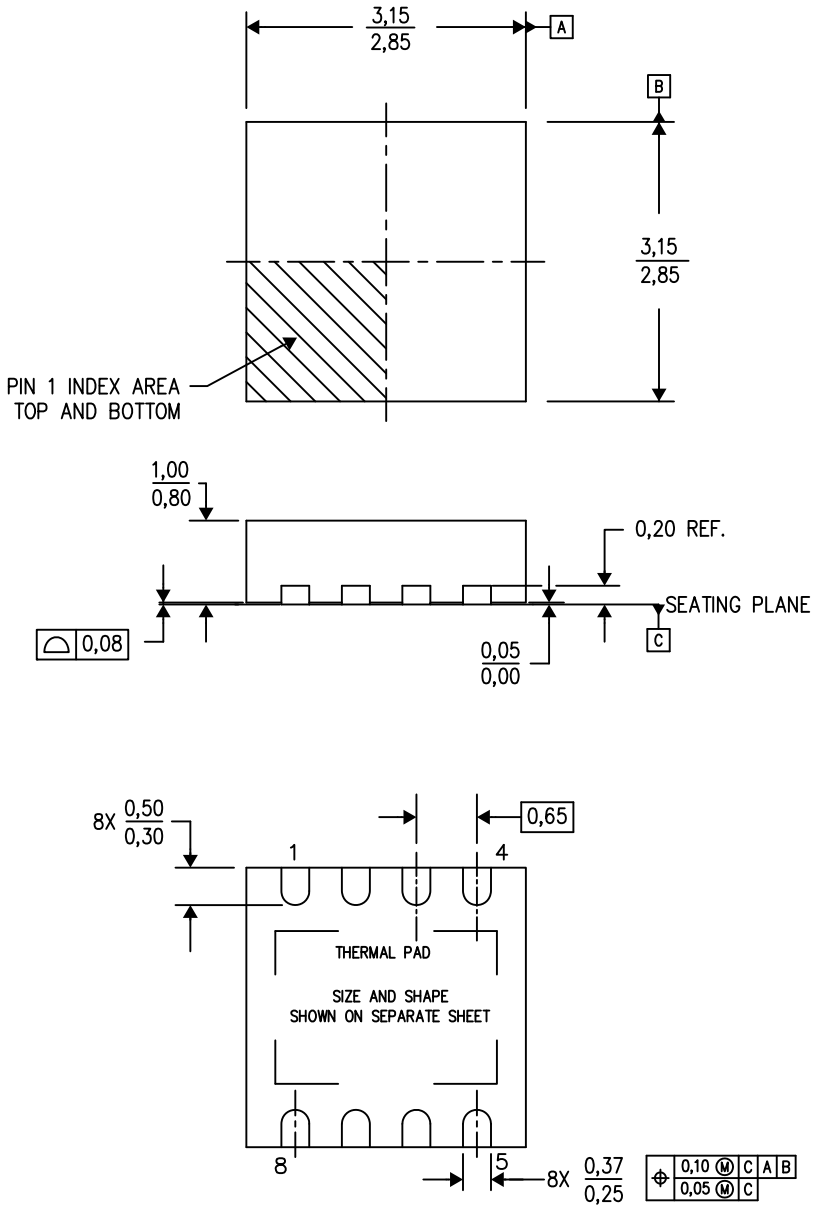
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



4203482–2/K 06/12

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

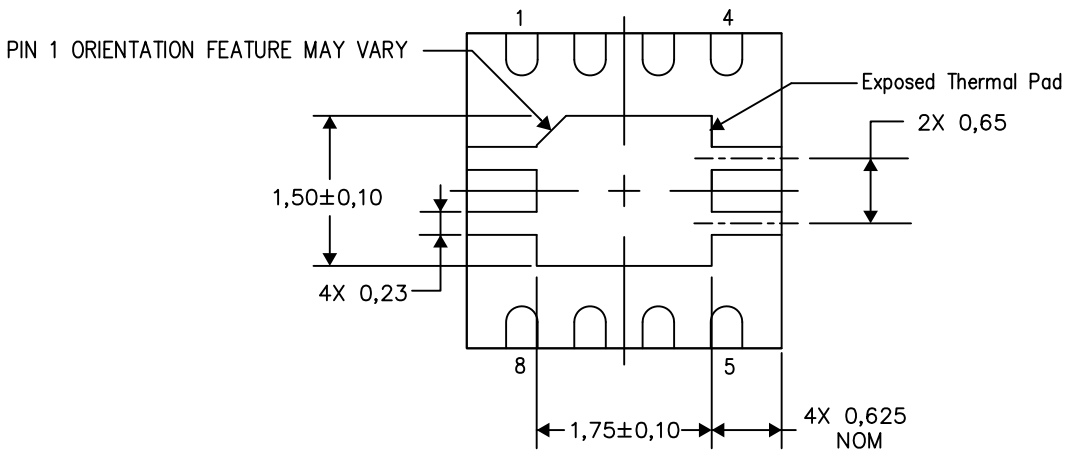
DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



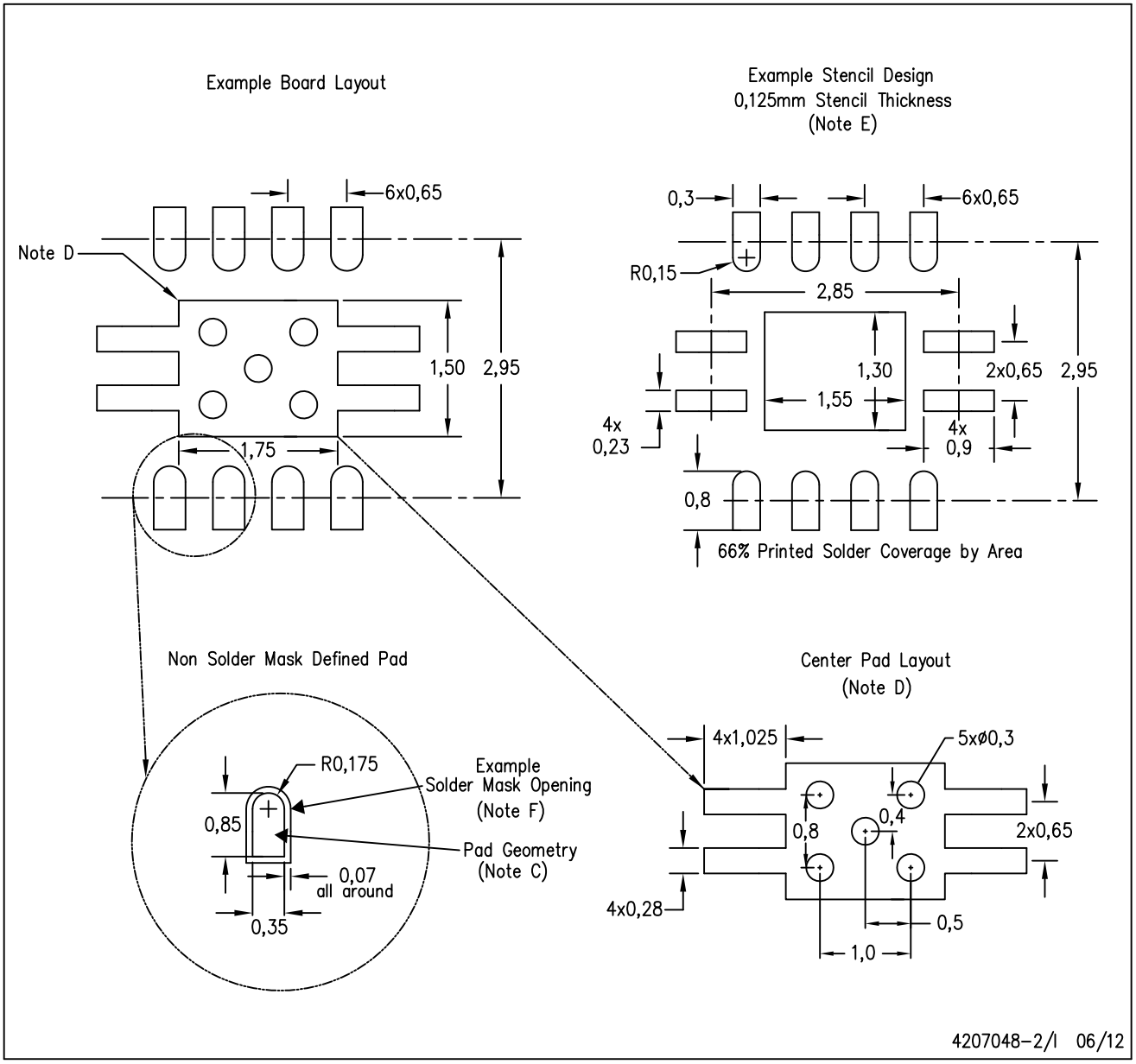
Bottom View

Exposed Thermal Pad Dimensions

4206340–2/M 06/12

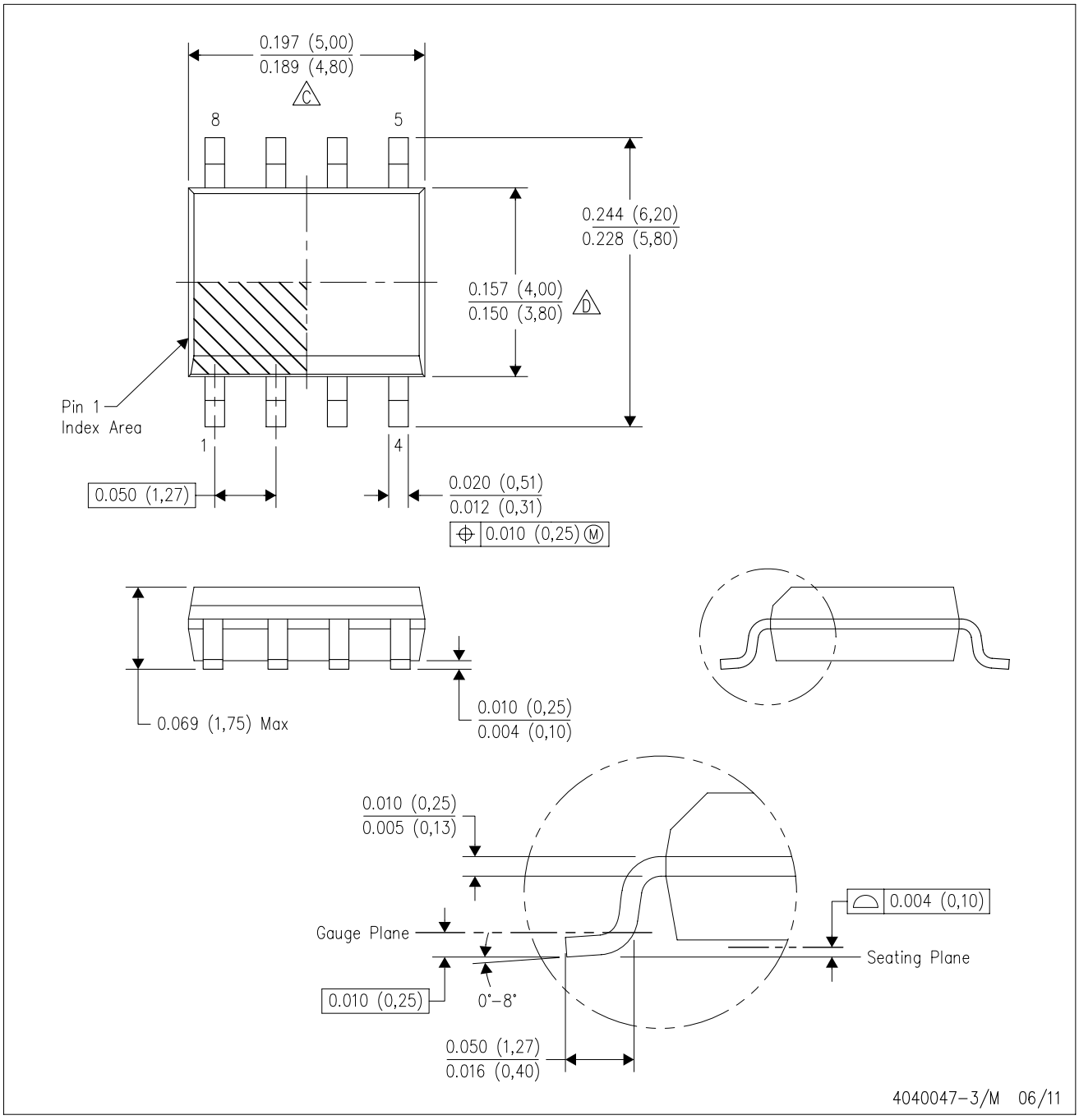
NOTE: All linear dimensions are in millimeters

DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



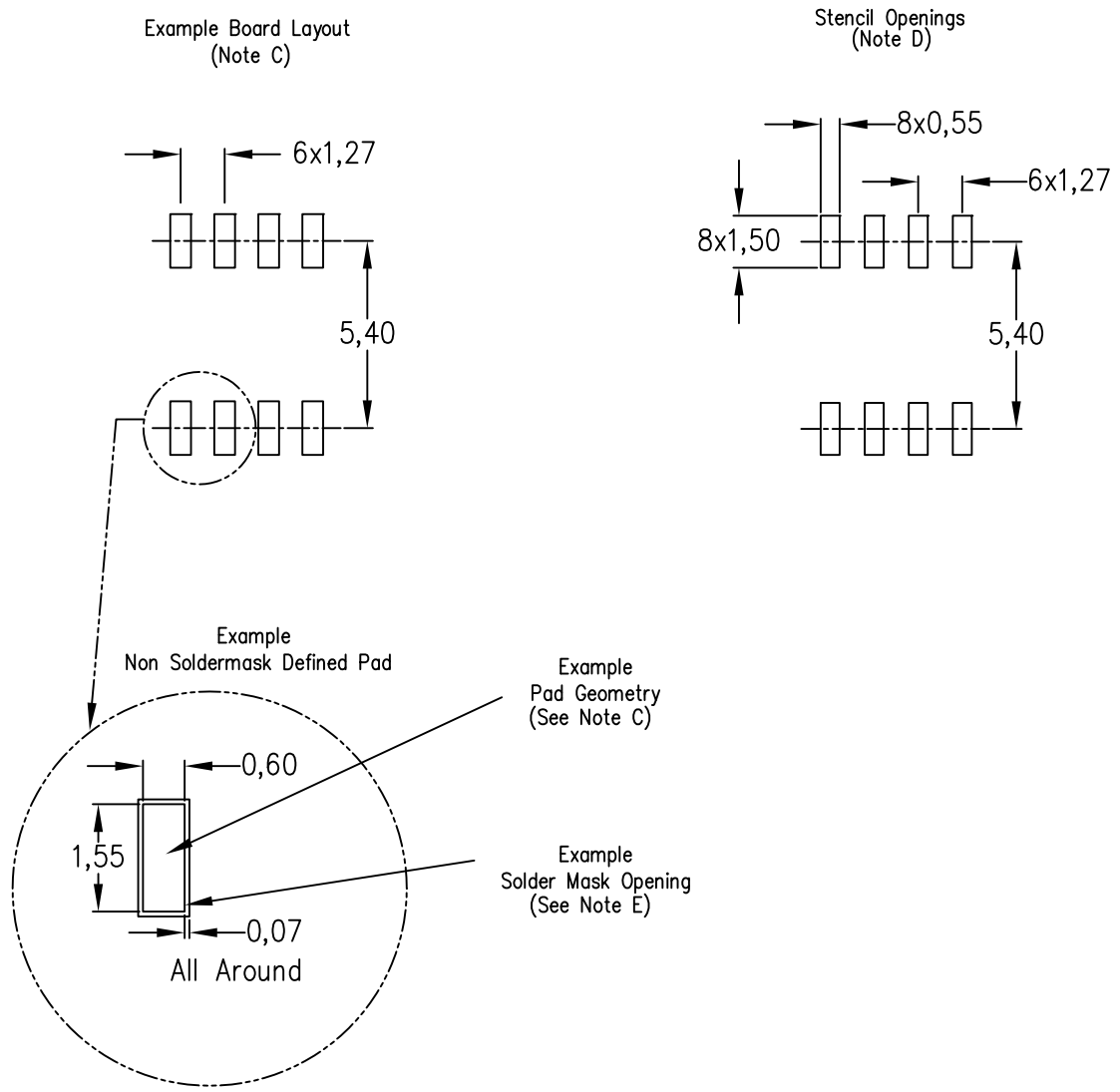
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



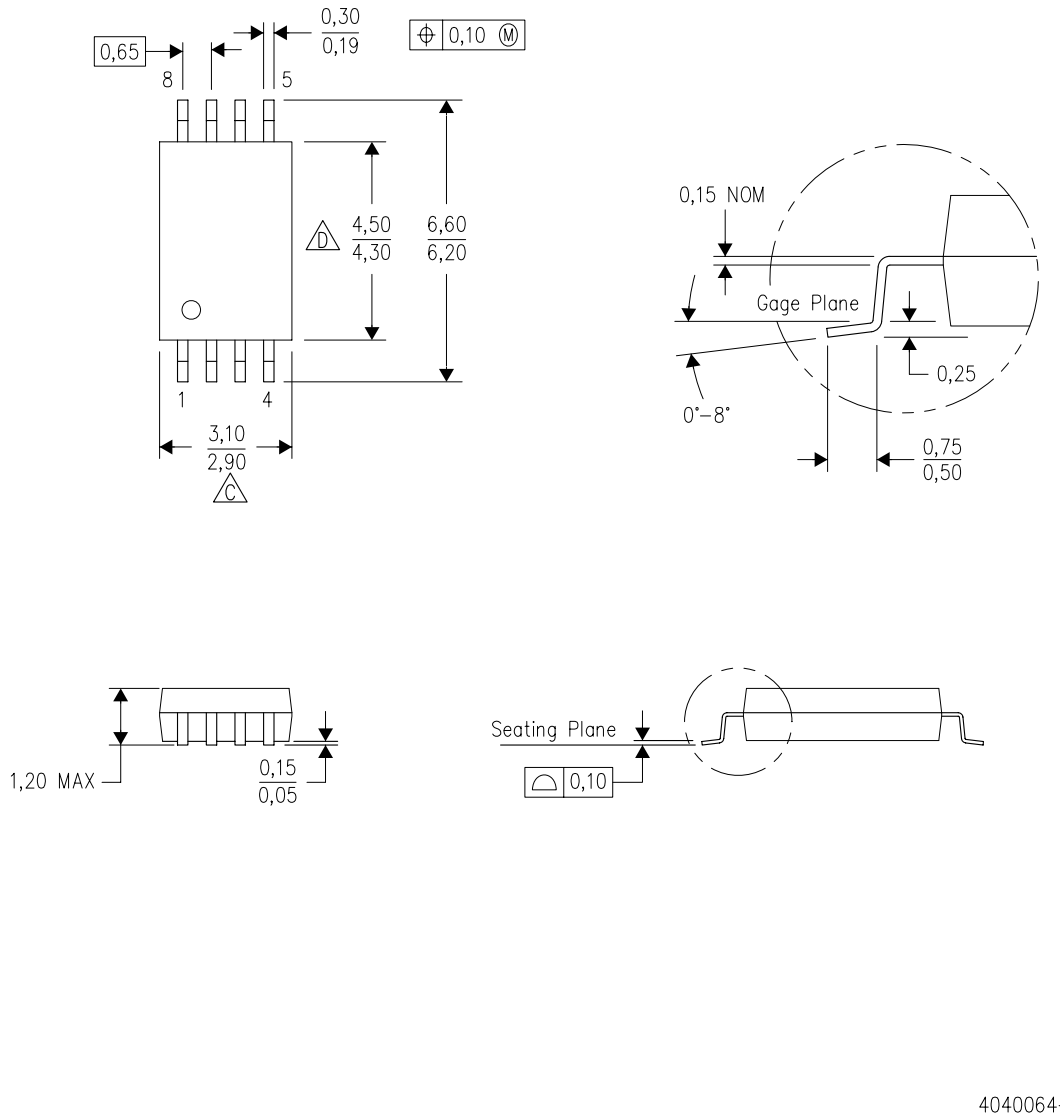
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G8) PLASTIC SMALL OUTLINE



4040064–2/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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