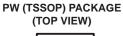
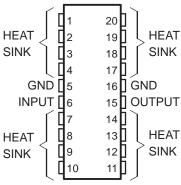
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- Fixed 1.8-V, 2.5-V, and 3.3-V Outputs
- ±1% Maximum Output Voltage Tolerance at T_J = 25°C
- 500-mV Maximum Dropout Voltage at 500 mA (3.3-V Option)





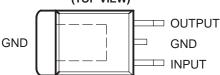
HEAT SINK – These terminals have an internal resistive connection to ground and should be grounded or electrically isolated.

KC (TO-220) PACKAGE (TOP VIEW)



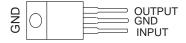
- ±2% Output Voltage Variation Across Load and Temperature
- Internal Overcurrent Limiting
- Internal Thermal-Overload Protection
- Internal Overvoltage Protection

KTP (PowerFLEX™/TO-252*) PACKAGE (TOP VIEW)



*Complies with JEDEC TO-252, variation AC

KCS (TO-220) PACKAGE (TOP VIEW)



description/ordering information

ORDERING INFORMATION

TJ	V _O (NOM)	PACKAGET		ORDERABLE PART NUMBER	TOP-SIDE MARKING
	1.8 V	PowerFLEX™/TO-252* (KTP)	Reel of 3000	TLV2217-18KTPR	2217–18
	1.6 V	TO-220 (KCS)	Tube of 50	TLV2217-18KCS	TLV2217-18
		TO-220 (KC)	Tube of 50	TLV2217-25KC	TLV2217-25
	0.5.1/	PowerFLEX™/TO-252* (KTP)	Reel of 3000	TLV2217-25KTPR	2217–25
0°C to 125°C	2.5 V	TOOOD (DIA))	Tube of 70	TLV2217-25PW	0047.05
		TSSOP (PW)	Reel of 2000	TLV2217-25PWR	2217–25
		PowerFLEX™/TO-252* (KTP)	Reel of 3000	TLV2217-33KTPR	2217–33
	3.3 V	TO-220 (KC)	Tube of 50	TLV2217-33KC	TLV2217-33
		TSSOP (PW)	Reel of 2000	TLV2217-33PWR	2217–33

^{*}Complies to TO-252, variation AC.

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerFLEX is a trademark of Texas Instruments.



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description/ordering information (continued)

The TLV2217 family of low-dropout regulators offers a variety of fixed-voltage options that offer a maximum continuous input voltage of 16 V, making them more versatile than CMOS regulators. Utilizing a pnp pass element, these regulators are capable of sourcing 500 mA of current, with a specified maximum dropout of 500 mV (3.3-V and 2.5-V options), making these regulators ideal for low-voltage applications. Additionally, the TLV2217 regulators offer very tight output accuracy of ±2% across operating load and temperature ranges. Other convenient features the regulators provide are internal overcurrent limiting, thermal-overload protection, and overvoltage protection. The TLV2217 family of regulators is available in fixed voltages of 1.8 V, 2.5 V, and 3.3 V.

absolute maximum ratings over operating virtual junction temperature range (unless otherwise noted)†

Continuous input voltage, V _I	16 V
Operating virtual junction temperature, T _J	150°C
Storage temperature range, T _{eta}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

package thermal data (see Note 1)

PACKAGE	BOARD	θ JP ‡	θJC	θ JA
PowerFLEX™/TO-252 (KTP)	High K, JESD 51-5	1.4°C/W	19°C/W	28°C/W
TO-220 (KC/KCS)	High K, JESD 51-5	3°C/W	17°C/W	19°C/W
TSSOP (PW)	High K, JESD 51-7		32°C/W	83°C/W

[‡] For packages with exposed thermal pads, such as QFN, PowerPAD, and PowerFLEX, 0,1p is defined as the thermal resistance between the die junction and the bottom of the exposed pad.

recommended operating conditions

		MIN	MAX	UNIT
VI	Input voltage	3.0	12	V
IO	Output current	0	500	mA
TJ	Operating virtual junction temperature range	0	125	°C

§ Minimum V_I is equal to 3.0 V or V_O(max) + 0.6 V, whichever is greater.



NOTE 1: Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

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electrical characteristics at V $_{I}$ = 4.5 V, I $_{O}$ = 500 mA, T $_{J}$ = 25 $^{\circ}\text{C}$ (unless otherwise noted)

DADAMETED		TL	UNIT				
PARAMETER		TEST CONDITIONS†					UNII
Output valta va		V 00V4-55V	T _J = 25°C	3.267	3.30	3.333	
Output voltage	$I_{O} = 20 \text{ mA to } 500 \text{ mA},$	V _I = 3.8 V to 5.5 V	$T_J = 0$ °C to 125°C	3.234		3.366	V
Input voltage regulation	V _I = 3.8 V to 5.5 V				5	15	mV
Ripple rejection	f = 120 Hz,	V _{ripple} = 1 V _{PP}	V _I = 4.5 V		-62		dB
Output voltage regulation	I _O = 20 mA to 500 mA				5	30	mV
Output noise voltage	f = 10 Hz to 100 kHz				500		μV
5	I _O = 250 mA					400	.,
Dropout voltage	I _O = 500 mA	O = 500 mA				500	mV
Dies surrent	IO = 0				2	5	A
Bias current	I _O = 500 mA				19	49	mA

[†] Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1- μ F capacitor across the input and a 22- μ F tantalum capacitor, with equivalent series resistance of 1.5 Ω , on the output.

electrical characteristics at $V_I = 3.3 \text{ V}$, $I_O = 500 \text{ mA}$, $T_J = 25^{\circ}\text{C}$ (unless otherwise noted)

2424455		TEGT CONDITIONS						
PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT	
Outrout valta na	l- 00 m 4 to 500 m 4	V 20V4555V	T _J = 25°C	2.475	2.5	2.525		
Output voltage	$I_{O} = 20 \text{ mA to } 500 \text{ mA},$	V _I = 3.0 V to 5.5 V	$T_J = 0$ °C to 125°C	2.45		2.55	٧	
Input voltage regulation	V _I = 3.0 V to 5.5 V				4	12	mV	
Ripple rejection	f = 120 Hz,	V _{ripple} = 1 V _{PP} ,	V _I = 4.5 V		-62		dB	
Output voltage regulation	I _O = 20 mA to 500 mA				4	23	mV	
Output noise voltage	f = 10 Hz to 100 kHz				500		μV	
Danasataallaas	I _O = 250 mA					400	>/	
Dropout voltage	I _O = 500 mA					500	mV	
Dice current	IO = 0				2	5	A	
Bias current	I _O = 500 mA				19	49	mA	

[†] Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1- μ F capacitor across the input and a 22- μ F tantalum capacitor, with equivalent series resistance of 1.5 Ω , on the output.

TLV2217 LOW-DROPOUT FIXED-VOLTAGE REGULATORS

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electrical characteristics at V_I = 3.3 V, I_O = 500 mA, T_J = 25°C (unless otherwise noted)

DADAMETED		TL	UNIT				
PARAMETER		TEST CONDITIONS†					
Outrotudiana		V 00V4-55V	T _J = 25°C	1.782	1.8	1.818	.,
Output voltage	$I_O = 20 \text{ mA to } 500 \text{ mA}, \qquad V_I = 3.0 \text{ V to } 5.5 \text{ V}$		$T_J = 0$ °C to 125°C	1.764		1.836	V
Input voltage regulation	V _I = 3.0 V to 5.5 V				3	9	mV
Ripple rejection	f = 120 Hz,	V _{ripple} = 1 V _{PP} ,	V _I = 4.5 V		-62		dB
Output voltage regulation	$I_O = 20 \text{ mA to } 500 \text{ mA}$				3	17	mV
Output noise voltage	f = 10 Hz to 100 kHz				500		μV
Day and a start and	I _O = 250 mA				‡		>/
Dropout voltage	I _O = 500 mA	O = 500 mA					mV
Bias current	IO = 0) = 0			2	5	m 1
Dias current	I _O = 500 mA				19	49	mA

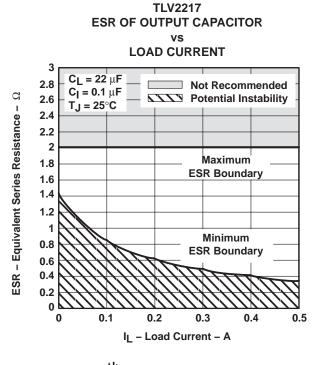
[†] Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1- μ F capacitor across the input and a 22- μ F tantalum capacitor, with equivalent series resistance of 1.5 Ω , on the output.

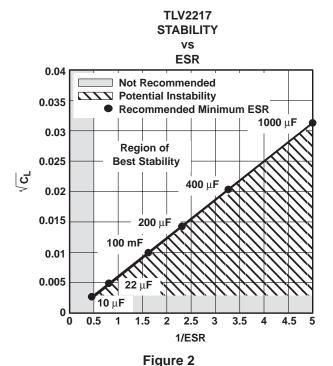


 $[\]mbox{\ensuremath{\ddagger}}$ Dropout voltage is limited by the input voltage range, with minimum VI = 3.0 V.

COMPENSATION-CAPACITOR SELECTION INFORMATION

The TLV2217 is a low-dropout regulator. This means that the capacitance loading is important to the performance of the regulator because it is a vital part of the control loop. The capacitor value and the equivalent series resistance (ESR) both affect the control loop and must be defined for the load range and the temperature range. Figures 1 and 2 can be used to establish the capacitance value and ESR range for the best regulator performance.





 $\Delta V_L = ESR \times \Delta I_L$

Applied Load Current Load Voltage

Figure 1

typical application schematic

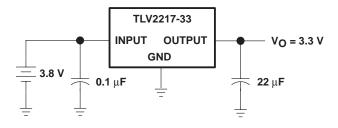
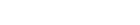


Figure 3





18-Mar-2008





PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TLV2217-18KCS	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type
TLV2217-18KCSE3	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type
TLV2217-18KTPR	OBSOLETE	PFM	KTP	2		TBD	Call TI	Call TI
TLV2217-18KTPRG3	OBSOLETE	PFM	KTP	2		TBD	Call TI	Call TI
TLV2217-18KVURG3	ACTIVE	PFM	KVU	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR
TLV2217-25KC	OBSOLETE	TO-220	KC	3		TBD	Call TI	Call TI
TLV2217-25KCE3	OBSOLETE	TO-220	KC	3		TBD	Call TI	Call TI
TLV2217-25KCSE3	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type
TLV2217-25KTPR	OBSOLETE	PFM	KTP	2		TBD	Call TI	Call TI
TLV2217-25KTPRG3	OBSOLETE	PFM	KTP	2		TBD	Call TI	Call TI
TLV2217-25KVURG3	ACTIVE	PFM	KVU	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR
TLV2217-25PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPD	Level-1-260C-UNLIM
TLV2217-25PWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPD	Level-1-260C-UNLIM
TLV2217-25PWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPD	Level-1-260C-UNLIM
TLV2217-25PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPD	Level-1-260C-UNLIM
TLV2217-25PWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPD	Level-1-260C-UNLIM
TLV2217-25PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPD	Level-1-260C-UNLIM
TLV2217-33KC	OBSOLETE	TO-220	KC	3		TBD	Call TI	Call TI
TLV2217-33KCE3	OBSOLETE	TO-220	KC	3		TBD	Call TI	Call TI
TLV2217-33KCSE3	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type
TLV2217-33KTPR	OBSOLETE	PFM	KTP	2		TBD	Call TI	Call TI
TLV2217-33KTPRG3	OBSOLETE	PFM	KTP	2		TBD	Call TI	Call TI
TLV2217-33KVURG3	ACTIVE	PFM	KVU	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR
TLV2217-33PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPD	Level-1-260C-UNLIM
TLV2217-33PWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPD	Level-1-260C-UNLIM
TLV2217-33PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPD	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows: **ACTIVE:** Product device recommended for new designs. **LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.



PACKAGE OPTION ADDENDUM

18-Mar-2008

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

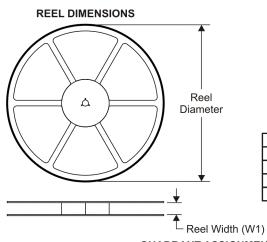
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

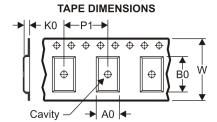
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TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2217-18KVURG3	PFM	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TLV2217-25KVURG3	PFM	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TLV2217-25PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TLV2217-33KVURG3	PFM	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TLV2217-33PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1





*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2217-18KVURG3	PFM	KVU	3	2500	340.0	340.0	38.0
TLV2217-25KVURG3	PFM	KVU	3	2500	340.0	340.0	38.0
TLV2217-25PWR	TSSOP	PW	20	2000	346.0	346.0	33.0
TLV2217-33KVURG3	PFM	KVU	3	2500	340.0	340.0	38.0
TLV2217-33PWR	TSSOP	PW	20	2000	346.0	346.0	33.0

PW (R-PDSO-G**)

14 PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

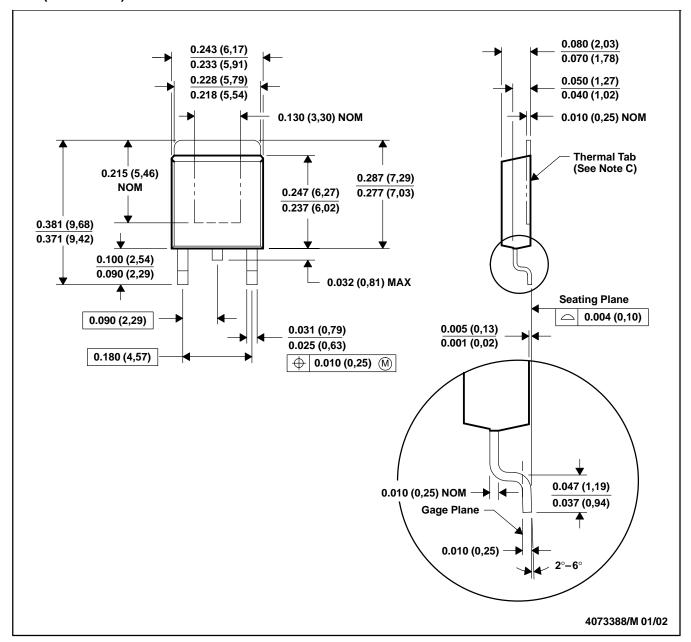
B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

KTP (R-PSFM-G2)

PowerFLEX™ PLASTIC FLANGE-MOUNT PACKAGE



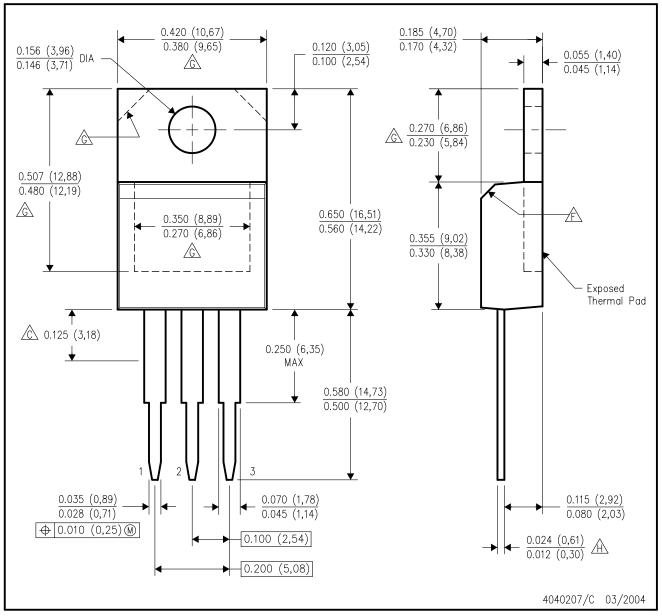
- NOTES: A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. The center lead is in electrical contact with the thermal tab.
 - D. Dimensions do not include mold protrusions, not to exceed 0.006 (0,15).
 - E. Falls within JEDEC TO-252 variation AC.

PowerFLEX is a trademark of Texas Instruments.



KC (R-PSFM-T3)

PLASTIC FLANGE-MOUNT PACKAGE



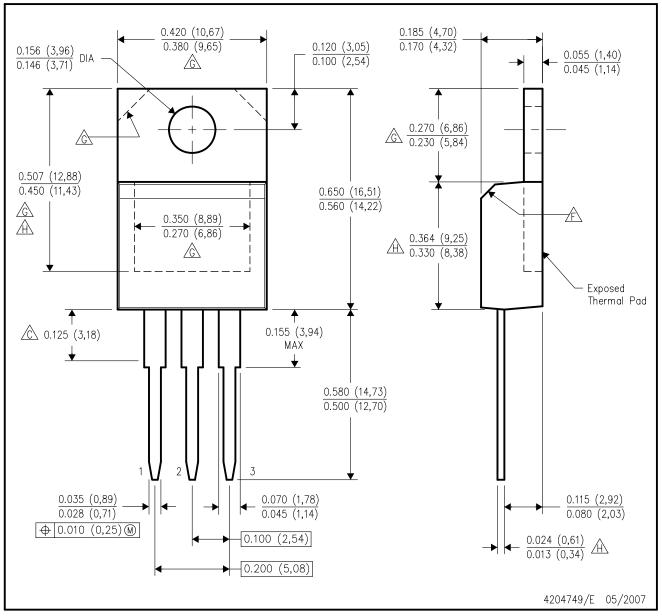
NOTES:

- A. All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- Lead dimensions are not controlled within this area.
- D. All lead dimensions apply before solder dip.
- E. The center lead is in electrical contact with the mounting tab.
- The chamfer is optional.
- Thermal pad contour optional within these dimensions.
- Falls within JEDEC TO-220 variation AB, except minimum lead thickness.



KCS (R-PSFM-T3)

PLASTIC FLANGE-MOUNT PACKAGE



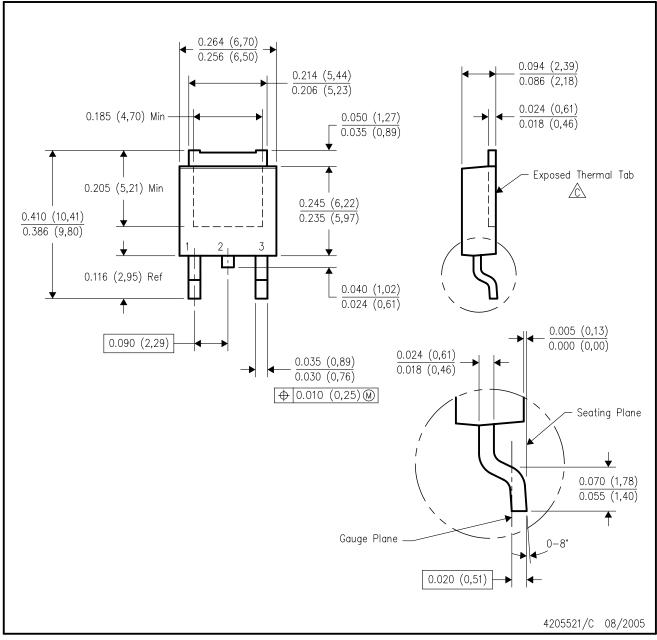
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Lead dimensions are not controlled within this area.
- D. All lead dimensions apply before solder dip.
- E. The center lead is in electrical contact with the mounting tab.
- The chamfer is optional.
- Thermal pad contour optional within these dimensions.
- Falls within JEDEC T0—220 variation AB, except minimum lead thickness, minimum exposed pad length, and maximum body length.



KVU (R-PSFM-G3)

PLASTIC FLANGE-MOUNT PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- The center lead is in electrical contact with the exposed thermal tab.
- D. Body Dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.006 (0,15) per side.
- E. Falls within JEDEC TO-252 variation AA.



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