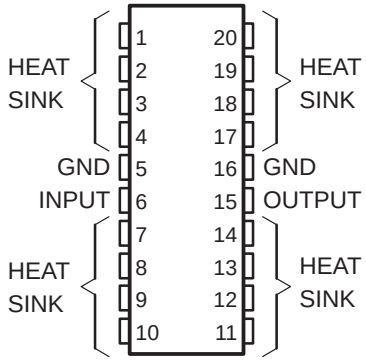
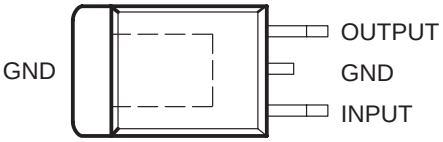
- **Fixed 1.8-V, 2.5-V, and 3.3-V Outputs**
- **±1% Maximum Output Voltage Tolerance at T_J = 25°C**
- **500-mV Maximum Dropout Voltage at 500 mA (3.3-V Option)**
- **±2% Output Voltage Variation Across Load and Temperature**
- **Internal Overcurrent Limiting**
- **Internal Thermal-Overload Protection**
- **Internal Overvoltage Protection**

PW (TSSOP) PACKAGE
(TOP VIEW)



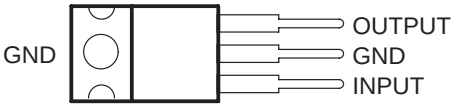
HEAT SINK − These terminals have an internal resistive connection to ground and should be grounded or electrically isolated.

KTP (PowerFLEX™/TO-252*) PACKAGE
(TOP VIEW)

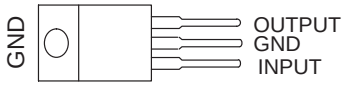


*Complies with JEDEC TO-252, variation AC

KC (TO-220) PACKAGE
(TOP VIEW)



KCS (TO-220) PACKAGE
(TOP VIEW)



description/ordering information

ORDERING INFORMATION

T_J	V_O (NOM)	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 125°C	1.8 V	PowerFLEX™/TO-252* (KTP)	Reel of 3000	TLV2217-18KTPR	2217−18
		TO-220 (KCS)	Tube of 50	TLV2217-18KCS	TLV2217−18
	2.5 V	TO-220 (KC)	Tube of 50	TLV2217-25KC	TLV2217−25
		PowerFLEX™/TO-252* (KTP)	Reel of 3000	TLV2217-25KTPR	2217−25
		TSSOP (PW)	Tube of 70	TLV2217-25PW	2217−25
			Reel of 2000	TLV2217-25PWR	
	3.3 V	PowerFLEX™/TO-252* (KTP)	Reel of 3000	TLV2217-33KTPR	2217−33
		TO-220 (KC)	Tube of 50	TLV2217-33KC	TLV2217−33
		TSSOP (PW)	Reel of 2000	TLV2217-33PWR	2217−33

*Complies to TO-252, variation AC.
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

description/ordering information (continued)

The TLV2217 family of low-dropout regulators offers a variety of fixed-voltage options that offer a maximum continuous input voltage of 16 V, making them more versatile than CMOS regulators. Utilizing a pnp pass element, these regulators are capable of sourcing 500 mA of current, with a specified maximum dropout of 500 mV (3.3-V and 2.5-V options), making these regulators ideal for low-voltage applications. Additionally, the TLV2217 regulators offer very tight output accuracy of ±2% across operating load and temperature ranges. Other convenient features the regulators provide are internal overcurrent limiting, thermal-overload protection, and overvoltage protection. The TLV2217 family of regulators is available in fixed voltages of 1.8 V, 2.5 V, and 3.3 V.

absolute maximum ratings over operating virtual junction temperature range (unless otherwise noted)†

Continuous input voltage, V_I . . . . . 16 V
Operating virtual junction temperature, T_J . . . . . 150°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

package thermal data (see Note 1)

PACKAGE	BOARD	θ_{JP}*	θ_{JC}	θ_{JA}
PowerFLEX™/TO-252 (KTP)	High K, JESD 51-5	3°C/W		28°C/W
TO-220 (KC/KCS)	High K, JESD 51-5	3°C/W		19°C/W
TSSOP (PW)	High K, JESD 51-7		32°C/W	83°C/W

*For packages with exposed thermal pads, such as QFN, PowerPAD, and PowerFLEX, θ_{JP} is defined as the thermal resistance between the die junction and the bottom of the exposed pad.

NOTE 1: Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

recommended operating conditions

		MIN	MAX	UNIT
V_I	Input voltage	3.0	12	V
I_O	Output current	0	500	mA
T_J	Operating virtual junction temperature range	0	125	°C

‡ Minimum V_I is equal to 3.0 V or $V_O(max)$ + 0.6 V, whichever is greater.

electrical characteristics at V_I = 4.5 V, I_O = 500 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		TLV2217-33			UNIT
			MIN	TYP	MAX	
Output voltage	I_O = 20 mA to 500 mA, V_I = 3.8 V to 5.5 V	T_J = 25°C	3.267	3.30	3.333	V
		T_J = 0°C to 125°C	3.234		3.366	
Input voltage regulation	V_I = 3.8 V to 5.5 V			5	15	mV
Ripple rejection	f = 120 Hz, V_{ripple} = 1 V_{PP}	V_I = 4.5 V		−62		dB
Output voltage regulation	I_O = 20 mA to 500 mA			5	30	mV
Output noise voltage	f = 10 Hz to 100 kHz			500		μV
Dropout voltage	I_O = 250 mA				400	mV
	I_O = 500 mA				500	
Bias current	I_O = 0			2	5	mA
	I_O = 500 mA			19	49	

† Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 22-μF tantalum capacitor, with equivalent series resistance of 1.5 Ω, on the output.

electrical characteristics at V_I = 3.3 V, I_O = 500 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		TLV2217-25			UNIT
			MIN	TYP	MAX	
Output voltage	I_O = 20 mA to 500 mA, V_I = 3.0 V to 5.5 V	T_J = 25°C	2.475	2.5	2.525	V
		T_J = 0°C to 125°C	2.45		2.55	
Input voltage regulation	V_I = 3.0 V to 5.5 V			4	12	mV
Ripple rejection	f = 120 Hz, V_{ripple} = 1 V_{PP},	V_I = 4.5 V		−62		dB
Output voltage regulation	I_O = 20 mA to 500 mA			4	23	mV
Output noise voltage	f = 10 Hz to 100 kHz			500		μV
Dropout voltage	I_O = 250 mA				400	mV
	I_O = 500 mA				500	
Bias current	I_O = 0			2	5	mA
	I_O = 500 mA			19	49	

† Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 22-μF tantalum capacitor, with equivalent series resistance of 1.5 Ω, on the output.

electrical characteristics at V_I = 3.3 V, I_O = 500 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		TLV2217-18			UNIT
			MIN	TYP	MAX	
Output voltage	I_O = 20 mA to 500 mA, V_I = 3.0 V to 5.5 V	T_J = 25°C	1.782	1.8	1.818	V
		T_J = 0°C to 125°C	1.764		1.836	
Input voltage regulation	V_I = 3.0 V to 5.5 V			3	9	mV
Ripple rejection	f = 120 Hz, V_{ripple} = 1 V_{PP}, V_I = 4.5 V			−62		dB
Output voltage regulation	I_O = 20 mA to 500 mA			3	17	mV
Output noise voltage	f = 10 Hz to 100 kHz			500		μV
Dropout voltage	I_O = 250 mA			‡		mV
	I_O = 500 mA			‡		
Bias current	I_O = 0			2	5	mA
	I_O = 500 mA			19	49	

† Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 22-μF tantalum capacitor, with equivalent series resistance of 1.5 Ω, on the output.

‡ Dropout voltage is limited by the input voltage range, with minimum V_I = 3.0 V.

COMPENSATION-CAPACITOR SELECTION INFORMATION

The TLV2217 is a low-dropout regulator. This means that the capacitance loading is important to the performance of the regulator because it is a vital part of the control loop. The capacitor value and the equivalent series resistance (ESR) both affect the control loop and must be defined for the load range and the temperature range. Figures 1 and 2 can be used to establish the capacitance value and ESR range for the best regulator performance.

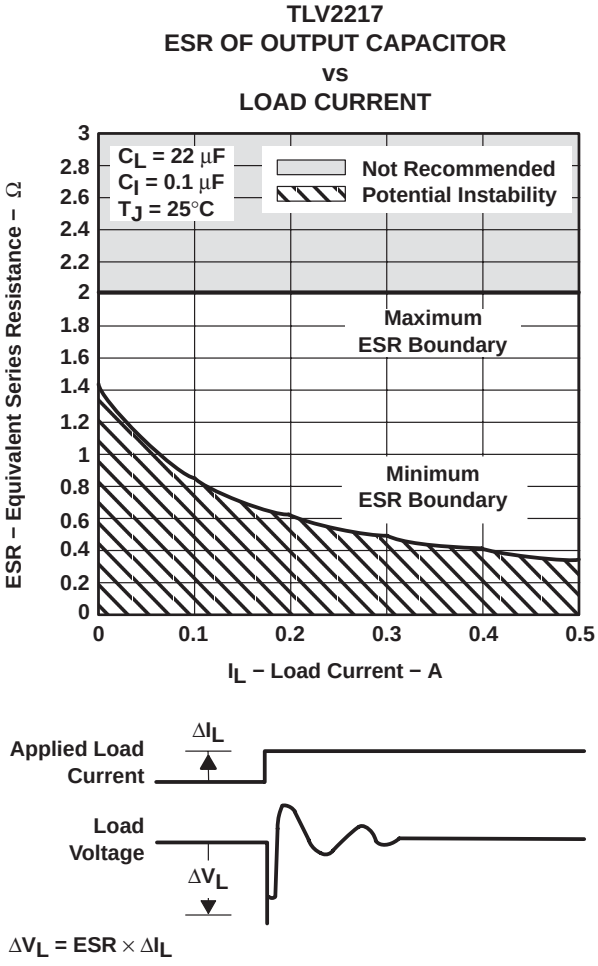


Figure 1

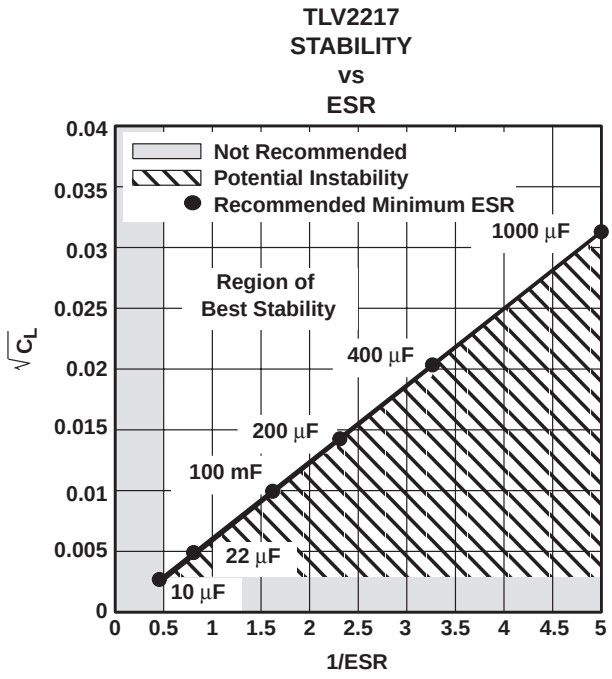


Figure 2

typical application schematic

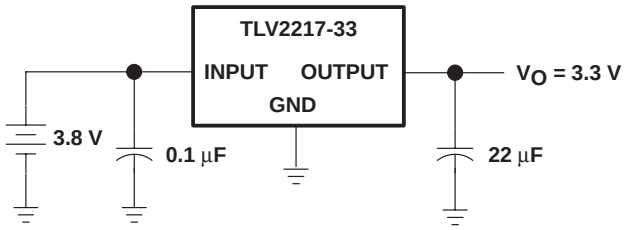
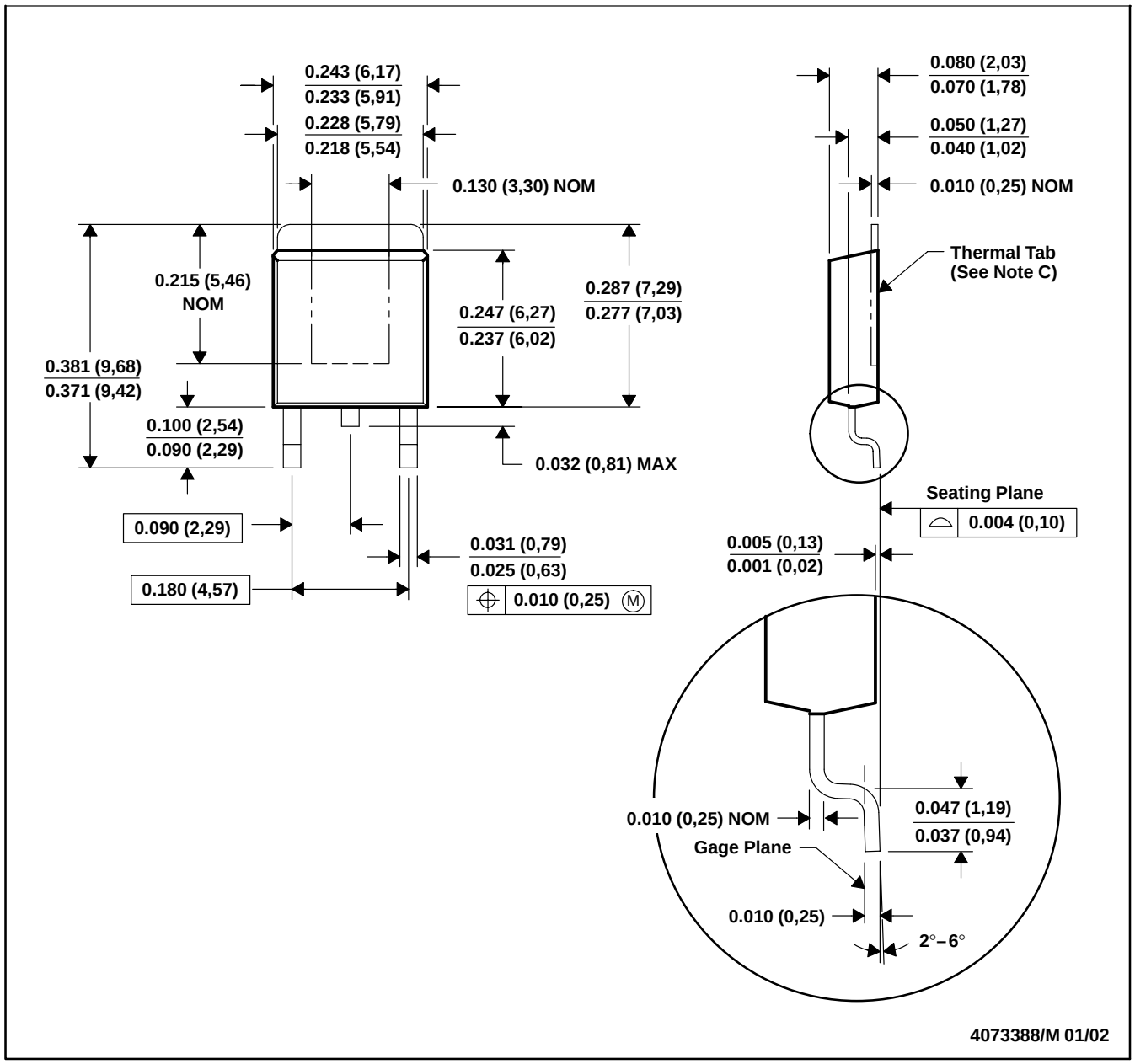


Figure 3

MPSF001F – JANUARY 1996 – REVISED JANUARY 2002

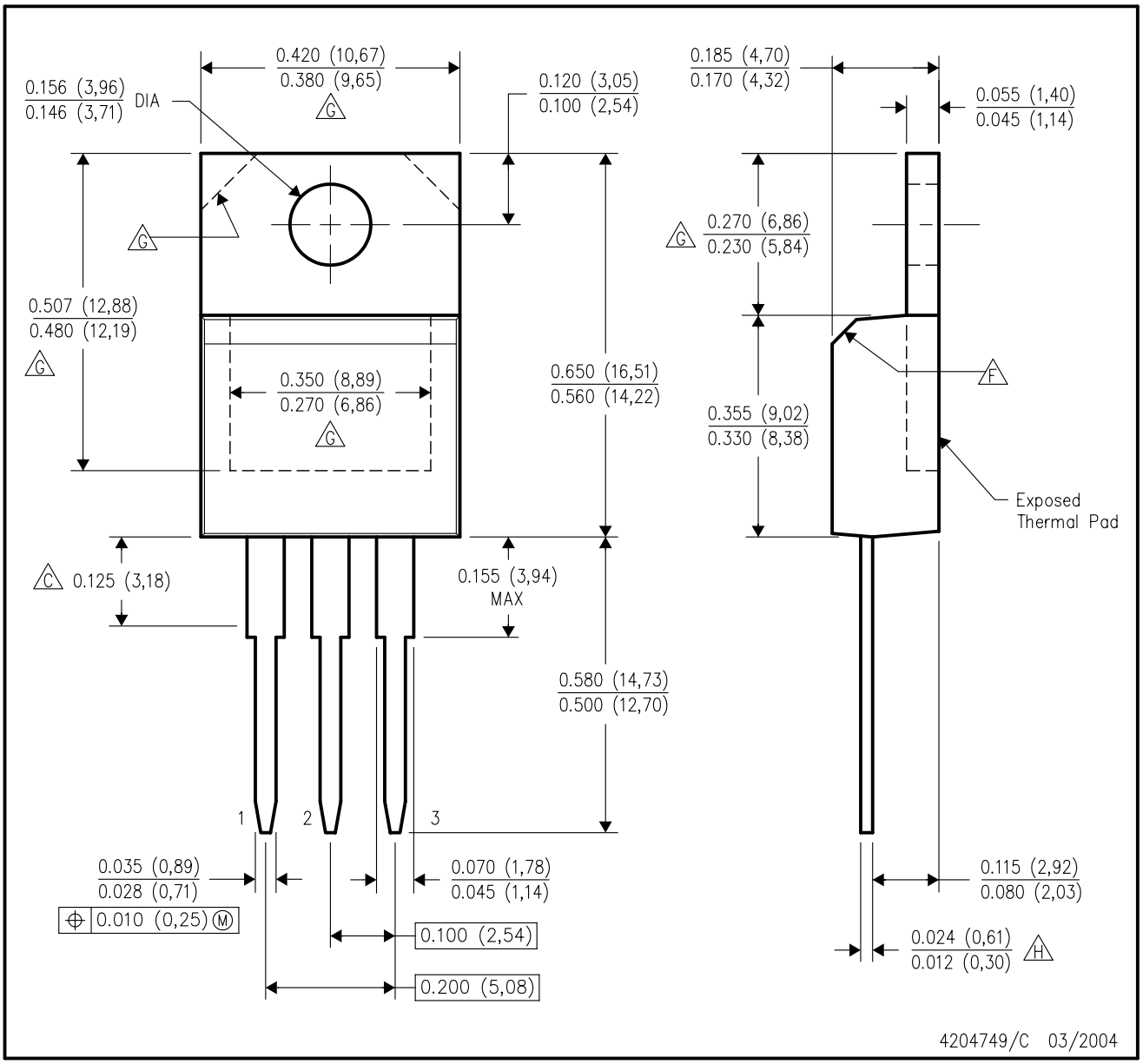
KTP (R-PSFM-G2) **PowerFLEX™ PLASTIC FLANGE-MOUNT PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the thermal tab.
D. Dimensions do not include mold protrusions, not to exceed 0.006 (0,15).
E. Falls within JEDEC TO-252 variation AC.

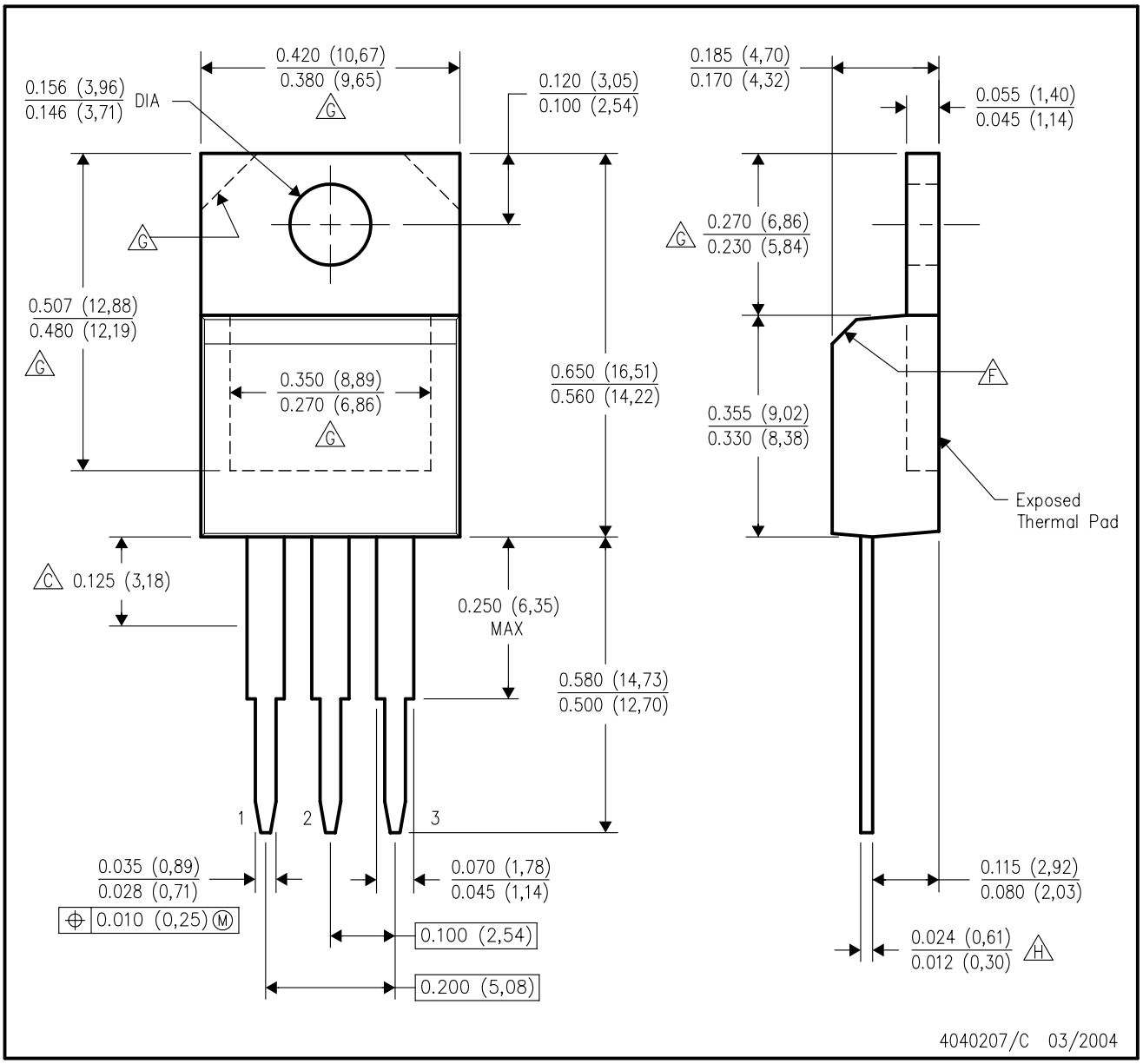
PowerFLEX is a trademark of Texas Instruments.

KCS (R–PSFM–T3) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Lead dimensions are not controlled within this area.
D. All lead dimensions apply before solder dip.
E. The center lead is in electrical contact with the mounting tab.
F. The chamfer is optional.
G. Thermal pad contour optional within these dimensions.
H. Falls within JEDEC TO–220 variation AB, except minimum lead thickness.

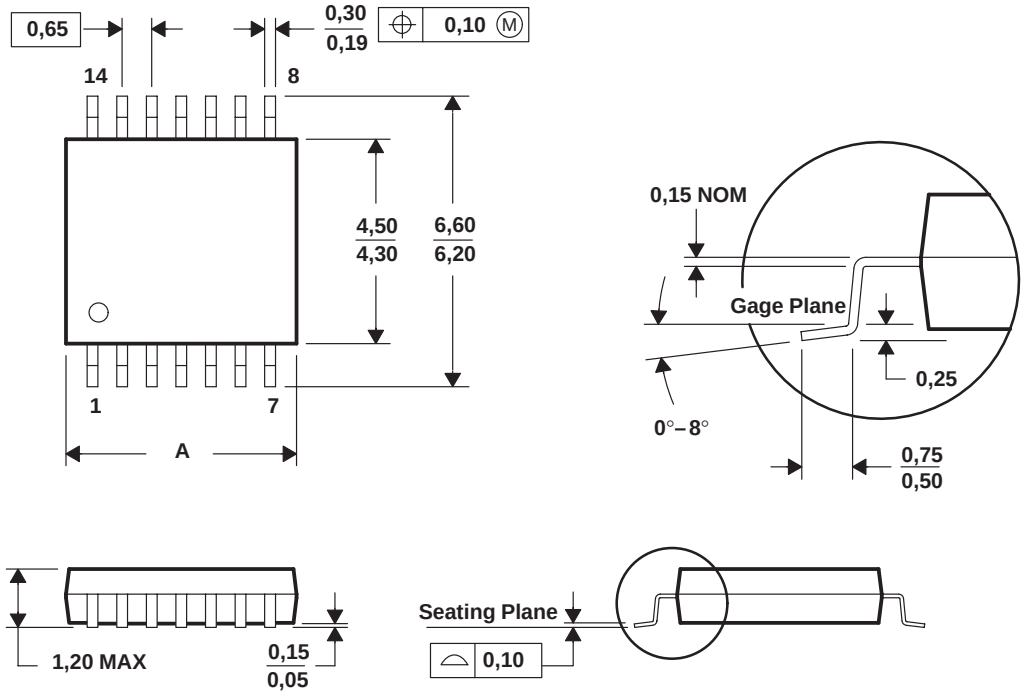
KC (R–PSFM–T3) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Lead dimensions are not controlled within this area.
- D. All lead dimensions apply before solder dip.
- E. The center lead is in electrical contact with the mounting tab.
- F. The chamfer is optional.
- G. Thermal pad contour optional within these dimensions.
- H. Falls within JEDEC TO–220 variation AB, except minimum lead thickness.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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