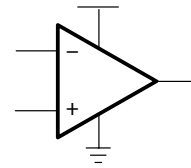


# TLV2760, TLV2761, TLV2762, TLV2763, TLV2764, TLV2765 FAMILY OF 1.8 V MICROPOWER RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

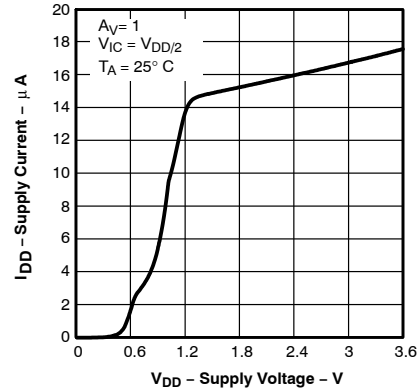
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- Low Supply Voltage . . . 1.8 V to 3.6 V
- Very Low Supply Current . . . 20  $\mu$ A (per channel)
- Ultralow Power Shut-Down Mode
  - $I_{DD}(SHDN) = 10$  nA/Channel
- CMOS Rail-to-Rail Input/Output
- Input Common-Mode Voltage Range . . .  $-0.2$  V to  $V_{DD} + 0.2$  V
- Input Offset Voltage . . . 550  $\mu$ V
- Wide Bandwidth . . . 500 kHz
- Slew Rate . . . 0.20 V/ $\mu$ s
- Specified Temperature Range:
  - 0°C to 70°C . . . Commercial Grade
  - 40°C to 85°C . . . Industrial Grade
- Ultrasmall Packaging
  - 5 or 6 Pin SOT-23 (TLV2760/1)
  - 8 or 10 Pin MSOP (TLV2762/3)
- Universal Op-Amp EVM

Operational Amplifier



SUPPLY CURRENT  
vs  
SUPPLY VOLTAGE



## description

The TLV276x single supply operational amplifiers provide 500 kHz bandwidth from only 20  $\mu$ A while operating down to 1.8 V over the industrial temperature range. The maximum recommended supply voltage is 3.6 V, which allows the devices to be operated from ( $\pm 1.8$  V supplies down to  $\pm 0.9$  V) two AA or AAA cells. The devices have been characterized at 1.8 V (end of life of 2 AA(A) cells) and at 2.4 V (nominal voltage of 2 NiCd/NiMH cells). The TLV276x have rail-to-rail input and output capability which is a necessity at 1.8 V.

The low supply current is coupled with extremely low input bias currents enabling them to be used with mega-ohm resistors. Low shutdown current of only 10 nA make these devices ideal for low frequency measurement applications desiring long active battery life.

All members are available in PDIP and SOIC with the singles in the small SOT-23 package, duals in the MSOP, and quads in the TSSOP package.

SELECTION OF SINGLE SUPPLY AMPLIFIER PRODUCTS

| DEVICE     | $V_{DD}$<br>(V) | $V_{IO}$<br>( $\mu$ V) | $I_{DD}/Ch$<br>( $\mu$ A) | $I_{IB}$<br>(pA) | GBW<br>(MHz) | SR<br>(V/ $\mu$ s) | $V_n$ , 1kHz<br>(nV/ $\sqrt{Hz}$ ) | $I_O$<br>(mA) | SHUT-<br>DOWN | RAIL-TO-<br>RAIL |
|------------|-----------------|------------------------|---------------------------|------------------|--------------|--------------------|------------------------------------|---------------|---------------|------------------|
| TLV224x    | 2.5 – 12        | 600                    | 1                         | 100              | 0.0055       | 0.002              | NA                                 | 0.2           | —             | I/O              |
| TLV2211    | 2.7 – 10        | 450                    | 13                        | 1                | 0.065        | 0.025              | 21                                 | 0.4           | —             | O                |
| TLV276x    | 1.8 – 3.6       | 550                    | 20                        | 3                | 0.5          | 0.23               | 95                                 | 5             | Y             | I/O              |
| TLV245x(A) | 2.7 – 6         | 20                     | 23                        | 500              | 0.22         | 0.11               | 49                                 | 2.5           | Y             | I/O              |
| TLV246x(A) | 2.7 – 6         | 150                    | 550                       | 1300             | 6.4          | 1.6                | 11                                 | 25            | Y             | I/O              |
| TLV278x(A) | 1.8 – 3.6       | 250                    | 650                       | 2.5              | 8            | 5                  | 18                                 | 10            | Y             | I/O              |



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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# TLV2760, TLV2761, TLV2762, TLV2763, TLV2764, TLV2765

## FAMILY OF 1.8 V MICROPOWER RAIL-TO-RAIL INPUT/OUTPUT

### OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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#### TLV2760 and TLV2761 AVAILABLE OPTIONS<sup>(1)</sup>

| T <sub>A</sub> | V <sub>IOmax</sub><br>AT 25°C | PACKAGED DEVICES                  |                            |              |                        |
|----------------|-------------------------------|-----------------------------------|----------------------------|--------------|------------------------|
|                |                               | SMALL OUTLINE<br>(D) <sup>†</sup> | SOT-23                     |              | PLASTIC DIP<br>(P)     |
|                |                               |                                   | (DBV) <sup>‡</sup>         | SYMBOL       |                        |
| 0°C to 70°C    | 3500 µV                       | TLV2760CD<br>TLV2761CD            | —<br>—                     | —<br>—       | —<br>—                 |
| –40°C to 85°C  | 3500 µV                       | TLV2760ID<br>TLV2761ID            | TLV2760IDBV<br>TLV2761IDBV | VANI<br>VAXI | TLV2760IP<br>TLV2761IP |

<sup>†</sup> This package is available taped and reeled. To order this packaging option, add an **R** suffix to the part number (e.g., TLV2760CDR).

<sup>‡</sup> This package is only available taped and reeled. For standard quantities (3,000 pieces per reel), add an **R** suffix (i.e., TLV2760CDBVR). For smaller quantities (250 pieces per mini-reel), add a **T** suffix to the part number (e.g., TLV2760CDBVT).

#### TLV2762 and TLV2763 AVAILABLE OPTIONS<sup>(1)</sup>

| T <sub>A</sub> | V <sub>IO</sub> max<br>AT 25°C | PACKAGED DEVICES                     |                  |              |                  |              |                       |                       |
|----------------|--------------------------------|--------------------------------------|------------------|--------------|------------------|--------------|-----------------------|-----------------------|
|                |                                | SMALL<br>OUTLINE<br>(D) <sup>†</sup> | MSOP             |              |                  |              | PLASTIC<br>DIP<br>(N) | PLASTIC<br>DIP<br>(P) |
|                |                                |                                      | DGK <sup>†</sup> | SYMBOL       | DGS <sup>†</sup> | SYMBOL       |                       |                       |
| 0°C to 70°C    | 3500 μV                        | TLV2762CD<br>TLV2763CD               | —<br>TLV2762CDGK | —<br>AJO     | —<br>—           | —<br>—       | —<br>—                | —<br>—                |
| –40°C to 85°C  | 3500 μV                        | TLV2762ID<br>TLV2763ID               | TLV2762IDGK<br>— | xxTIAJP<br>— | —<br>TLV2763IDGS | —<br>xxTIAJR | —<br>TLV2763IN        | TLV2762IP<br>—        |

<sup>†</sup> This package is available taped and reeled. To order this packaging option, add an **R** suffix to the part number (e.g., TLV2762CDR).

#### TLV2764 and TLV2765 AVAILABLE OPTIONS<sup>(1)</sup>

| T <sub>A</sub> | V <sub>IOmax</sub><br>AT 25°C | PACKAGED DEVICES                  |                        |                            |
|----------------|-------------------------------|-----------------------------------|------------------------|----------------------------|
|                |                               | SMALL OUTLINE<br>(D) <sup>†</sup> | PLASTIC DIP<br>(N)     | TSSOP<br>(PW) <sup>†</sup> |
| 0°C to 70°C    | 3500 µV                       | TLV2764CD<br>TLV2765CD            | —<br>—                 | —<br>—                     |
| –40°C to 85°C  | 3500 µV                       | TLV2764ID<br>TLV2765ID            | TLV2764IN<br>TLV2765IN | TLV2764IPW<br>TLV2765IPW   |

<sup>†</sup> This package is available taped and reeled. To order this packaging option, add an **R** suffix to the part number (e.g., TLV2764CDR).

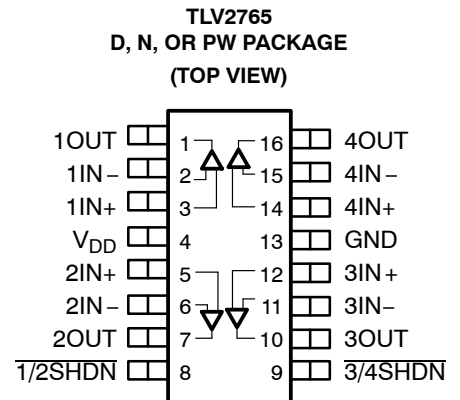
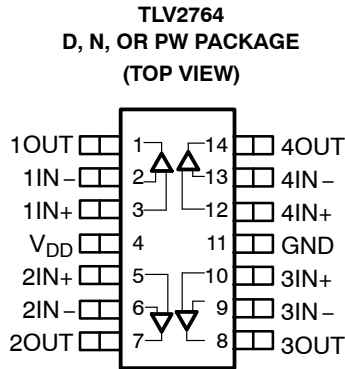
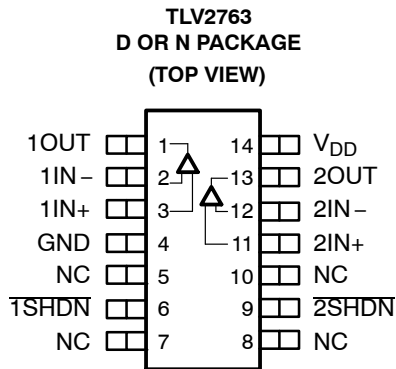
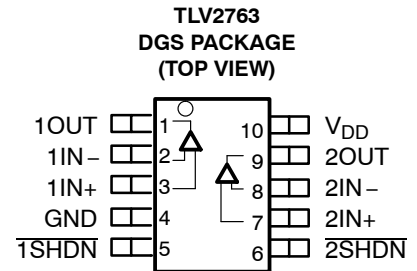
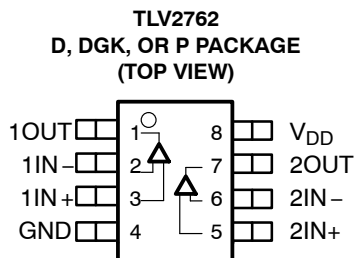
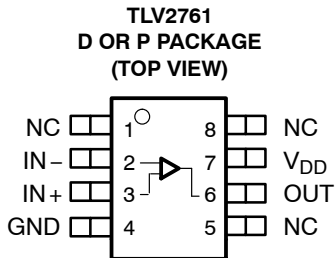
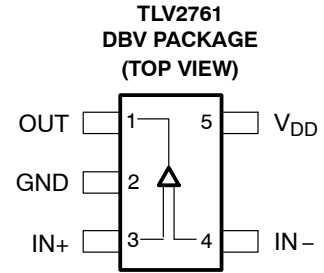
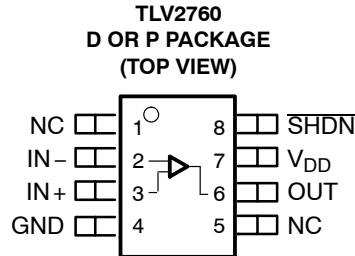
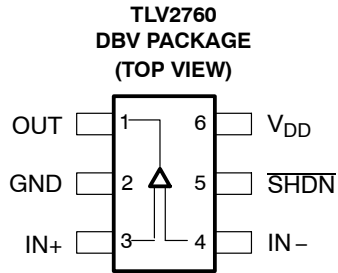
- For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).



# TLV2760, TLV2761, TLV2762, TLV2763, TLV2764, TLV2765 FAMILY OF 1.8 V MICROPOWER RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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## TLV276x PACKAGE PINOUTS



NC – No internal connection

# TLV2760, TLV2761, TLV2762, TLV2763, TLV2764, TLV2765

## FAMILY OF 1.8 V MICROPOWER RAIL-TO-RAIL INPUT/OUTPUT

### OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|                                                              |                              |
|--------------------------------------------------------------|------------------------------|
| Supply voltage, $V_{DD}$ (see Note 1)                        | 4 V                          |
| Differential input voltage range, $V_{ID}$                   | $\pm V_{DD}$                 |
| Input current range, $I_I$                                   | $\pm 10$ mA                  |
| Output current range, $I_O$                                  | $\pm 10$ mA                  |
| Continuous total power dissipation                           | See Dissipation Rating Table |
| Operating free-air temperature range, $T_A$ : C-suffix       | 0°C to 70°C                  |
| I-suffix                                                     | –40°C to 85°C                |
| Maximum junction temperature, $T_J$                          | 150°C                        |
| Storage temperature range, $T_{stg}$                         | –65°C to 150°C               |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C                        |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential voltages, are with respect to GND

DISSIPATION RATING TABLE

| PACKAGE   | $\Theta_{JC}$<br>(°C/W) | $\Theta_{JA}$<br>(°C/W) | $T_A \leq 25^\circ\text{C}$<br>POWER RATING | $T_A = 85^\circ\text{C}$<br>POWER RATING |
|-----------|-------------------------|-------------------------|---------------------------------------------|------------------------------------------|
| D (8)     | 38.3                    | 176                     | 710 mW                                      | 369 mW                                   |
| D (14)    | 26.9                    | 122                     | 1022 mW                                     | 531 mW                                   |
| D (16)    | 25.7                    | 114                     | 1090 mW                                     | 567 mW                                   |
| DBV (5)   | 55                      | 324                     | 385 mW                                      | 201 mW                                   |
| DBV (6)   | 55                      | 294                     | 425 mW                                      | 221 mW                                   |
| DGK(8)    | 54.2                    | 260                     | 481 mW                                      | 250 mW                                   |
| DGS(10)   | 54.1                    | 258                     | 485 mW                                      | 252 mW                                   |
| N (14,16) | 32                      | 78                      | 1600 mW                                     | 833 mW                                   |
| P         | 41                      | 104                     | 1200 mW                                     | 625 mW                                   |
| PW (14)   | 29.3                    | 174                     | 720 mW                                      | 374 mW                                   |
| PW (16)   | 28.7                    | 161                     | 774 mW                                      | 403 mW                                   |

#### recommended operating conditions

|                                                   |                 |                                | MIN                  | MAX                  | UNIT |
|---------------------------------------------------|-----------------|--------------------------------|----------------------|----------------------|------|
| Supply voltage, V <sub>DD</sub>                   | Single supply   |                                | 1.8                  | 3.6                  | V    |
|                                                   | Split supply    |                                | ±0.8                 | ±1.8                 |      |
| Common-mode input voltage range, V <sub>ICR</sub> |                 |                                | −0.2                 | V <sub>DD</sub> +0.2 | V    |
| Operating free-air temperature, T <sub>A</sub>    | C-suffix        |                                | 0                    | 70                   | °C   |
|                                                   | I-suffix        |                                | −40                  | 85                   |      |
| Shutdown on/off voltage level (see Note 2)        | V <sub>IH</sub> | V <sub>DD</sub> < 2.7 V        | 0.75 V <sub>DD</sub> |                      | V    |
|                                                   |                 | V <sub>DD</sub> = 2.7 to 3.6 V | 2                    |                      |      |
|                                                   | V <sub>IL</sub> |                                | 0.6                  |                      |      |

NOTE 2: Relative to GND



# TLV2760, TLV2761, TLV2762, TLV2763, TLV2764, TLV2765 FAMILY OF 1.8 V MICROPOWER RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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**electrical characteristics at recommended operating conditions,  $V_{DD} = 1.8\text{ V}$ ,  $2.4\text{ V}$  (unless otherwise noted)**

## dc performance

| PARAMETER                                                | TEST CONDITIONS                                                                                         | $T_A^\dagger$                         | MIN        | TYP  | MAX  | UNIT          |
|----------------------------------------------------------|---------------------------------------------------------------------------------------------------------|---------------------------------------|------------|------|------|---------------|
| $V_{IO}$ Input offset voltage                            | $V_{IC} = V_{DD}/2$ ,<br>$V_O = V_{DD}/2$ ,<br>$R_L = 300\text{ k}\Omega$ ,<br>$R_S = 50\text{ }\Omega$ | TLV276x                               | 25°C       | 550  | 3500 | $\mu\text{V}$ |
| $\alpha_{VIO}$ Offset voltage drift                      |                                                                                                         |                                       | Full range | 6800 |      |               |
| $CMRR$ Common-mode rejection ratio                       | $V_{ICR} = 0\text{ V to }V_{DD}$ ,<br>$R_S = 50\text{ }\Omega$                                          | $V_{DD} = 1.8\text{ V}$               | 25°C       | 50   | 70   | $\text{dB}$   |
|                                                          |                                                                                                         |                                       | Full range | 48   |      |               |
|                                                          |                                                                                                         | $V_{DD} = 2.4\text{ V}$               | 25°C       | 53   | 72   | $\text{dB}$   |
|                                                          |                                                                                                         |                                       | Full range | 50   |      | $\text{dB}$   |
|                                                          |                                                                                                         | $V_{DD} = 3.6\text{ V}$               | 25°C       | 55   | 76   | $\text{dB}$   |
|                                                          |                                                                                                         |                                       | Full range | 55   |      |               |
|                                                          | $V_{ICR} = 1.2\text{ V to }V_{DD}$ ,<br>$R_S = 50\text{ }\Omega$                                        | $V_{DD} = 2.4\text{ V}, 3.6\text{ V}$ | 25°C       | 63   | 82   | $\text{dB}$   |
|                                                          |                                                                                                         |                                       | Full range | 60   |      |               |
| $A_{VD}$ Large-signal differential voltage amplification | $R_L = 10\text{ k}\Omega$ ,<br>$V_{O(PP)} = V_{DD}/2$                                                   | $V_{DD} = 1.8\text{ V}$               | 25°C       | 20   | 60   | $\text{V/mV}$ |
|                                                          |                                                                                                         |                                       | Full range | 18   |      |               |
|                                                          |                                                                                                         | $V_{DD} = 2.4\text{ V}$               | 25°C       | 28   | 78   | $\text{V/mV}$ |
|                                                          |                                                                                                         |                                       | Full range | 23   |      |               |
|                                                          |                                                                                                         | $V_{DD} = 3.6\text{ V}$               | 25°C       | 45   | 120  | $\text{V/mV}$ |
|                                                          |                                                                                                         |                                       | Full range | 37   |      |               |

$^\dagger$  Full range is 0°C to 70°C for the C-suffix and –40°C to 85°C for the I-suffix. If not specified, full range is –40°C to 85°C.

## input characteristics

| PARAMETER                                | TEST CONDITIONS                                                                                         | $T_A^\dagger$ | MIN        | TYP | MAX | UNIT             |
|------------------------------------------|---------------------------------------------------------------------------------------------------------|---------------|------------|-----|-----|------------------|
| $I_{IO}$ Input offset current            | $V_{IC} = V_{DD}/2$ ,<br>$V_O = V_{DD}/2$ ,<br>$R_L = 300\text{ k}\Omega$ ,<br>$R_S = 50\text{ }\Omega$ | TLV276xC      | 25°C       | 3   | 15  | $\text{pA}$      |
|                                          |                                                                                                         | TLV276xI      | Full range | 100 |     |                  |
| $I_{IB}$ Input bias current              |                                                                                                         |               | 25°C       | 3   | 15  | $\text{pA}$      |
|                                          |                                                                                                         | TLV276xC      | Full range | 100 |     |                  |
|                                          |                                                                                                         | TLV276xI      | Full range | 200 |     |                  |
| $r_{i(d)}$ Differential input resistance |                                                                                                         | 25°C          | 1000       |     |     | $\text{G}\Omega$ |
| $c_{i(c)}$ Common-mode input capacitance | $f = 16\text{ kHz}$                                                                                     | 25°C          | 10         |     |     | $\text{pF}$      |

$^\dagger$  Full range is 0°C to 70°C for the C-suffix and –40°C to 85°C for the I-suffix. If not specified, full range is –40°C to 85°C.



**TLV2760, TLV2761, TLV2762, TLV2763, TLV2764, TLV2765**  
**FAMILY OF 1.8 V MICROWPOWER RAIL-TO-RAIL INPUT/OUTPUT**  
**OPERATIONAL AMPLIFIERS WITH SHUTDOWN**

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**electrical characteristics at recommended operating conditions,  $V_{DD} = 1.8\text{ V}$ ,  $2.4\text{ V}$  (unless otherwise noted) (continued)**

**output characteristics**

| PARAMETER                             | TEST CONDITIONS                                             |                         | $T_A^\dagger$ | MIN   | TYP  | MAX | UNIT |
|---------------------------------------|-------------------------------------------------------------|-------------------------|---------------|-------|------|-----|------|
| $V_{OH}$ High-level output voltage    | $V_{IC} = V_{DD}/2$ ,<br>$I_{OH} = -100\text{ }\mu\text{A}$ | $V_{DD} = 1.8\text{ V}$ | 25°C          | 1.77  | 1.79 |     | V    |
|                                       |                                                             |                         | Full range    | 1.76  |      |     |      |
|                                       |                                                             | $V_{DD} = 2.4\text{ V}$ | 25°C          | 2.38  | 2.39 |     |      |
|                                       |                                                             |                         | Full range    | 2.37  |      |     |      |
|                                       |                                                             | $V_{DD} = 3.6\text{ V}$ | 25°C          | 3.58  | 3.59 |     |      |
|                                       |                                                             |                         | Full range    | 3.57  |      |     |      |
|                                       | $V_{IC} = V_{DD}/2$ ,<br>$I_{OH} = -500\text{ }\mu\text{A}$ | $V_{DD} = 1.8\text{ V}$ | 25°C          | 1.725 | 1.75 |     |      |
|                                       |                                                             |                         | Full range    | 1.7   |      |     |      |
|                                       |                                                             | $V_{DD} = 2.4\text{ V}$ | 25°C          | 2.325 | 2.35 |     |      |
|                                       |                                                             |                         | Full range    | 2.3   |      |     |      |
| $V_{OL}$ Low-level output voltage     | $V_{IC} = V_{DD}/2$ ,<br>$I_{OL} = 100\text{ }\mu\text{A}$  | $V_{DD} = 1.8\text{ V}$ | 25°C          |       | 10   | 20  | mV   |
|                                       |                                                             |                         | Full range    |       |      | 30  |      |
|                                       | $V_{IC} = V_{DD}/2$ ,<br>$I_{OL} = 500\text{ }\mu\text{A}$  | $V_{DD} = 1.8\text{ V}$ | 25°C          |       | 50   | 75  |      |
|                                       |                                                             |                         | Full range    |       |      | 100 |      |
| $I_O$ Output current                  | $V_{DD} = 1.8\text{ V}$ ,<br>$V_O = 0.5\text{ V from}$      | Positive rail           | 25°C          |       | 4.8  |     | mA   |
|                                       |                                                             | Negative rail           |               |       | 7.2  |     |      |
|                                       | $V_{DD} = 2.4\text{ V}$ ,<br>$V_O = 0.5\text{ V from}$      | Positive rail           | 25°C          |       | 7.3  |     |      |
|                                       |                                                             | Negative rail           |               |       | 10.2 |     |      |
| $I_{OS}$ Short-circuit output current | $V_{DD} = 1.8\text{ V}$                                     | Sourcing                | 25°C          |       | 7    |     | mA   |
|                                       |                                                             | Sinking                 |               |       | 10   |     |      |
|                                       | $V_{DD} = 2.4\text{ V}$                                     | Sourcing                | 25°C          |       | 15   |     |      |
|                                       |                                                             | Sinking                 |               |       | 19   |     |      |

$^\dagger$  Full range is 0°C to 70°C for the C-suffix and -40°C to 85°C for the I-suffix. If not specified, full range is -40°C to 85°C.

**power supply,  $V_{DD} = 1.8\text{ V}$ ,  $2.4\text{ V}$ ,  $3.6\text{ V}$  (unless otherwise noted)**

| PARAMETER        |                                                                         | TEST CONDITIONS                                                                             |         | T <sub>A</sub> <sup>†</sup> | MIN | TYP | MAX | UNIT |
|------------------|-------------------------------------------------------------------------|---------------------------------------------------------------------------------------------|---------|-----------------------------|-----|-----|-----|------|
| I <sub>DD</sub>  | Supply current (per channel)                                            | V <sub>O</sub> = V <sub>DD</sub> /2, <span style="float:right">SHDN = V<sub>DD</sub></span> |         | 25°C                        |     | 20  | 28  | μA   |
|                  |                                                                         |                                                                                             |         | Full range                  |     |     | 30  |      |
| k <sub>SVR</sub> | Supply voltage rejection ratio<br>(ΔV <sub>DD</sub> /ΔV <sub>IO</sub> ) | V <sub>DD</sub> = 1.8 V to 2.4 V,<br>V <sub>IC</sub> = V <sub>DD</sub> /2                   | No load | 25°C                        | 65  | 85  |     | dB   |
|                  |                                                                         |                                                                                             |         | Full range                  | 63  |     |     |      |
|                  |                                                                         | V <sub>DD</sub> = 2.4 V to 3.6 V,<br>V <sub>IC</sub> = V <sub>DD</sub> /2                   |         | 25°C                        | 65  | 85  |     |      |
|                  |                                                                         |                                                                                             |         | Full range                  | 63  |     |     |      |
|                  |                                                                         | V <sub>DD</sub> = 1.8 V to 3.6 V,<br>V <sub>IC</sub> = V <sub>DD</sub> /2                   |         | 25°C                        | 65  | 85  |     |      |
|                  |                                                                         |                                                                                             |         | Full range                  | 63  |     |     |      |

$^\dagger$  Full range is 0°C to 70°C for the C-suffix and -40°C to 85°C for the I-suffix. If not specified, full range is -40°C to 85°C.

**TLV2760, TLV2761, TLV2762, TLV2763, TLV2764, TLV2765**  
**FAMILY OF 1.8 V MICROPOWER RAIL-TO-RAIL INPUT/OUTPUT**  
**OPERATIONAL AMPLIFIERS WITH SHUTDOWN**

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**electrical characteristics at recommended operating conditions,  $V_{DD} = 1.8\text{ V}$ ,  $2.4\text{ V}$  (unless otherwise noted) (continued)**

**dynamic performance**

| PARAMETER      |                                  | TEST CONDITIONS                                                                                                            |                         | T <sub>A</sub> <sup>†</sup> | MIN  | TYP  | MAX | UNIT |
|----------------|----------------------------------|----------------------------------------------------------------------------------------------------------------------------|-------------------------|-----------------------------|------|------|-----|------|
| UGBW           | Unity gain bandwidth             | R <sub>L</sub> = 300 kΩ, C <sub>L</sub> = 10 pF                                                                            |                         | 25°C                        | 500  |      |     | kHz  |
| SR+            | Positive slew rate at unity gain | V <sub>O(PP)</sub> = 1 V, R <sub>L</sub> = 300 kΩ, C <sub>L</sub> = 50 pF,                                                 | V <sub>DD</sub> = 1.8 V | 25°C                        | 0.11 | 0.20 |     | V/μs |
|                |                                  |                                                                                                                            |                         | Full range                  | 0.09 |      |     |      |
|                |                                  |                                                                                                                            | V <sub>DD</sub> = 2.4 V | 25°C                        | 0.11 | 0.22 |     | V/μs |
|                |                                  |                                                                                                                            |                         | Full range                  | 0.09 |      |     |      |
|                |                                  |                                                                                                                            | V <sub>DD</sub> = 3.6 V | 25°C                        | 0.11 | 0.23 |     | V/μs |
|                |                                  |                                                                                                                            |                         | Full range                  | 0.09 |      |     |      |
| SR−            | Negative slew rate at unity gain | V <sub>O(PP)</sub> = 1 V, R <sub>L</sub> = 300 kΩ, C <sub>L</sub> = 50 pF,                                                 | V <sub>DD</sub> = 1.8 V | 25°C                        | 0.08 | 0.15 |     | V/μs |
|                |                                  |                                                                                                                            |                         | Full range                  | 0.07 |      |     |      |
|                |                                  |                                                                                                                            | V <sub>DD</sub> = 2.4 V | 25°C                        | 0.10 | 0.18 |     | V/μs |
|                |                                  |                                                                                                                            |                         | Full range                  | 0.09 |      |     |      |
|                |                                  |                                                                                                                            | V <sub>DD</sub> = 3.6 V | 25°C                        | 0.10 | 0.22 |     | V/μs |
|                |                                  |                                                                                                                            |                         | Full range                  | 0.09 |      |     |      |
| φ <sub>m</sub> | Phase margin                     | R <sub>L</sub> = 300 kΩ, C <sub>L</sub> = 100 pF                                                                           |                         | 25°C                        | 63   |      |     | °    |
|                | Gain margin                      |                                                                                                                            |                         | 25°C                        | 20   |      |     | dB   |
| t <sub>s</sub> | Settling time                    | V <sub>DD</sub> = 1.8 V, V <sub>(STEP)PP</sub> = 1 V, A <sub>V</sub> = −1, C <sub>L</sub> = 10 pF, R <sub>L</sub> = 300 kΩ | 0.1%                    | 25°C                        | 6.4  |      |     | μs   |
|                |                                  |                                                                                                                            | 0.01%                   |                             | 13.7 |      |     |      |
|                |                                  | V <sub>DD</sub> = 2.4 V, V <sub>(STEP)PP</sub> = 1 V, A <sub>V</sub> = −1, C <sub>L</sub> = 10 pF, R <sub>L</sub> = 300 kΩ | 0.1%                    |                             | 6    |      |     |      |
|                |                                  |                                                                                                                            | 0.01%                   |                             | 13.9 |      |     |      |

$^\dagger$  Full range is  $0^\circ\text{C}$  to  $70^\circ\text{C}$  for the C-suffix and  $-40^\circ\text{C}$  to  $85^\circ\text{C}$  for the I-suffix. If not specified, full range is  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

**noise/distortion**

| PARAMETER |                                      | TEST CONDITIONS                                                                                                      |             | $T_A$              | MIN | TYP   | MAX | UNIT                         |
|-----------|--------------------------------------|----------------------------------------------------------------------------------------------------------------------|-------------|--------------------|-----|-------|-----|------------------------------|
| THD + N   | Total harmonic distortion plus noise | $V_{DD} = 1.8\text{ V}$ ,<br>$V_{O(PP)} = V_{DD}/2\text{ V}$ ,<br>$R_L = 300\text{ k}\Omega$ ,<br>$f = 1\text{ kHz}$ | $A_V = 1$   | $25^\circ\text{C}$ |     | 0.08% |     |                              |
|           |                                      |                                                                                                                      | $A_V = 10$  |                    |     | 0.10% |     |                              |
|           |                                      |                                                                                                                      | $A_V = 100$ |                    |     | 0.27% |     |                              |
|           |                                      | $V_{DD} = 2.4\text{ V}$ ,<br>$V_{O(PP)} = V_{DD}/2\text{ V}$ ,<br>$R_L = 300\text{ k}\Omega$ ,<br>$f = 1\text{ kHz}$ | $A_V = 1$   | $25^\circ\text{C}$ |     | 0.06% |     |                              |
|           |                                      |                                                                                                                      | $A_V = 10$  |                    |     | 0.08% |     |                              |
|           |                                      |                                                                                                                      | $A_V = 100$ |                    |     | 0.24% |     |                              |
| $V_n$     | Equivalent input noise voltage       | $f = 1\text{ kHz}$                                                                                                   |             | $25^\circ\text{C}$ |     | 95    |     | $\text{nV}/\sqrt{\text{Hz}}$ |
|           |                                      | $f = 10\text{ kHz}$                                                                                                  |             | $25^\circ\text{C}$ |     | 75    |     |                              |
| $I_n$     | Equivalent input noise current       | $f = 1\text{ kHz}$                                                                                                   |             | $25^\circ\text{C}$ |     | 0.8   |     | $\text{fA}/\sqrt{\text{Hz}}$ |

**shutdown characteristics**

| PARAMETER             |                                                                                         | TEST CONDITIONS            | $T_A^\dagger$      | MIN | TYP | MAX | UNIT          |
|-----------------------|-----------------------------------------------------------------------------------------|----------------------------|--------------------|-----|-----|-----|---------------|
| $I_{DD(\text{SHDN})}$ | Supply current, all channels in shutdown mode (TLV2760, TLV2763, TLV2765) (per channel) | $\text{SHDN} = 0\text{ V}$ | $25^\circ\text{C}$ |     | 10  | 50  | nA            |
|                       |                                                                                         |                            | Full range         |     |     | 400 |               |
| $t_{(\text{on})}$     | Amplifier turnon time (see Note 3)                                                      | $R_L = 300\text{ k}\Omega$ | $25^\circ\text{C}$ |     | 5   |     | $\mu\text{s}$ |
| $t_{(\text{off})}$    | Amplifier turnoff time (see Note 3)                                                     | $R_L = 300\text{ k}\Omega$ | $25^\circ\text{C}$ |     | 0.8 |     | $\mu\text{s}$ |

$^\dagger$  Full range is  $0^\circ\text{C}$  to  $70^\circ\text{C}$  for the C-suffix and  $-40^\circ\text{C}$  to  $85^\circ\text{C}$  for the I-suffix. If not specified, full range is  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

NOTE 3: Disable time and enable time are defined as the interval between application of the logic signal to  $\text{SHDN}$  and the point at which the supply current has reached half its final value.



**TLV2760, TLV2761, TLV2762, TLV2763, TLV2764, TLV2765**  
**FAMILY OF 1.8 V MICROPOWER RAIL-TO-RAIL INPUT/OUTPUT**  
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**TYPICAL CHARACTERISTICS**

**Table of Graphs**

|                |                                              |                              | <b>FIGURE</b> |
|----------------|----------------------------------------------|------------------------------|---------------|
| $V_{IO}$       | Input offset voltage                         | vs Common-mode input voltage | 1, 2          |
| CMRR           | Common-mode rejection ratio                  | vs Frequency                 | 3             |
| $V_{OH}$       | High-level output voltage                    | vs High-level output current | 4, 6          |
| $V_{OL}$       | Low-level output voltage                     | vs Low-level output current  | 5, 7          |
| $V_{O(PP)}$    | Maximum peak-to-peak output voltage          | vs Frequency                 | 8             |
| $I_{DD}$       | Supply current                               | vs Supply voltage            | 9             |
| $I_{DD}$       | Supply current                               | vs Free-air temperature      | 10            |
| PSRR           | Power supply rejection ratio                 | vs Frequency                 | 11            |
| $A_{VD}$       | Differential voltage amplification & phase   | vs Frequency                 | 12            |
|                | Gain-bandwidth product                       | vs Temperature               | 13            |
|                |                                              | vs Supply voltage            | 14            |
|                |                                              | vs Supply voltage            | 15            |
| SR             | Slew rate                                    | vs Free-air temperature      | 16, 17        |
|                |                                              | vs Load capacitance          | 18            |
| $\phi_m$       | Phase margin                                 | vs Load capacitance          | 18            |
| $V_n$          | Equivalent input noise voltage               | vs Frequency                 | 19            |
|                | Supply current and output voltage            | vs Time                      | 20            |
|                | Voltage-follower large-signal pulse response | vs Time                      | 21            |
|                | Voltage-follower small-signal pulse response | vs Time                      | 22            |
|                | Inverting large-signal response              | vs Time                      | 23            |
|                | Inverting small-signal response              | vs Time                      | 24            |
|                | Crosstalk                                    | vs Frequency                 | 25            |
|                | Shutdown forward & reverse isolation         | vs Frequency                 | 26            |
| $I_{DD(SHDN)}$ | Shutdown supply current                      | vs Supply voltage            | 27            |
| $I_{DD(SHDN)}$ | Shutdown supply current                      | vs Free-air temperature      | 28            |
| $I_{DD(SHDN)}$ | Shutdown pin leakage current                 | vs Shutdown pin voltage      | 29            |
| $I_{DD(SHDN)}$ | Shutdown supply current/output voltage       | vs Time                      | 30            |

# TLV2760, TLV2761, TLV2762, TLV2763, TLV2764, TLV2765 FAMILY OF 1.8 V MICROPOWER RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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## TYPICAL CHARACTERISTICS

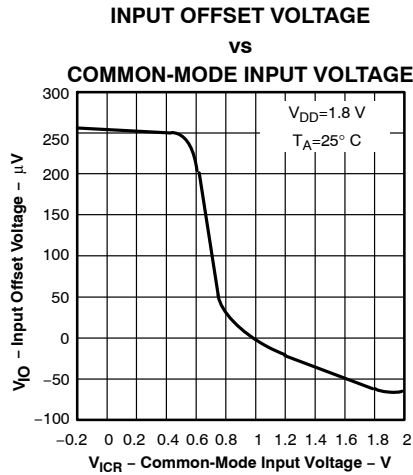


Figure 1

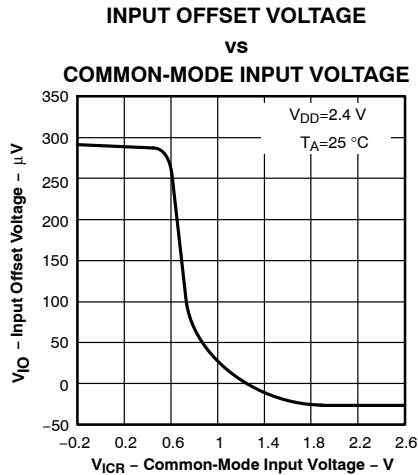


Figure 2

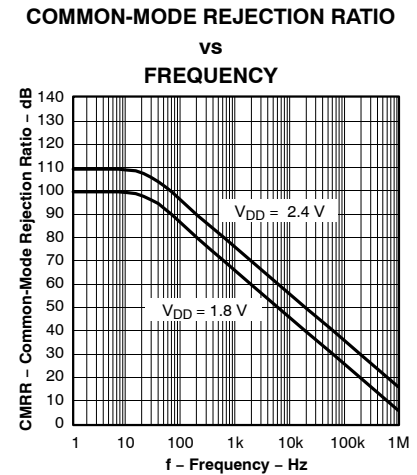


Figure 3

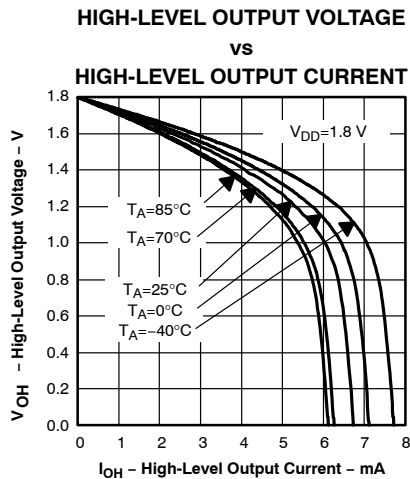


Figure 4

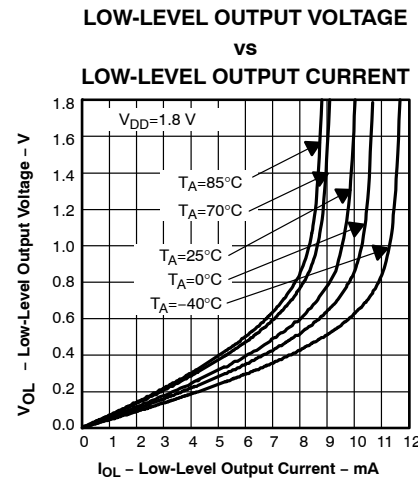


Figure 5

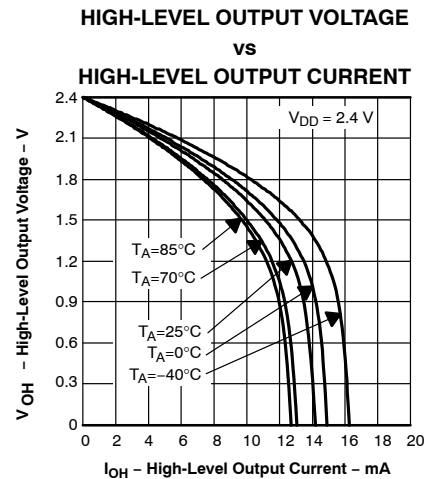


Figure 6

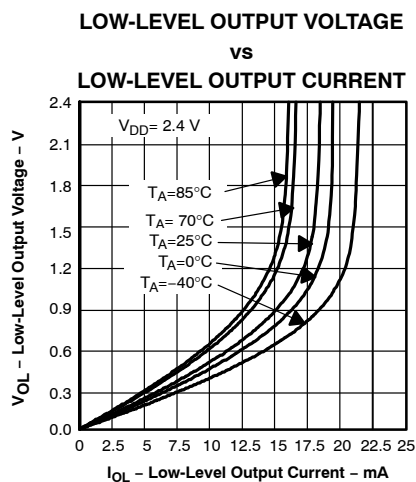


Figure 7

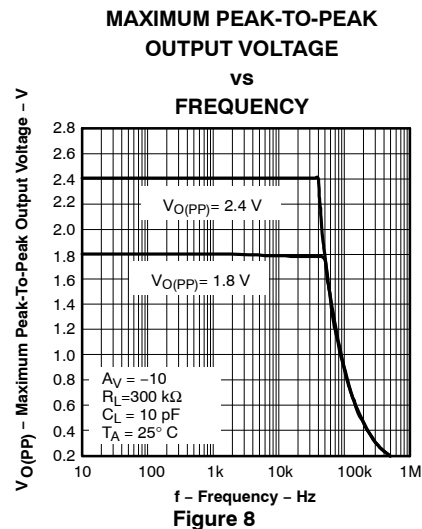


Figure 8



# TLV2760, TLV2761, TLV2762, TLV2763, TLV2764, TLV2765

## FAMILY OF 1.8 V MICROPOWER RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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### TYPICAL CHARACTERISTICS

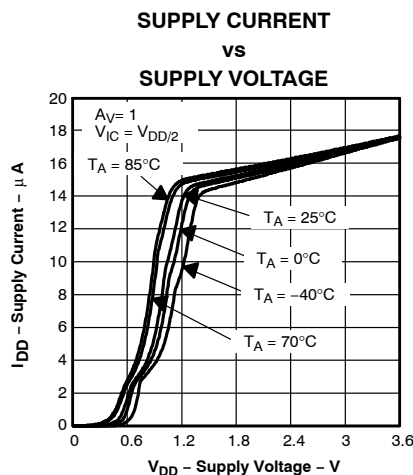


Figure 9

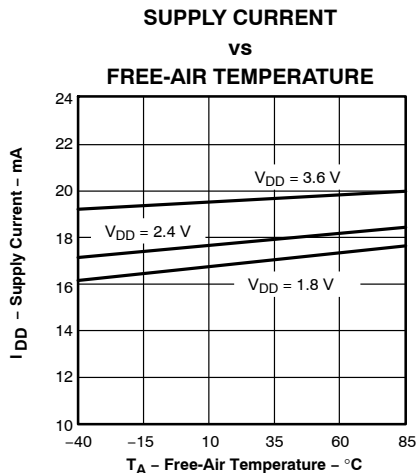


Figure 10

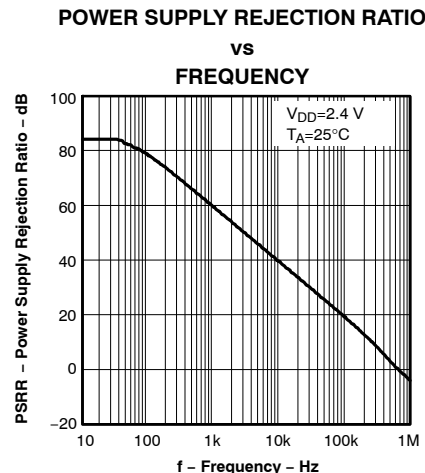


Figure 11

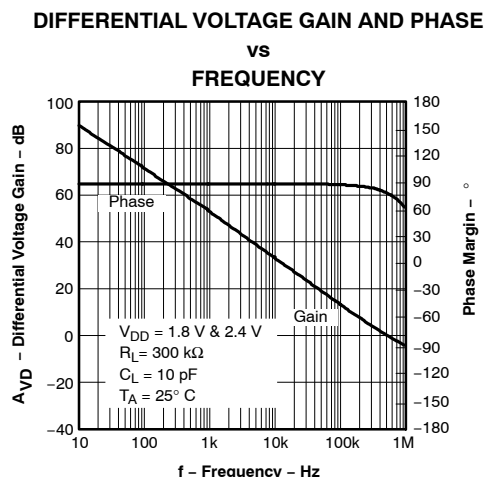


Figure 12

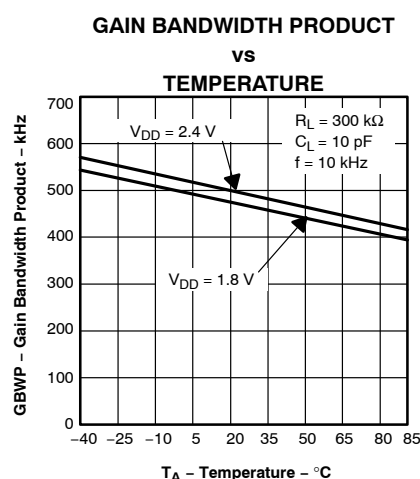


Figure 13

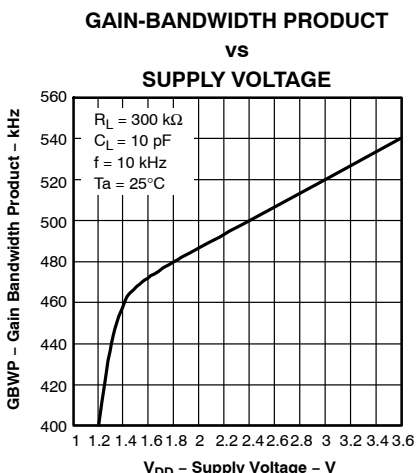


Figure 14

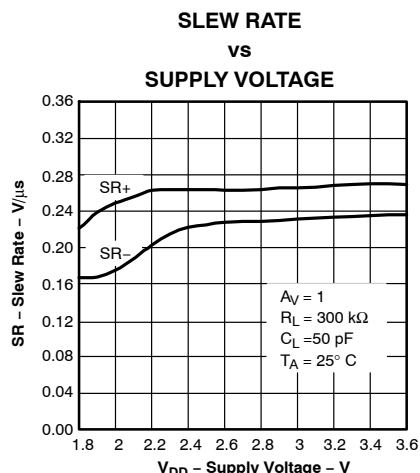


Figure 15

# TLV2760, TLV2761, TLV2762, TLV2763, TLV2764, TLV2765 FAMILY OF 1.8 V MICROPOWER RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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## TYPICAL CHARACTERISTICS

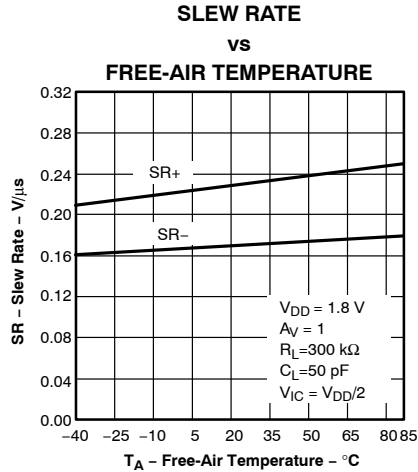


Figure 16

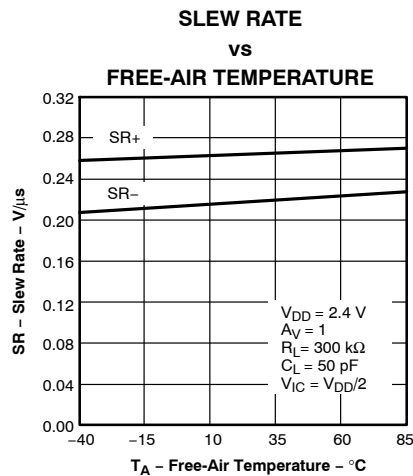


Figure 17

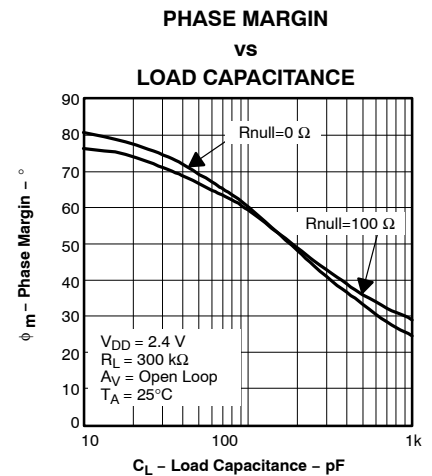


Figure 18

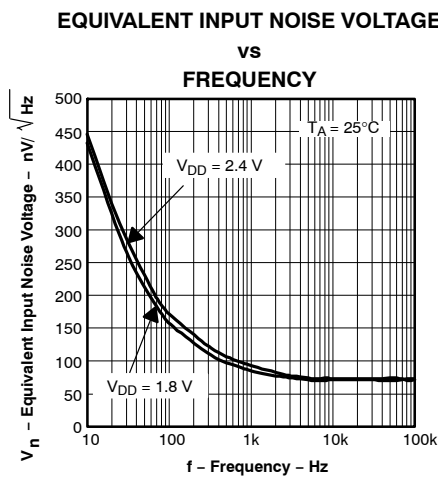


Figure 19

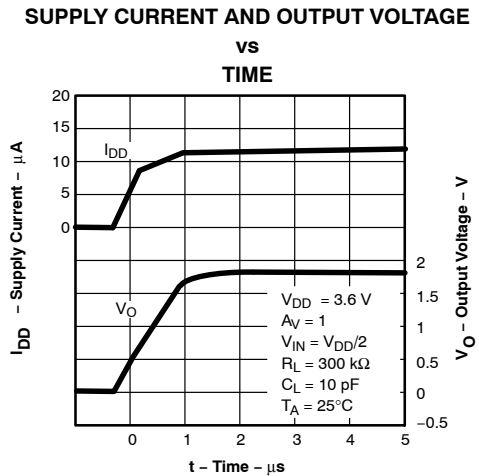


Figure 20

### VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

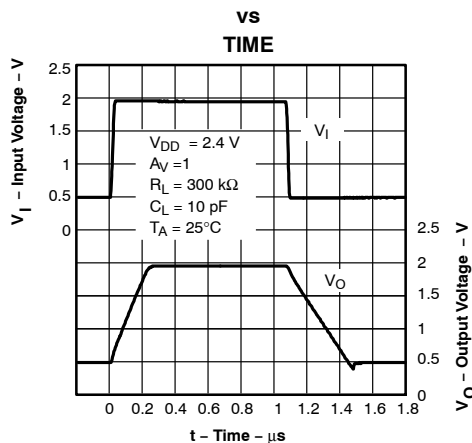


Figure 21

### VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

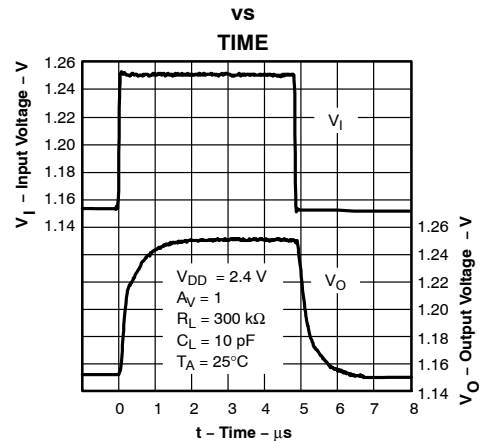


Figure 22



# TLV2760, TLV2761, TLV2762, TLV2763, TLV2764, TLV2765

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## TYPICAL CHARACTERISTICS

### INVERTING LARGE-SIGNAL RESPONSE

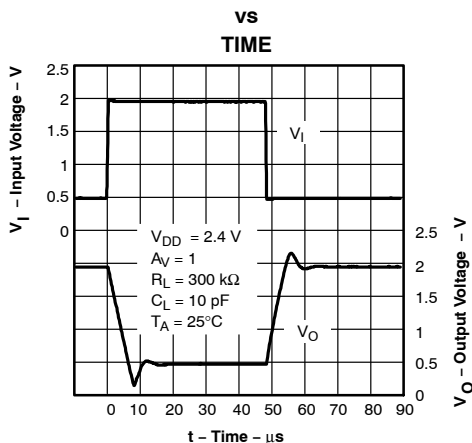


Figure 23

### INVERTING SMALL-SIGNAL PULSE RESPONSE

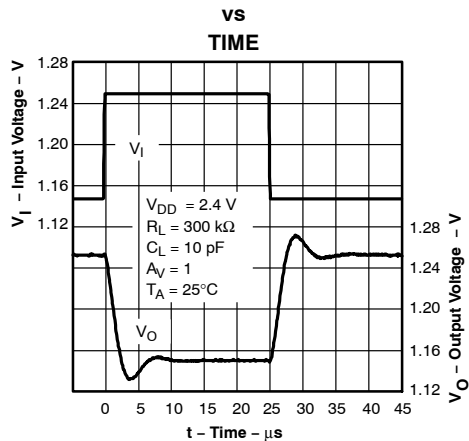


Figure 24

### CROSSTALK

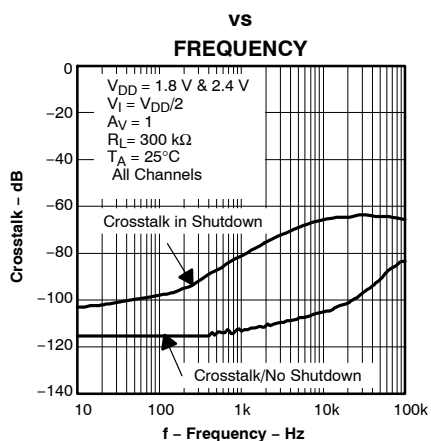


Figure 25

### SHUTDOWN FORWARD AND REVERSE ISOLATION

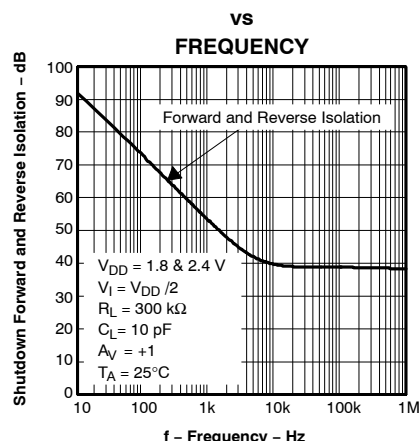


Figure 26

### SHUTDOWN SUPPLY CURRENT

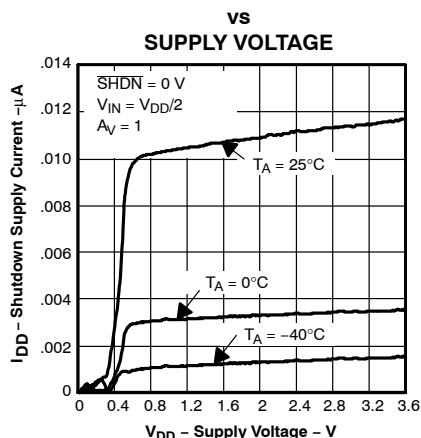


Figure 27

### SHUTDOWN SUPPLY CURRENT

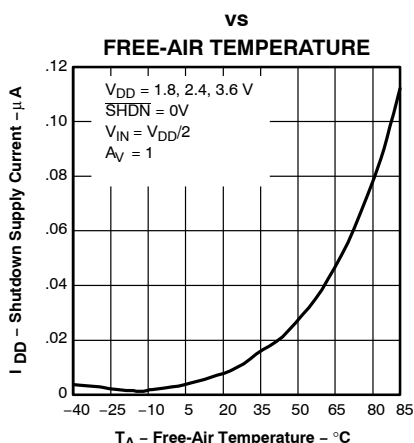


Figure 28

### SHUTDOWN PIN LEAKAGE CURRENT

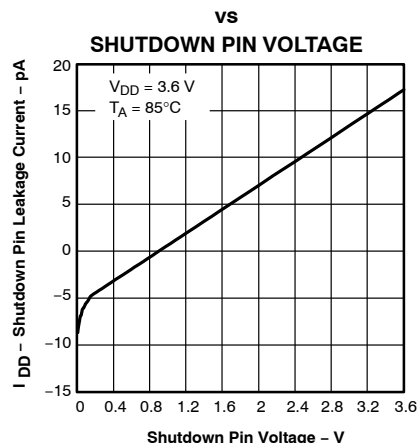


Figure 29



TLV2760, TLV2761, TLV2762, TLV2763, TLV2764, TLV2765  
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TYPICAL CHARACTERISTICS

SHUTDOWN SUPPLY CURRENT / OUTPUT VOLTAGE  
vs  
TIME

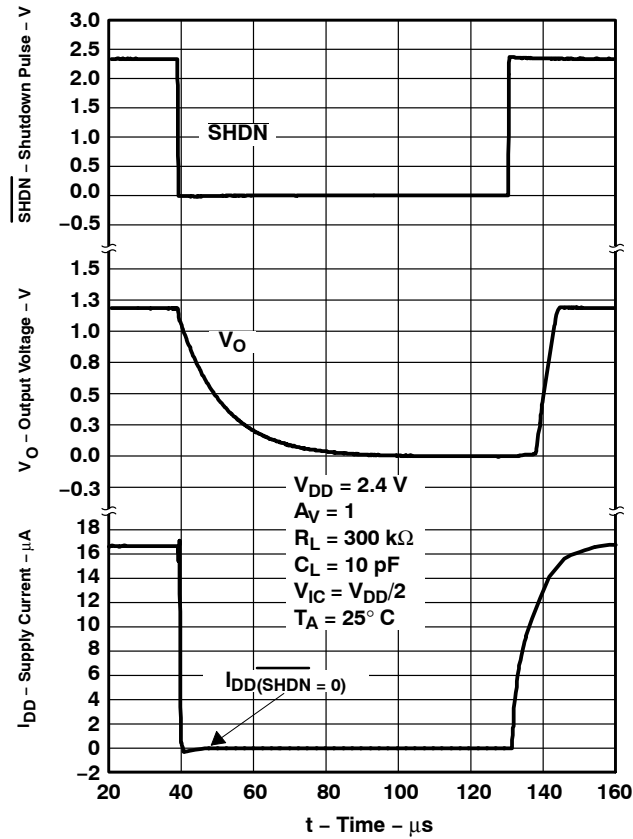


Figure 30

# TLV2760, TLV2761, TLV2762, TLV2763, TLV2764, TLV2765 FAMILY OF 1.8 V MICROPOWER RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

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## APPLICATION INFORMATION

### driving a capacitive load

When the amplifier is configured in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series ( $R_{NULL}$ ) with the output of the amplifier, as shown in Figure 31. A minimum value of 20  $\Omega$  should work well for most applications.

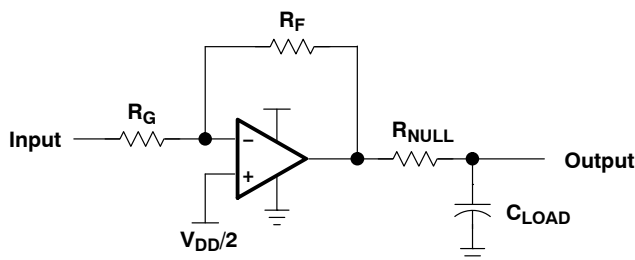


Figure 31. Driving a Capacitive Load

### offset voltage

The output offset voltage, ( $V_{OO}$ ) is the sum of the input offset voltage ( $V_{IO}$ ) and both input bias currents ( $I_{IB}$ ) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:

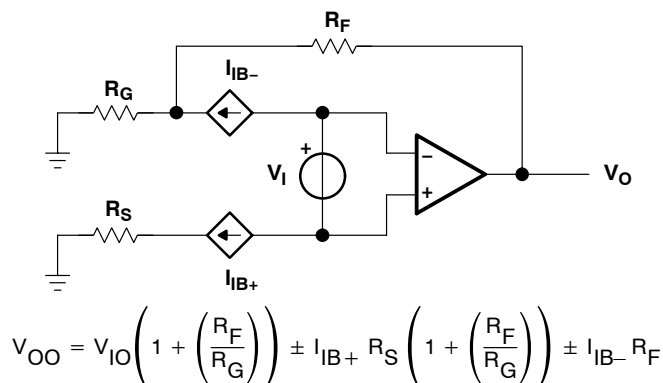


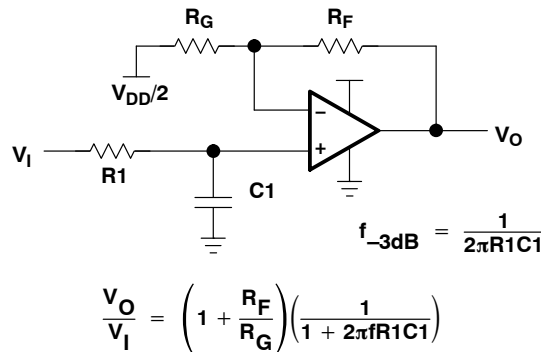
Figure 32. Output Offset Voltage Model

### general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 33).

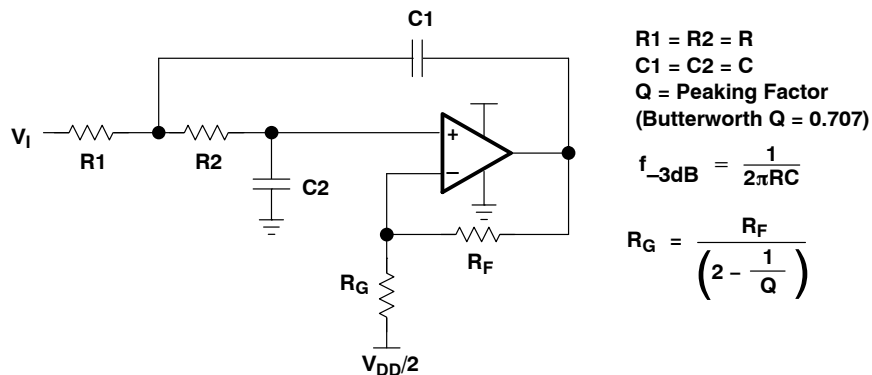
## APPLICATION INFORMATION

### general configurations (continued)



**Figure 33. Single-Pole Low-Pass Filter**

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.



**Figure 34. 2-Pole Low-Pass Sallen-Key Filter**

### circuit layout considerations

To achieve the levels of high performance of the TLV276x, follow proper printed-circuit board design techniques. A general set of guidelines is given in the following.

- **Ground planes**—It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- **Proper power supply decoupling**—Use a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.

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## APPLICATION INFORMATION

### circuit layout considerations (continued)

- Sockets—Sockets can be used but are not recommended. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements—Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components—Using surface-mount passive components is recommended for high performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

### shutdown function

Three members of the TLV276x family (TLV2760/3/5) have a shutdown terminal for conserving battery life in portable applications. When the shutdown terminal is pulled low, the supply current is reduced to 10 nA/channel, the amplifier is disabled, and the outputs are placed in a high impedance mode. To enable the amplifier, the shutdown terminal must be pulled high. The shutdown terminal should never be left floating. If the shutdown feature is not desired, directly tie the shutdown terminal to the positive rail. The shutdown terminal threshold is always referenced to the GND terminal of the device. Therefore, when operating the device with split supply voltages (e.g.  $\pm 1.8$  V), the shutdown terminal needs to be pulled to the negative rail, not the system ground, to disable the operational amplifier.

The amplifier is powered with a single 2.4-V supply and configured as a noninverting configuration with a unity gain. Turnon and turnoff times are defined as the interval between application of the logic signal to the shutdown pin and the point at which the supply current has reached half its final value. The times for the single, dual, and quad are listed in the data tables.

### general power dissipation considerations

For a given  $\theta_{JA}$ , the maximum power dissipation is shown in Figure 35 and is calculated by the following formula:

$$P_D = \left( \frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

$P_D$  = Maximum power dissipation of TLV276x IC (watts)

$T_{MAX}$  = Absolute maximum junction temperature (150°C)

$T_A$  = Free-ambient air temperature (°C)

$\theta_{JA}$  =  $\theta_{JC} + \theta_{CA}$

$\theta_{JC}$  = Thermal coefficient from junction to case

$\theta_{CA}$  = Thermal coefficient from case to ambient air (°C/W)

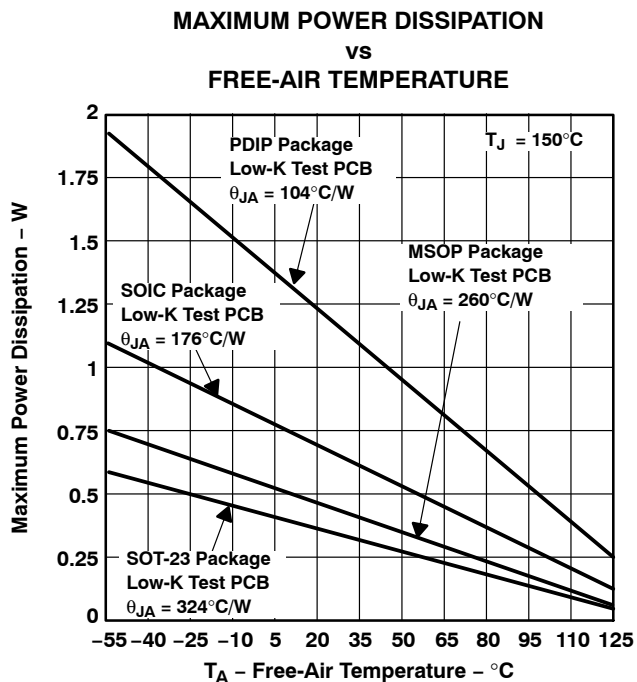


**TLV2760, TLV2761, TLV2762, TLV2763, TLV2764, TLV2765**  
**FAMILY OF 1.8 V MICROPOWER RAIL-TO-RAIL INPUT/OUTPUT**  
**OPERATIONAL AMPLIFIERS WITH SHUTDOWN**

SLOS326F – JUNE 2000 – REVISED AUGUST 2013

**APPLICATION INFORMATION**

**general power dissipation considerations (continued)**



NOTE A: Results are with no air flow and using JEDEC Standard Low-K test PCB.

**Figure 35. Maximum Power Dissipation vs Free-Air Temperature**

# TLV2760, TLV2761, TLV2762, TLV2763, TLV2764, TLV2765 FAMILY OF 1.8 V MICROPOWER RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS326F – JUNE 2000 – REVISED AUGUST 2013

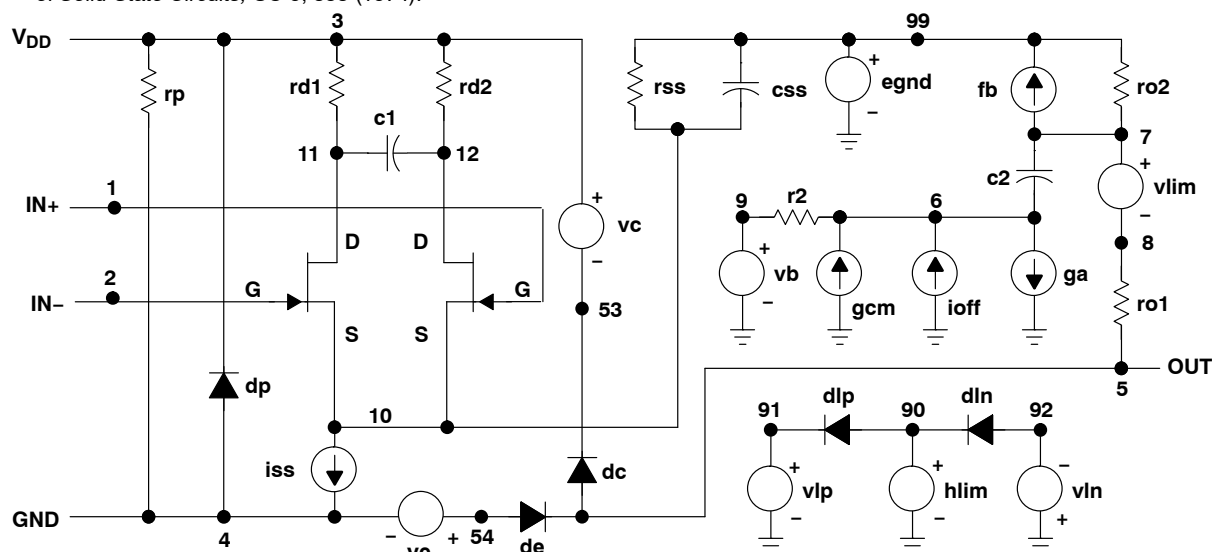
## APPLICATION INFORMATION

### macromodel information

Macromodel information provided was derived using Microsim *Parts*™ Release 9.1, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 4) and subcircuit in Figure 36 are generated using TLV276x typical electrical and operating characteristics at  $T_A = 25^\circ\text{C}$ . Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 4: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers," *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).



\*DEVICE=amp\_tlv276x\_highVdd,OPAMP,NJF,INT  
\* amp\_tlv\_276x\_highVdd operational amplifier "macromodel"  
\* subcircuit updated using Model Editor release 9.1 on 05/15/00  
\* at 14:40 Model Editor is an OrCAD product.

\* connections:

non-inverting input  
inverting input  
positive power supply  
negative power supply  
output

.subckt amp\_tlv276x\_highVdd

1 2 3 4 5

c1 11 12 457.48E-15  
c2 6 7 5.0000E-12  
css 10 99 1.1431E-12  
dc 5 53 dy  
de 54 5 dy  
dip 90 91 dx  
din 92 90 dx  
dp 4 3 dx  
egnd 99 0 poly(2) (3,0) (4,0) 0 .5 .5  
fb 7 99 poly(5) vb vc ve vlp vln 0

176.02E6 -1E3 1E3 180E6  
-180E6

ga 6 0 11 12 16.272E-6  
gcm 0 6 10 99 6.8698E-9  
iss 10 4 dc 1.3371E-6  
hlim 90 0 vlim 1K  
j1 11 2 10 jx1  
J2 12 1 10 jx2  
r2 6 9 100.00E3  
rd1 3 11 61.456E3  
rd2 3 12 61.456E3  
ro1 8 5 10  
ro2 7 99 10  
rp 3 4 150.51E3  
rss 10 99 149.58E6  
vb 9 0 dc 0  
vc 3 53 dc .78905  
ve 54 4 dc .78905  
vlim 7 8 dc 0  
vlp 91 0 dc 14.200  
vln 0 92 dc 14.200  
.model dx D(Is=800.00E-18)  
.model dy D(Is=800.00E-18 Rs=1m Cjo=10p)  
.model jx1 NJF(Is=500.00E-15 Beta=198.03E-6 Vto=-1)  
.model jx2 NJF(Is=500.00E-15 Beta=198.03E-6 Vto=-1)  
.ends

Figure 36. Boyle Macromodel and Subcircuit

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**Revision History**

| DATE   | REV | PAGE | SECTION                     | DESCRIPTION                                           |
|--------|-----|------|-----------------------------|-------------------------------------------------------|
| 8/2013 | F   | 2    | 2nd Available Options Table | Added TLVZ762CDGK and AJO to Available Options Table. |

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DRAFT ONLY

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TLV2760ID        | ACTIVE        | SOIC         | D                  | 8    | 75             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | T2760I                  | <a href="#">Samples</a> |
| TLV2760IDBVR     | ACTIVE        | SOT-23       | DBV                | 6    | 3000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | VANI                    | <a href="#">Samples</a> |
| TLV2760IDBVT     | ACTIVE        | SOT-23       | DBV                | 6    | 250            | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | VANI                    | <a href="#">Samples</a> |
| TLV2760IDBVTG4   | ACTIVE        | SOT-23       | DBV                | 6    | 250            | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | VANI                    | <a href="#">Samples</a> |
| TLV2760IDG4      | ACTIVE        | SOIC         | D                  | 8    | 75             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | T2760I                  | <a href="#">Samples</a> |
| TLV2760IP        | ACTIVE        | PDIP         | P                  | 8    | 50             | Pb-Free<br>(RoHS)          | CU NIPDAU               | N / A for Pkg Type   | -40 to 85    | T2760I                  | <a href="#">Samples</a> |
| TLV2760IPE4      | ACTIVE        | PDIP         | P                  | 8    | 50             | Pb-Free<br>(RoHS)          | CU NIPDAU               | N / A for Pkg Type   | -40 to 85    | T2760I                  | <a href="#">Samples</a> |
| TLV2761CD        | ACTIVE        | SOIC         | D                  | 8    | 75             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | T2761C                  | <a href="#">Samples</a> |
| TLV2761CDG4      | ACTIVE        | SOIC         | D                  | 8    | 75             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | T2761C                  | <a href="#">Samples</a> |
| TLV2761ID        | ACTIVE        | SOIC         | D                  | 8    | 75             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | T2761I                  | <a href="#">Samples</a> |
| TLV2761IDBVR     | ACTIVE        | SOT-23       | DBV                | 5    | 3000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | VAXI                    | <a href="#">Samples</a> |
| TLV2761IDBVT     | ACTIVE        | SOT-23       | DBV                | 5    | 250            | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | VAXI                    | <a href="#">Samples</a> |
| TLV2761IDBVTG4   | ACTIVE        | SOT-23       | DBV                | 5    | 250            | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | VAXI                    | <a href="#">Samples</a> |
| TLV2761IP        | ACTIVE        | PDIP         | P                  | 8    | 50             | Pb-Free<br>(RoHS)          | CU NIPDAU               | N / A for Pkg Type   | -40 to 85    | T2761I                  | <a href="#">Samples</a> |
| TLV2762CD        | ACTIVE        | SOIC         | D                  | 8    | 75             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | 2762C                   | <a href="#">Samples</a> |
| TLV2762CDGK      | ACTIVE        | VSSOP        | DGK                | 8    | 80             | Green (RoHS<br>& no Sb/Br) | CU NIPDAUAG             | Level-1-260C-UNLIM   | 0 to 70      | AJO                     | <a href="#">Samples</a> |
| TLV2762CDGKR     | ACTIVE        | VSSOP        | DGK                | 8    | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAUAG             | Level-1-260C-UNLIM   | 0 to 70      | AJO                     | <a href="#">Samples</a> |

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6)    | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|----------------------------|----------------------|--------------|-------------------------|-------------------------|
| TLV2762CDR       | ACTIVE        | SOIC         | D                  | 8    | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU                  | Level-1-260C-UNLIM   | 0 to 70      | 2762C                   | <a href="#">Samples</a> |
| TLV2762ID        | ACTIVE        | SOIC         | D                  | 8    | 75             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU                  | Level-1-260C-UNLIM   | -40 to 85    | 2762I                   | <a href="#">Samples</a> |
| TLV2762IDG4      | ACTIVE        | SOIC         | D                  | 8    | 75             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU                  | Level-1-260C-UNLIM   | -40 to 85    | 2762I                   | <a href="#">Samples</a> |
| TLV2762IDGK      | ACTIVE        | VSSOP        | DGK                | 8    | 80             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU  <br>CU NIPDAUAG | Level-1-260C-UNLIM   | -40 to 85    | AJP                     | <a href="#">Samples</a> |
| TLV2762IDGKG4    | ACTIVE        | VSSOP        | DGK                | 8    | 80             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU                  | Level-1-260C-UNLIM   | -40 to 85    | AJP                     | <a href="#">Samples</a> |
| TLV2762IDGKR     | ACTIVE        | VSSOP        | DGK                | 8    | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU  <br>CU NIPDAUAG | Level-1-260C-UNLIM   | -40 to 85    | AJP                     | <a href="#">Samples</a> |
| TLV2762IDGKRG4   | ACTIVE        | VSSOP        | DGK                | 8    | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU                  | Level-1-260C-UNLIM   | -40 to 85    | AJP                     | <a href="#">Samples</a> |
| TLV2762IDR       | ACTIVE        | SOIC         | D                  | 8    | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU                  | Level-1-260C-UNLIM   | -40 to 85    | 2762I                   | <a href="#">Samples</a> |
| TLV2763CDR       | ACTIVE        | SOIC         | D                  | 14   | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU                  | Level-1-260C-UNLIM   | 0 to 70      | TLV2763C                | <a href="#">Samples</a> |
| TLV2763IDGS      | ACTIVE        | VSSOP        | DGS                | 10   | 80             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU  <br>CU NIPDAUAG | Level-1-260C-UNLIM   | -40 to 85    | AJR                     | <a href="#">Samples</a> |
| TLV2763IDGSG4    | ACTIVE        | VSSOP        | DGS                | 10   | 80             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU                  | Level-1-260C-UNLIM   | -40 to 85    | AJR                     | <a href="#">Samples</a> |
| TLV2763IDGSR     | ACTIVE        | VSSOP        | DGS                | 10   | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU  <br>CU NIPDAUAG | Level-1-260C-UNLIM   | -40 to 85    | AJR                     | <a href="#">Samples</a> |
| TLV2763IDSGRG4   | ACTIVE        | VSSOP        | DGS                | 10   | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU                  | Level-1-260C-UNLIM   | -40 to 85    | AJR                     | <a href="#">Samples</a> |
| TLV2764CD        | ACTIVE        | SOIC         | D                  | 14   | 50             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU                  | Level-1-260C-UNLIM   | 0 to 70      | TLV2764C                | <a href="#">Samples</a> |
| TLV2764CDR       | ACTIVE        | SOIC         | D                  | 14   | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU                  | Level-1-260C-UNLIM   | 0 to 70      | TLV2764C                | <a href="#">Samples</a> |
| TLV2764ID        | ACTIVE        | SOIC         | D                  | 14   | 50             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU                  | Level-1-260C-UNLIM   | -40 to 85    | TLV2764I                | <a href="#">Samples</a> |
| TLV2764IDR       | ACTIVE        | SOIC         | D                  | 14   | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU                  | Level-1-260C-UNLIM   | -40 to 85    | TLV2764I                | <a href="#">Samples</a> |
| TLV2764IN        | ACTIVE        | PDIP         | N                  | 14   | 25             | Pb-Free<br>(RoHS)          | CU NIPDAU                  | N / A for Pkg Type   | -40 to 85    | TLV2764I                | <a href="#">Samples</a> |

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TLV2764IPW       | ACTIVE        | TSSOP        | PW                 | 14   | 90             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | 2764I                   | <a href="#">Samples</a> |
| TLV2764IPWG4     | ACTIVE        | TSSOP        | PW                 | 14   | 90             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | 2764I                   | <a href="#">Samples</a> |
| TLV2764IPWR      | ACTIVE        | TSSOP        | PW                 | 14   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | 2764I                   | <a href="#">Samples</a> |
| TLV2764IPWRG4    | ACTIVE        | TSSOP        | PW                 | 14   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | 2764I                   | <a href="#">Samples</a> |
| TLV2765CD        | ACTIVE        | SOIC         | D                  | 16   | 40             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | TLV2765C                | <a href="#">Samples</a> |
| TLV2765CDR       | ACTIVE        | SOIC         | D                  | 16   | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | TLV2765C                | <a href="#">Samples</a> |
| TLV2765ID        | ACTIVE        | SOIC         | D                  | 16   | 40             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | TLV2765I                | <a href="#">Samples</a> |
| TLV2765IDG4      | ACTIVE        | SOIC         | D                  | 16   | 40             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | TLV2765I                | <a href="#">Samples</a> |
| TLV2765IDR       | ACTIVE        | SOIC         | D                  | 16   | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | TLV2765I                | <a href="#">Samples</a> |
| TLV2765IPW       | ACTIVE        | TSSOP        | PW                 | 16   | 90             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | 2765I                   | <a href="#">Samples</a> |
| TLV2765IPWG4     | ACTIVE        | TSSOP        | PW                 | 16   | 90             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | 2765I                   | <a href="#">Samples</a> |
| TLV2765IPWR      | ACTIVE        | TSSOP        | PW                 | 16   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | 2765I                   | <a href="#">Samples</a> |
| TLV2765IPWRG4    | ACTIVE        | TSSOP        | PW                 | 16   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | 2765I                   | <a href="#">Samples</a> |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

---

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

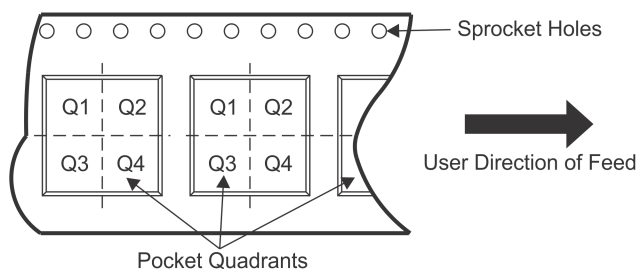
<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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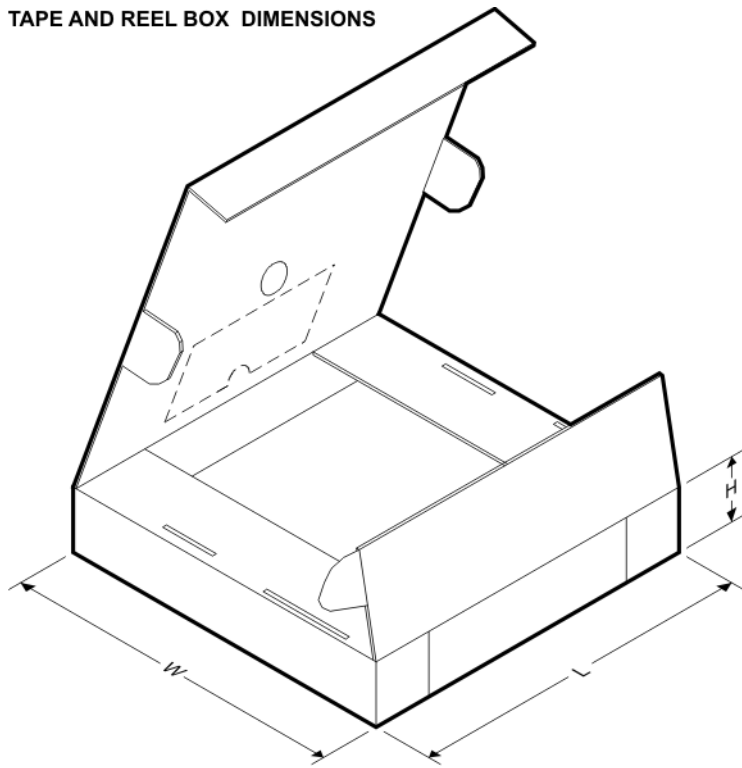
**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TLV2760IDBVR | SOT-23       | DBV             | 6    | 3000 | 180.0              | 9.0                | 3.15    | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| TLV2760IDBVT | SOT-23       | DBV             | 6    | 250  | 180.0              | 9.0                | 3.15    | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| TLV2761IDBVR | SOT-23       | DBV             | 5    | 3000 | 180.0              | 9.0                | 3.15    | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| TLV2761IDBVT | SOT-23       | DBV             | 5    | 250  | 180.0              | 9.0                | 3.15    | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| TLV2762CDGKR | VSSOP        | DGK             | 8    | 2500 | 330.0              | 12.4               | 5.3     | 3.4     | 1.4     | 8.0     | 12.0   | Q1            |
| TLV2762CDR   | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| TLV2762IDGKR | VSSOP        | DGK             | 8    | 2500 | 330.0              | 12.4               | 5.3     | 3.4     | 1.4     | 8.0     | 12.0   | Q1            |
| TLV2762IDGKR | VSSOP        | DGK             | 8    | 2500 | 330.0              | 12.4               | 5.3     | 3.4     | 1.4     | 8.0     | 12.0   | Q1            |
| TLV2762IDR   | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| TLV2763CDR   | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| TLV2763IDGSR | VSSOP        | DGS             | 10   | 2500 | 330.0              | 12.4               | 5.3     | 3.4     | 1.4     | 8.0     | 12.0   | Q1            |
| TLV2763IDGSR | VSSOP        | DGS             | 10   | 2500 | 330.0              | 12.4               | 5.3     | 3.4     | 1.4     | 8.0     | 12.0   | Q1            |
| TLV2764CDR   | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| TLV2764IDR   | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| TLV2764IPWR  | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| TLV2765CDR   | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| TLV2765IDR   | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| TLV2765IPWR  | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TLV2760IDBVR | SOT-23       | DBV             | 6    | 3000 | 182.0       | 182.0      | 20.0        |
| TLV2760IDBVT | SOT-23       | DBV             | 6    | 250  | 182.0       | 182.0      | 20.0        |
| TLV2761IDBVR | SOT-23       | DBV             | 5    | 3000 | 182.0       | 182.0      | 20.0        |
| TLV2761IDBVT | SOT-23       | DBV             | 5    | 250  | 182.0       | 182.0      | 20.0        |
| TLV2762CDGKR | VSSOP        | DGK             | 8    | 2500 | 364.0       | 364.0      | 27.0        |
| TLV2762CDR   | SOIC         | D               | 8    | 2500 | 340.5       | 338.1      | 20.6        |
| TLV2762IDGKR | VSSOP        | DGK             | 8    | 2500 | 364.0       | 364.0      | 27.0        |
| TLV2762IDGKR | VSSOP        | DGK             | 8    | 2500 | 358.0       | 335.0      | 35.0        |
| TLV2762IDR   | SOIC         | D               | 8    | 2500 | 340.5       | 338.1      | 20.6        |
| TLV2763CDR   | SOIC         | D               | 14   | 2500 | 367.0       | 367.0      | 38.0        |
| TLV2763IDGSR | VSSOP        | DGS             | 10   | 2500 | 358.0       | 335.0      | 35.0        |
| TLV2763IDGSR | VSSOP        | DGS             | 10   | 2500 | 366.0       | 364.0      | 50.0        |
| TLV2764CDR   | SOIC         | D               | 14   | 2500 | 333.2       | 345.9      | 28.6        |
| TLV2764IDR   | SOIC         | D               | 14   | 2500 | 333.2       | 345.9      | 28.6        |
| TLV2764IPWR  | TSSOP        | PW              | 14   | 2000 | 367.0       | 367.0      | 35.0        |
| TLV2765CDR   | SOIC         | D               | 16   | 2500 | 333.2       | 345.9      | 28.6        |
| TLV2765IDR   | SOIC         | D               | 16   | 2500 | 333.2       | 345.9      | 28.6        |
| TLV2765IPWR  | TSSOP        | PW              | 16   | 2000 | 367.0       | 367.0      | 35.0        |

P (R-PDIP-T8)

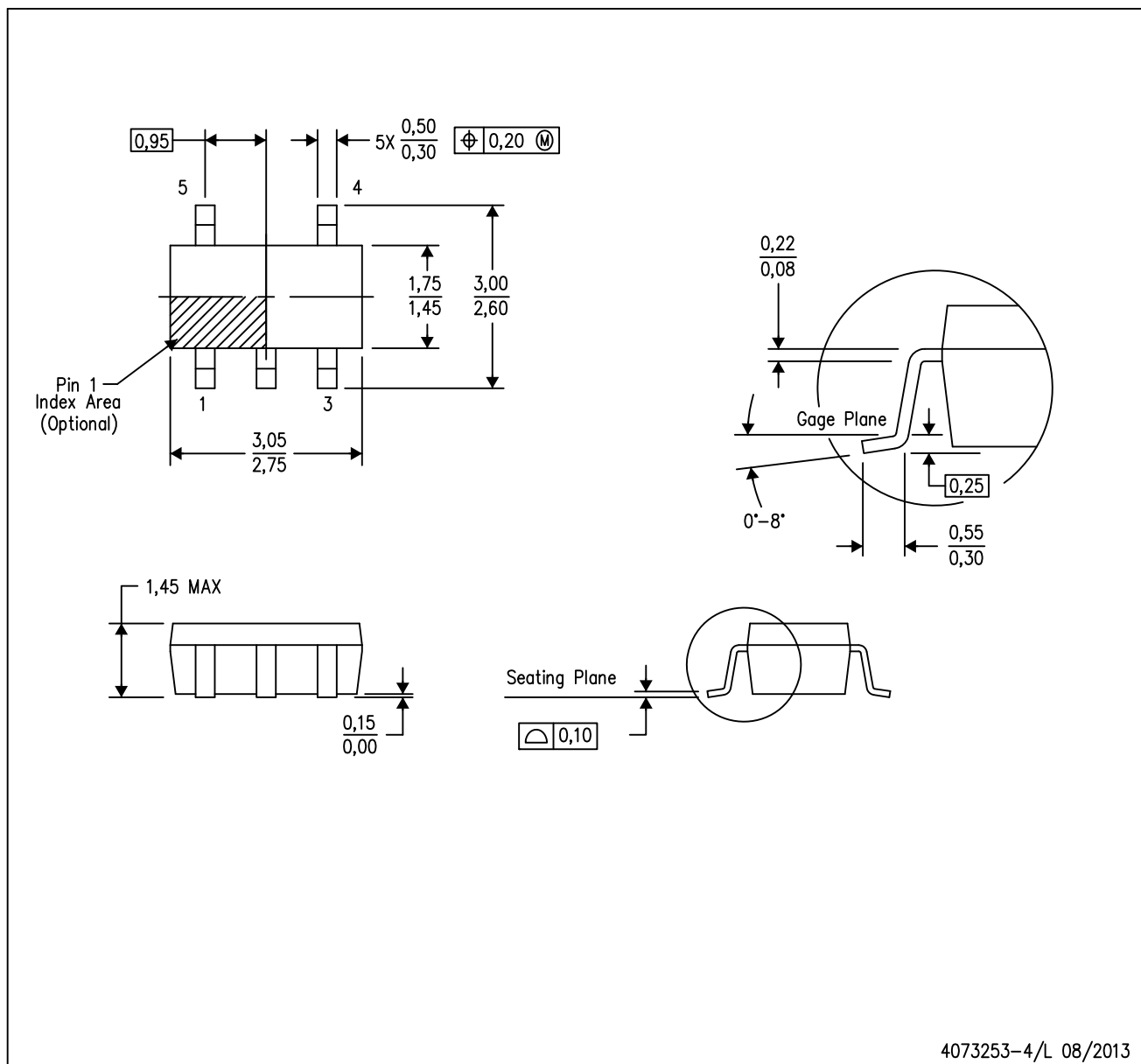
PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

DBV (R-PDSO-G5)

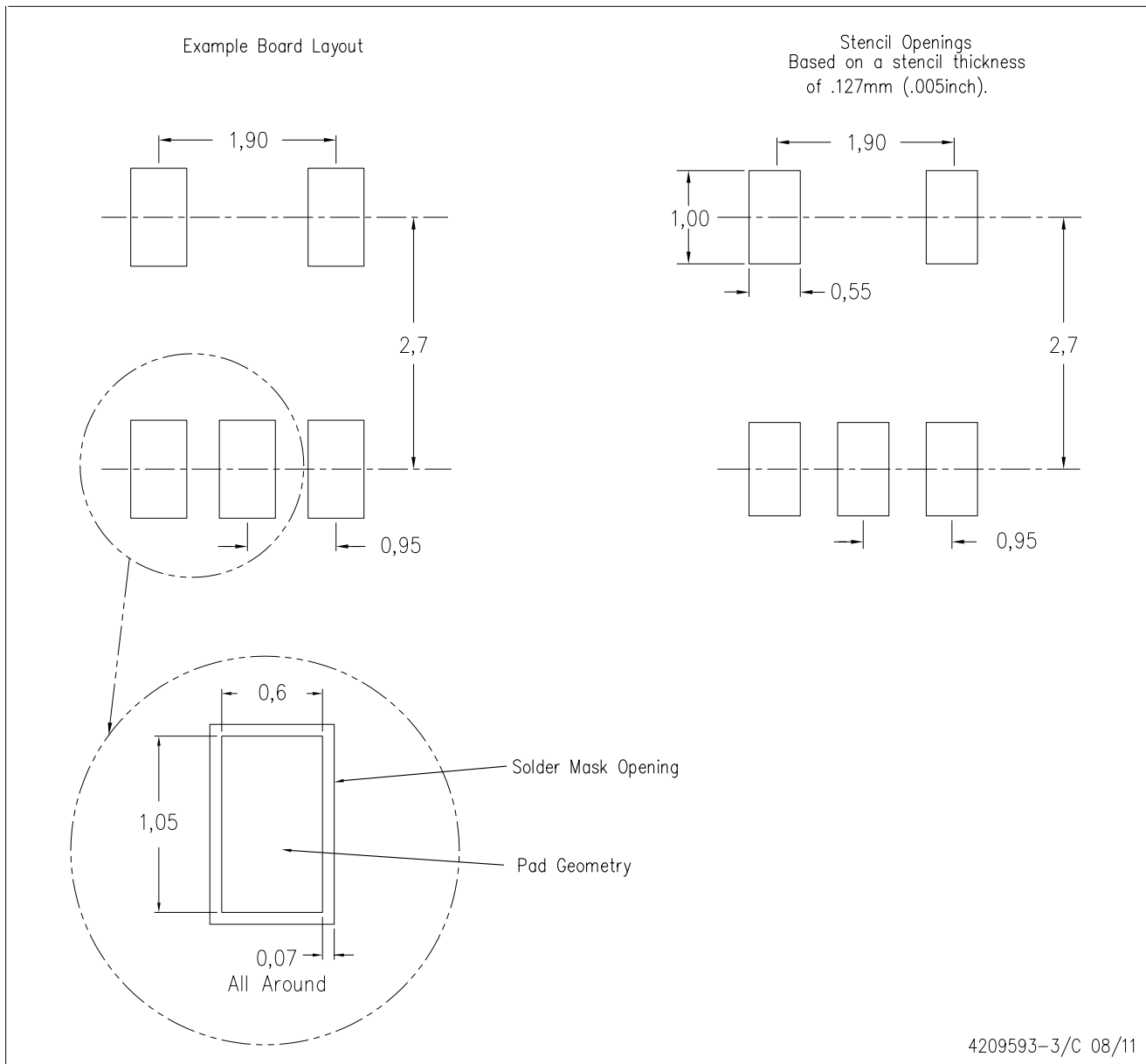
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

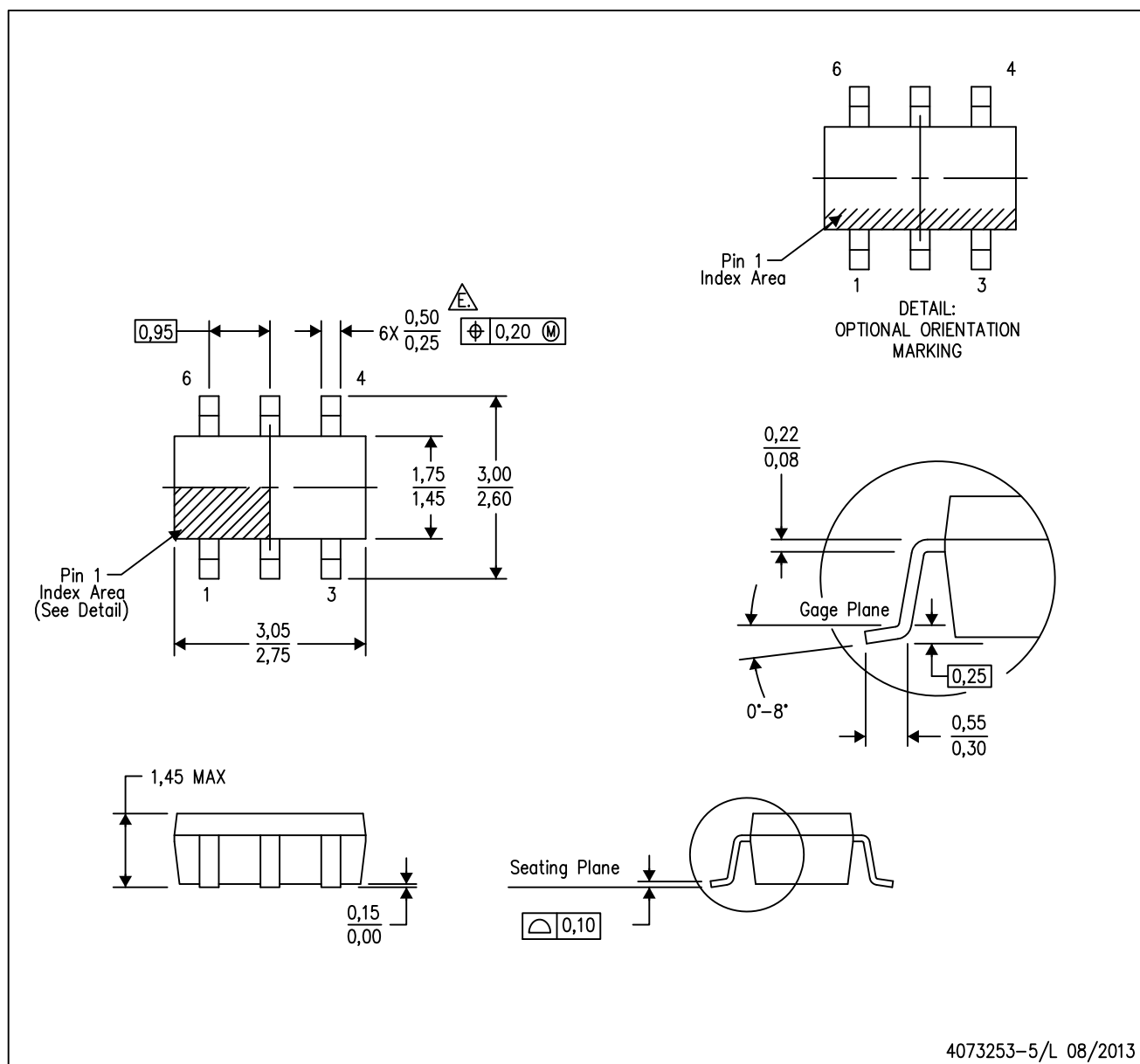
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DBV (R-PDSO-G6)

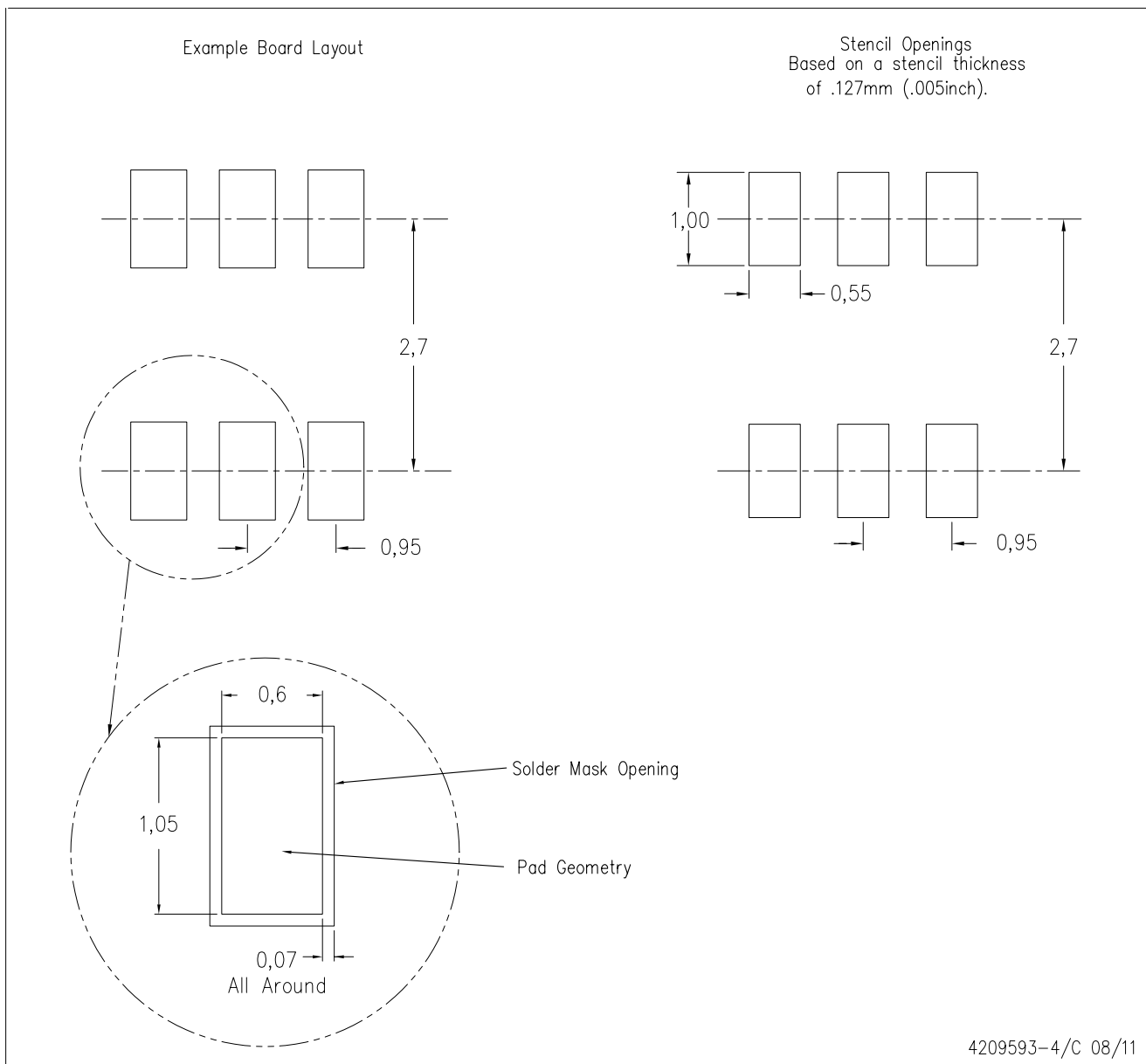
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
  - Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DBV (R-PDSO-G6)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

## DGK (S-PDSO-G8)

## PLASTIC SMALL-OUTLINE PACKAGE

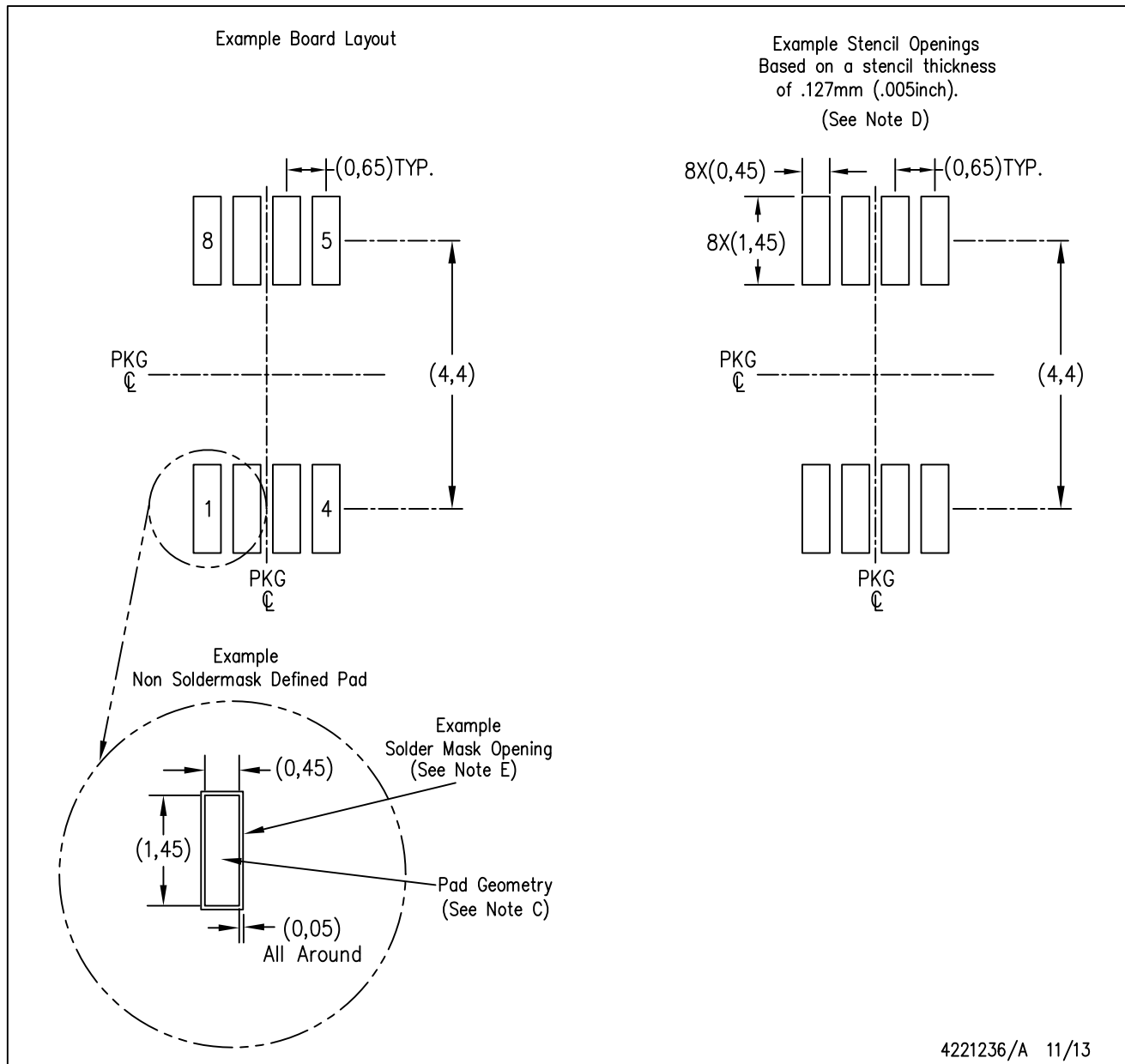


## NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGK (S-PDSO-G8)

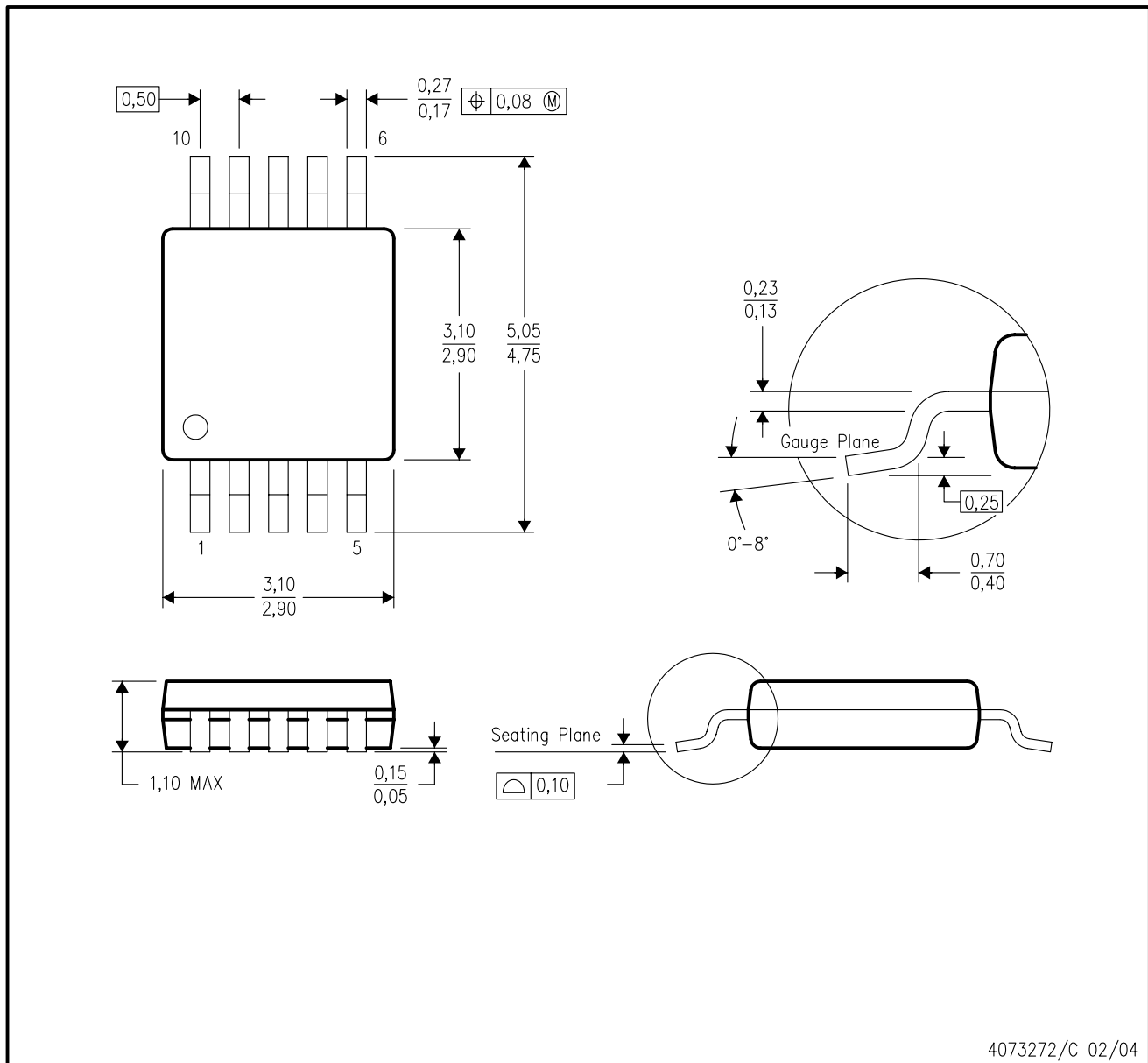
PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## DGS (S-PDSO-G10)

## PLASTIC SMALL-OUTLINE PACKAGE

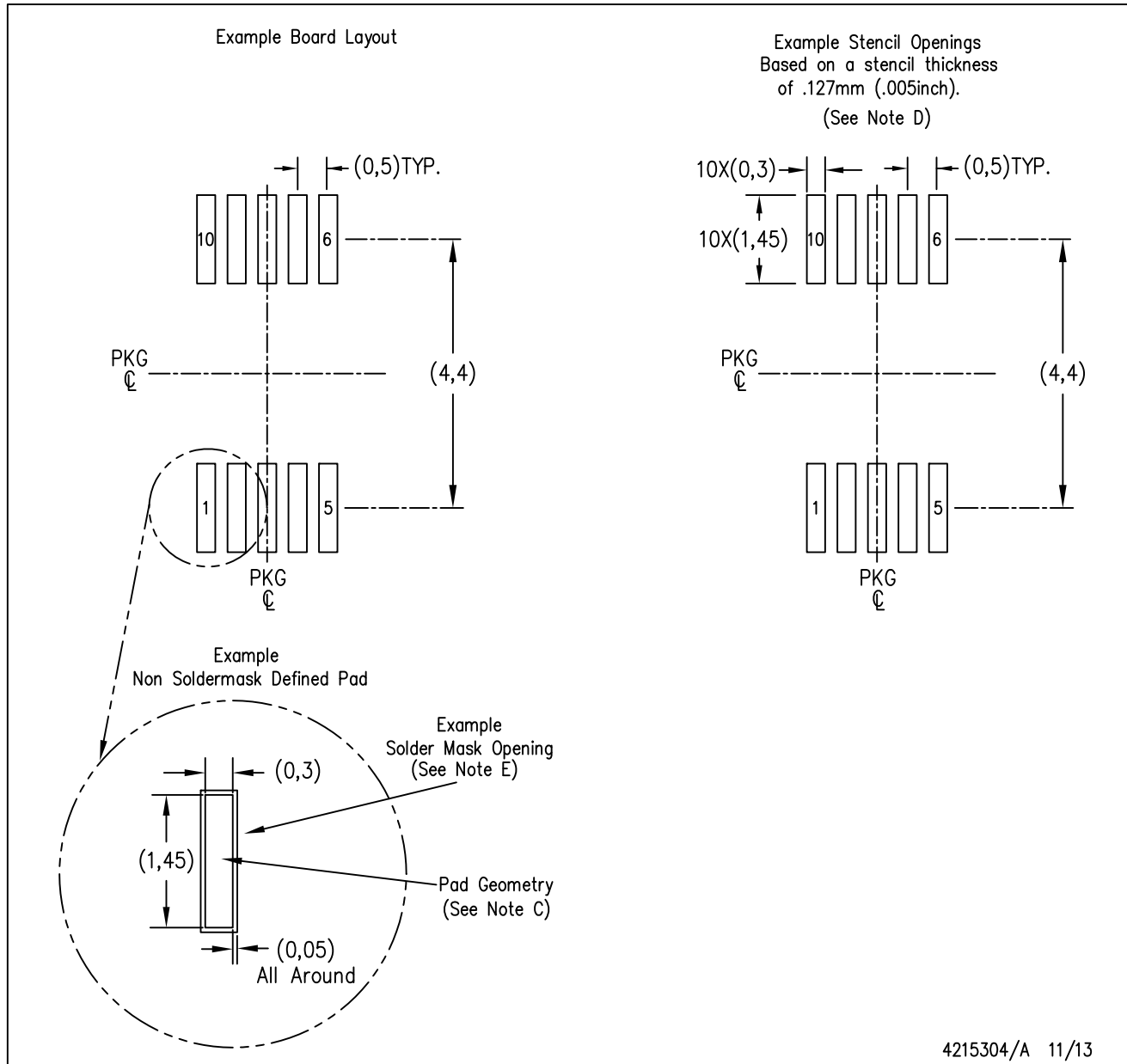


4073272/C 02/04

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion.
  - Falls within JEDEC MO-187 variation BA.

DGS (S-PDSO-G10)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

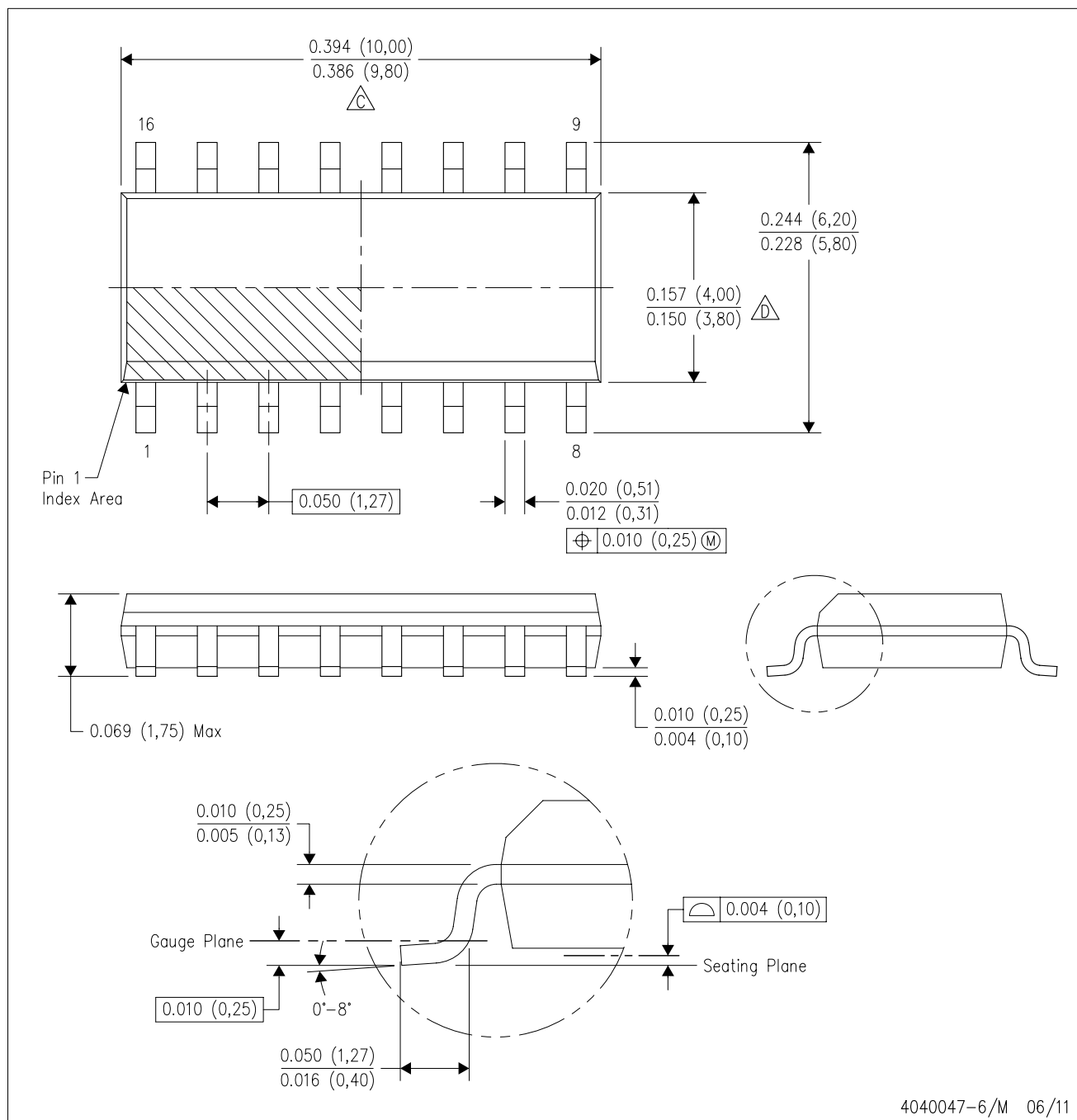
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G16)

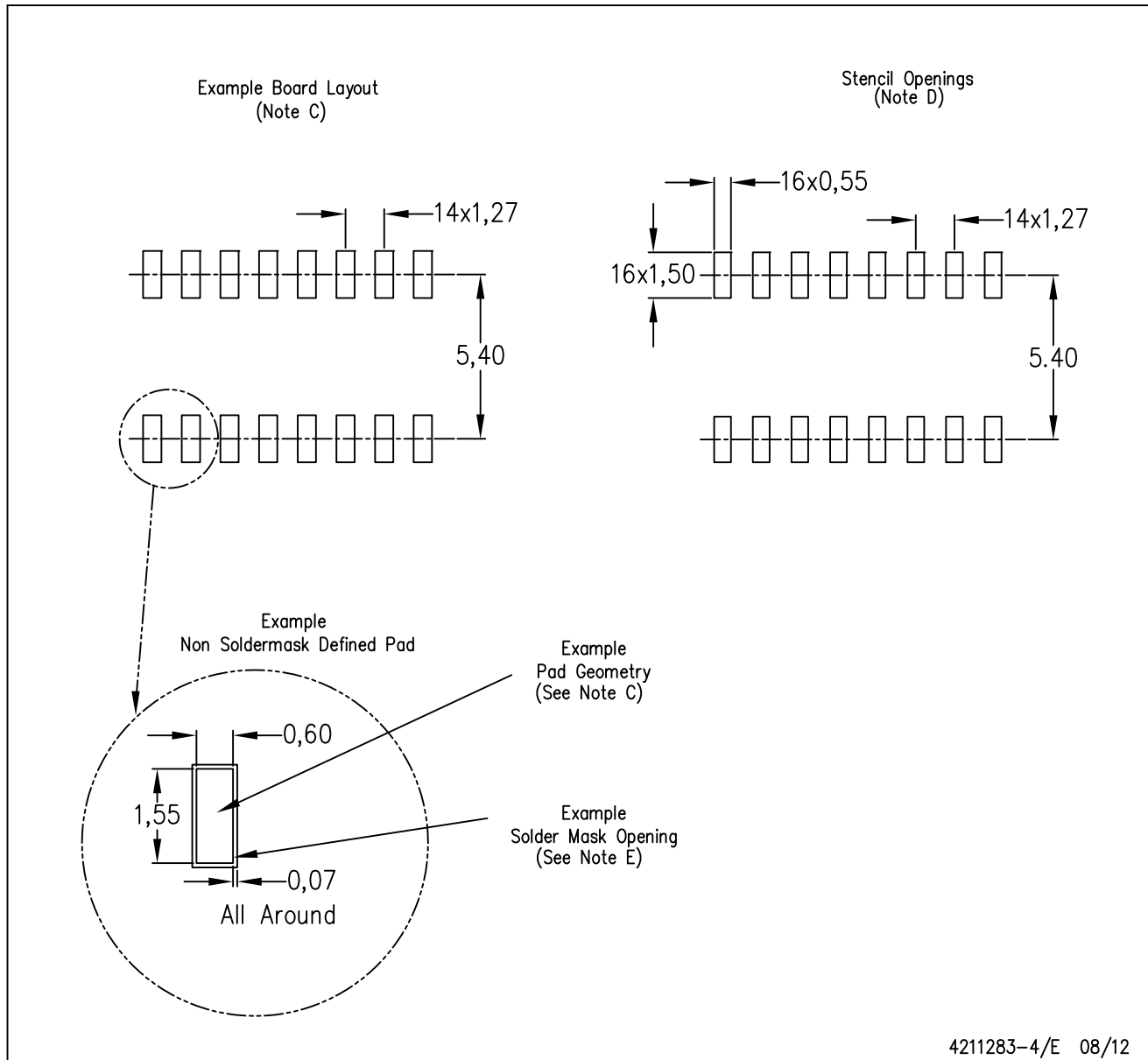
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

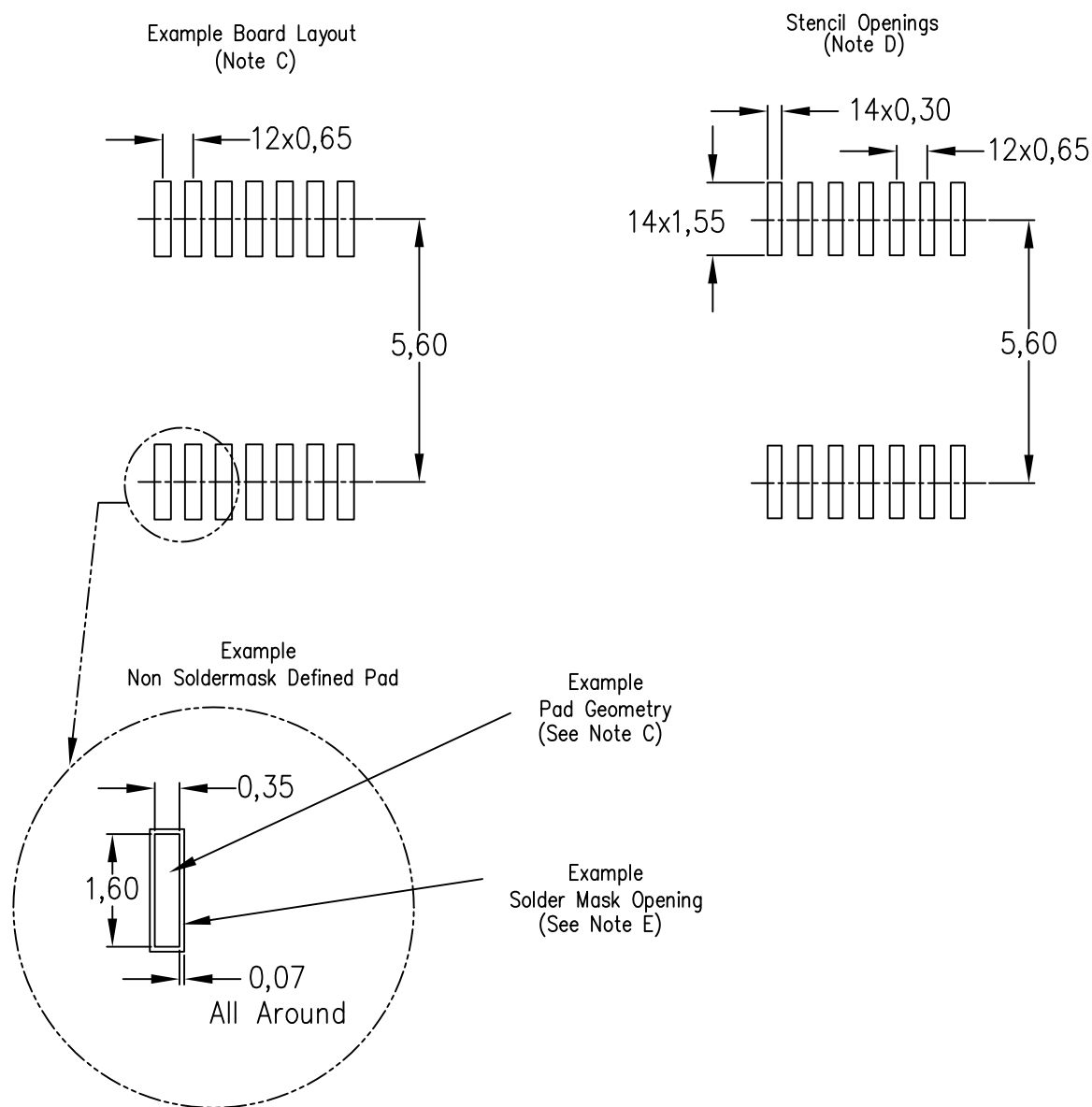


- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE





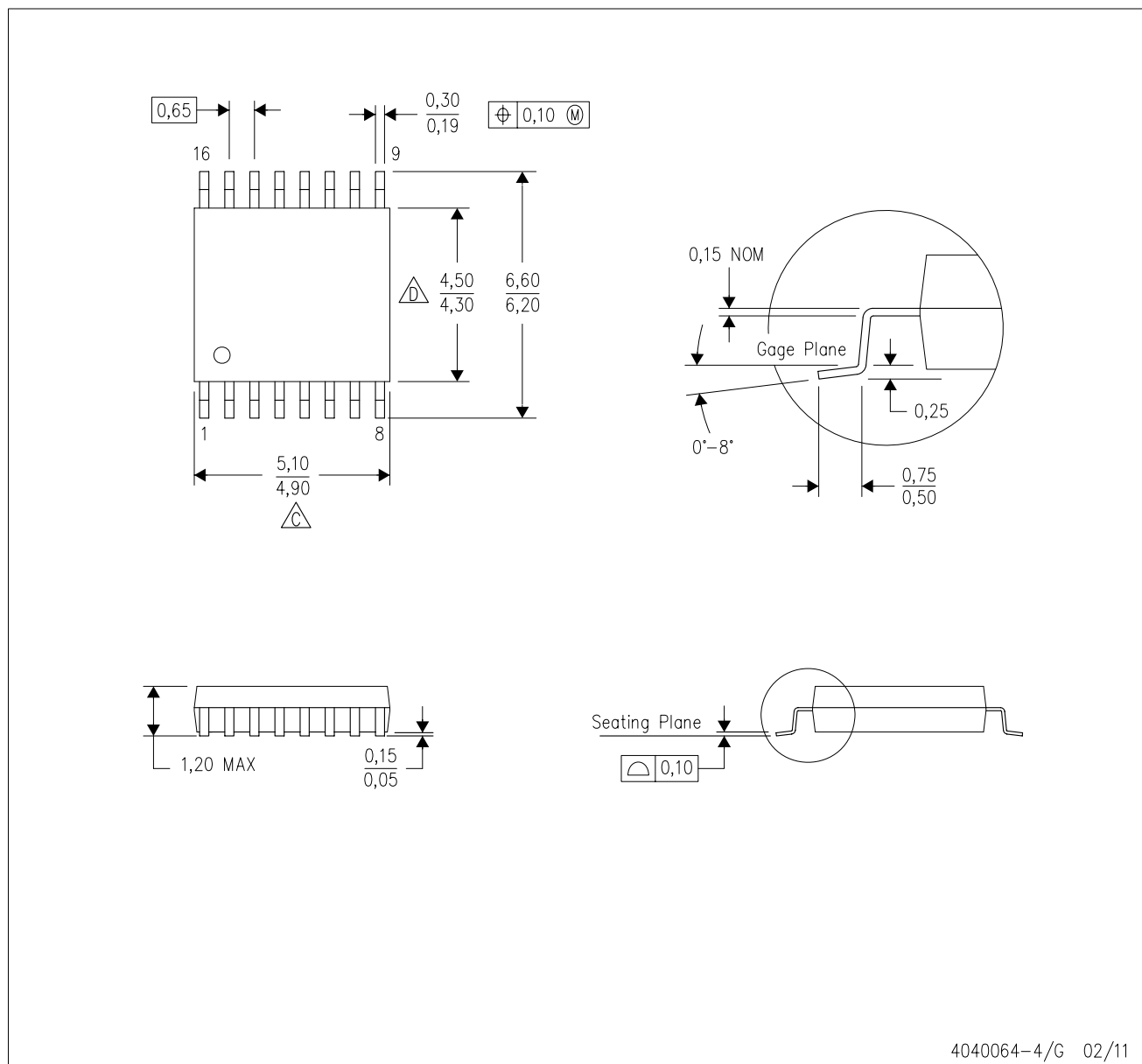
4211284-2/F 12/12

NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

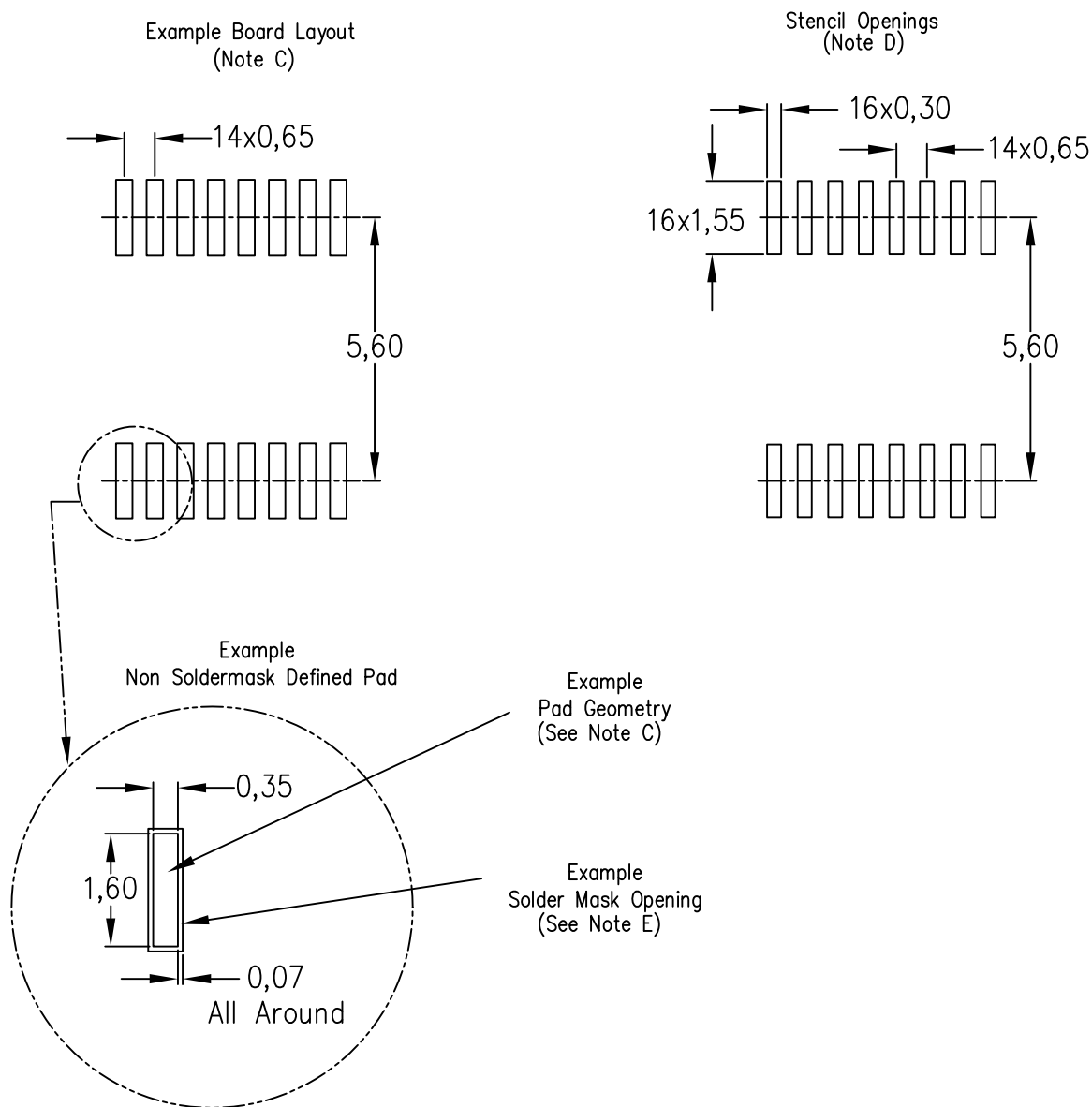


4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

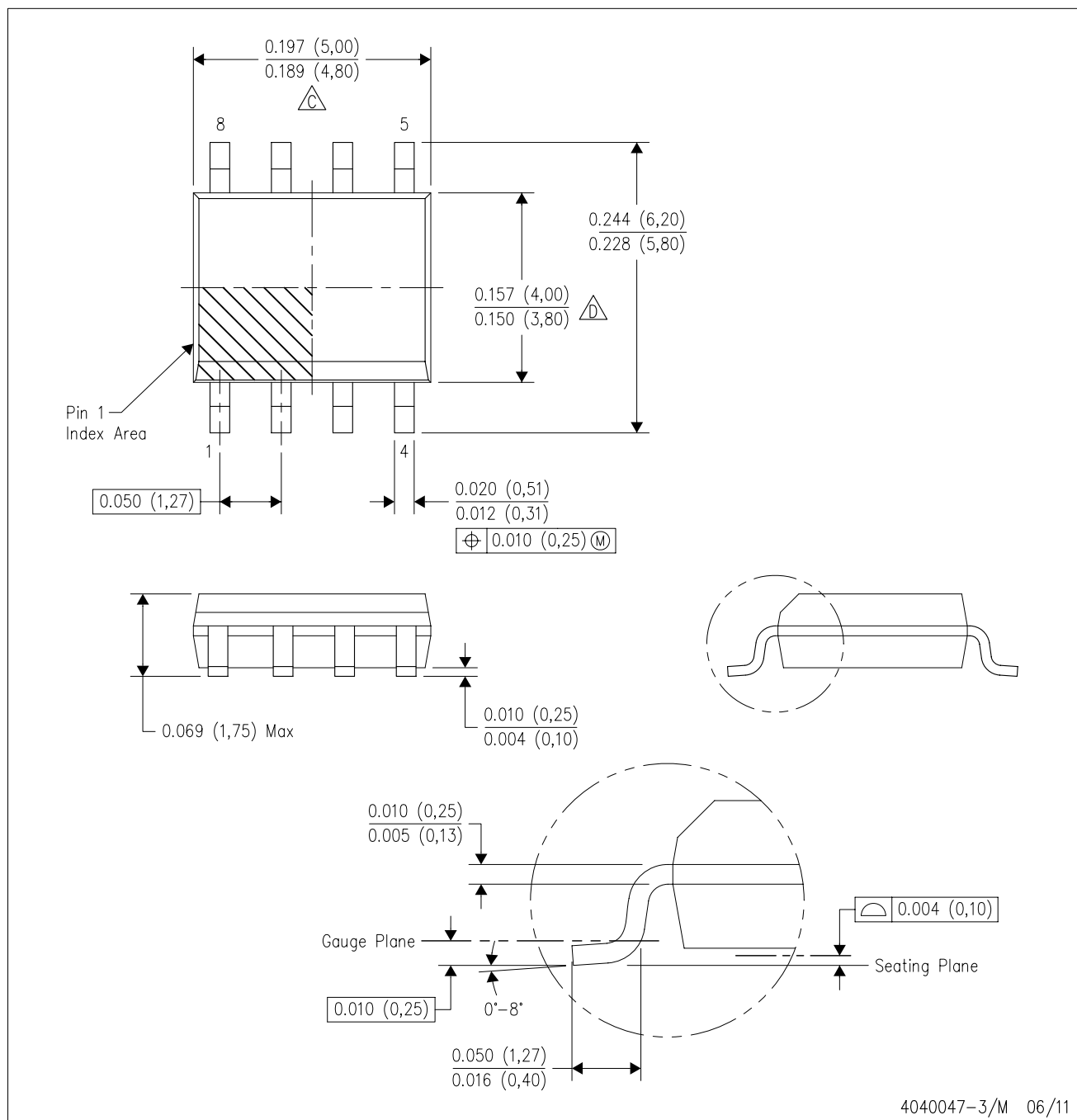


4211284-3/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8)

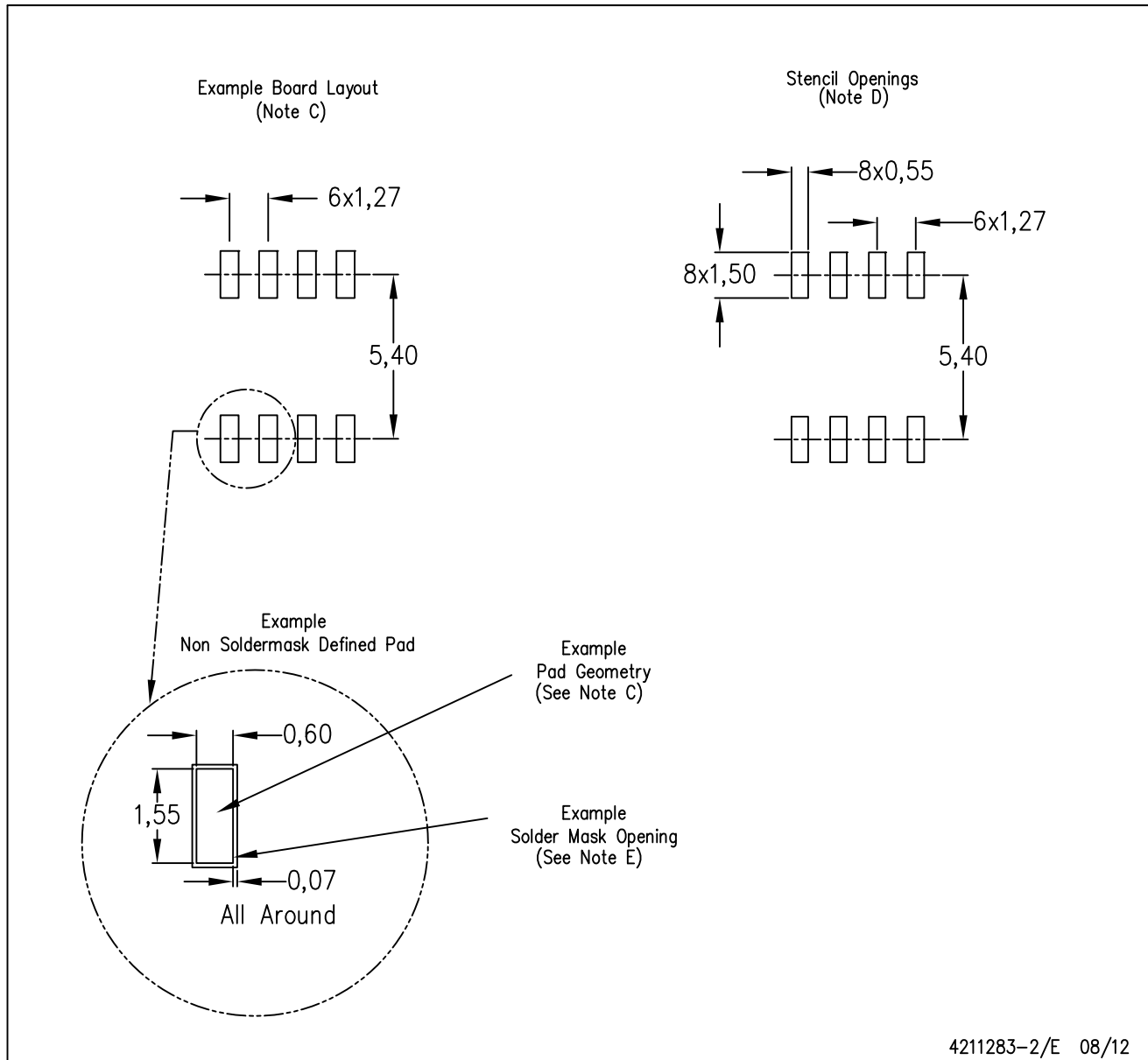
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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| Computers and Peripherals     | <a href="http://www.ti.com/computers">www.ti.com/computers</a>                           |
| Consumer Electronics          | <a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>                   |
| Energy and Lighting           | <a href="http://www.ti.com/energy">www.ti.com/energy</a>                                 |
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