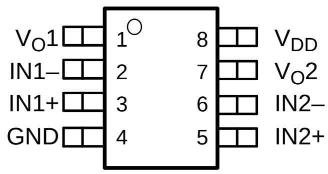
# 150-mW STEREO AUDIO POWER AMPLIFIER

## FEATURES

- **150-mW Stereo Output**
- **Wide Range of Supply Voltages**
  - **– Fully Specified for 3.3-V and 5-V Operation**
  - **– Operational From 2.5 V to 5.5 V**
- **Thermal and Short-Circuit Protection**
- **Surface-Mount Packaging**
  - **– PowerPAD™ MSOP**
  - **– SOIC**
- **Standard Operational Amplifier Pinout**

**D OR DGN PACKAGE**
**(TOP VIEW)**

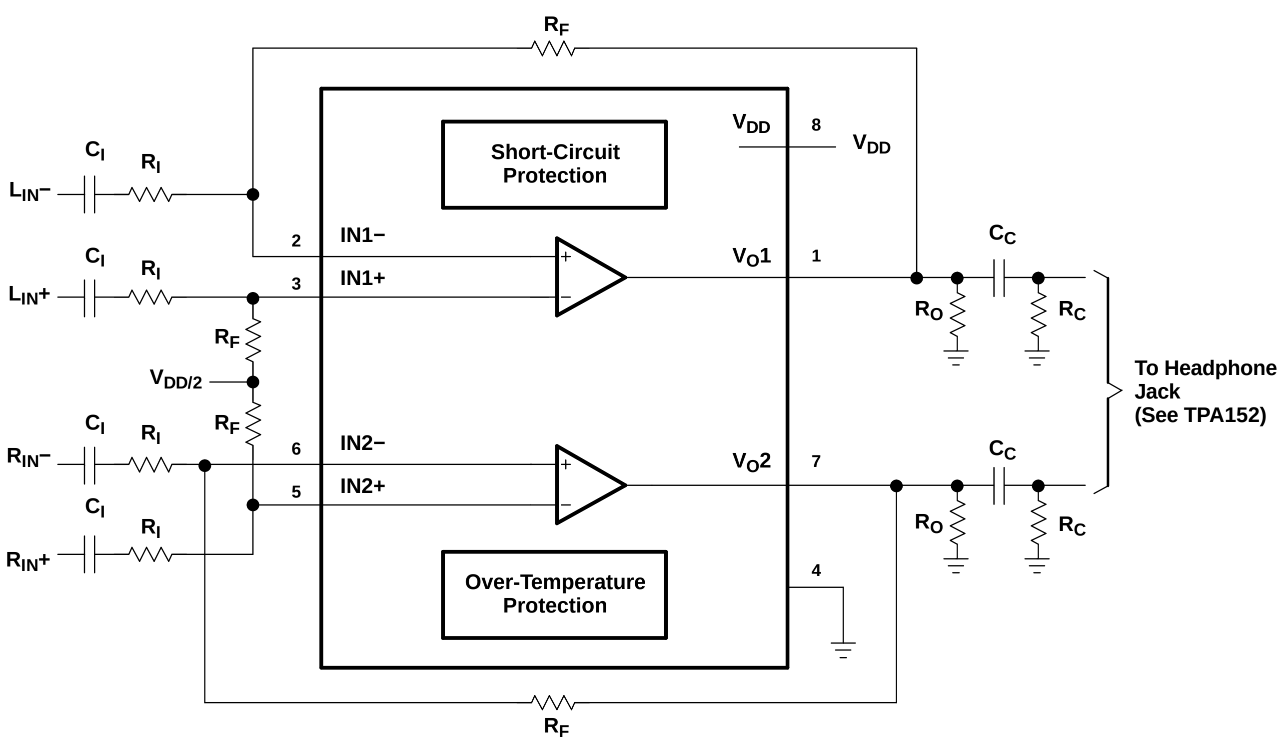



## DESCRIPTION

The TPA112 is a stereo audio power amplifier packaged in an 8-pin PowerPAD™ MSOP package capable of delivering 150 mW of continuous RMS power per channel into 8-Ω loads. Amplifier gain is externally configured by means of two resistors per input channel and does not require external compensation for settings of 1 to 10.

THD+N when driving an 8-Ω load from 5 V is 0.1% at 1 kHz, and less than 2% across the audio band of 20 Hz to 20 kHz. For 32-Ω loads, the THD+N is reduced to less than 0.06% at 1 kHz, and is less than 1% across the audio band of 20 Hz to 20 kHz. For 10-kΩ loads, the THD+N performance is 0.01% at 1 kHz, and less than 0.02% across the audio band of 20 Hz to 20 kHz.

## FUNCTIONAL BLOCK DIAGRAM




Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## AVAILABLE OPTIONS

| $T_A$ | PACKAGED DEVICES | | MSOP SYMBOLIZATION |
|---|---|---|---|
| | SMALL OUTLINE(1) (D) | MSOP(1) (DGN) | |
| –40°C to 85°C | TPA112D | TPA112DGN | TI AAD |

(1) The D and DGN packages are available in left-ended tape and reel only (e.g., TPA112DR, TPA112DGNR).

## Terminal Functions

| TERMINAL NAME | TERMINAL NO. | I/O | DESCRIPTION |
|---|---|---|---|
| GND | 4 | I | GND is the ground connection. |
| IN1- | 2 | I | IN1- is the inverting input for channel 1. |
| IN1+ | 3 | I | IN1+ is the noninverting input for channel 1. |
| IN2- | 6 | I | IN2- is the inverting input for channel 2. |
| IN2+ | 5 | I | IN2+ is the noninverting input for channel 2. |
| $V_{DD}$ | 8 | I | $V_{DD}$ is the supply voltage terminal. |
| $V_O1$ | 1 | O | $V_O1$ is the audio output for channel 1. |
| $V_O2$ | 7 | O | $V_O2$ is the audio output for channel 2. |

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

| | | UNIT |
|---|---|---|
| $V_{DD}$ | Supply voltage | 6 V |
| $V_I$ | Differential input voltage | –0.3 V to $V_{DD}$ + 0.3 V |
| $I_I$ | Input current | ±2.5 µA |
| $I_O$ | Output current | ±250 mA |
| | Continuous total power dissipation | Internally llimited |
| $T_J$ | Operating junction temperature range | –40°C to 150°C |
| $T_{stg}$ | Storage temperature range | –65°C to 150°C |
| | Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## DISSIPATION RATING TABLE

| PACKAGE | $T_A \leq 25°C$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25°C$ | $T_A = 70°C$ POWER RATING | $T_A = 85°C$ POWER RATING |
|---|---|---|---|---|
| D | 725 mW | 5.8 mW/°C | 464 mW | 377 mW |
| DGN | 2.14 W(1) | 17.1 mW/°C | 1.37 W | 1.11 W |

(1) See the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD,* of that document.

## RECOMMENDED OPERATING CONDITIONS

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 2.5 | 5.5 | V |
| $T_A$ | Operating free-air temperature | –40 | 85 | °C |

## DC ELECTRICAL CHARACTERISTICS

at $T_A$ = 25°C, $V_{DD}$ = 3.3 V

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OO}$ | Output offset voltage | | | | 10 | mV |
| PSRR | Power supply rejection ratio | $V_{DD}$ = 3.2 V to 3.4 V | | 83 | | dB |
| $I_{DD(q)}$ | Supply current | | | 1.5 | 3 | mA |
| $Z_I$ | Input impedance | | | > 1 | | MΩ |

## AC OPERATING CHARACTERISTICS

$V_{DD}$ = 3.3 V, $T_A$ = 25°C, $R_L$ = 8 Ω

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $P_O$ | Output power (each channel) | THD ≤ 0.1% | | 70 (1) | | mW |
| THD+N | Total harmonic distortion + noise | $P_O$ = 70 mW, 20 Hz–20 kHz | | 2% | | |
| $B_{OM}$ | Maximum output power BW | G = 10, THD < 5% | | > 20 | | kHz |
| | Phase margin | Open loop | | 58° | | |
| $S_{VRR}$ | Supply ripple rejection | f = 1 kHz | | 68 | | dB |
| | Channel/channel output separation | f = 1 kHz | | 86 | | dB |
| SNR | Signal-to-noise ratio | $P_O$ = 100 mW | | 100 | | dB |
| $V_n$ | Noise output voltage | | | 9.5 | | µV(rms) |

(1) Measured at 1 kHz

## DC ELECTRICAL CHARACTERISTICS

at $T_A$ = 25°C, $V_{DD}$ = 5 V

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OO}$ | Output offset voltage | | | | 10 | mV |
| PSRR | Power supply rejection ratio | $V_{DD}$ = 4.9 V to 5.1 V | | 76 | | dB |
| $I_{DD(q)}$ | Supply current | | | 1.5 | 3 | mA |
| $Z_I$ | Input impedance | | | > 1 | | MΩ |

## AC OPERATING CHARACTERISTICS

$V_{DD}$ = 5 V, $T_A$ = 25°C, $R_L$ = 8 Ω

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $P_O$ | Output power (each channel) | THD ≤ 0.1% | | 70 (1) | | mW |
| THD+N | Total harmonic distortion + noise | $P_O$ = 150 mW, 20 Hz–20 kHz | | 2% | | |
| $B_{OM}$ | Maximum output power BW | G = 10, THD < 5% | | > 20 | | kHz |
| | Phase margin | Open loop | | 56° | | |
| $S_{VRR}$ | Supply ripple rejection | f = 1 kHz | | 68 | | dB |
| | Channel/channel output separation | f = 1 kHz | | 86 | | dB |
| SNR | Signal-to-noise ratio | $P_O$ = 150 mW | | 100 | | dB |
| $V_n$ | Noise output voltage | | | 9.5 | | µV(rms) |

(1) Measured at 1 kHz

## AC OPERATING CHARACTERISTICS

$V_{DD}$ = 3.3 V, $T_A$ = 25°C, $R_L$ = 32 Ω

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $P_O$ | Output power (each channel) | THD ≤ 0.1% | | 40 (1) | | mW |
| THD+N | Total harmonic distortion + noise | $P_O$ = 30 mW, 20 Hz–20 kHz | | 0.5% | | |
| $B_{OM}$ | Maximum output power BW | G = 10, THD < 2% | | > 20 | | kHz |
| | Phase margin | Open loop | | 58° | | |
| $S_{VRR}$ | Supply ripple rejection | f = 1 kHz | | 68 | | dB |
| | Channel/channel output separation | f = 1 kHz | | 86 | | dB |
| SNR | Signal-to-noise ratio | $P_O$ = 100 mW | | 100 | | dB |
| $V_n$ | Noise output voltage | | | 9.5 | | µV(rms) |

(1) Measured at 1 kHz

## AC OPERATING CHARACTERISTICS

$V_{DD}$ = 5 V, $T_A$ = 25°C, $R_L$ = 32 Ω

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $P_O$ | Output power (each channel) | THD ≤ 0.1% | | 40 (1) | | mW |
| THD+N | Total harmonic distortion + noise | $P_O$ = 60 mW, 20 Hz–20 kHz | | 0.4% | | |
| $B_{OM}$ | Maximum output power BW | G = 10, THD < 2% | | > 20 | | kHz |
| | Phase margin | Open loop | | 56° | | |
| $S_{VRR}$ | Supply ripple rejection | f = 1 kHz | | 68 | | dB |
| | Channel/channel output separation | f = 1 kHz | | 86 | | dB |
| SNR | Signal-to-noise ratio | $P_O$ = 150 mW | | 100 | | dB |
| $V_n$ | Noise output voltage | | | 9.5 | | µV(rms) |

(1) Measured at 1 kHz

# TYPICAL CHARACTERISTICS

## Table of Graphs

| | | | FIGURE |
|---|---|---|---|
| THD+N | Total harmonic distortion plus noise | vs Frequency | 1, 2, 4, 5, 7, 8, 10, 11, 13, 14, 16, 17, 34, 36 |
| | | vs Output power | 3, 6, 9, 12, 15, 18 |
| PSSR | Power supply rejection ratio | vs Frequency | 19, 20 |
| $V_n$ | Output noise voltage | vs Frequency | 21, 22 |
| | Crosstalk | vs Frequency | 23-26, 37, 38 |
| | Mute attenuation | vs Frequency | 27, 28 |
| | Open-loop gain | vs Frequency | 29, 30 |
| | Phase margin | vs Frequency | 29, 30 |
| | Phase | vs Frequency | 39-44 |
| | Output power | vs Load resistance | 31, 32 |
| $I_{CC}$ | Supply current | vs Supply voltage | 33 |
| SNR | Signal-to-noise ratio | vs Voltage gain | 35 |
| | Closed-loop gain | vs Frequency | 39-44 |
| | Power dissipation/amplifier | vs Output power | 45, 46 |

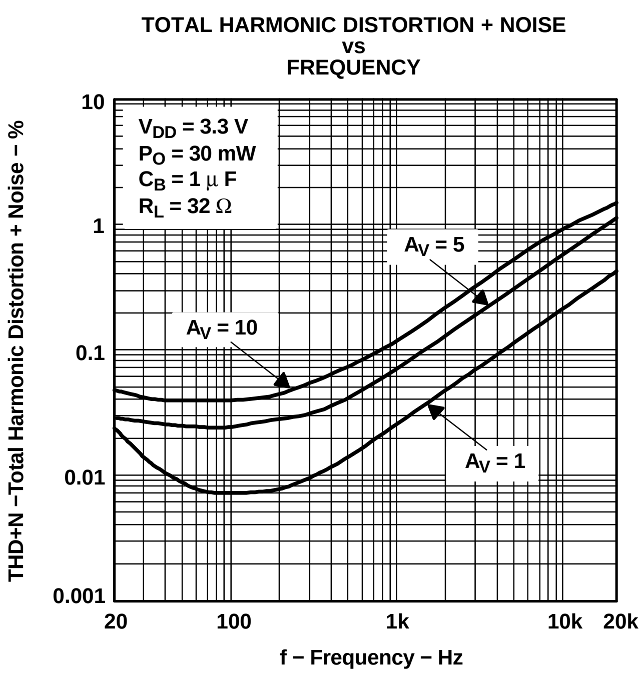



Figure 1.

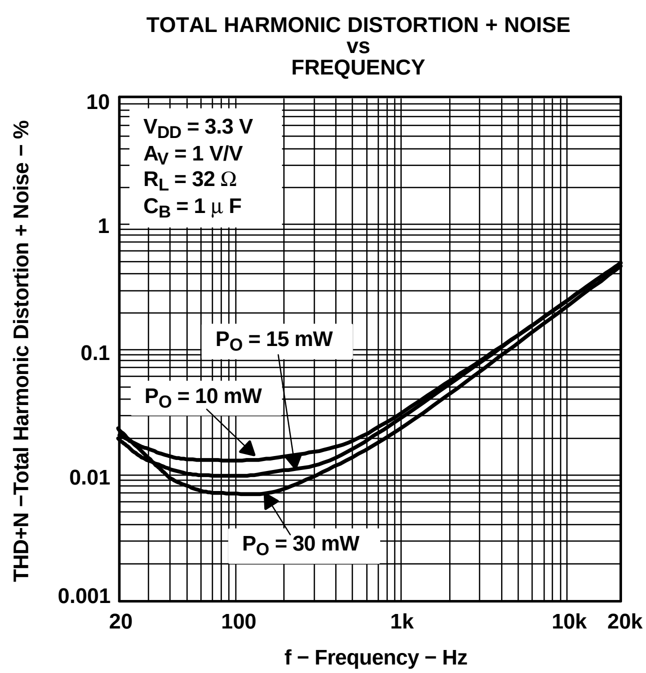



Figure 2.

**TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER**

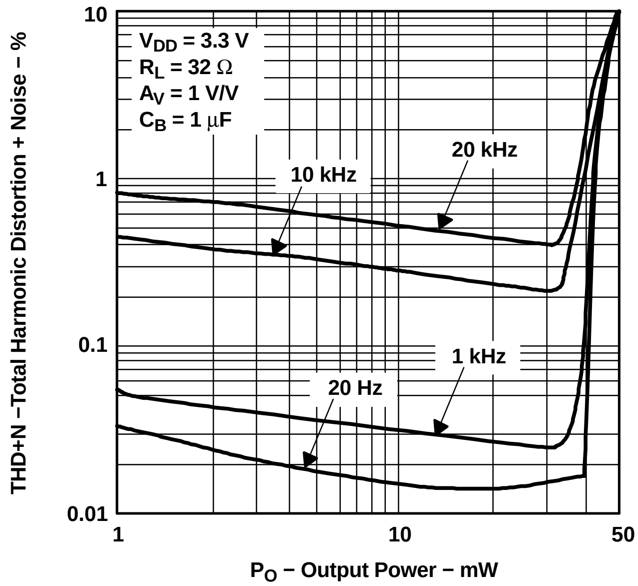



**Figure 3.**

**TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY**

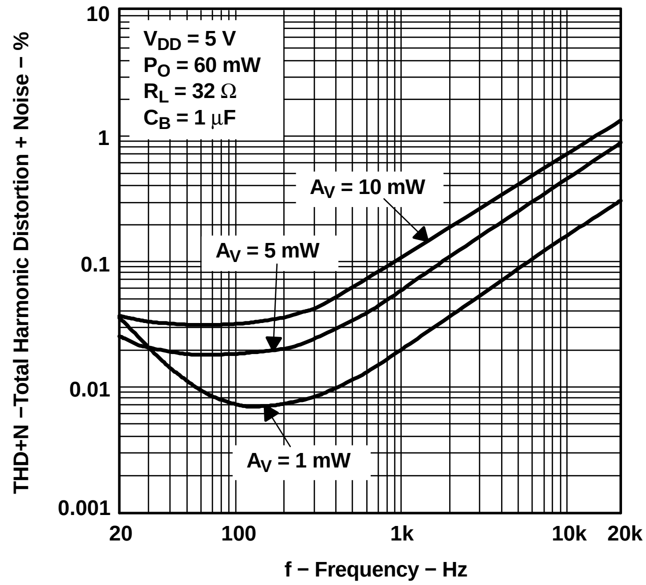



**Figure 4.**

**TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY**

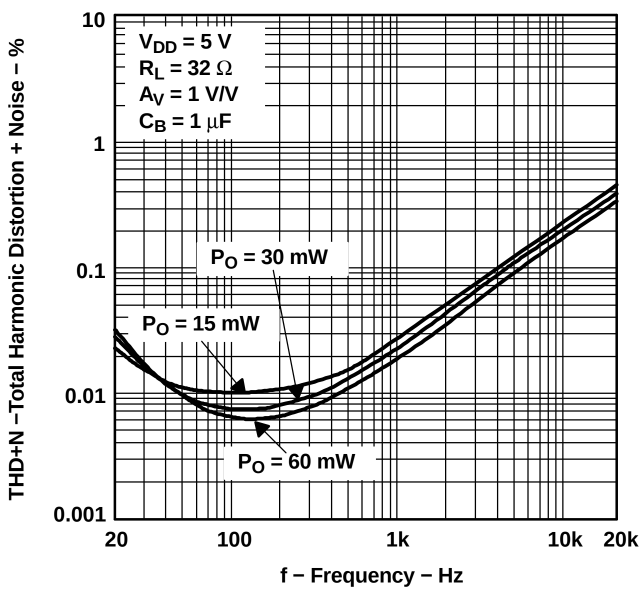



**Figure 5.**

**TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER**

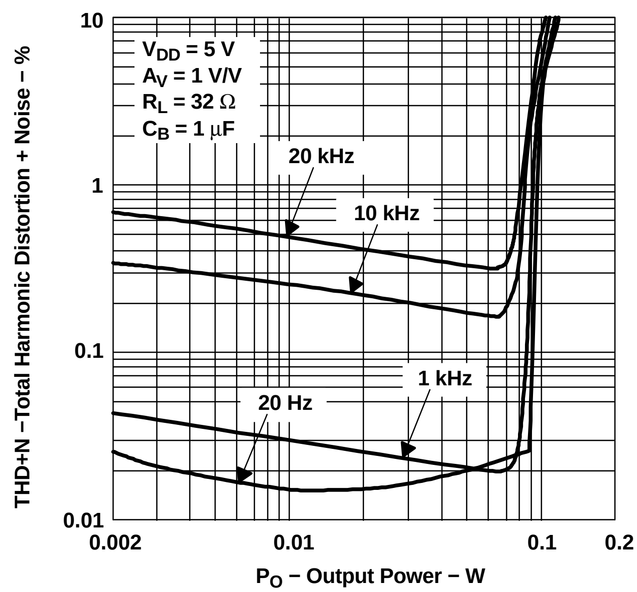



**Figure 6.**

**TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY**

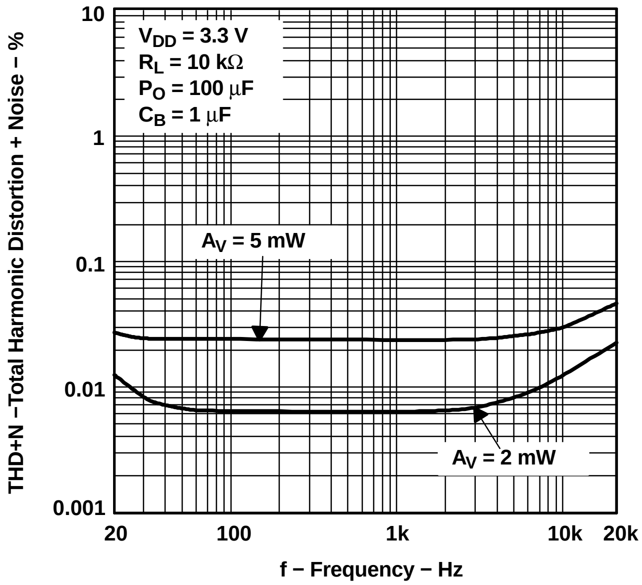



**Figure 7.**

**TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY**

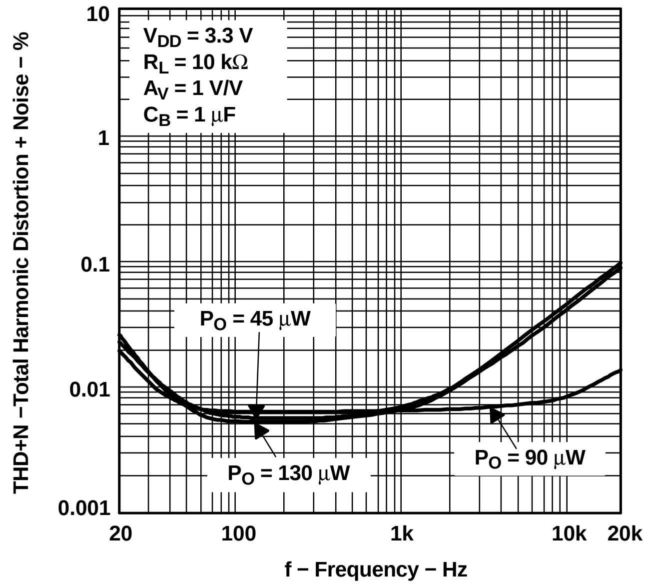



**Figure 8.**

**TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER**

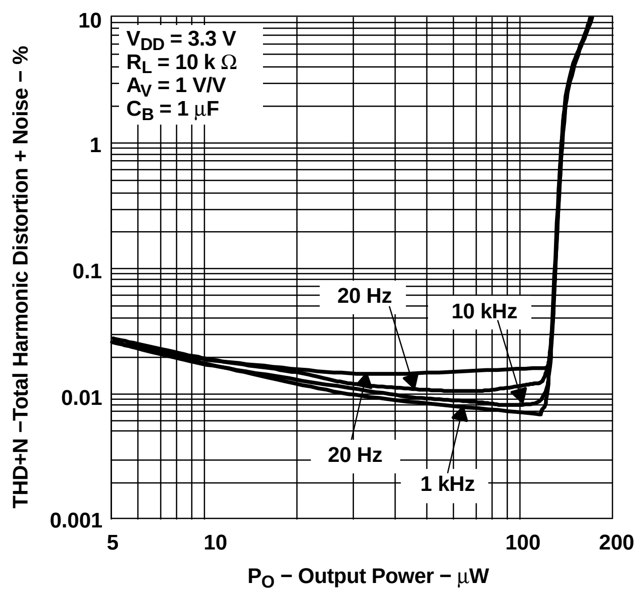



**Figure 9.**

**TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY**

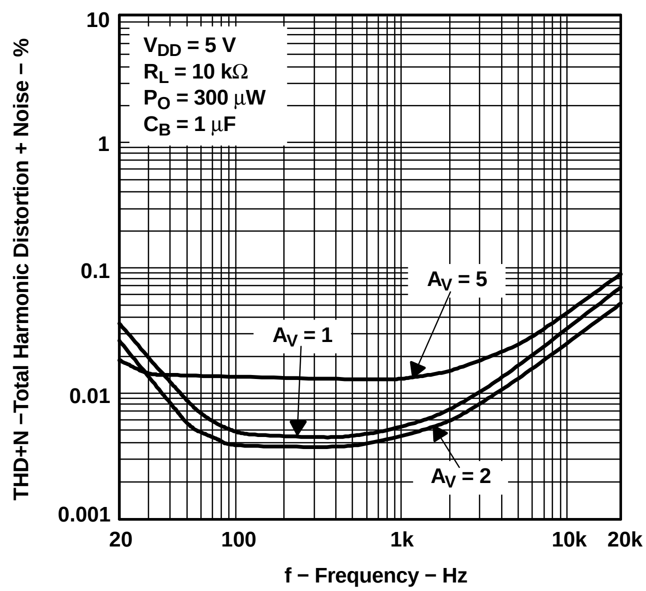



**Figure 10.**

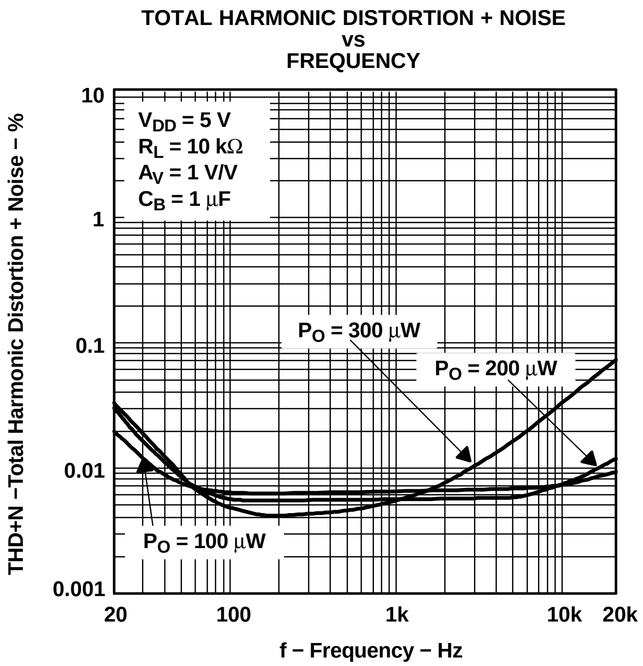



Figure 11.

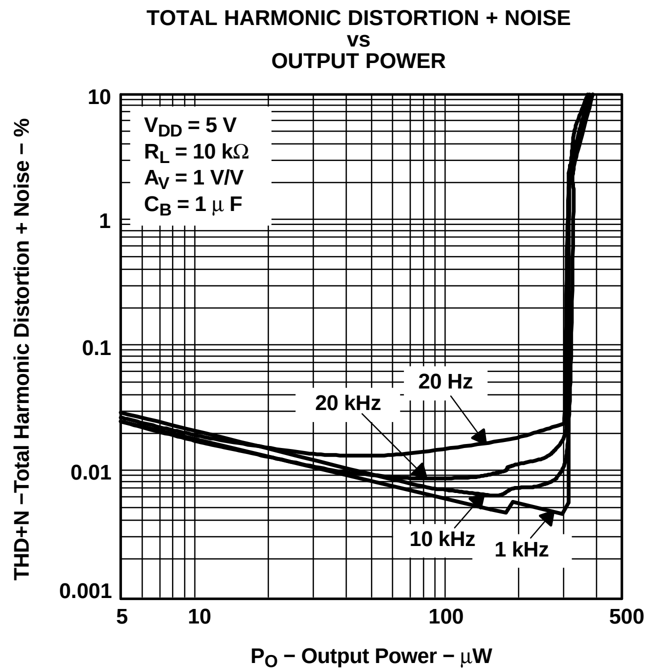



Figure 12.

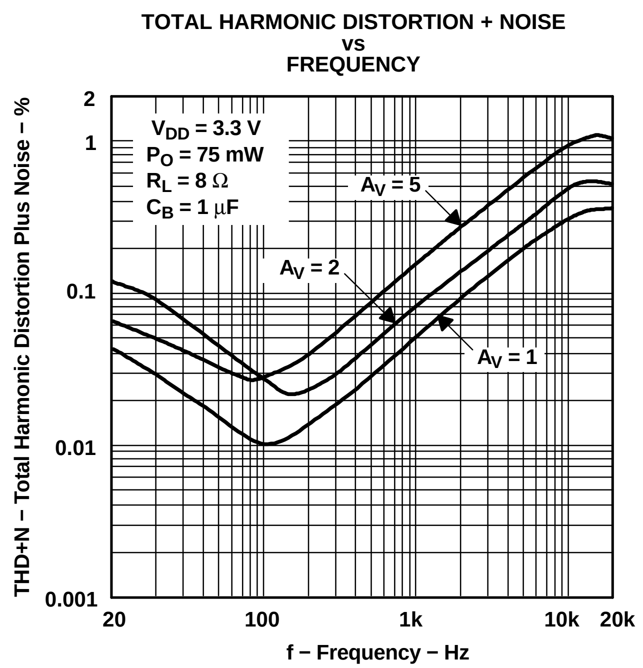



Figure 13.

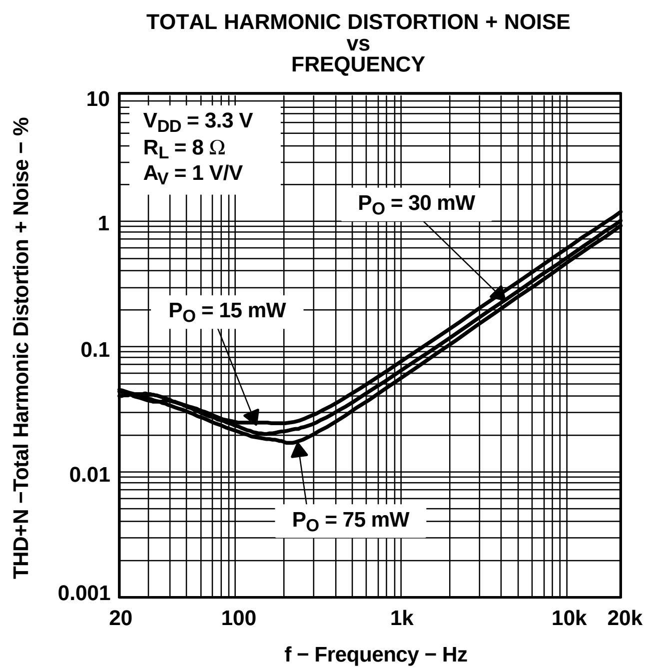



Figure 14.

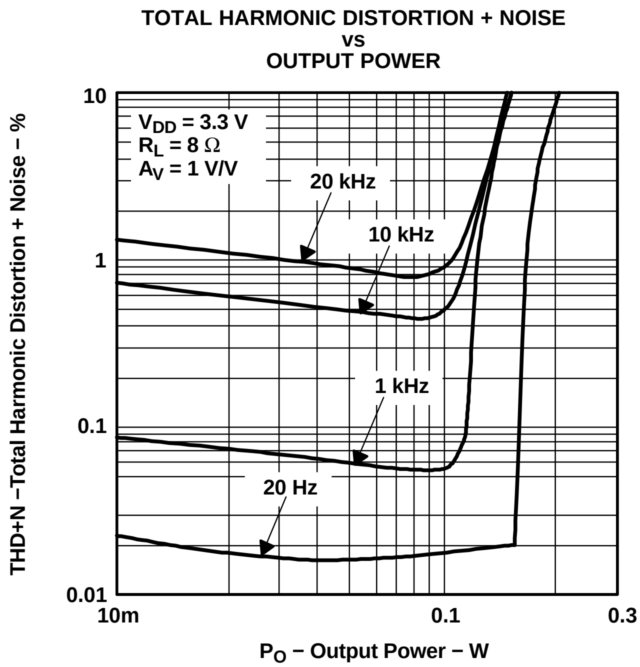



Figure 15.

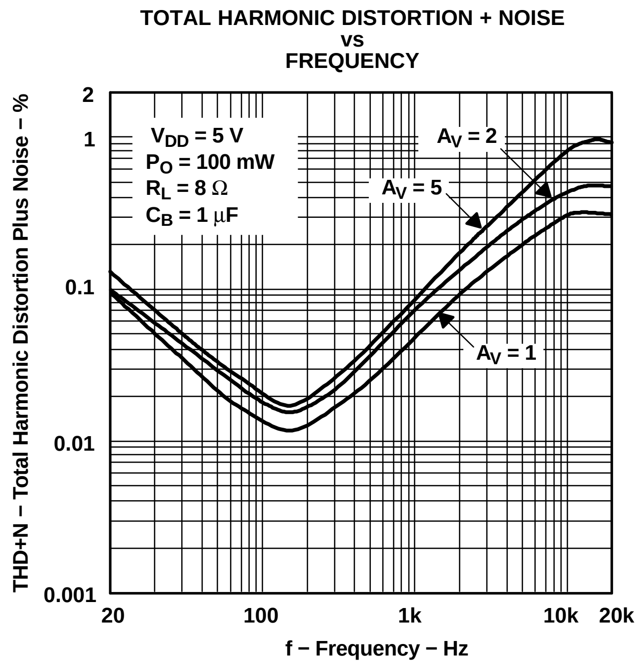



Figure 16.

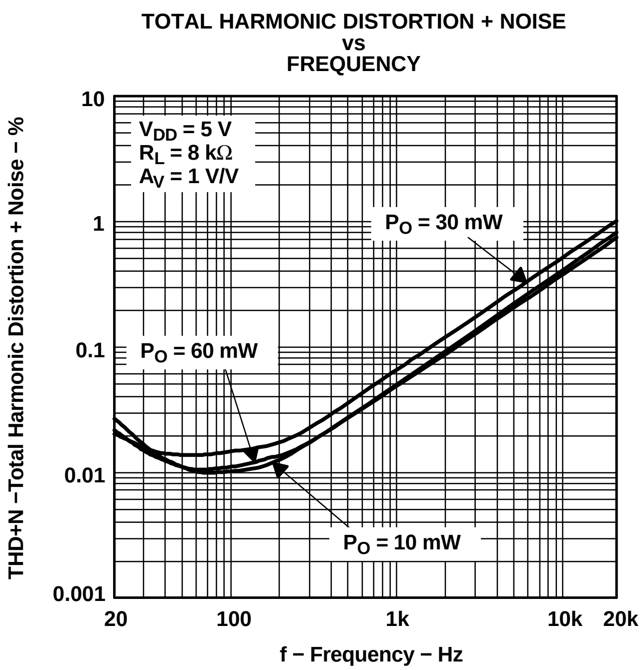



Figure 17.

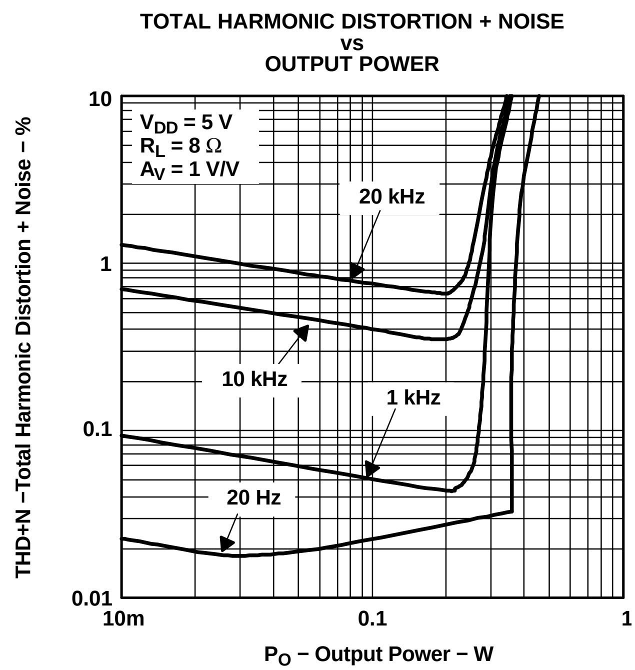



Figure 18.

**POWER SUPPLY REJECTION RATIO**
**vs**
**FREQUENCY**

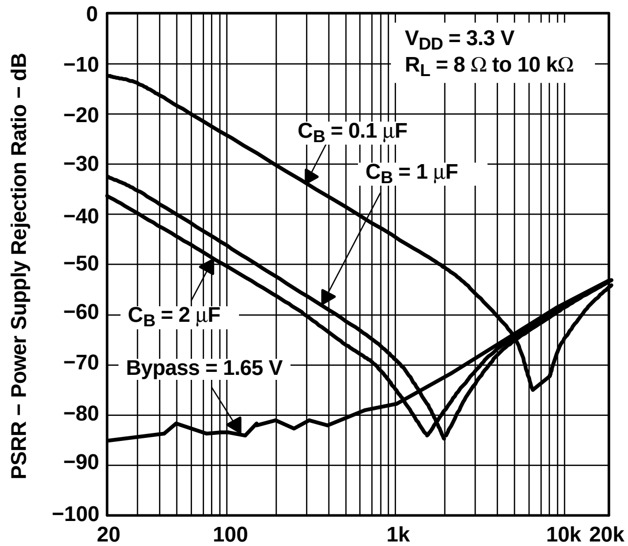



**Figure 19.**

**POWER SUPPLY REJECTION RATIO**
**vs**
**FREQUENCY**

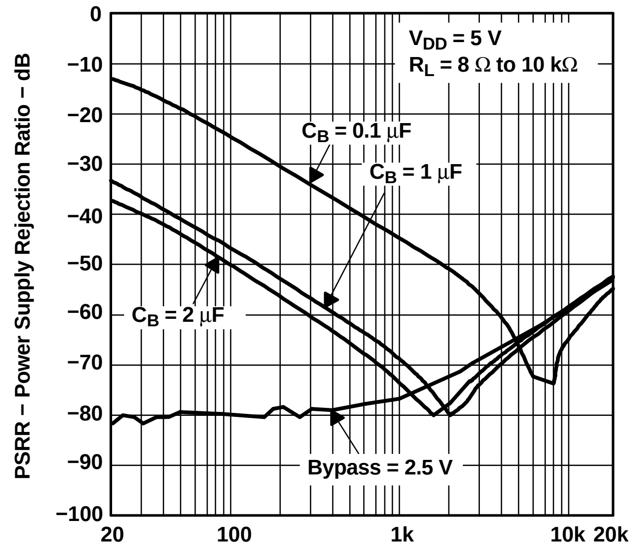



**Figure 20.**

**OUTPUT NOISE VOLTAGE**
**vs**
**FREQUENCY**

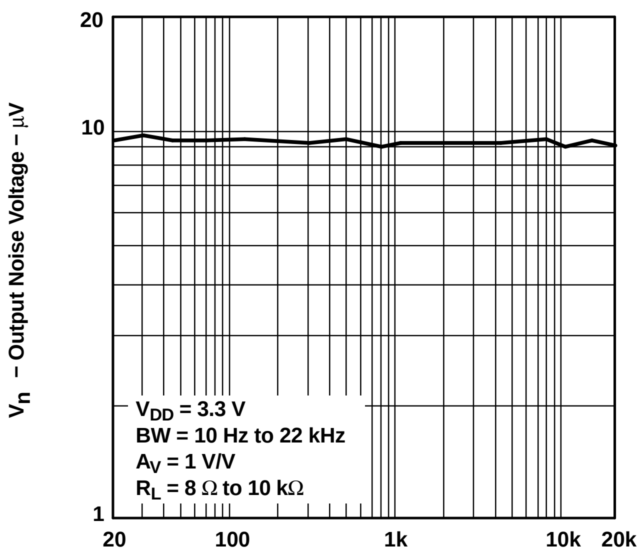



**Figure 21.**

**OUTPUT NOISE VOLTAGE**
**vs**
**FREQUENCY**

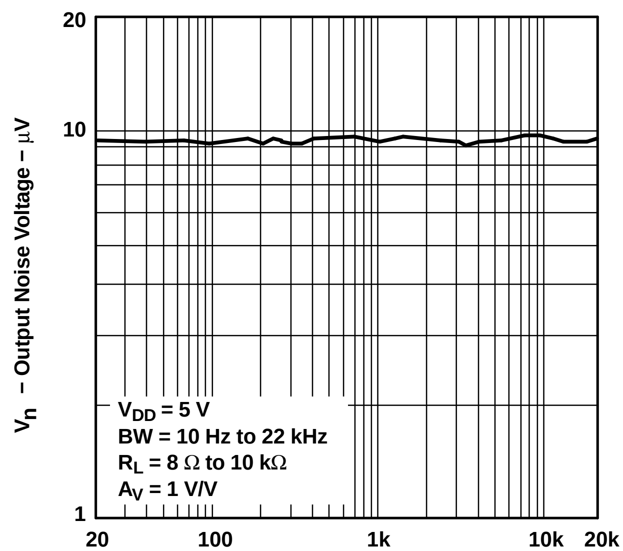



**Figure 22.**

**CROSSTALK vs FREQUENCY**

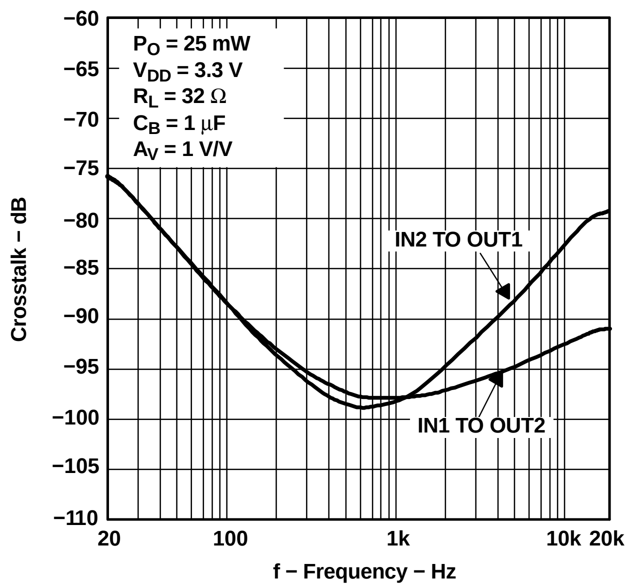



Figure 23.

**CROSSTALK vs FREQUENCY**

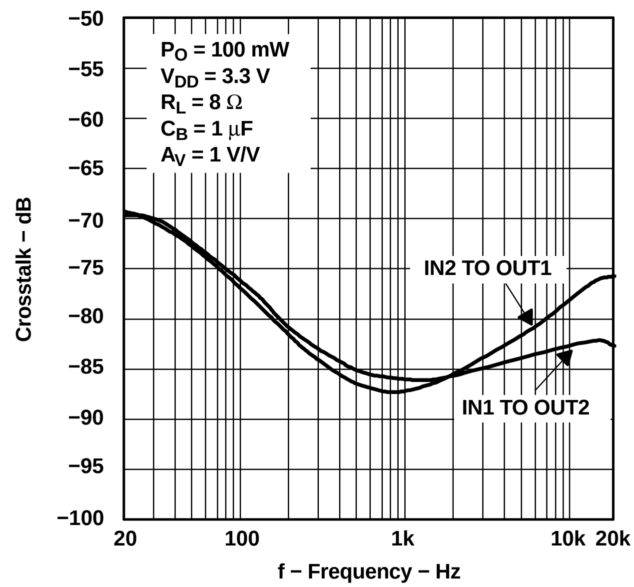



Figure 24.

**CROSSTALK vs FREQUENCY**

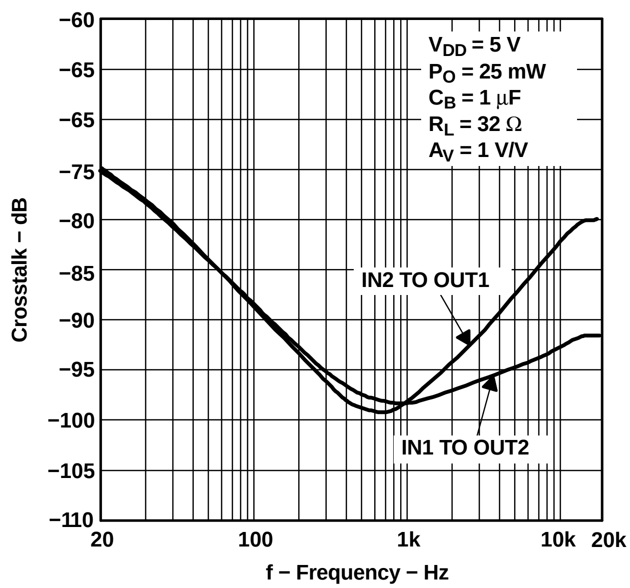



Figure 25.

**CROSSTALK vs FREQUENCY**

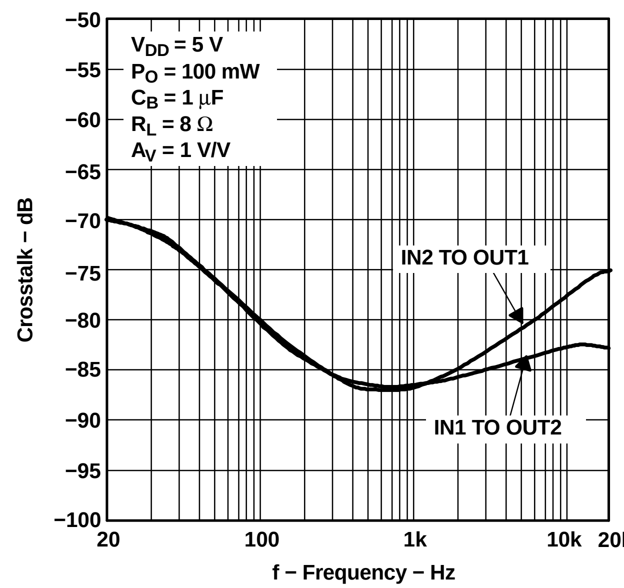



Figure 26.

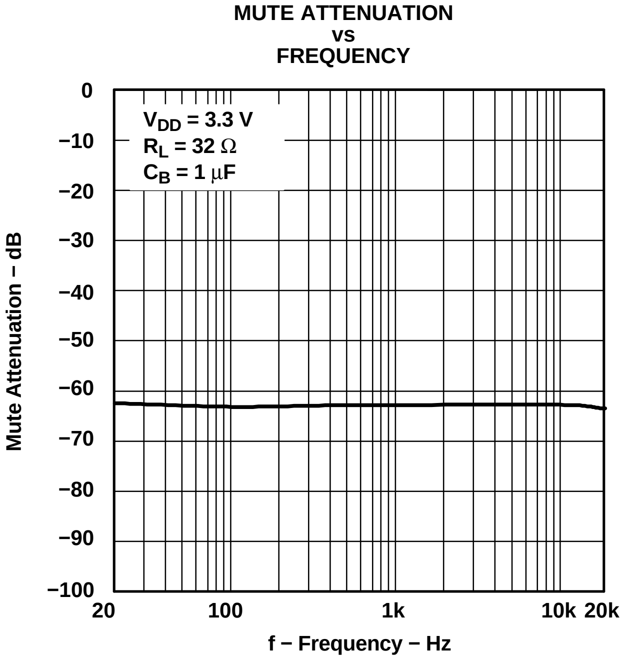



Figure 27.

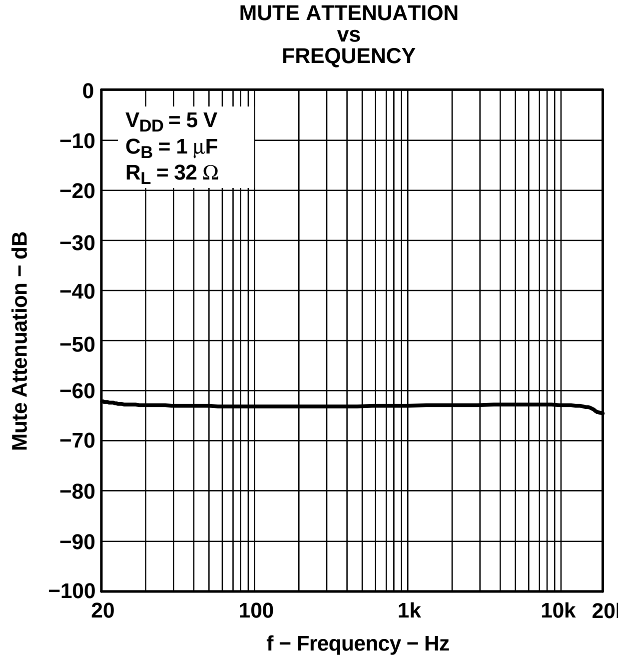



Figure 28.

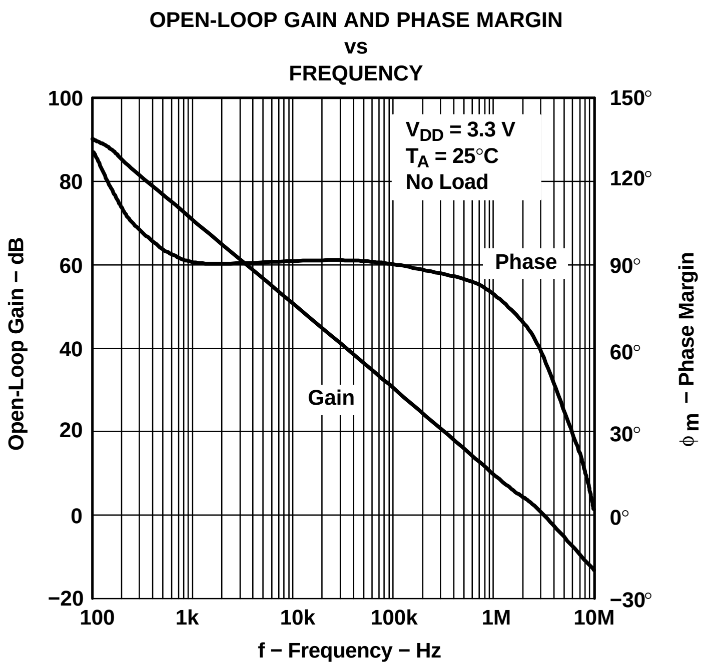



Figure 29.

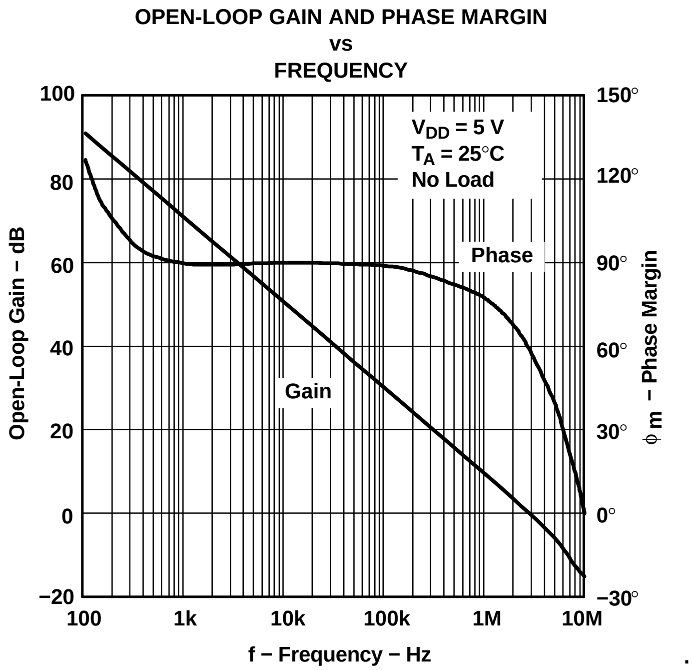



Figure 30.

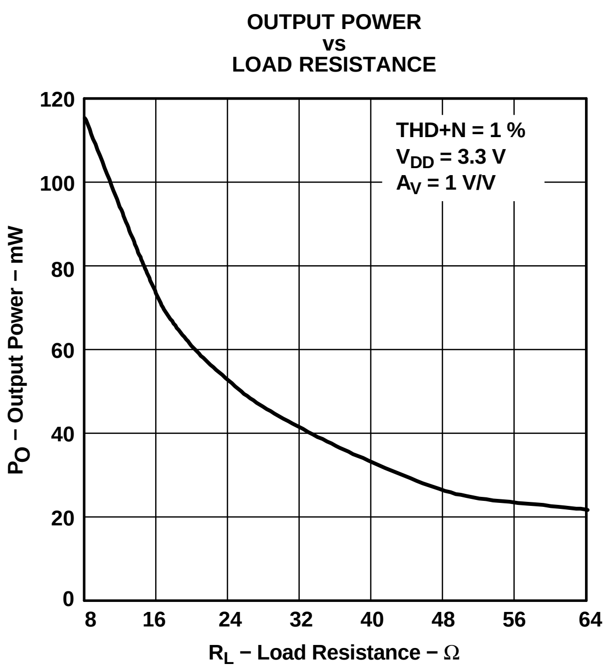



Figure 31.

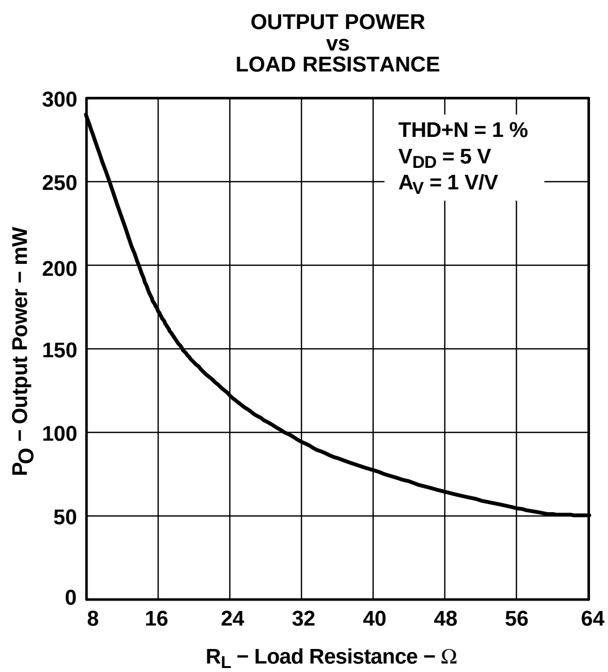



Figure 32.

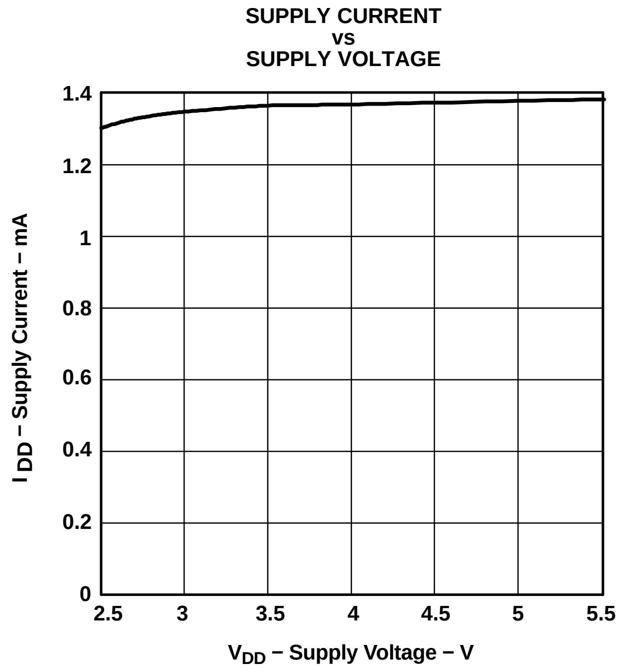



Figure 33.

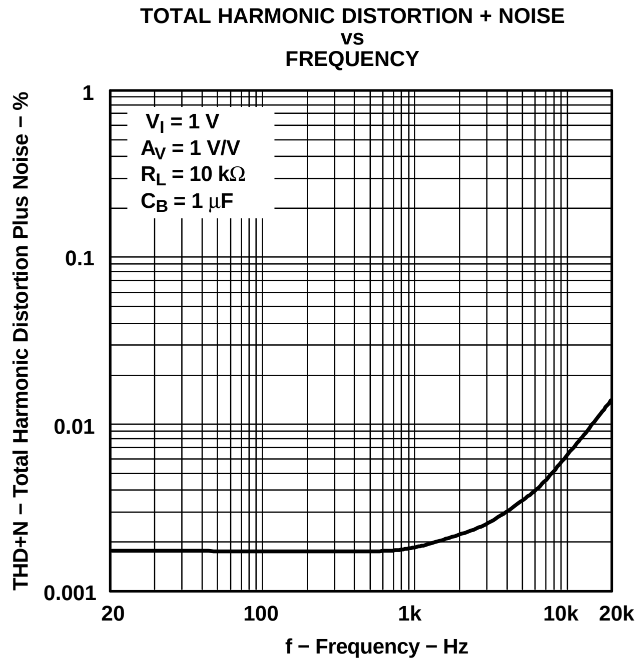



Figure 34.

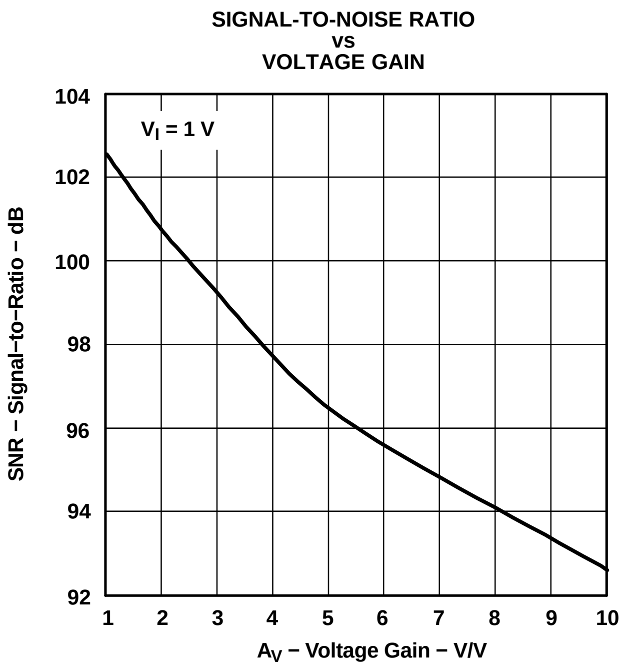



Figure 35.

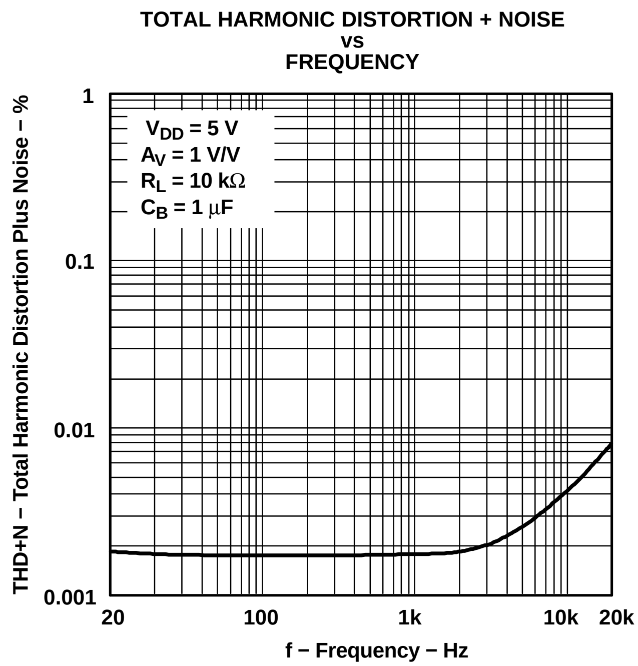



Figure 36.

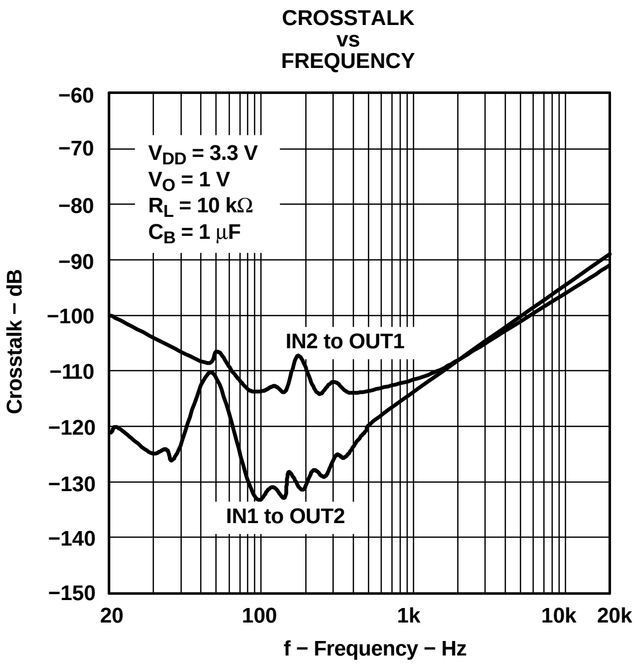



Figure 37.

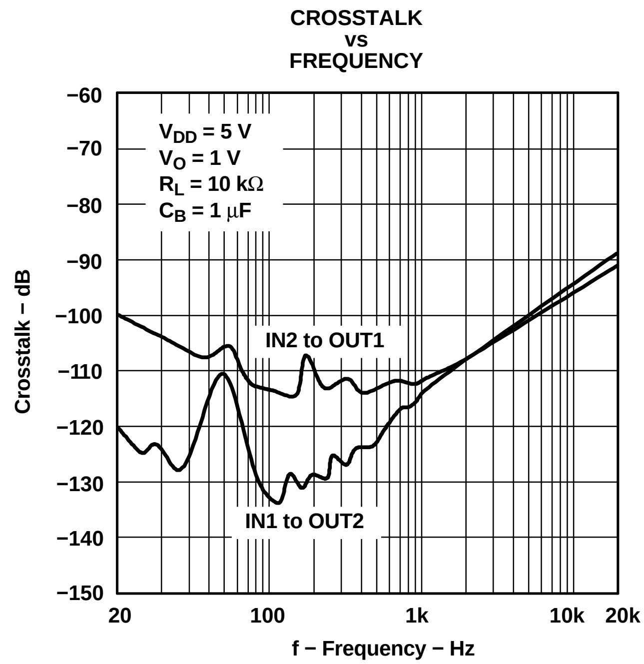



Figure 38.

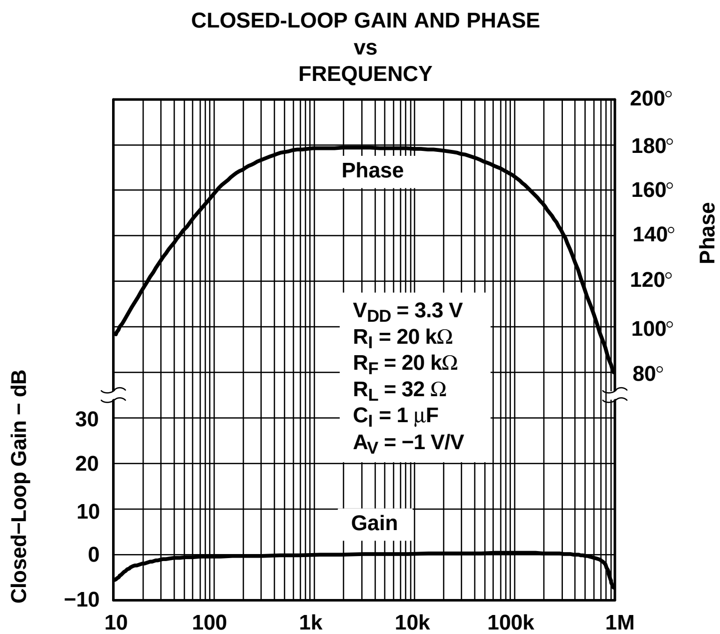



Figure 39.

**CLOSED-LOOP GAIN AND PHASE vs FREQUENCY**

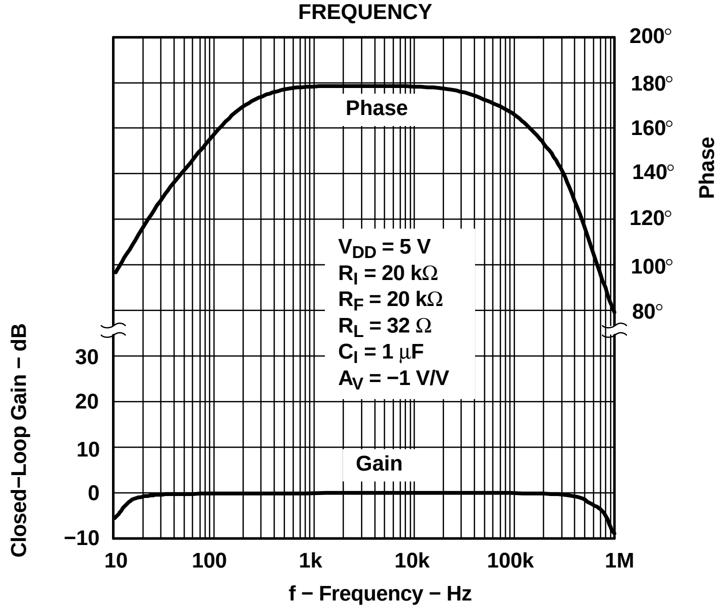



Figure 40.

**CLOSED-LOOP GAIN AND PHASE vs FREQUENCY**

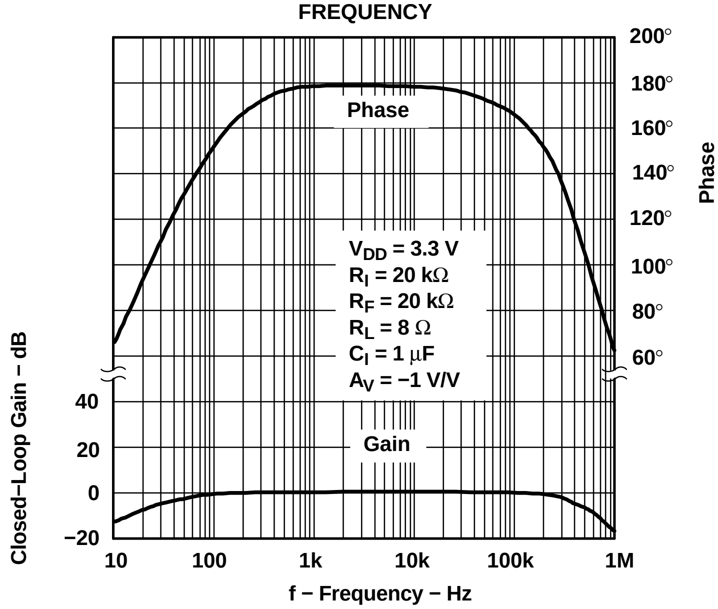



Figure 41.

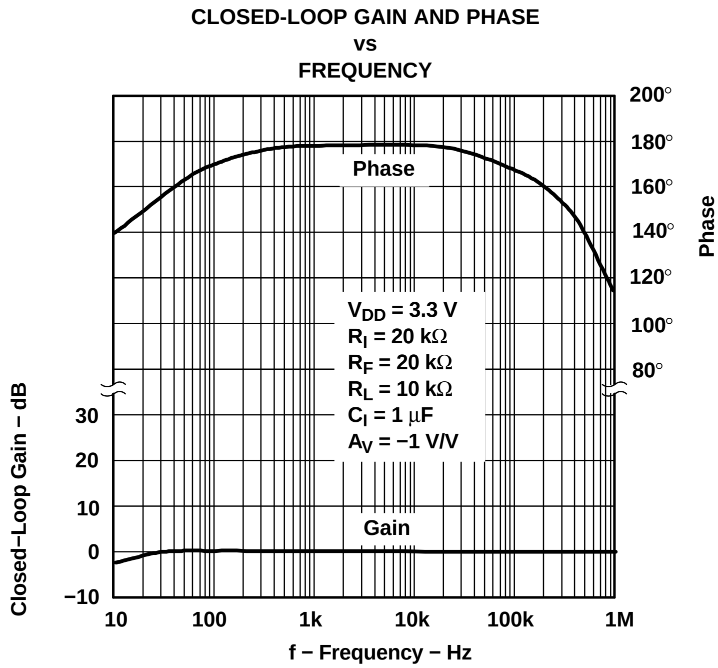



Figure 42.

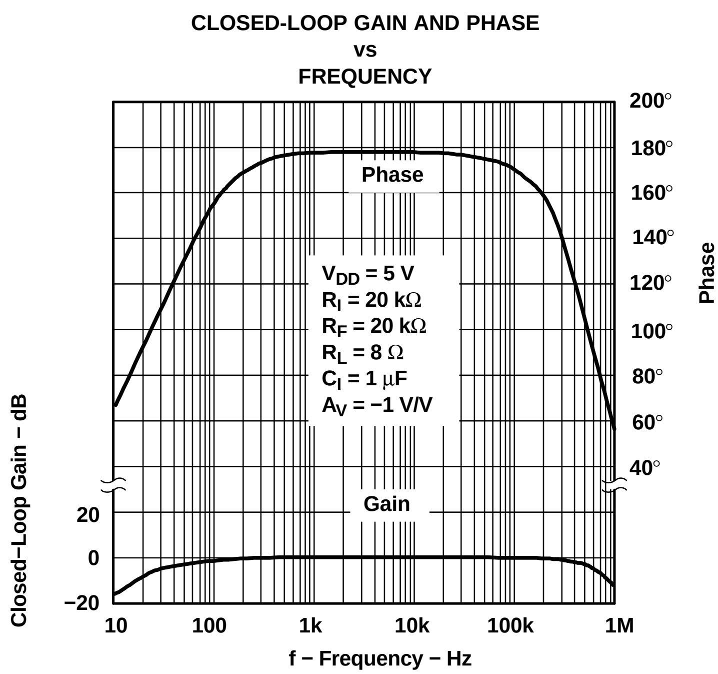



Figure 43.

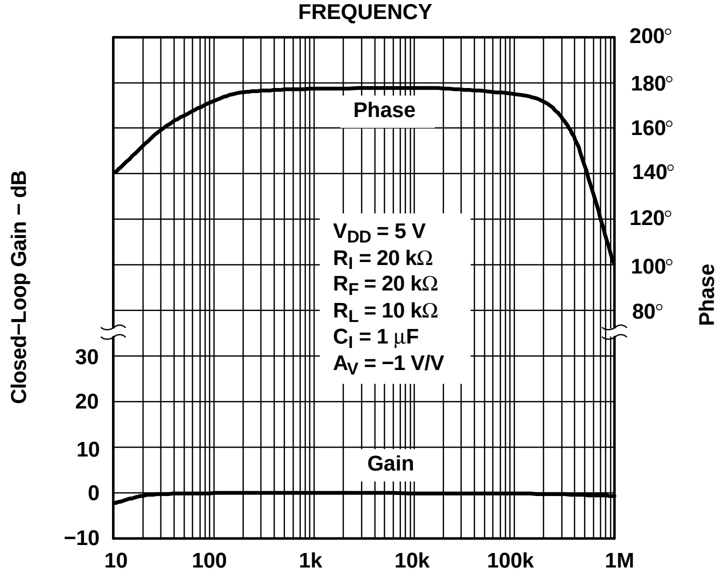



Figure 44.

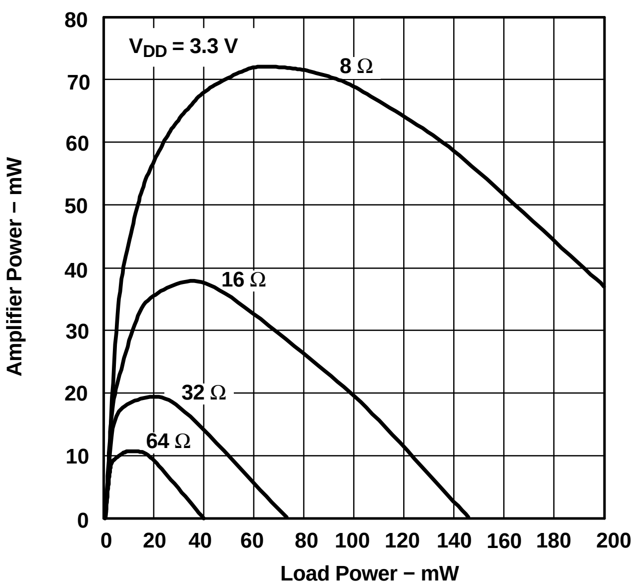



Figure 45.

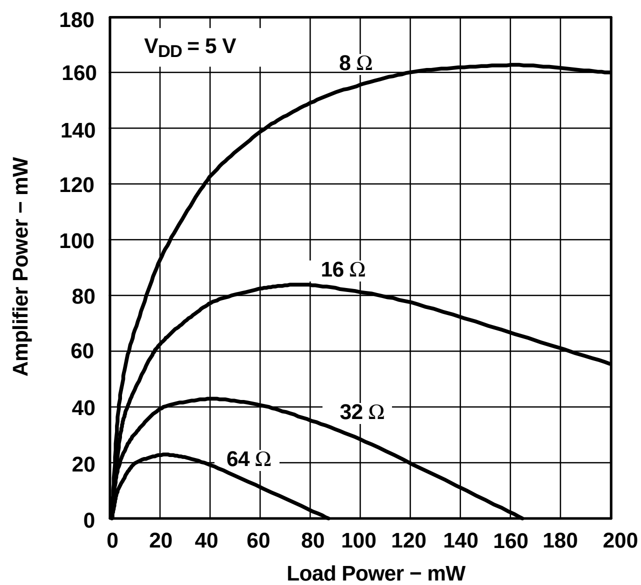



Figure 46.

## APPLICATION INFORMATION

### GAIN SETTING RESISTORS, $R_F$ and $R_I$

The gain for the TPA112 is set by resistors $R_F$ and $R_I$ according to Equation 1.

$$\text{Gain} = -\left(\frac{R_F}{R_I}\right) \tag{1}$$

Given that the TPA112 is an MOS amplifier, the input impedance is high. Consequently, input leakage currents are not generally a concern, although noise in the circuit increases as the value of $R_F$ increases. In addition, a certain range of $R_F$ values is required for proper start-up operation of the amplifier. Taken together, it is recommended that the effective impedance seen by the inverting node of the amplifier be set between 5 kΩ and 20 kΩ. The effective impedance is calculated in Equation 2.

$$\text{Effective Impedance} = \frac{R_F R_I}{R_F + R_I} \tag{2}$$

As an example, consider an input resistance of 20 kΩ and a feedback resistor of 20 kΩ. The gain of the amplifier would be -1 and the effective impedance at the inverting terminal would be 10 kΩ, which is within the recommended range.

For high-performance applications, metal film resistors are recommended because they tend to have lower noise levels than carbon resistors. For values of $R_F$ above 50 kΩ, the amplifier tends to become unstable due to a pole formed from $R_F$ and the inherent input capacitance of the MOS input structure. For this reason, a small compensation capacitor of approximately 5 pF should be placed in parallel with $R_F$. In effect, this creates a low-pass filter network with the cutoff frequency defined in Equation 3.

$$f_{co(lowpass)} = \frac{1}{2\pi R_F C_F} \tag{3}$$

For example, if $R_F$ is 100 kΩ and $C_F$ is 5 pF then $f_{co(lowpass)}$ is 318 kHz, which is well outside the audio range.

### INPUT CAPACITOR, $C_I$

In the typical application, input capacitor $C_I$ is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, $C_I$ and $R_I$ form a high-pass filter with the corner frequency determined in Equation 4.

$$f_{co(highpass)} = \frac{1}{2\pi R_I C_I} \tag{4}$$

The value of $C_I$ is important to consider, as it directly affects the bass (low-frequency) performance of the circuit. Consider the example where $R_I$ is 20 kΩ and the specification calls for a flat bass response down to 20 Hz. Equation 4 is reconfigured as Equation 5.

$$C_I = \frac{1}{2\pi R_I f_{co(highpass)}} \tag{5}$$

In this example, $C_I$ is 0.4 µF, so one would likely choose a value in the range of 0.47 µF to 1 µF. A further consideration for this capacitor is the leakage path from the input source through the input network ($R_I$, $C_I$) and the feedback resistor ($R_F$) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high-gain applications (> 10). For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications, as the dc level there is held at $V_{DD}/2$, which is likely higher that the source dc level. It is important to confirm the capacitor polarity in the application.

## APPLICATION INFORMATION (continued)

### POWER SUPPLY DECOUPLING, $C_S$

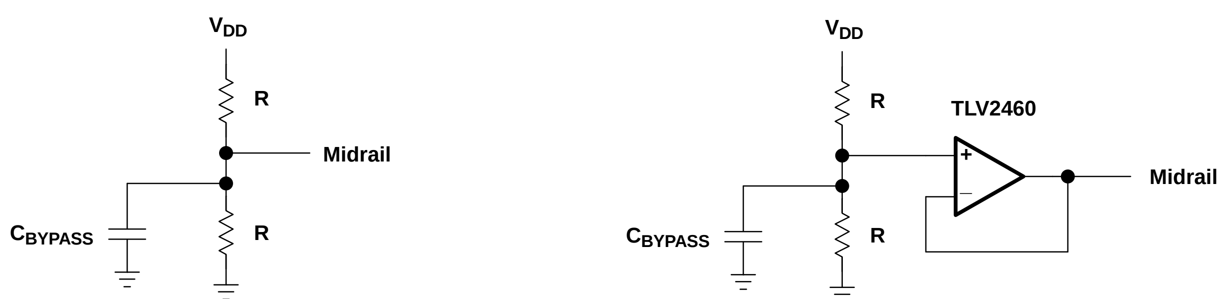
The TPA112 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor; typically, 0.1 µF, placed as close as possible to the device $V_{DD}$ lead, works best. For filtering lower frequency noise signals, a larger aluminum electrolytic capacitor of 10 µF or greater placed near the power amplifier is recommended.

### MIDRAIL VOLTAGE

The TPA112 is a single-supply amplifier; so, it must be properly biased to accommodate audio signals. Normally, the amplifier is biased at $V_{DD}/2$, but it can actually be biased at any voltage between $V_{DD}$ and ground. However, biasing the amplifier at a point other than $V_{DD}/2$ reduces the amplifier's maximum output swing. In some applications where the circuitry driving the TPA112 has a different midrail voltage, it might make sense to use the same midrail voltage for the TPA112, and possibly eliminate the use of the dc-blocking capacitors.

The two concerns with the midrail voltage source are the amount of noise present and its output impedance. Any noise present on the midrail voltage source that is not present on the audio input signal will be input to the amplifier, and passed to the output (and increased by the gain of the circuit). Common-mode noise is cancelled out by the differential configuration of the circuit.

The output impedance of the circuit used to generate the midrail voltage needs to be low enough so as not to be influenced by the audio signal path. A common method of generating the midrail voltage is to form a voltage divider from the supply to ground, with a bypass capacitor from the common node to ground. This capacitor improves the PSRR of the circuit. However, this circuit has a limited range of output impedances; so, to achieve low output impedances, the voltage generated by the voltage divider is fed into a unity-gain amplifier to lower the output impedance of the circuit.




a) Midrail Voltage Generator Using a Simple Resistor-Divider

b) Buffered Midrail Voltage Generator to Provide Low Output Impedance

**Figure 47. Midrail Voltage Generator**

If a voltage step is applied to a speaker, it causes a noise pop. To reduce popping, the midrail voltage should rise at a subsonic rate. That is, a rate less than the rise time of a 20-Hz waveform. If the voltage rises faster than that, there is the possibility of a pop from the speaker.

Pop can also be heard in the speaker if the midrail voltage rises faster than the charge of either the input coupling capacitor or the output coupling capacitor. If midrail rises first, the charging of the input and output capacitors is heard in the speaker. To keep this noise as low as possible, the relationship shown in Equation 6 should be maintained.

## APPLICATION INFORMATION (continued)

$$\frac{1}{\left(C_B \times R_{SOURCE}\right)} \leq \frac{1}{\left(C_I R_I\right)} \ll \frac{1}{R_L C_C} \tag{6}$$

Where $C_{BYPASS}$ is the value of the bypass capacitor, and $R_{SOURCE}$ is the equivalent source impedance of the voltage divider (the parallel combination of the two resistors). For example, if the voltage divider is constructed using two 20-kΩ resistors, then $R_{SOURCE}$ is 10 kΩ.

## MIDRAIL BYPASS CAPACITOR, $C_B$

The midrail bypass capacitor $C_B$ serves several important functions. During start-up, $C_B$ determines the rate at which the amplifier starts up. This helps to push the start-up pop noise into the subaudible range (so slow it can not be heard). The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier. The capacitor is fed from the resistor divider with equivalent resistance of $R_{SOURCE}$. To keep the start-up pop as low as possible, the relationship shown in Equation 7 should be maintained.

$$\frac{1}{\left(C_B \times R_{SOURCE}\right)} \leq \frac{1}{\left(C_I R_I\right)} \tag{7}$$

As an example, consider a circuit where $C_B$ is 1 µF, $R_{SOURCE}$ = 160 kΩ, $C_I$ is 1 µF, and $R_I$ is 20 kΩ. Inserting these values into the Equation 8 results in:

$$6.25 \leq 50 \tag{8}$$

which satisfies the rule. Recommended values for bypass capacitor $C_B$ are 0.1 µF to 1 µF, ceramic or tantalum low-ESR, for the best THD and noise performance.

## OUTPUT COUPLING CAPACITOR, $C_C$

In the typical single-supply, single-ended (SE) configuration, an output coupling capacitor ($C_C$) is required to block the dc bias at the output of the amplifier, thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by Equation 9.

$$f_{(out\ high)} = \frac{1}{2\pi R_L C_C} \tag{9}$$

The main disadvantage, from a performance standpoint, is that the typically small load impedances drive the low-frequency corner higher. Large values of $C_C$ are required to pass low frequencies into the load. Consider the example where a $C_C$ of 68 µF is chosen and loads vary from 32 Ω to 47 kΩ. Table 1 summarizes the frequency response characteristics of each configuration.

**Table 1. Common Load Impedances vs Low Frequency Output Characteristics in SE Mode**

| $R_L$ | $C_C$ | LOWEST FREQUENCY |
|---|---|---|
| 32 Ω | 68 µF | 73 Hz |
| 10,000 Ω | 68 µF | 0.23 Hz |
| 47,000 Ω | 68 µF | 0.05 Hz |

As Table 1 indicates, headphone response is adequate and drive into line level inputs (a home stereo for example) is good.

The output coupling capacitor required in single-supply, SE mode also places additional constraints on the selection of other components in the amplifier circuit. With the rules described earlier still valid, add the following relationship:

- **Output Pulldown Resistor, $R_C$ + $R_O$**
  – Placing a 100-Ω resistor, $R_C$, from the output side of the coupling capacitor to ground ensures the coupling capacitor, $C_C$, is charged before a plug is inserted into the jack. Without this resistor, the coupling capacitor would charge rapidly upon insertion of a plug, leading to an audible pop in the headphones.

– Placing a 20-kΩ resistor, $R_O$, from the output of the IC to ground ensures that the coupling capacitor fully discharges at power down. If the supply is rapidly cycled without this capacitor, a small pop may be audible in 10-kΩ loads.

- **Using Low-ESR Capacitors**

  – Low-ESR capacitors are recommended throughout this application. A real capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

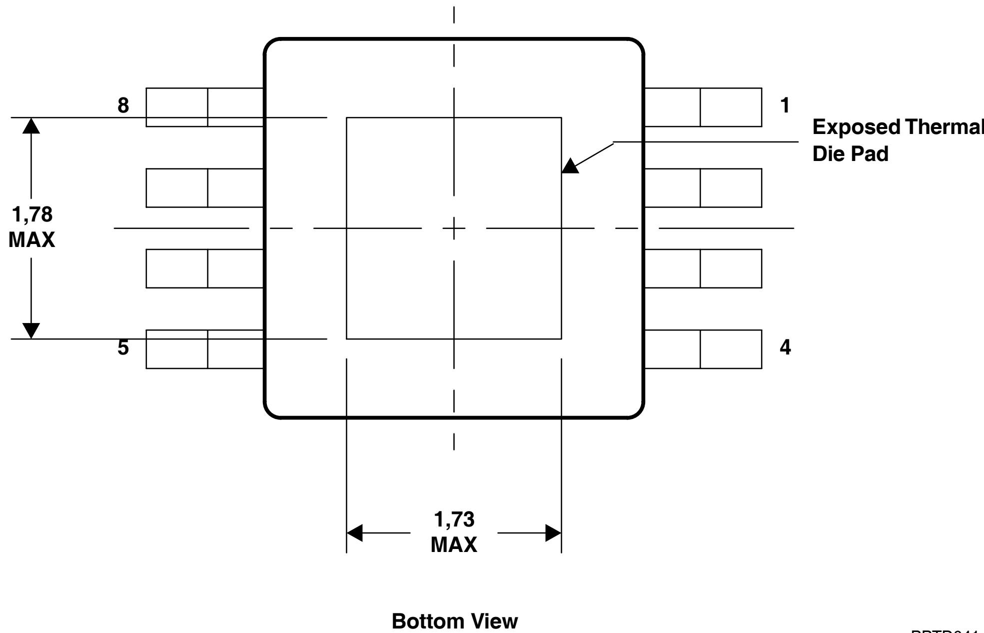
## 5-V VERSUS 3.3-V OPERATION

The TPA112 is designed for operation over a supply range of 2.5 V to 5.5 V. This data sheet provides full specifications for 5-V and 3.3-V operation because these are considered to be the two most common standard voltages. There are no special considerations for 3.3-V versus 5-V operation as far as supply bypassing, gain setting, or stability. The most important consideration is that of output power. Each amplifier in the TPA112 can produce a maximum voltage swing of $V_{DD}$ – 1 V. This means, for 3.3-V operation, clipping starts to occur when $V_{O(PP)}$ = 2.3 V, as opposed to $V_{O(PP)}$ = 4 V for 5-V operation. The reduced voltage swing subsequently reduces maximum output power into the load before distortion begins to become significant.

## THERMAL INFORMATION

The DGN PowerPAD™ package incorporates an exposed thermal die pad that is designed to be attached directly to an external heat sink. When the thermal die pad is soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal die pad can be attached directly to a ground plane or special heat sink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, *PowerPAD Thermally Enhanced Package*, Texas Instruments Literature No. SLMA002 and Application Brief, *PowerPAD Made Easy*, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com. See Figure 1 for DGN package exposed thermal die pad dimensions.

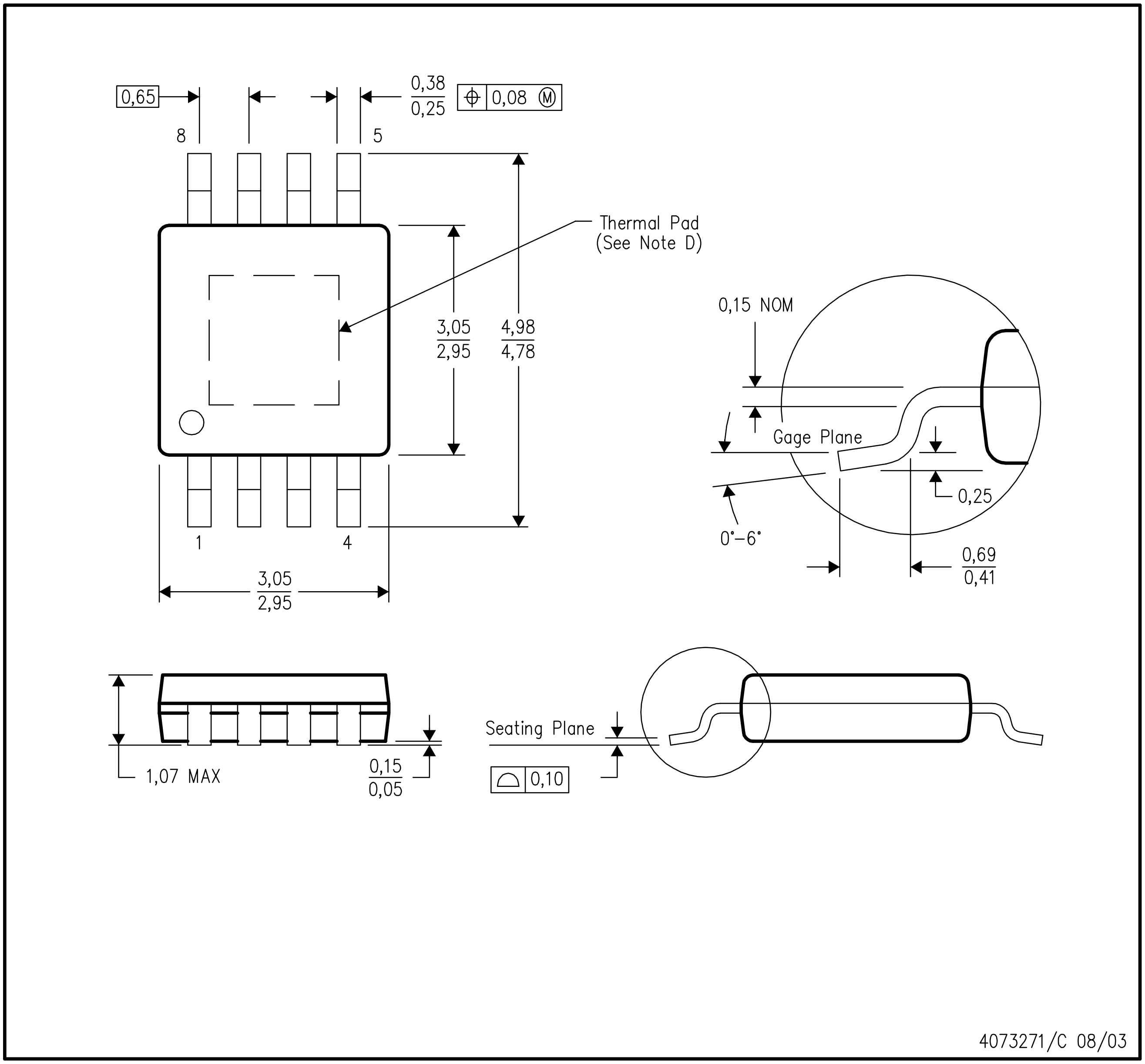



NOTE: All linear dimensions are in millimeters.

**Figure 1. DGN Package Exposed Thermal Die Pad Dimensions**

PowerPAD is a trademark of Texas Instruments.

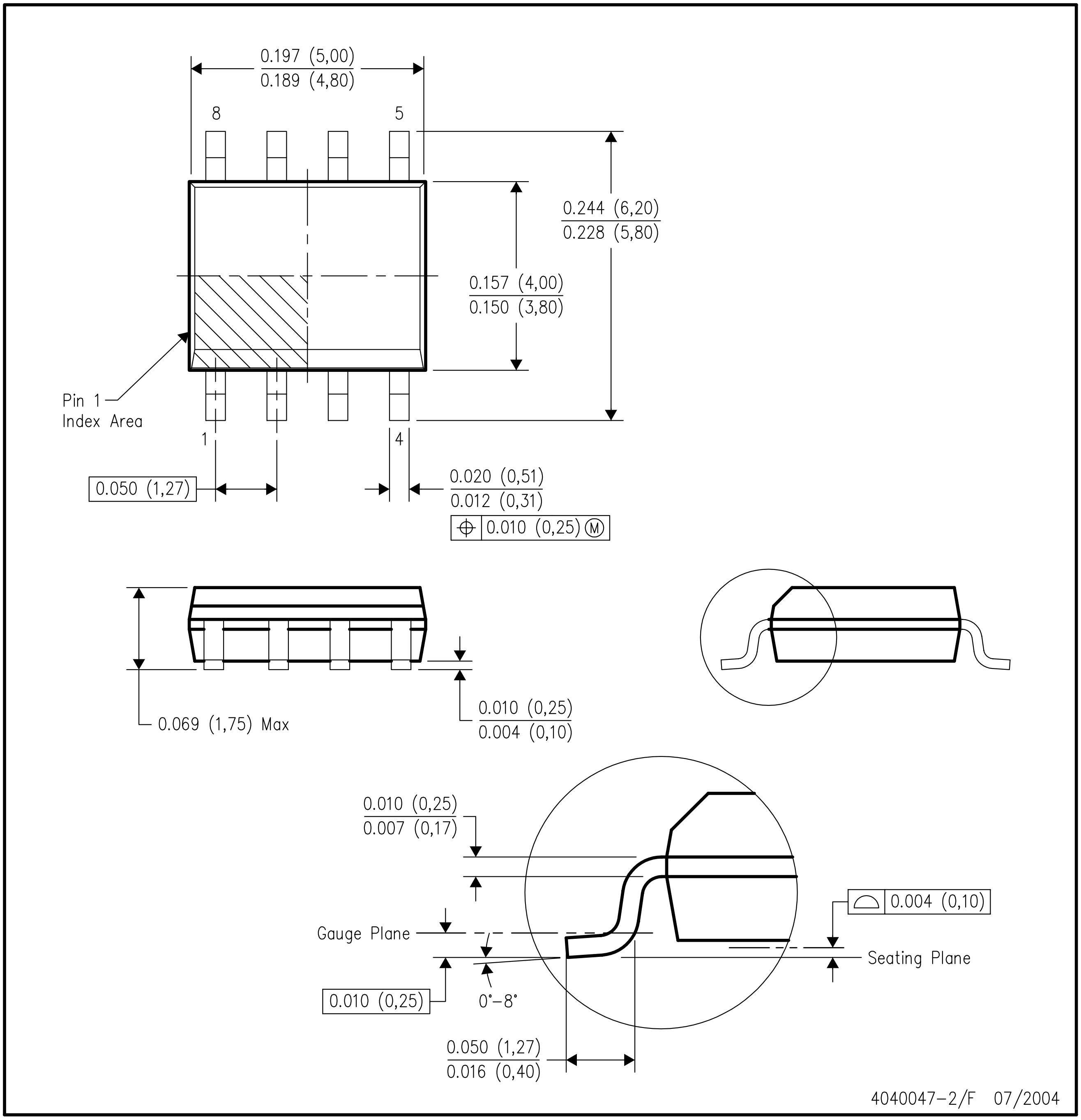
## DGN (S-PDSO-G8) PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE




NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
- E. Falls within JEDEC MO-187

**PowerPAD is a trademark of Texas Instruments.**

## D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE




NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AA.

## IMPORTANT NOTICE



Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

| **Products** | | **Applications** | |
|---|---|---|---|
| Amplifiers | amplifier.ti.com | Audio | www.ti.com/audio |
| Data Converters | dataconverter.ti.com | Automotive | www.ti.com/automotive |
| DSP | dsp.ti.com | Broadband | www.ti.com/broadband |
| Interface | interface.ti.com | Digital Control | www.ti.com/digitalcontrol |
| Logic | logic.ti.com | Military | www.ti.com/military |
| Power Mgmt | power.ti.com | Optical Networking | www.ti.com/opticalnetwork |
| Microcontrollers | microcontroller.ti.com | Security | www.ti.com/security |
| | | Telephony | www.ti.com/telephony |
| | | Video & Imaging | www.ti.com/video |
| | | Wireless | www.ti.com/wireless |

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265