2.1 W/CH STEREO FILTER-FREE CLASS-D AUDIO POWER AMPLIFIER

FEATURES

- **Output Power By Package:**
  - **QFN:**
    - **2.1 W/Ch Into 4 Ω at 5 V**
    - **1.4 W/Ch Into 8 Ω at 5 V**
    - **720 mW/Ch Into 8 Ω at 3.6 V**
  - **WCSP:**
    - **1.2 W/Ch Into 4 Ω at 5 V(1)**
    - **1.3 W/Ch Into 8 Ω at 5 V**
    - **720 mW/Ch Into 8 Ω at 3.6 V**
- **Only Two External Components Required**
- **Power Supply Range: 2.5 V to 5.5 V**
- **Independent Shutdown Control for Each Channel**
- **Selectable Gain of 6, 12, 18, and 24 dB**
- **Internal Pulldown Resistor On Shutdown Pins**
- **High PSRR: 77 dB at 217 Hz**
- **Fast Startup Time (3.5 ms)**
- **Low Supply Current**
- **Low Shutdown Current**
- **Short-Circuit and Thermal Protection**
- **Space Saving Packages**
  - **2,01 mm X 2,01 mm NanoFree™ WCSP (YZH)**
  - **4 mm X 4 mm Thin QFN (RTJ) with PowerPAD™**

(1) Thermally limited

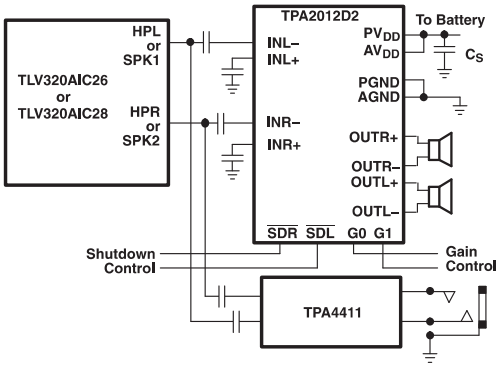
APPLICATIONS

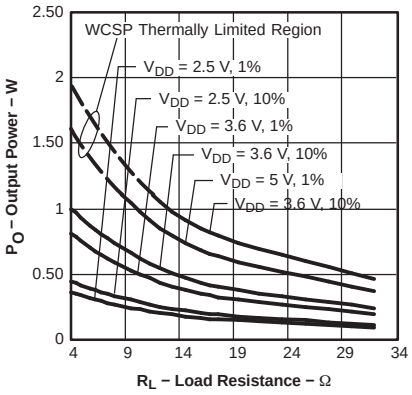
- **Wireless or Cellular Handsets and PDAs**
- **Portable DVD Player**
- **Notebook PC**
- **Portable Radio**
- **Portable Gaming**
- **Educational Toys**
- **USB Speakers**

DESCRIPTION

The TPA2012D2 is a stereo, filter-free, Class-D audio amplifier (class-D amp) available in a WCSP, QFN, or PWP package. The TPA2012D2 only requires two external components for operation.

The TPA2012D2 features independent shutdown controls for each channel. The gain can be selected to 6, 12, 18, or 24 dB utilizing the G0 and G1 gain select pins. High PSRR and differential architecture provide increased immunity to noise and RF rectification. In addition to these features, a fast startup time and small package size make the TPA2012D2 class-D amp an ideal choice for both cellular handsets and PDAs.





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

The TPA2012D2 is capable of driving 1.4 W/Ch at 5 V or 720 mW/Ch at 3.6 V into 8 Ω. The TPA2012D2 is also capable of driving 4 Ω. The TPA2012D2 is thermally limited in WCSP and may not achieve 2.1 W/Ch for 4 Ω. The maximum output power in the WCSP is determined by the ability of the circuit board to remove heat. The output power versus load resistance graph below shows thermally limited region of the WCSP in relation to the QFN package. The TPA2012D2 provides thermal and short circuit protection.

AVAILABLE OPTIONS

T_A	PACKAGE	PART NUMBER	SYMBOL
–40°C to 85°C	2 mm x 2 mm, 16-ball WCSP (YZH)	TPA2012D2YZH	AKR
	4 mm x 4 mm, 20-pin QFN (RTJ)	TPA2012D2RTJ	AKS

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature (unless otherwise noted)(1)

			VALUE	UNIT
V_{SS}	Supply voltage, AVDD, PVDD	In active mode	–0.3 to 6.0	V
		In shutdown mode	–0.3 to 7.0	V
V_I	Input voltage		–0.3 to V_{DD} + 0.3	V
	Continuous total power dissipation		See Dissipation Rating Table	
T_A	Operating free-air temperature range		–40 to 85	°C
T_J	Operating junction temperature range		–40 to 150	°C
T_{stg}	Storage temperature range		–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	T_A = 25°C POWER RATING(1)	DERATING FACTOR	T_A = 75°C POWER RATING	T_A = 85°C POWER RATING
RTJ	5.2 W	41.6 mW/°C	3.12 W	2.7 W
YZH	1.2 W	9.12 mW/°C	690 mW	600 mW

(1) This data was taken using 2 oz trace and copper pad that is soldered directly to a JEDEC standard 4-layer 3 in × 3 in PCB.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{SS}	Supply voltage	AVDD, PVDD	2.5	5.5	V
V_{IH}	High-level input voltage	$\overline{SDL}$, $\overline{SDR}$, G0, G1	1.3		V
V_{IL}	Low-level input voltage	$\overline{SDL}$, $\overline{SDR}$, G0, G1		0.35	V
T_A	Operating free-air temperature		÷40	85	°C

ELECTRICAL CHARACTERISTICS

T_A = 25°C (unless otherwise noted)

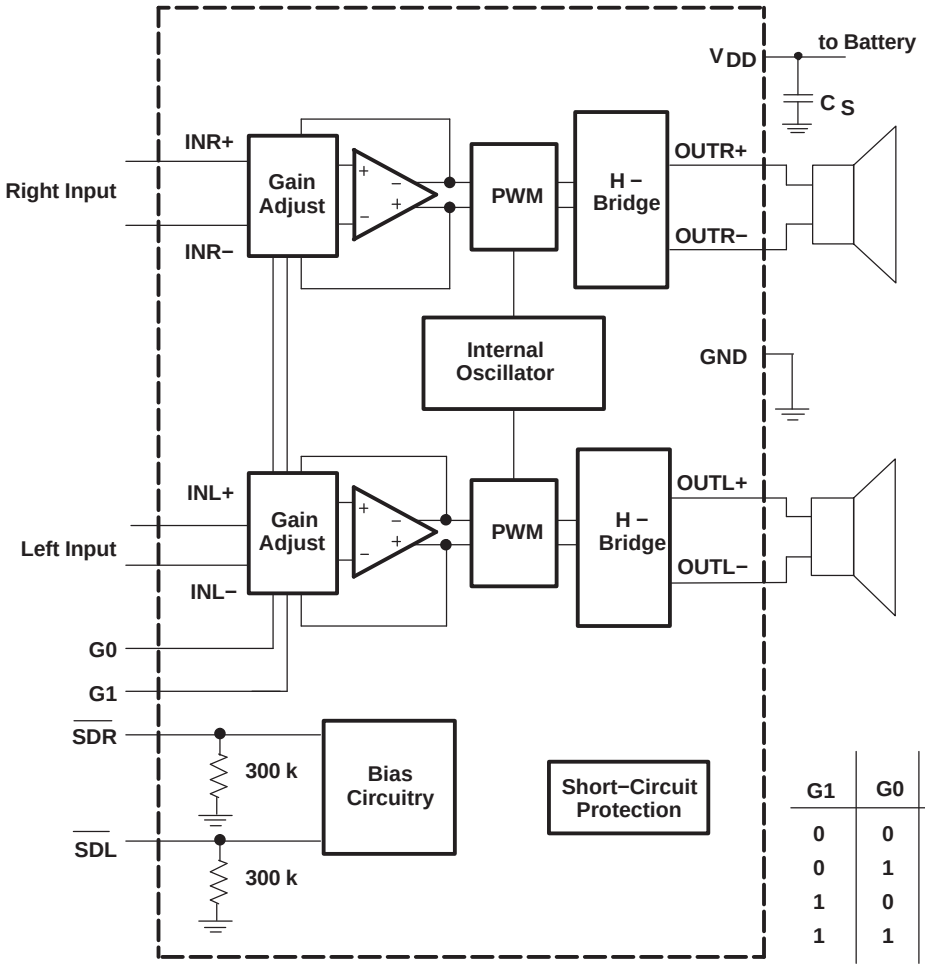
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OO}\|$	Output offset voltage (measured differentially)	Inputs ac grounded, A_V = 6 dB, V_{DD} = 2.5 to 5.5 V		5	25	mV
PSRR	Power supply rejection ratio	V_{DD} = 2.5 to 5.5 V		–75	–55	dB
V_{icm}	Common-mode input voltage		0.5		V_{DD}–0.8	V
CMRR	Common-mode rejection ration	Inputs shorted together, V_{DD} = 2.5 to 5.5 V		–69	–50	dB
$\|I_{IH}\|$	High-level input current	V_{DD} = 5.5 V, V_I = V_{DD}			50	µA
$\|I_{IL}\|$	Low-level input current	V_{DD} = 5.5 V, V_I = 0 V			5	µA
I_{DD}	Supply current	V_{DD} = 5.5 V, No load or output filter		6	9	mA
		V_{DD} = 3.6 V, No load or output filter		5	7.5	
		V_{DD} = 2.5 V, No load or output filter		4	6	
		Shutdown mode			1.5	µA
$r_{DS(on)}$	Static drain-source on-state resistance	V_{DD} = 5.5 V		500		mΩ
		V_{DD} = 3.6 V		570		
		V_{DD} = 2.5 V		700		
	Output impedance in shutdown mode	$V_{(\overline{SDR}, \overline{SDL})}$= 0.35 V		2		kΩ
$f_{(sw)}$	Switching frequency	V_{DD} = 2.5 V to 5.5 V	250	300	350	kHz
	Closed-loop voltage gain	G0, G1 = 0.35 V	5.5	6	6.5	dB
		G0 = V_{DD}, G1 = 0.35 V	11.5	12	12.5	
		G0 = 0.35 V, G1 = V_{DD}	17.5	18	18.5	
		G0, G1 = V_{DD}	23.5	24	24.5	

OPERATING CHARACTERISTICS

T_A = 25°C, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power (per channel)	R_L = 8 Ω	V_{DD} = 5.0 V, f = 1 kHz, THD = 10%		1.4		W
			V_{DD} = 3.6 V, f = 1 kHz, THD = 10%		0.72		
		R_L = 4 Ω	V_{DD} = 5.0 V, f = 1 kHz, THD = 10%		2.1		
THD+N	Total harmonic distortion plus noise	P_O = 1 W, V_{DD} = 5 V, A_V = 6 dB, f = 1 kHz			0.14%		
		P_O = 0.5 W, V_{DD} = 5 V, A_V = 6 dB, f = 1 kHz			0.11%		
	Channel crosstalk	f = 1 kHz			–85		dB
k_{SVR}	Supply ripple rejection ratio	V_{DD} = 5 V, A_V = 6 dB, f = 217 Hz			–77		dB
		V_{DD} = 3.6 V, A_V = 6 dB, f = 217 Hz			–73		
CMRR	Common mode rejection ratio	V_{DD} = 3.6 V, V_{IC} = 1 V_{pp}, f = 217 Hz			–69		dB
	Input impedance	Av = 6 dB			28.1		kΩ
		Av = 12 dB			17.3		
		Av = 18 dB			9.8		
		Av = 24 dB			5.2		
	Start-up time from shutdown	V_{DD} = 3.6 V			3.5		ms
V_n	Output voltage noise	V_{DD} = 3.6 V, f = 20 to 20 kHz, Inputs are ac grounded, A_V = 6 dB	No weighting		35		µV
			A weighting		27		

BLOCK DIAGRAM

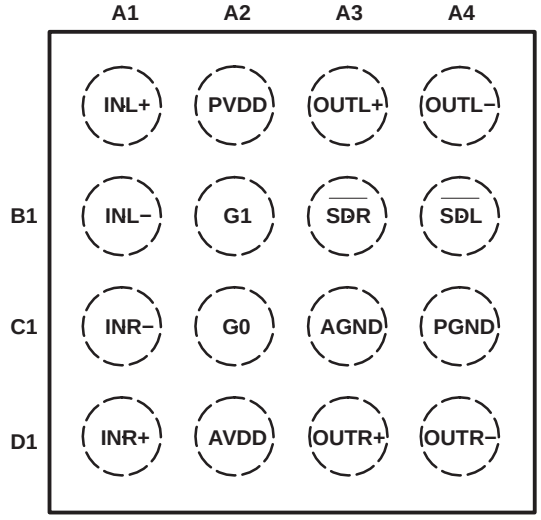


G1	G0	Gain V/V	Gain dB
0	0	2	6
0	1	4	12
1	0	8	18
1	1	16	24

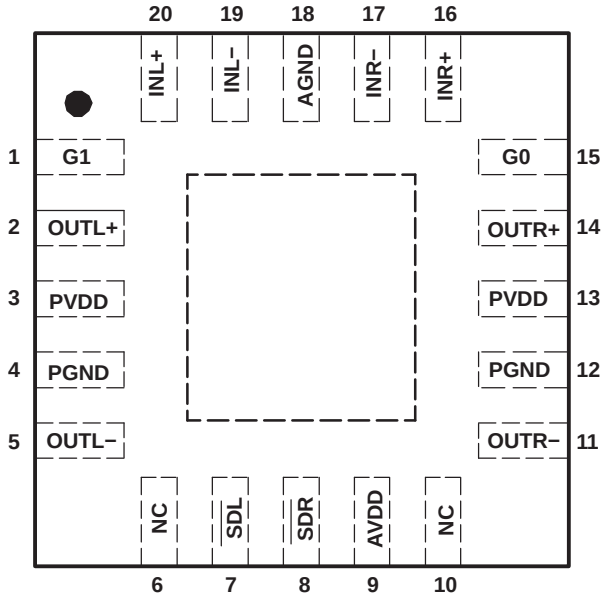
Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	QFN	WCSP		
INR+	16	D1	I	Right channel positive input
INR-	17	C1	I	Right channel negative input
INL+	20	A1	I	Left channel positive input
INL-	19	B1	I	Left channel negative input
$\overline{SDR}$	8	B3	I	Right channel shutdown terminal (active low)
$\overline{SDL}$	7	B4	I	Left channel shutdown terminal (active low)
G0	15	C2	I	Gain select (LSB)
G1	1	B2	I	Gain select (MSB)
PVDD	3, 13	A2	I	Power supply (Must be same voltage as AVDD)
AVDD	9	D2	I	Analog supply (Must be same voltage as PVDD)
PGND	4, 12	C4	I	Power ground
AGND	18	C3	I	Analog ground
OUTR+	14	D3	O	Right channel positive differential output
OUTR-	11	D4	O	Right channel negative differential output
OUTL+	2	A3	O	Left channel positive differential output
OUTL-	5	A4	O	Left channel negative differential output
NC	6, 10	N/A		No internal connection
Thermal Pad				Connect the thermal pad of QFN or PWP package to PCB GND

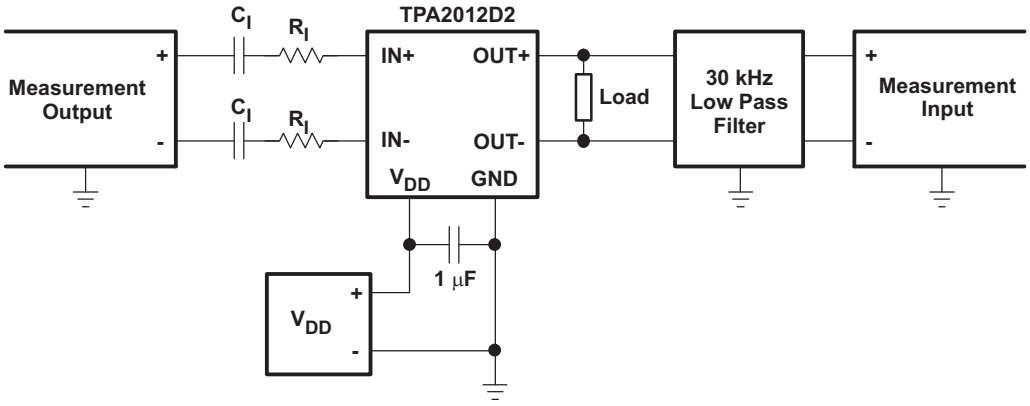
WCSP PIN OUT
TOP VIEW



RTJ PIN OUT
TOP VIEW



TEST SET-UP FOR GRAPHS (per channel)



(1) C_I was Shorted for any Common-Mode input voltage measurement.

(2) A 33-µH inductor was placed in series with the load resistor to emulate a small speaker for efficiency measurements.

(3) The 30–kHz low–pass filter is required even if the analyzer has an internal low–pass filter. An RC low pass filter (100 Ω, 47 nF) is used on each output for the data sheet graphs.

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION VS OUTPUT POWER

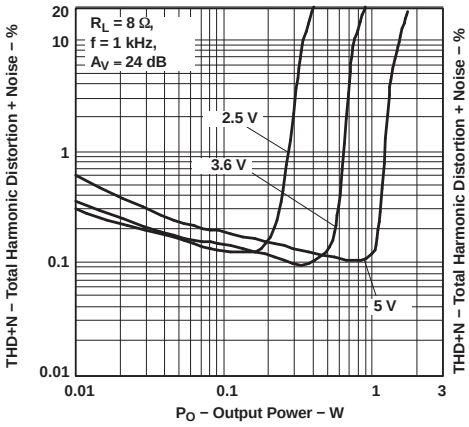


Figure 1.

TOTAL HARMONIC DISTORTION VS OUTPUT POWER

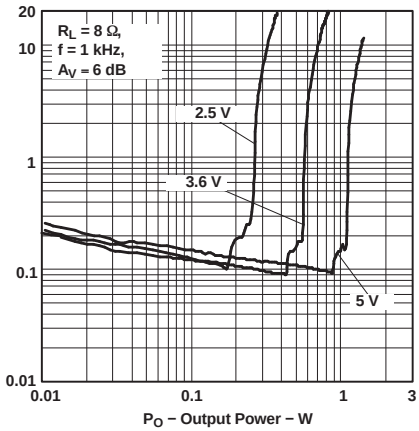


Figure 2.

TOTAL HARMONIC DISTORTION VS OUTPUT POWER

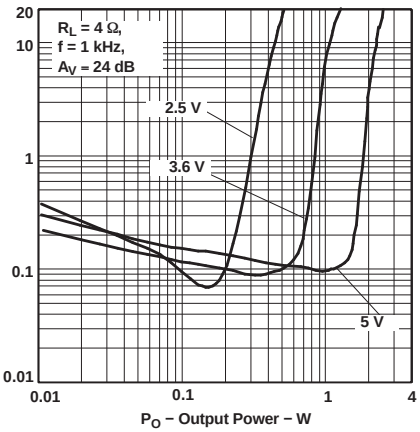


Figure 3.

TOTAL HARMONIC DISTORTION VS OUTPUT POWER

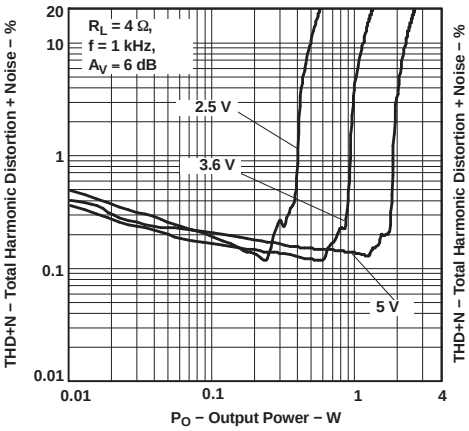


Figure 4.

TOTAL HARMONIC DISTORTION VS FREQUENCY

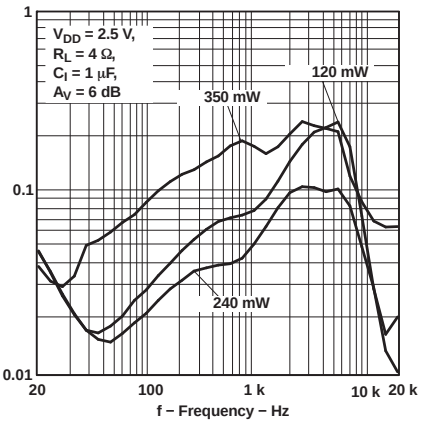


Figure 5.

TOTAL HARMONIC DISTORTION VS FREQUENCY

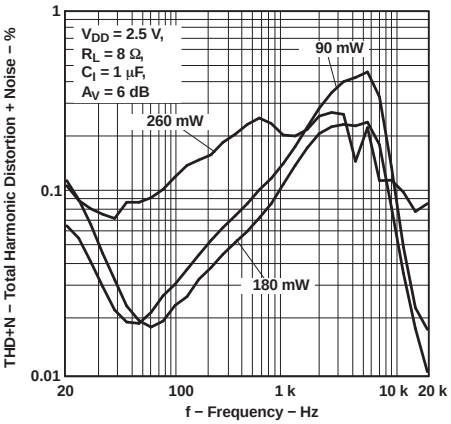


Figure 6.

TOTAL HARMONIC DISTORTION VS FREQUENCY

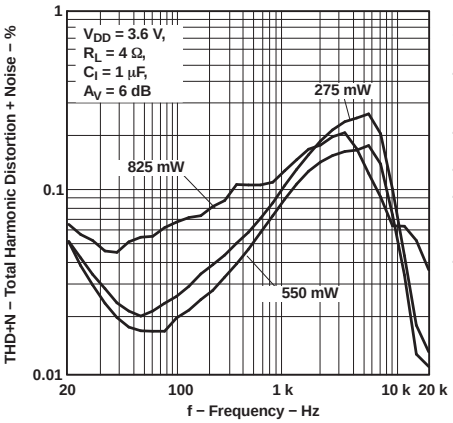


Figure 7.

TOTAL HARMONIC DISTORTION VS FREQUENCY

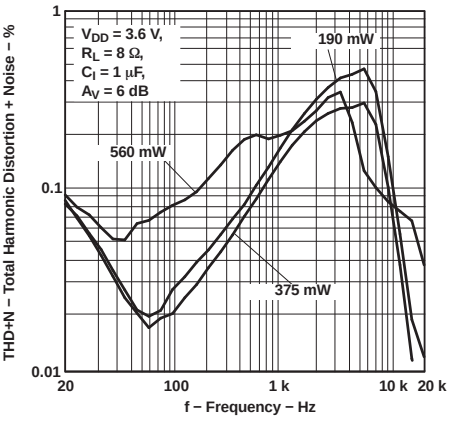


Figure 8.

TOTAL HARMONIC DISTORTION VS FREQUENCY

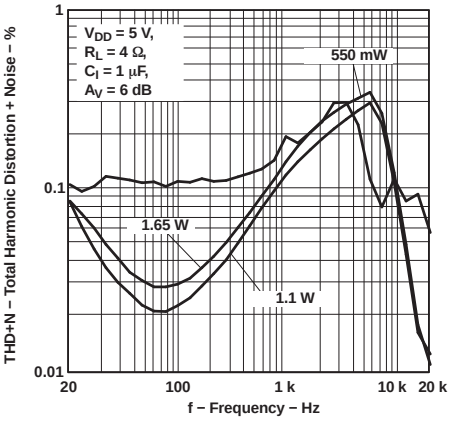


Figure 9.

TYPICAL CHARACTERISTICS (continued)

TOTAL HARMONIC DISTORTION VS FREQUENCY

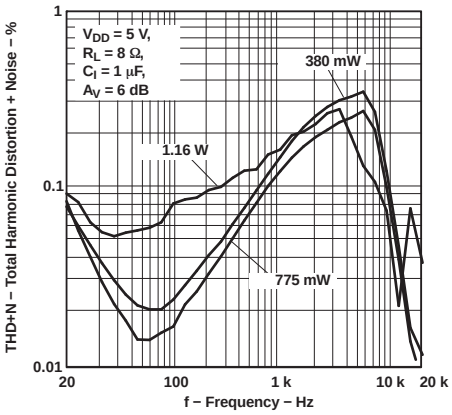


Figure 10.

SUPPLY CURRENT VS SHUTDOWN VOLTAGE

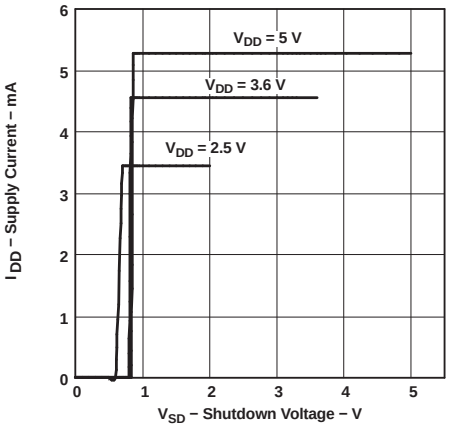


Figure 11.

SUPPLY CURRENT VS SUPPLY VOLTAGE

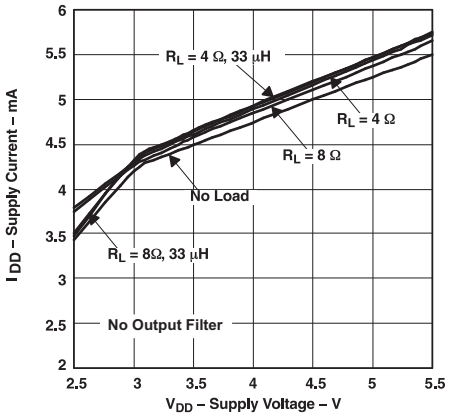


Figure 12.

SUPPLY CURRENT VS OUTPUT POWER

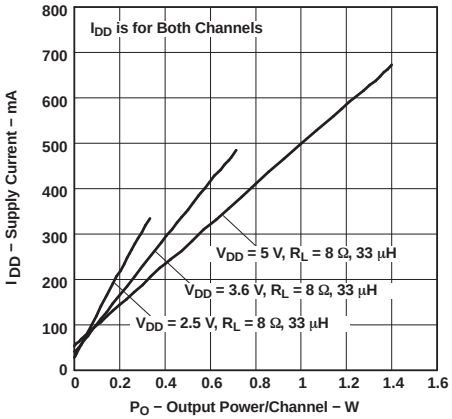


Figure 13.

SUPPLY CURRENT VS OUTPUT POWER

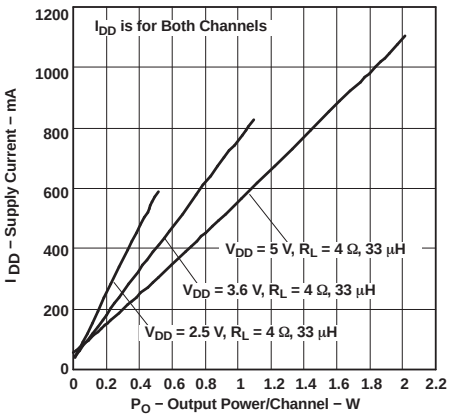


Figure 14.

CROSSTALK VS FREQUENCY

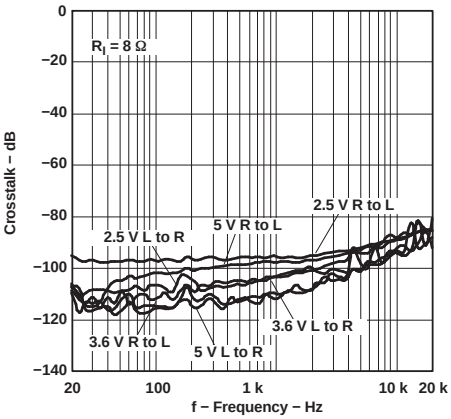


Figure 15.

CROSSTALK VS FREQUENCY

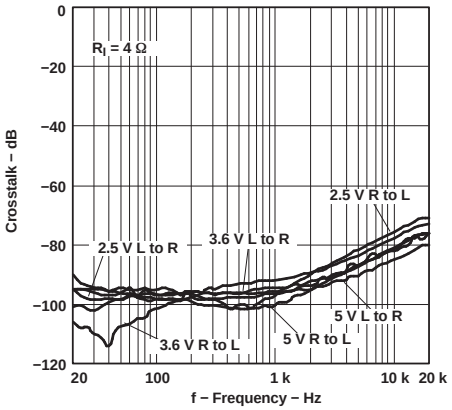


Figure 16.

POWER SUPPLY REJECTION RATIO VS FREQUENCY

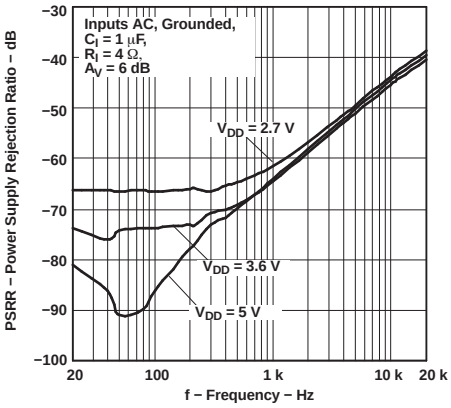


Figure 17.

POWER SUPPLY REJECTION RATIO VS FREQUENCY

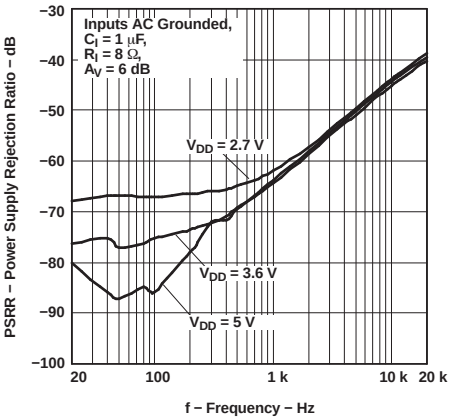


Figure 18.

TYPICAL CHARACTERISTICS (continued)

COMMOM-MODE REJECTION RATIO VS COMMON-MODE INPUT VOLTAGE

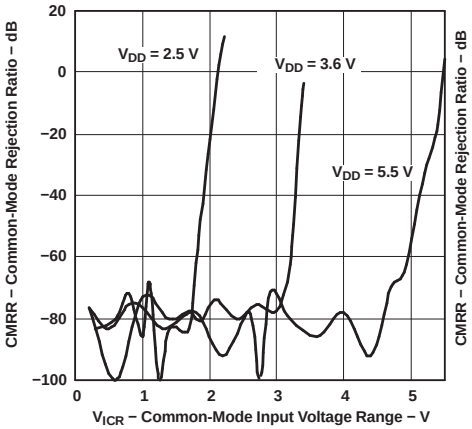


Figure 19.

COMMON-MODE REJECTION RATIO VS FREQUENCY

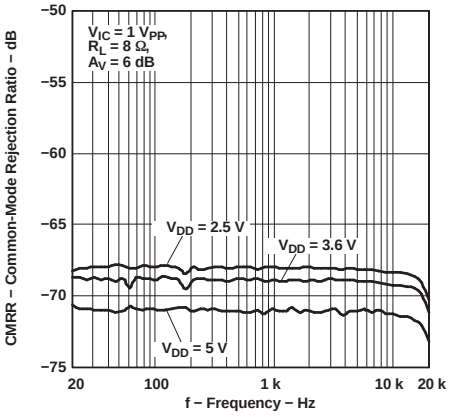


Figure 20.

GSM POWER SUPPLY REJECTION VS TIME

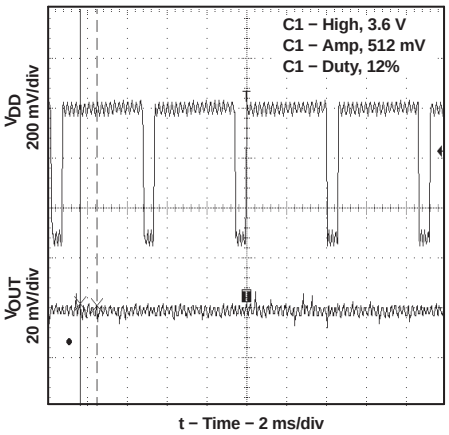


Figure 21.

POWER SUPPLY REJECTION VS FREQUENCY

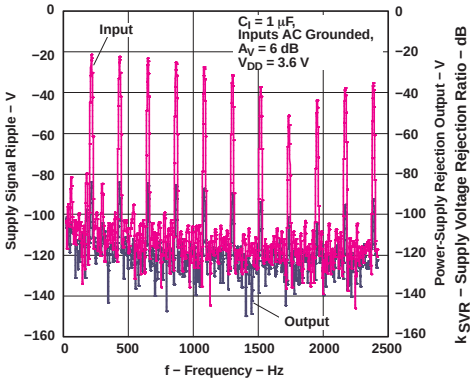


Figure 22.

SUPLY VOLTAGE REJECTION RATIO VS DC COMMON-MODE VOLTAGE

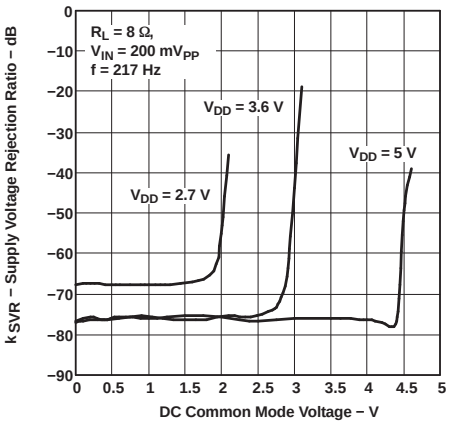


Figure 23.

POWER DISSIPATION VS OUTPUT POWER

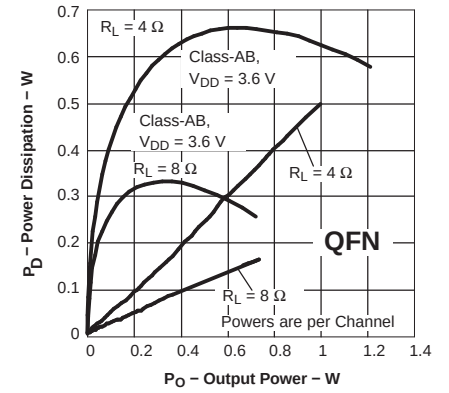


Figure 24.

POWER DISSIPATION VS OUTPUT POWER

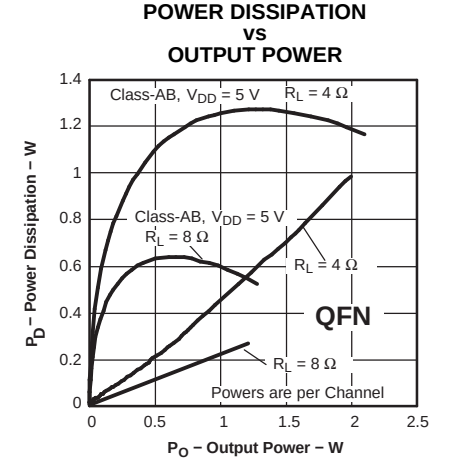


Figure 25.

EFFICIENCY VS OUTPUT POWER

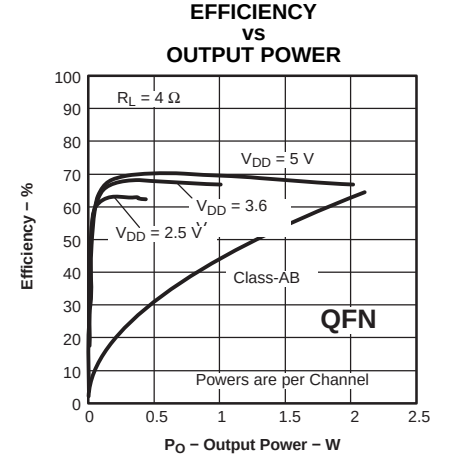


Figure 26.

EFFICIENCY VS OUTPUT POWER

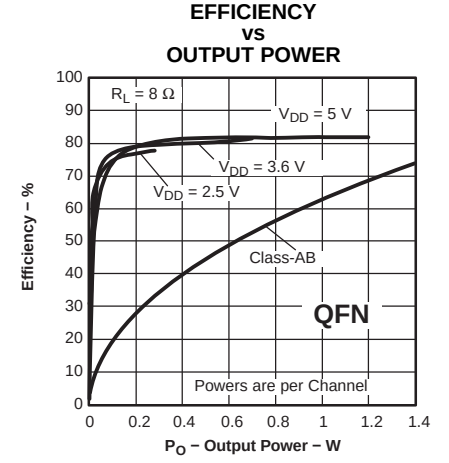


Figure 27.

TYPICAL CHARACTERISTICS (continued)

POWER DISSIPATION VS OUTPUT POWER

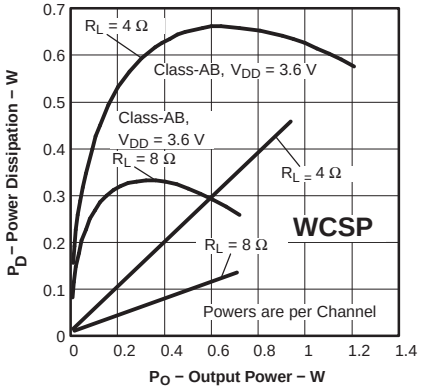


Figure 28.

POWER DISSIPATION VS OUTPUT POWER

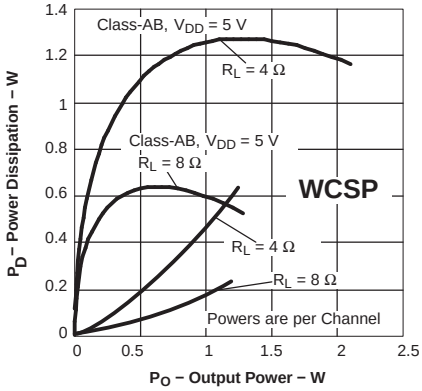


Figure 29.

EFFICIENCY VS OUTPUT POWER

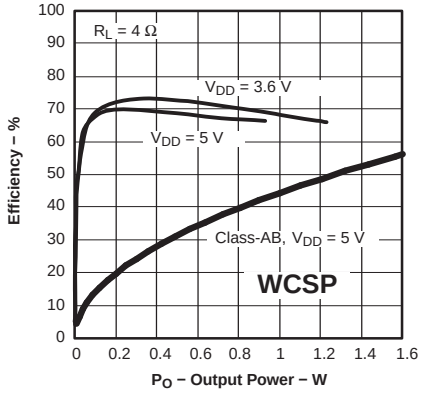


Figure 30.

EFFICIENCY VS OUTPUT POWER

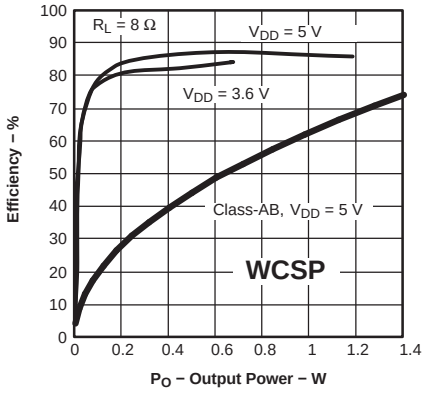


Figure 31.

OUTPUT POWER VS SUPPLY VOLTAGE

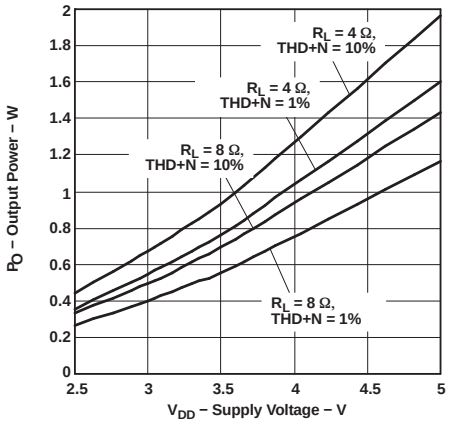
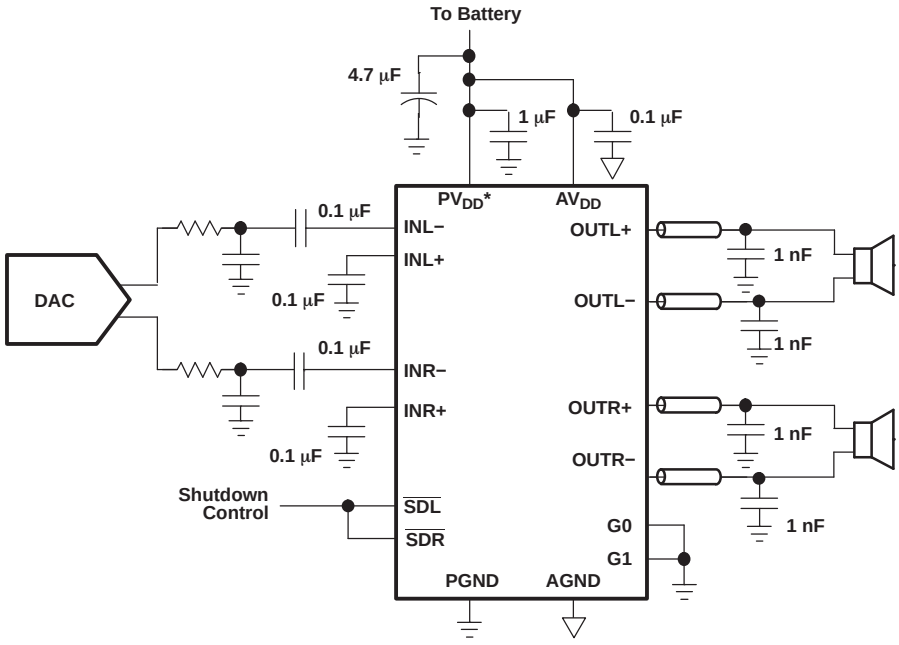


Figure 32.

APPLICATION INFORMATION



* For QFN, an additional capacitor is recomended for the second PV_{DD} pin.

Figure 33. Typical Application Circuit

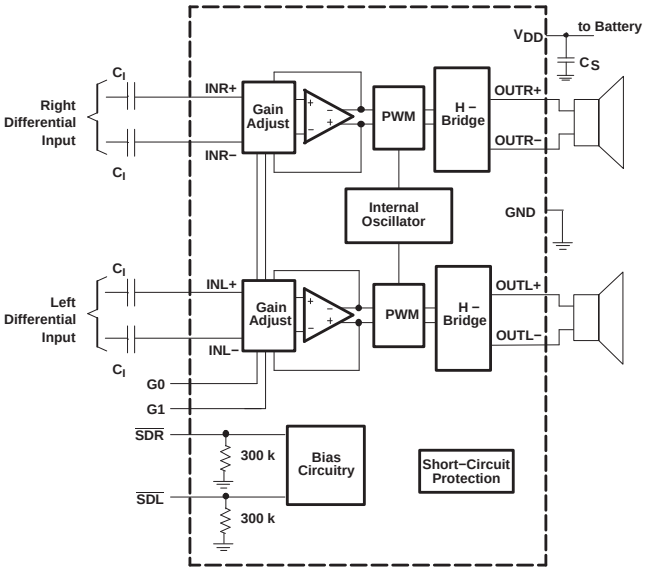


Figure 34. TPA2012D2 Application Schematic With Differential Input and Input Capacitors

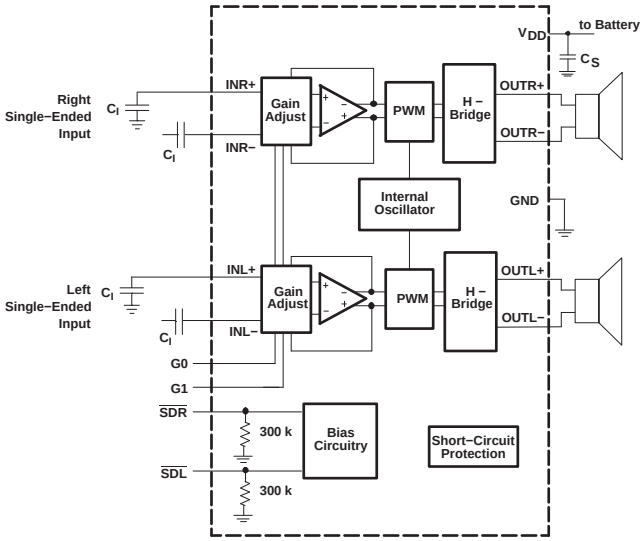


Figure 35. TPA2012D2 Application Schematic With Single-Ended Input

Decoupling Capacitor (C_S)

The TPA2012D2 is a high-performance Class-D audio amplifier that requires adequate power supply decoupling to ensure the efficiency is high and total harmonic distortion (THD) is low. For higher frequency transients, spikes, or digital hash on the line a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1 µF, placed as close as possible to the device PV_{DD} lead works best. Placing this decoupling capacitor close to the TPA2012D2 is important for the efficiency of the Class-D amplifier, because any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency. For filtering lower-frequency noise signals, a 4.7 µF or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

Table 1. Gain Setting

G1	G0	GAIN (V/V)	GAIN (dB)	INPUT IMPEDANCE (R_I) (kΩ)
0	0	2	6	28.1
0	1	4	12	17.3
1	0	8	18	9.8
1	1	16	24	5.2

Input Capacitors (C_I)

The TPA2012D2 does not require input coupling capacitors if the design uses a differential source that is biased from 0.5 V to V_{DD} – 0.8 V. If the input signal is not biased within the recommended common-mode input range, if high pass filtering is needed (see Figure 34), or if using a single-ended source (see Figure 35), input coupling capacitors are required.

The input capacitors and input resistors form a high-pass filter with the corner frequency, f_c, determined in Equation 1.

$$f_C = \frac{1}{\left(2\pi R_I C_I\right)} \tag{1}$$

The value of the input capacitor is important to consider as it directly affects the bass (low frequency) performance of the circuit. Speakers in wireless phones cannot usually respond well to low frequencies, so the corner frequency can be set to block low frequencies in this application. Not using input capacitors can increase output offset.

Equation 2 is used to solve for the input coupling capacitance.

$$C_I = \frac{1}{\left(2\pi R_I f_C\right)} \tag{2}$$

If the corner frequency is within the audio band, the capacitors should have a tolerance of ±10% or better, because any mismatch in capacitance causes an impedance mismatch at the corner frequency and below.

BOARD LAYOUT

In making the pad size for the WCSP balls, it is recommended that the layout use nonsolder mask defined (NSMD) land. With this method, the solder mask opening is made larger than the desired land area, and the opening size is defined by the copper pad width. Figure 36 and Table 2 shows the appropriate diameters for a WCSP layout. The TPA2012D2 evaluation module (EVM) layout is shown in the next section as a layout example.

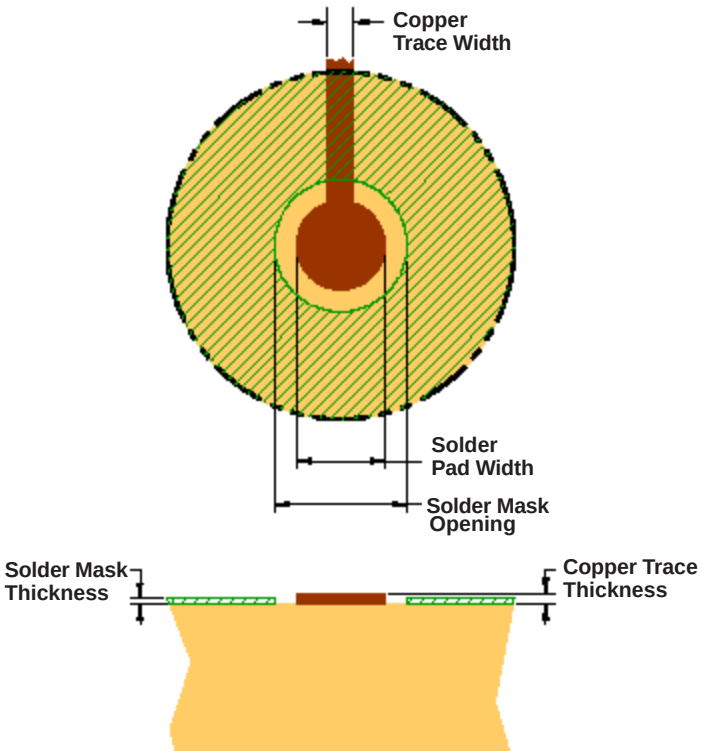


Figure 36. Land Pattern Dimensions

Table 2. Land Pattern Dimensions(1)(2)(3)(4)

SOLDER PAD DEFINITIONS	COPPER PAD	SOLDER MASK (5) OPENING	COPPER THICKNESS	STENCIL (6)(7) OPENING	STENCIL THICKNESS
Nonsolder mask defined (NSMD)	275 µm (+0.0, -25 µm)	375 µm (+0.0, -25 µm)	1 oz max (32 µm)	275 µm x 275 µm Sq. (rounded corners)	125 µm thick

(1) Circuit traces from NSMD defined PWB lands should be 75 µm to 100 µm wide in the exposed area inside the solder mask opening. Wider trace widths reduce device stand off and impact reliability.
(2) Best reliability results are achieved when the PWB laminate glass transition temperature is above the operating the range of the intended application.
(3) Recommend solder paste is Type 3 or Type 4.
(4) For a PWB using a Ni/Au surface finish, the gold thickness should be less 0.5 mm to avoid a reduction in thermal fatigue performance.
(5) Solder mask thickness should be less than 20 µm on top of the copper circuit pattern
(6) Best solder stencil performance is achieved using laser cut stencils with electro polishing. Use of chemically etched stencils results in inferior solder paste volume control.
(7) Trace routing away from WCSP device should be balanced in X and Y directions to avoid unintentional component movement due to solder wetting forces.

Component Location

Place all the external components very close to the TPA2012D2. Placing the decoupling capacitor, C_S, close to the TPA2012D2 is important for the efficiency of the Class-D amplifier. Any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency.

Trace Width

Recommended trace width at the solder balls is 75 µm to 100 µm to prevent solder wicking onto wider PCB traces.

For high current pins (PV_{DD}, PGND, and audio output pins) of the TPA2012D2, use 100-µm trace widths at the solder balls and at least 500-µm PCB traces to ensure proper performance and output power for the device.

For the remaining signals of the TPA2012D2, use 75-µm to 100-µm trace widths at the solder balls. The audio input pins (INR+/- and INL+/-) must run side-by-side to maximize common-mode noise cancellation.

EFFICIENCY AND THERMAL INFORMATION

The maximum ambient temperature depends on the heat-sinking ability of the PCB system. The derating factor for the packages are shown in the dissipation rating table. Converting this to θ_{JA} for the QFN package:

$$\theta_{JA} = \frac{1}{\text{Derating Factor}} = \frac{1}{0.041} = 24°C/W \quad (3)$$

Given θ_{JA} of 24°C/W, the maximum allowable junction temperature of 150°C, and the maximum internal dissipation of 1.5W (0.75 W per channel) for 2.1 W per channel, 4-Ω load, 5-V supply, from Figure 25, the maximum ambient temperature can be calculated with the following equation.

$$T_A Max = T_J Max - \theta_{JA} P_{Dmax} = 150 - 24\,(1.5) = 114°C \quad (4)$$

Equation 4 shows that the calculated maximum ambient temperature is 114°C at maximum power dissipation with a 5-V supply and 4-Ω a load. The TPA2012D2 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Also, using speakers more resistive than 4-Ω dramatically increases the thermal performance by reducing the output current and increasing the efficiency of the amplifier.

OPERATION WITH DACs AND CODECs

In using Class-D amplifiers with CODECs and DACs, sometimes there is an increase in the output noise floor from the audio amplifier. This occurs when mixing of the output frequencies of the CODEC/DAC mix with the switching frequencies of the audio amplifier input stage. The noise increase can be solved by placing a low-pass filter between the CODEC/DAC and audio amplifier. This filters off the high frequencies that cause the problem and allow proper performance. See Figure 33 for the block diagram.

FILTER FREE OPERATION AND FERRITE BEAD FILTERS

A ferrite bead filter can often be used if the design is failing radiated emissions without an LC filter and the frequency sensitive circuit is greater than 1 MHz. This filter functions well for circuits that just have to pass FCC and CE because FCC and CE only test radiated emissions greater than 30 MHz. When choosing a ferrite bead, choose one with high impedance at high frequencies, and very low impedance at low frequencies. In addition, select a ferrite bead with adequate current rating to prevent distortion of the output signal.

Use an LC output filter if there are low frequency (< 1 MHz) EMI sensitive circuits and/or there are long leads from amplifier to speaker.

Figure 37 shows typical ferrite bead and LC output filters.

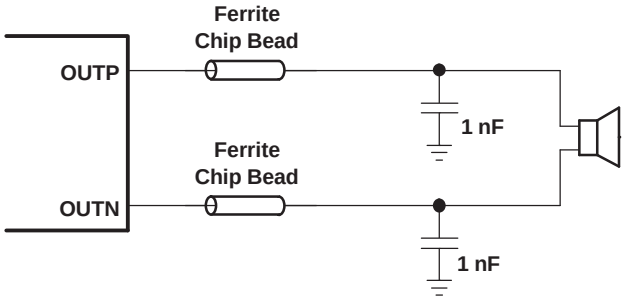


Figure 37. Typical Ferrite Chip Bead Filter (Chip bead example: TDK: MPZ1608S221A)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPA2012D2RTJR	ACTIVE	QFN	RTJ	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPA2012D2RTJRG4	ACTIVE	QFN	RTJ	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPA2012D2RTJT	ACTIVE	QFN	RTJ	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPA2012D2RTJTG4	ACTIVE	QFN	RTJ	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPA2012D2YZHR	ACTIVE	DSBGA	YZH	16	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPA2012D2YZHT	ACTIVE	DSBGA	YZH	16	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

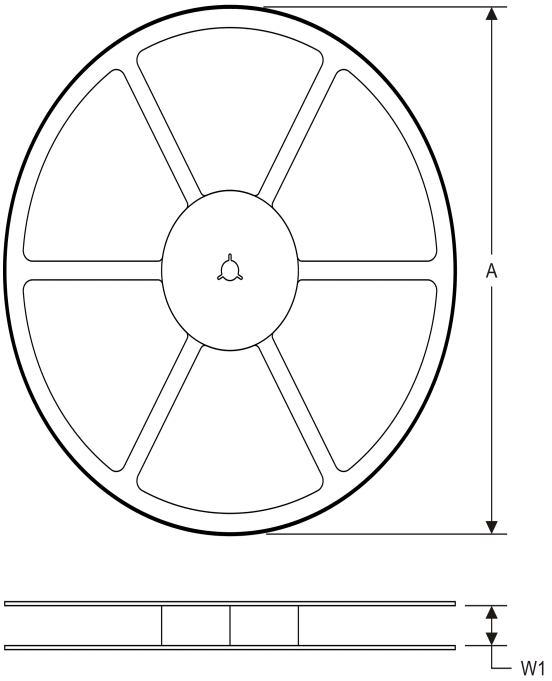
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

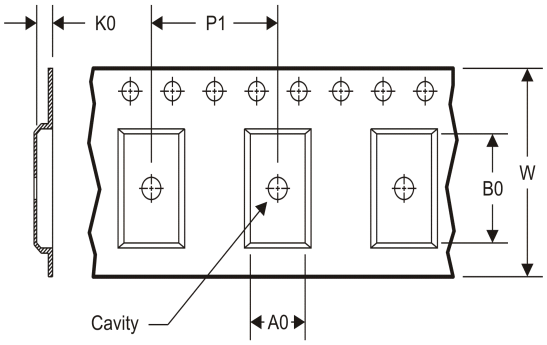
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



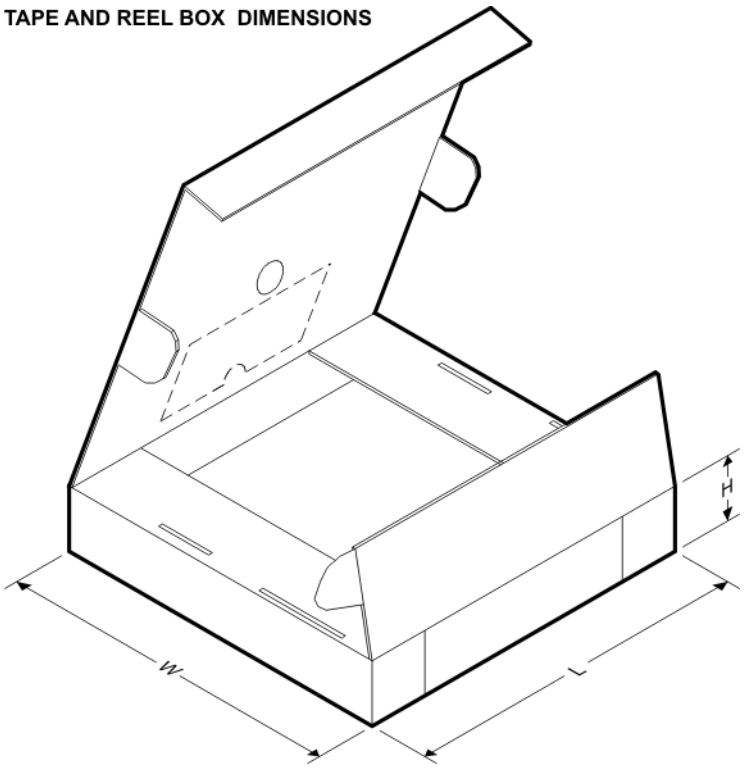
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA2012D2RTJR	QFN	RTJ	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPA2012D2RTJR	QFN	RTJ	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPA2012D2RTJT	QFN	RTJ	20	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPA2012D2YZHR	DSBGA	YZH	16	3000	178.0	8.4	2.18	2.18	0.81	4.0	8.0	Q1
TPA2012D2YZHR	DSBGA	YZH	16	3000	180.0	8.4	2.18	2.18	0.81	4.0	8.0	Q1
TPA2012D2YZHT	DSBGA	YZH	16	250	180.0	8.4	2.18	2.18	0.81	4.0	8.0	Q1
TPA2012D2YZHT	DSBGA	YZH	16	250	178.0	8.4	2.18	2.18	0.81	4.0	8.0	Q1

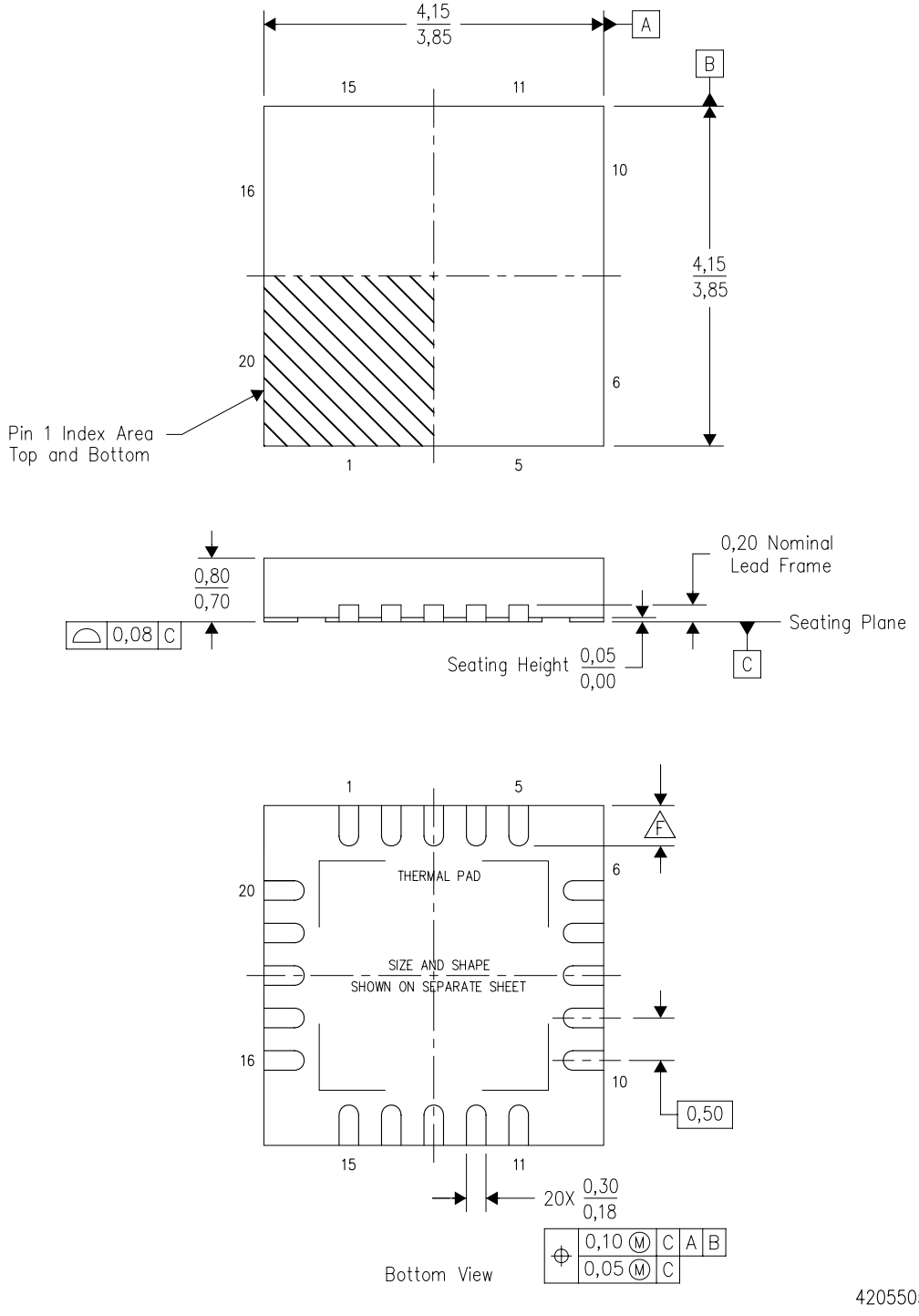
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA2012D2RTJR	QFN	RTJ	20	3000	367.0	367.0	35.0
TPA2012D2RTJR	QFN	RTJ	20	3000	367.0	367.0	35.0
TPA2012D2RTJT	QFN	RTJ	20	250	210.0	185.0	35.0
TPA2012D2YZHR	DSBGA	YZH	16	3000	217.0	193.0	35.0
TPA2012D2YZHR	DSBGA	YZH	16	3000	210.0	185.0	35.0
TPA2012D2YZHT	DSBGA	YZH	16	250	210.0	185.0	35.0
TPA2012D2YZHT	DSBGA	YZH	16	250	217.0	193.0	35.0

RTJ (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Check thermal pad mechanical drawing in the product datasheet for nominal lead length dimensions.

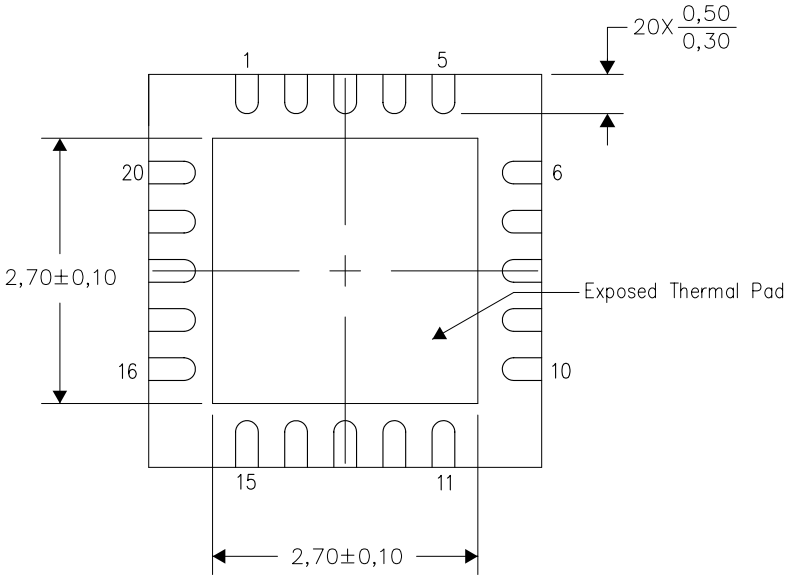
RTJ (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



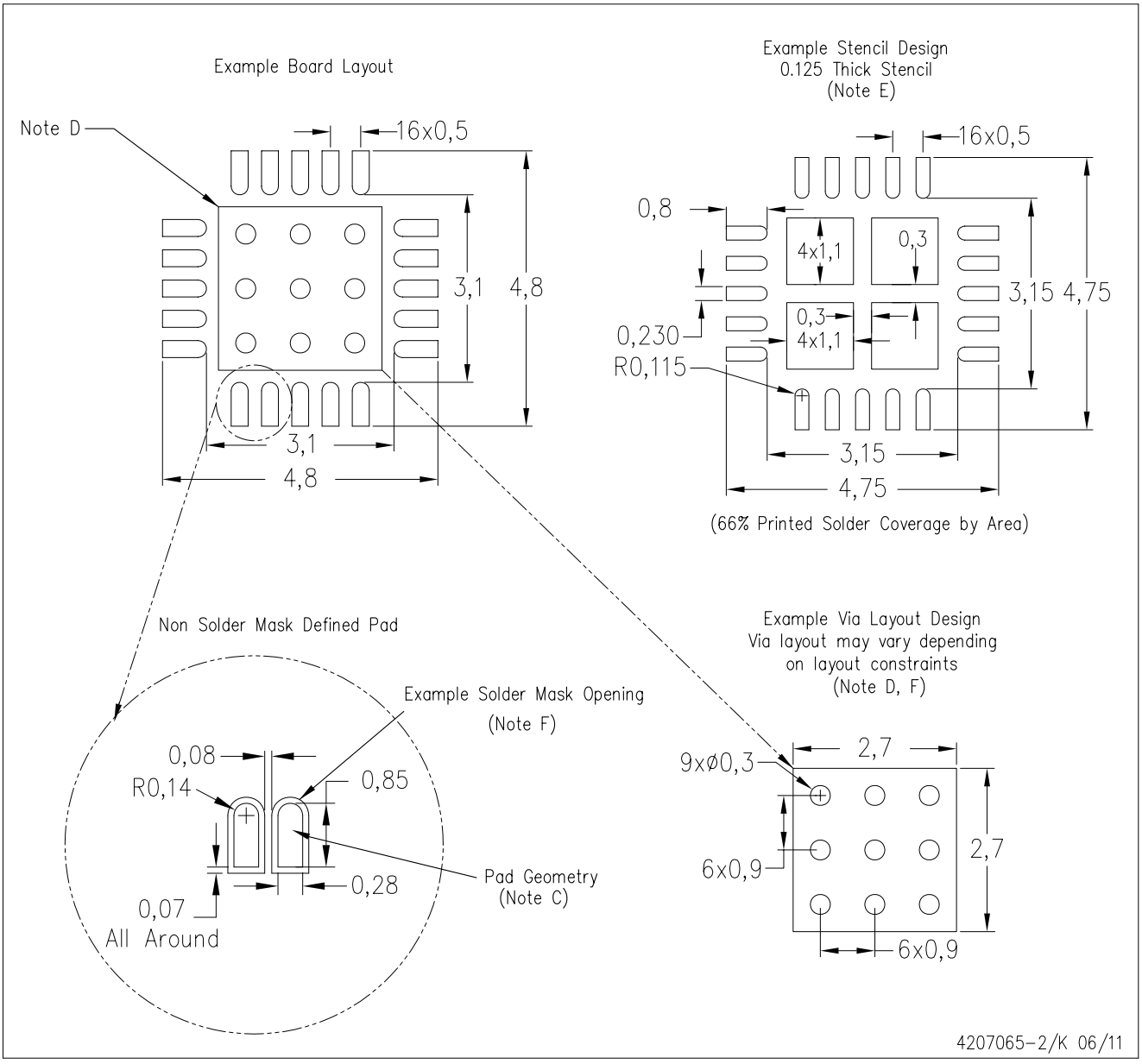
Bottom View

Exposed Thermal Pad Dimensions

4206256–2/Q 07/11

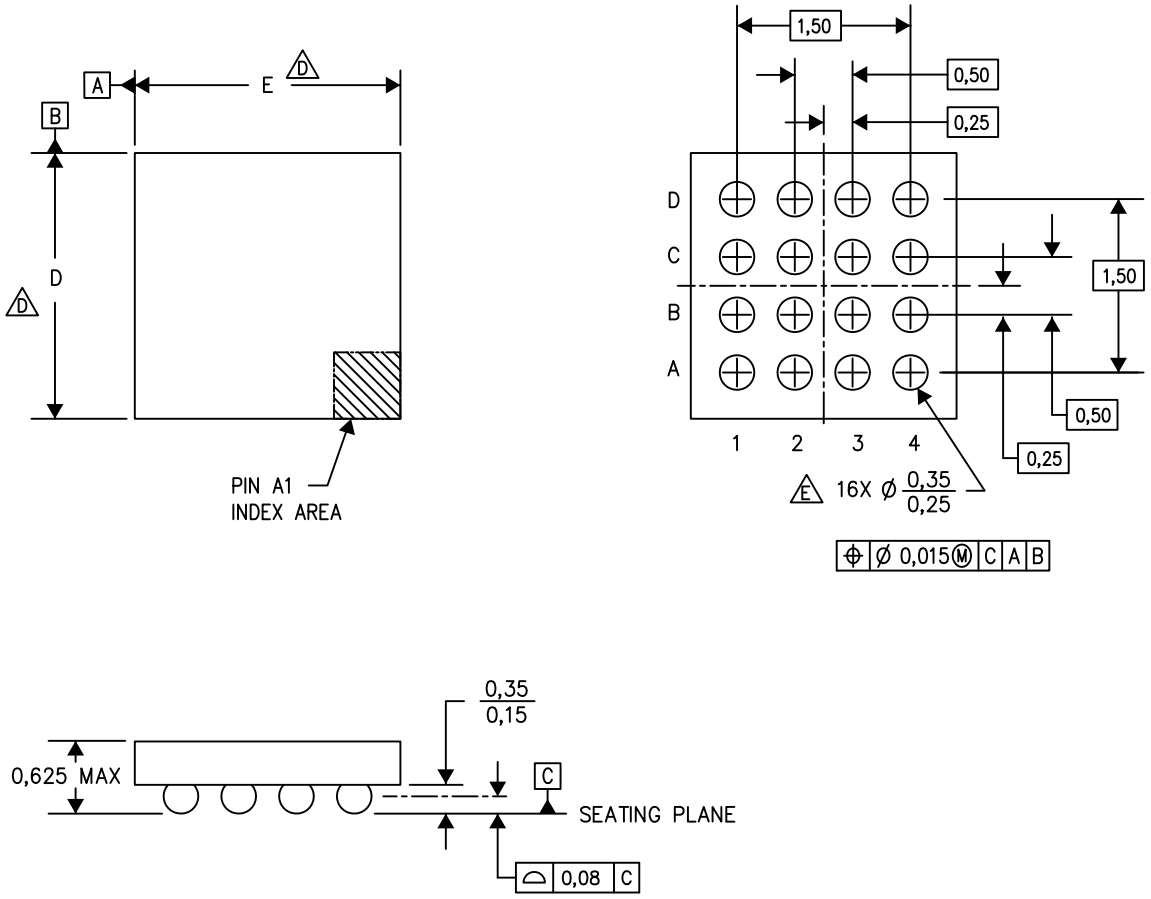
NOTE: All linear dimensions are in millimeters

RTJ (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

YZH (S–XBGA–N16) DIE–SIZE BALL GRID ARRAY



4205060/E 06/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
E. Reference Product Data Sheet for array population.
4 x 4 matrix pattern is shown for illustration only.
F. This package contains Pb–free balls.
Refer to YEH (Drawing #4204183) for tin–lead (SnPb) balls.

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