DIRECTPATH™ Stereo Headphone Amplifier With Differential Input and HI-Z Mode

FEATURES

- **Patented DirectPath™ Technology Eliminates Need for DC-Blocking Capacitors**
  - **Outputs Biased at 0 V**
  - **Excellent Low Frequency Fidelity**
- **Active Click and Pop Suppression**
- **HI-Z Output Mode**
- **2.1 mA Typical Supply Current**
- **Fully Differential or Single-Ended Inputs**
  - **Built-In Resistors Reduces Component Count**
  - **Improves System Noise Performance**
- **Constant Maximum Output Power from 2.3 V to 5.5 V Supply**
  - **Simplifies Design to Prevent Acoustic Shock**
- **Improved RF Noise Immunity**
- **Microsoft™ Windows Vista™ Compliant**
- **High Power Supply Noise Rejection**
  - **100 dB PSRR at 217 Hz**
  - **90 dB PSRR at 10 kHz**
- **Wide Power Supply Range: 2.3 V to 5.5 V**
- **Gain Settings: 0 dB and 6 dB**
- **Short-Circuit and Thermal-Overload Protection**
- **±8 kV HBM ESD Protected Outputs**
- **Small Package Available**
  - **16-Pin, 3 mm × 3 mm Thin QFN**

APPLICATIONS

- **Smart Phones / Cellular Phones**
- **Notebook Computers**
- **CD / MP3 Players**
- **Portable Gaming**

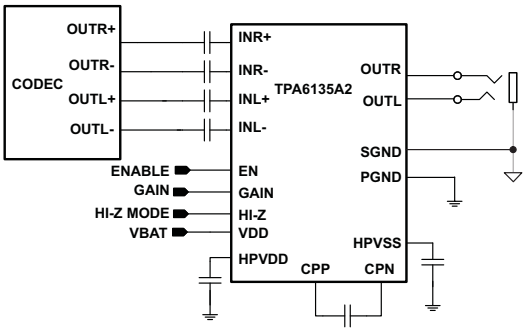
DESCRIPTION

The TPA6135A2 (sometimes referred to as TPA6135) is a DirectPath™ stereo headphone amplifier that eliminates the need for external dc-blocking output capacitors. Differential stereo inputs and built-in resistors set the device gain, further reducing external component count. Gain is selectable at 0 dB or 6 dB. The amplifier drives 25 mW into 16 Ω speakers from a single 2.3 V supply. The TPA6135A2 (TPA6135) provides a constant maximum output power independent of the supply voltage, thus facilitating the design for prevention of acoustic shock.

The TPA6135A2 (TPA6135) features HI-Z mode which can set the outputs to a high impedance configuration. The fully differential inputs reduce system noise pickup between the audio source and the headphone amplifier. The high power supply noise rejection performance and differential architecture provide increased RF noise immunity. For single-ended input signals, connect INL+ and INR+ to ground.

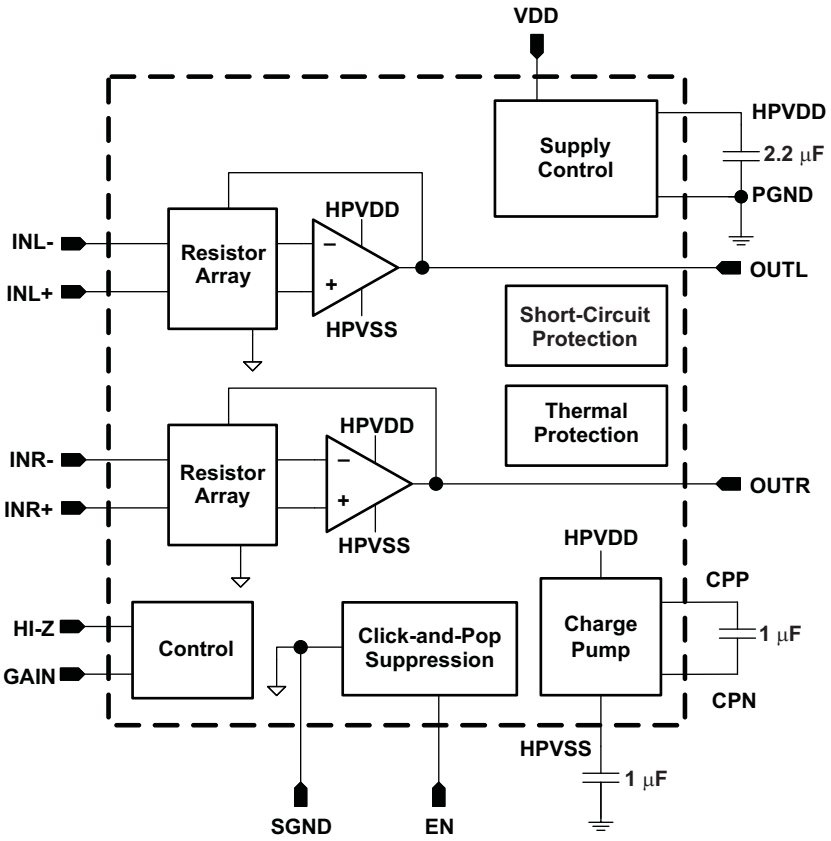
The device has built-in pop suppression circuitry to completely eliminate disturbing pop noise during turn-on and turn-off. The amplifier outputs have short-circuit and thermal-overload protection along with ±8 kV HBM ESD protection, simplifying end equipment compliance to the IEC 61000-4-2 ESD standard.

The TPA6135A2 (TPA6135) operates from a single 2.3 V to 5.5 V supply with 2.1 mA of typical supply current. Shutdown mode reduces supply current to less than 1 μA.



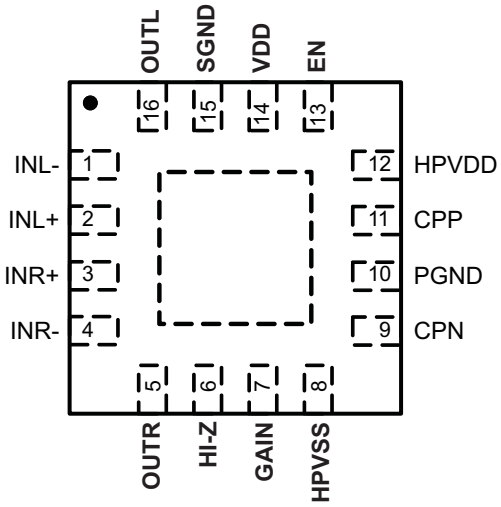
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FUNCTIONAL BLOCK DIAGRAM



DEVICE PINOUT

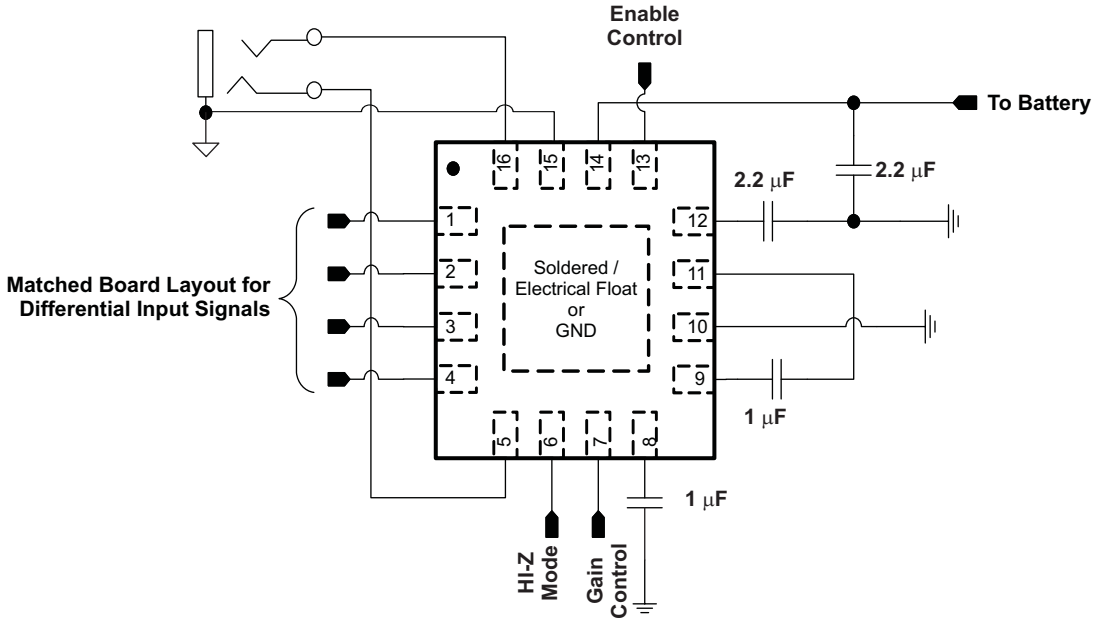
RTE (QFN) PACKAGE
(TOP VIEW)



PIN FUNCTIONS

PIN		I/O/P	PIN DESCRIPTION
NAME	QFN		
INL-	1	I	Inverting left input for differential signals; left input for single-ended signals
INL+	2	I	Non-inverting left input for differential signals. Connect to ground for single-ended input applications
INR+	3	I	Non-inverting right input for differential signals. Connect to ground for single-ended input applications
INR-	4	I	Inverting right input for differential signals; right input for single-ended signals
OUTR	5	O	Right headphone amplifier output. Connect to right terminal of headphone jack
HI-Z	6	I	Output impedance select. Set to logic LOW for normal operation and to logic HIGH for high output impedance
GAIN	7	I	Gain select. Set to logic LOW for a gain of 0dB and to logic HIGH for a gain of 6dB
HPVSS	8	P	Charge pump output and negative power supply for output amplifiers; connect 1µF capacitor to GND
CPN	9	P	Charge pump negative flying cap. Connect to negative side of 1µF capacitor between CPP and CPN
PGND	10	P	Ground
CPP	11	P	Charge pump positive flying cap. Connect to positive side of 1µF capacitor between CPP and CPN
HPVDD	12	P	Positive power supply for headphone amplifiers. Connect to a 2.2µF capacitor. Do not connect to VDD
EN	13	I	Amplifier enable. Connect to logic LOW to shutdown; connect to logic HIGH to activate
VDD	14	P	Positive power supply for TPA6135A2
SGND	15	I	Amplifier reference voltage. Connect to ground terminal of headphone jack
OUTL	16	O	Left headphone amplifier output. Connect to left terminal of headphone jack
Thermal Pad	–	P	Solder the exposed metal pad on the TPA6135A2RTE QFN package to the landing pad on the PCB. Connect the landing pad to ground or leave it electrically unconnected (floating).

BOARD LAYOUT CONCEPT



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range, T_A = 25°C (unless otherwise noted)

			VALUE / UNIT
	Supply voltage, VDD		–0.3 V to 6.0 V
	Headphone amplifier supply voltage, HPVDD (do not connect to external supply)		–0.3 V to 1.9 V
V_I	Input voltage (INR+, INR-, INL+, INL-)		1.4 V_{RMS}
	Output continuous total power dissipation		See Dissipation Rating Table
T_A	Operating free-air temperature range		–40°C to 85°C
T_J	Operating junction temperature range		–40°C to 150°C
T_{stg}	Storage temperature range		–65°C to 150°C
	ESD Protection – HBM	OUTL, OUTR	8 kV
		All Other Pins	2 kV

ORDERING GUIDE

T_A	PACKAGED DEVICES(1)	PART NUMBER(2)	SYMBOL
–40°C to 85°C	16-pin, 3 mm × 3 mm Thin QFN	TPA6135A2RTER	AOTI
		TPA6135A2RTET	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) The RTE packages is only available taped and reeled. The suffix “R” indicates a reel of 3000, the suffix “T” indicates a reel of 250

DISSIPATION RATINGS TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR (1)	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
RTE (QFN)	2567 mW	48.7 °C/W	1643 mW	1335 mW

(1) See JEDEC Standard 51-3 for Low-K board, JEDEC Standard 51-7 for High-K board, and JEDEC Standard 51-12 for using package thermal information. See JEDEC document page for downloadable copies: http://www.jedec.org/download/default.cfm.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
	Supply voltage, VDD	2.3	5.5	V
V_{IH}	High-level input voltage; EN, GAIN, HI-Z	1.3		V
V_{IL}	Low-level input voltage; EN, GAIN, HI-Z		0.6	V
	Voltage applied to Output; OUTR, OUTL (when EN = 0 V)	–0.3	3.6	V
	Voltage applied to Output; OUTR, OUTL (when EN ≥ 1.3 V and HI-Z ≥ 1.3 V)	–1.8	1.8	V
T_A	Operating free-air temperature	–40	85	°C

ELECTRICAL CHARACTERISTICS

T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output offset voltage		–0.5		0.5	mV
Power supply rejection ratio	V_{DD} = 2.3 V to 5.5 V		100		dB
High-level intput current (EN, HI-Z, GAIN)				1	µA
Low-level intput current (EN, HI-Z, GAIN)				1	µA
Supply Current	V_{DD} = 2.3 V, No load, EN = V_{DD}, HI-Z = 0 V		2.1	2.8	mA
	V_{DD} = 3.6 V, No load, EN = V_{DD}, HI-Z = 0 V		2.1	2.8	
	V_{DD} = 5.5 V, No load, EN = V_{DD}, HI-Z = 0 V		2.2	2.9	
	V_{DD} = 2.3 to 5.5 V, No load, EN = HI-Z = V_{DD}		0.7	1	
Shutdown Supply Current	EN = 0 V, V_{DD} = 2.3 V to 5.5 V		0.7	1.2	µA

OPERATING CHARACTERISTICS

V_{DD} = 3.6 V , T_A = 25°C, R_L = 16 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power(1) (Outputs in phase)	THD = 1%, f = 1 kHz		25		mW
		THD = 1%, f = 1 kHz, R_L = 32 Ω		22		
V_O	Output voltage(1) (Outputs in phase)	THD = 1%, f = 1 kHz, R_L = 100 Ω		1.1		V_{RMS}
A_V	Closed-loop voltage gain (OUT / IN–)	GAIN = 0 V, (0 dB)	–0.95	–1.0	–1.05	V/V
		GAIN ≥ 1.3 V, (6 dB)	–1.95	–2.0	–2.05	
ΔA_v	Gain matching	Between Left and Right channels		1%		
R_{IN}	Input impedance (per input pin)	GAIN = 0 V, (0 dB)		19.8		kΩ
		GAIN ≥ 1.3 V, (6 dB)		13.2		
	Input impedance in shutdown (per input pin)	EN = 0 V		10		kΩ
V_{CM}	Input common-mode voltage range		–0.5		1.5	V
	Output impedance	EN = HI-Z ≥ 1.3 V, f = 10 kHz		40		kΩ
		EN = HI-Z ≥ 1.3 V, f = 1 MHz		4.5		
		EN = HI-Z ≥ 1.3 V, f = 10 MHz		0.75		
		EN = 0 V (shutdown mode)		25		Ω
	Input-to-output attenuation in shutdown	EN = 0 V		80		dB
k_{SVR}	AC-power supply rejection ratio	200 mV_{pp} ripple, f = 217 Hz		-100		dB
		200 mV_{pp} ripple, f = 10 kHz		-90		
THD+N	Total harmonic distortion plus noise(2)	P_O = 20 mW, f = 1 kHz		0.02%		
		P_O = 25 mW into 32 Ω, V_{DD} = 5.5 V, f = 1 kHz		0.01%		
SNR	Signal-to-noise ratio	P_O = 20 mW; GAIN = 0 V, (A_V = 0 dB)		100		dB
E_n	Noise output voltage	A-weighted		5.5		μV_{RMS}
f_{osc}	Charge pump switching frequency		1200	1275	1350	kHz
t_{ON}	Start-up time from shutdown			5		ms
	Crosstallk	P_O = 20 mW, f = 1 kHz		–80		dB
	Thermal shutdown	Threshold		150		°C
		Hysteresis		20		°C

(1) Per output channel
(2) A-weighted

TYPICAL CHARACTERISTICS

T_A = 25°C, V_{DD} = 3.6 V, Gain = 0 dB, EN = 3.6 V, C_{HPVDD} = C_{HPVSS} = 2.2 µF, C_{INPUT} = C_{FLYING} = 1 µF, Outputs in Phase

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

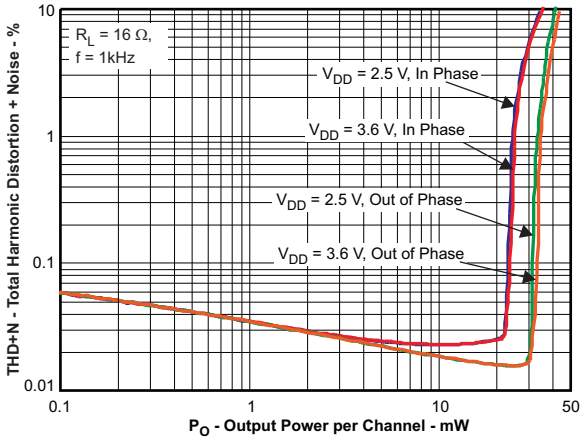


Figure 1.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

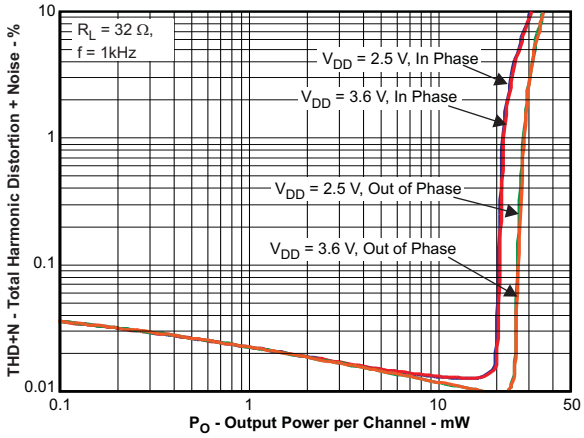


Figure 2.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

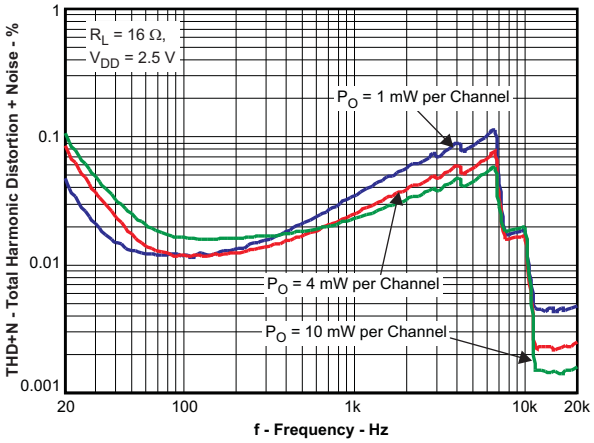


Figure 3.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

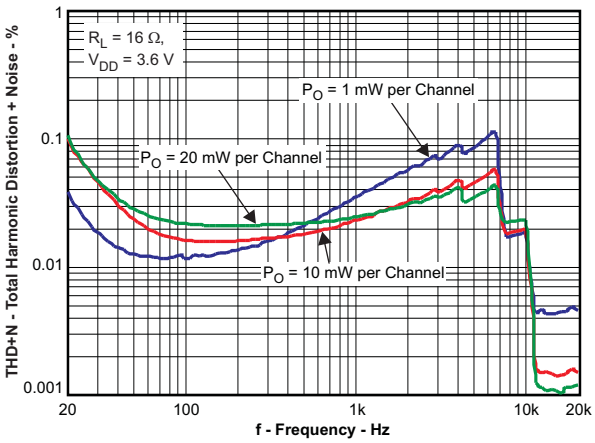


Figure 4.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

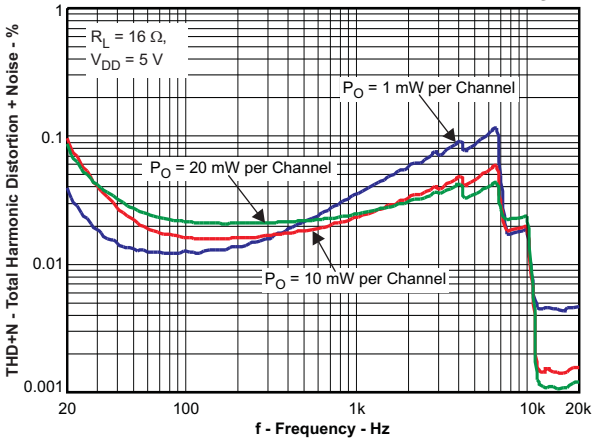


Figure 5.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

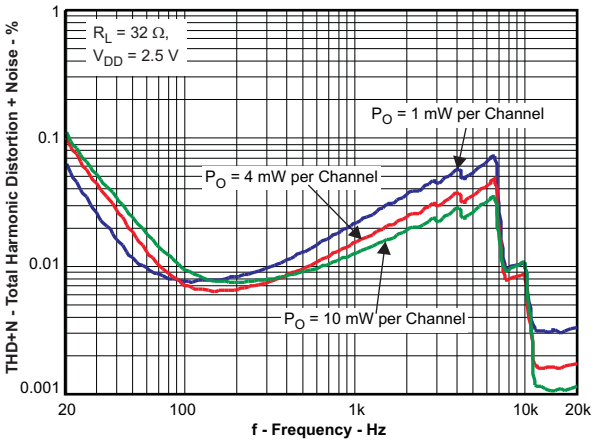


Figure 6.

TYPICAL CHARACTERISTICS (continued)

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

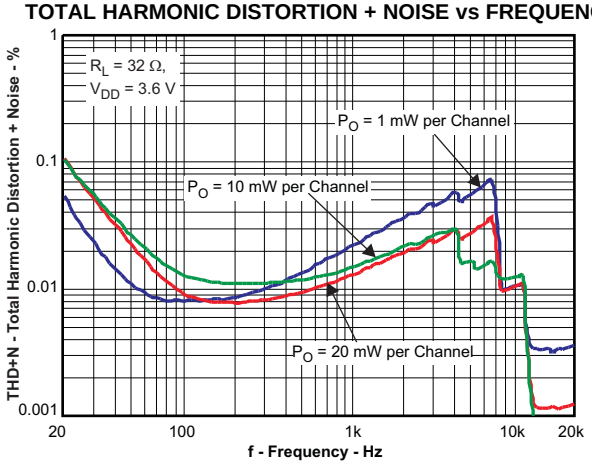


Figure 7.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

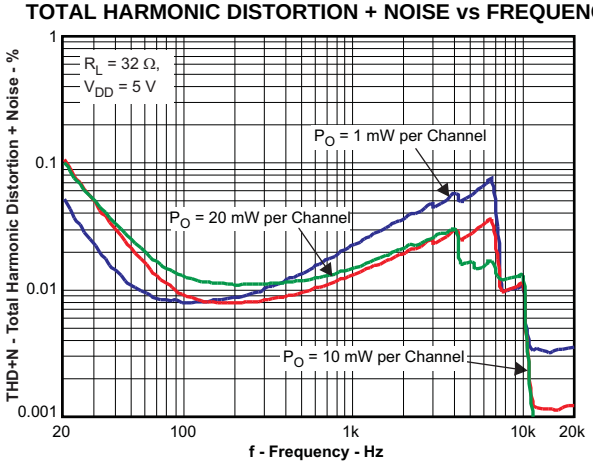


Figure 8.

OUTPUT POWER vs SUPPLY VOLTAGE

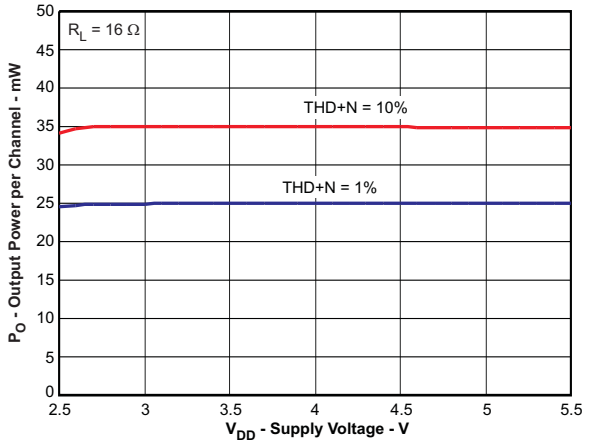


Figure 9.

OUTPUT POWER vs SUPPLY VOLTAGE

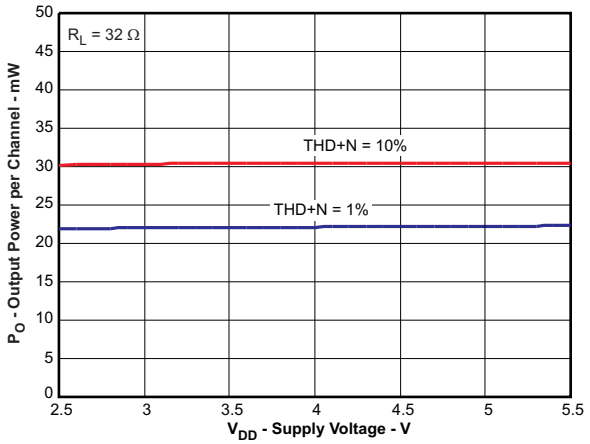


Figure 10.

OUTPUT POWER vs LOAD RESISTANCE

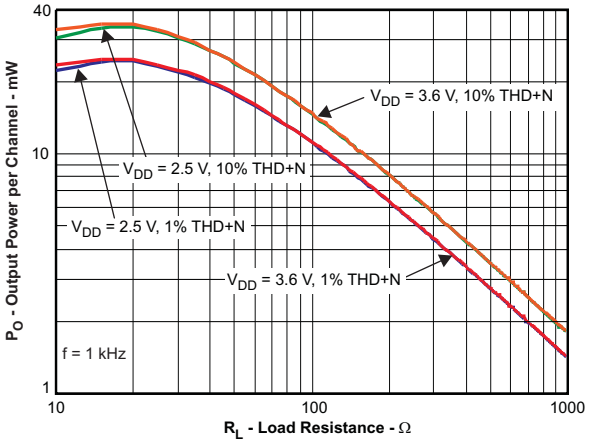


Figure 11.

OUTPUT POWER vs LOAD RESISTANCE

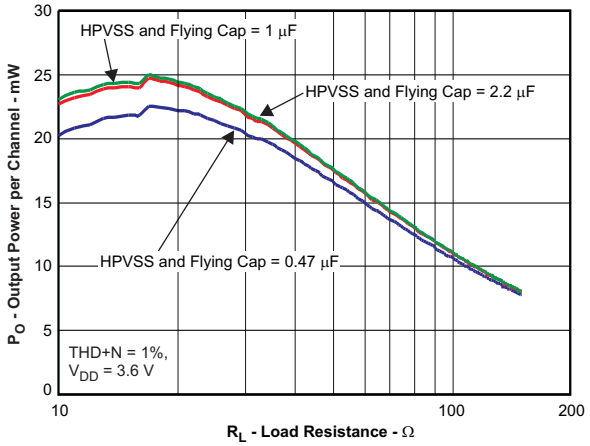


Figure 12.

TYPICAL CHARACTERISTICS (continued)

OUTPUT VOLTAGE vs SUPPLY VOLTAGE

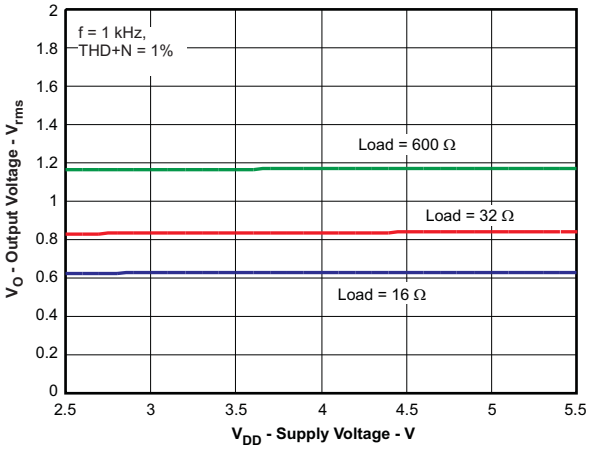


Figure 13.

SUPPLY VOLTAGE REJECTION RATIO vs FREQUENCY

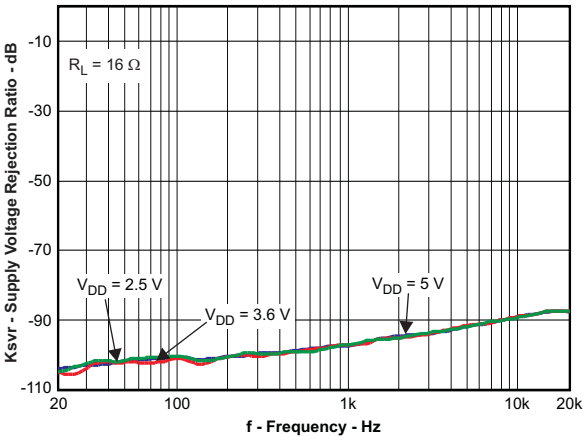


Figure 14.

SUPPLY VOLTAGE REJECTION RATIO vs FREQUENCY

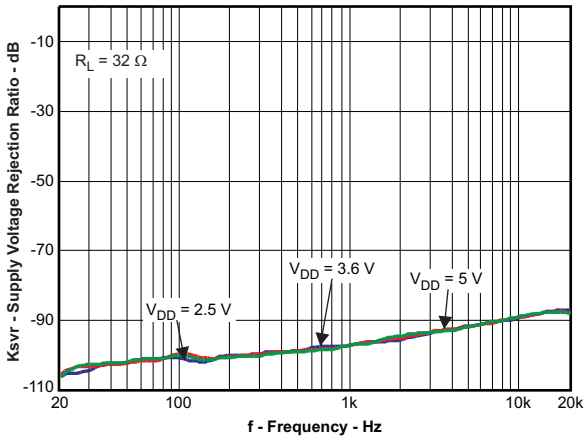


Figure 15.

QUIESCENT SUPPLY CURRENT vs SUPPLY VOLTAGE

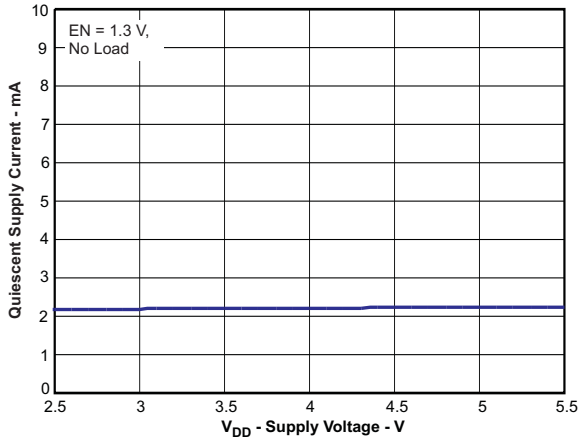


Figure 16.

SUPPLY CURRENT vs TOTAL OUTPUT POWER

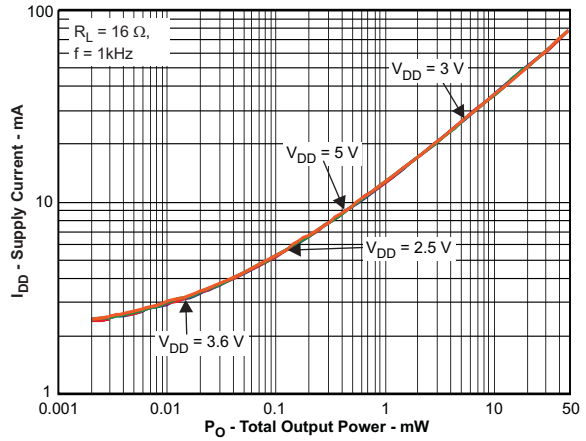


Figure 17.

SUPPLY CURRENT vs TOTAL OUTPUT POWER

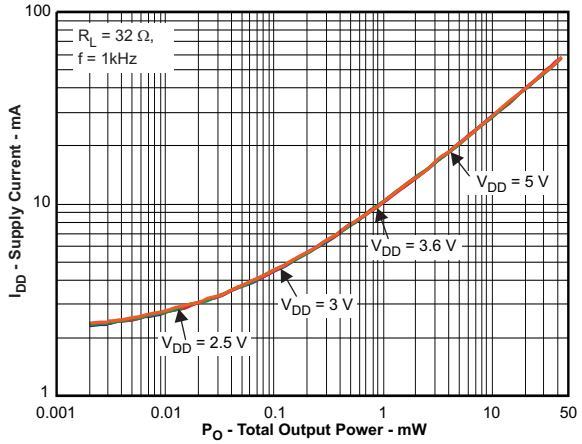


Figure 18.

TYPICAL CHARACTERISTICS (continued)

CROSSTALK vs FREQUENCY

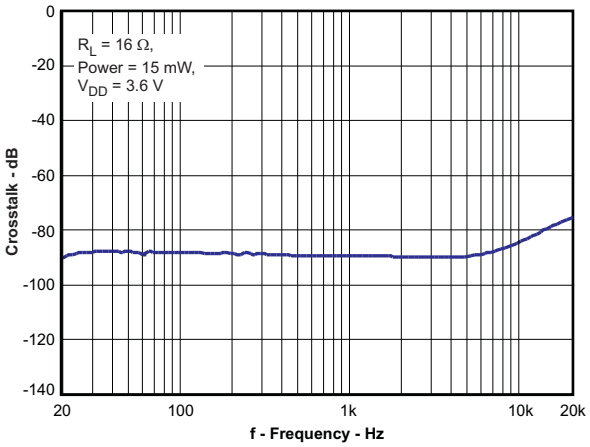


Figure 19.

OUTPUT SPECTRUM vs FREQUENCY

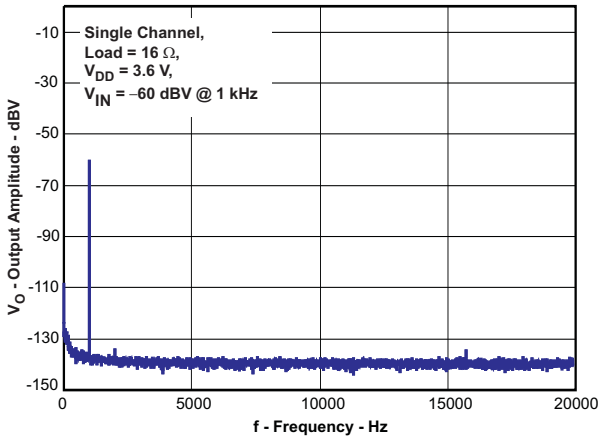


Figure 20.

HI-Z OUTPUT IMPEDANCE vs FREQUENCY

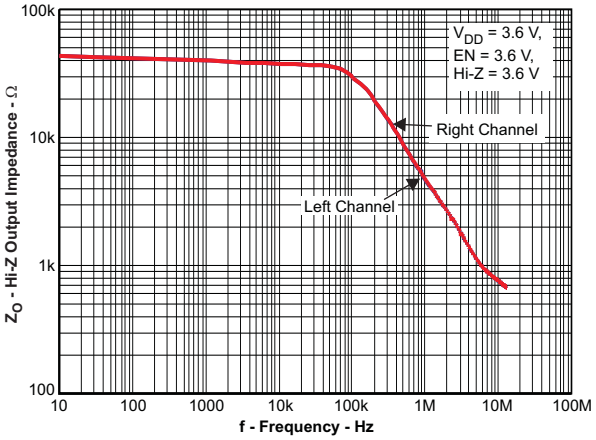


Figure 21.

STARTUP WAVEFORMS vs TIME

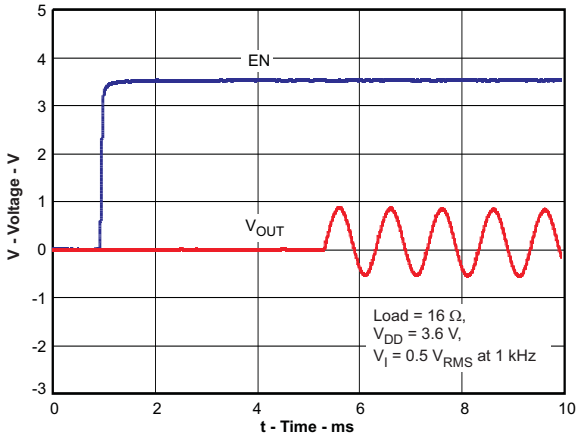


Figure 22.

SHUTDOWN WAVEFORMS vs TIME

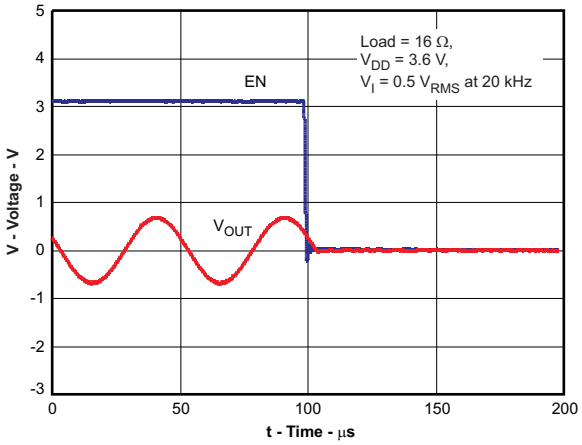


Figure 23.

APPLICATION INFORMATION

APPLICATION CIRCUIT

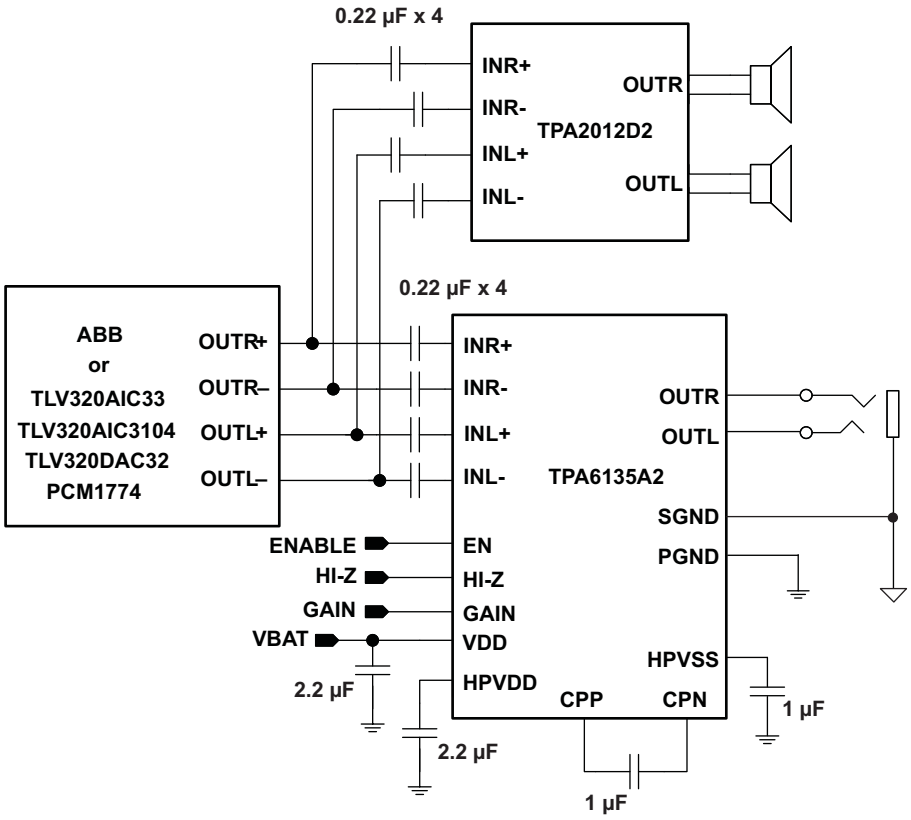


Figure 24. Typical Application Configuration with Differential Input Signals

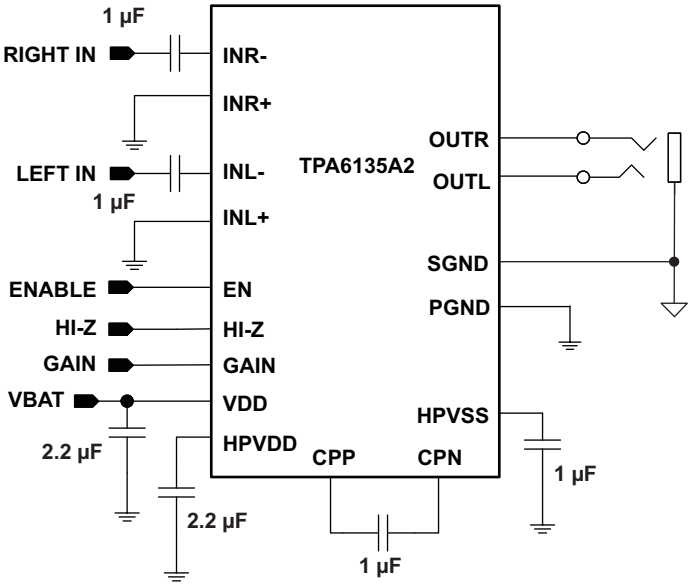


Figure 25. Typical Application Configuration with Single-Ended Input Signals

GAIN CONTROL

The TPA6135A2 has two gain settings which are controlled with the GAIN pin. The following table gives an overview of the gain function.

GAIN VOLTAGE	AMPLIFIER GAIN
≤ 0.6 V	0 dB
≥ 1.3 V	6 dB

Table 1. Windows Vista™ Premium Mobile Mode Specifications

Device Type	Requirement	Windows Premium Mobile Vista Specifications	TPA6135A2 Typical Performance
Analog Speaker Line Jack (R_L = 10 kΩ, FS = 0.707 Vrms)	THD+N	≤ –65 dB FS [20 Hz, 20 kHz]	–75 dB FS [20 Hz, 20 kHz]
	Dynamic Range with Signal Present	≤ –80 dB FS A-Weight	–100 dB FS A-Weight
	Line Output Crosstalk	≤ –60 dB [20 Hz, 20 kHz]	–90 dB [20 Hz, 20 kHz]
Analog Headphone Out Jack (R_L = 32Ω, FS = 0.300 Vrms)	THD+N	≤ –45 dB FS [20 Hz, 20 kHz]	–65 dB FS [20 Hz, 20 kHz]
	Dynamic Range with Signal Present	≤ –80 dB FS A-Weight	–94 dB FS A-Weight
	Headphone Output Crosstalk	≤ –60 dB [20 Hz, 20 kHz]	–90 dB [20 Hz, 20 kHz]

High Output Impedance

The TPA6135A2 has a HI-Z control pin that increases output impedance while mutting the amplifier. Apply a voltage greater than 1.3 V to the HI-Z and EN pin to activate the HI-Z mode. This feature allows the headphone output jack to be shared for other functions besides audio. For example, sharing of a headphone jack between audio and video as shwon in Figure 26. The TPA6135A2 output impedance is high enough to prevent attenuating the video signal.

Enable Voltage	HI-Z Voltage	Output Impedance	Maximum External Voltage Applied to the Output Pins	Comments
≤ 0.6 V	≤ 0.6 V	20 Ω – 30 Ω	–0.3 V to 3.3 V(1)	Shutdown Mode
≤ 0.6 V	≥ 1.3 V	20 Ω –30 Ω		
≥ 1.3 V	≤ 0.6 V	≤ 1 Ω	–	Active Mode
≥ 1.3 V	≥ 1.3 V	40 kΩ @ 10 kHz	–1.8 V to 1.8 V	HI-Z Mode
		4.5 kΩ @ 1 MHz		
		750 Ω @ 10 MHz		

(1) If V_{DD} is < 3.3 V, then maximum allowed external voltage applied is V_{DD} in this mode

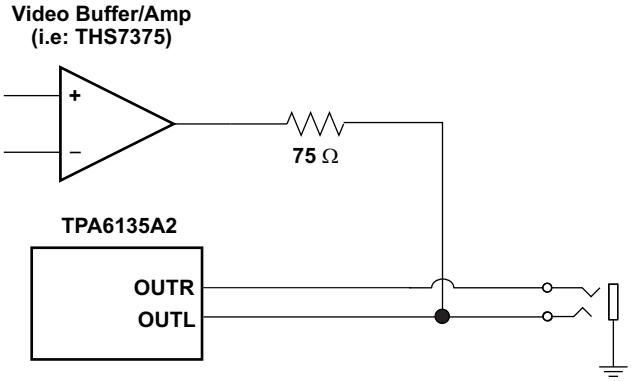


Figure 26. Sharing One Connector Between Audio and Video Signals Example

HEADPHONE AMPLIFIERS

Single-supply headphone amplifiers typically require dc-blocking capacitors to remove dc bias from their output voltage. The top drawing in Figure 27 illustrates this connection. If dc bias is not removed, large dc current will flow through the headphones which wastes power, clips the output signal, and potentially damages the headphones.

These dc-blocking capacitors are often large in value and size. Headphone speakers have a typical resistance between 16 Ω and 32 Ω. This combination creates a high-pass filter with a cutoff frequency as shown in Equation 1, where R_L is the load impedance, C_O is the dc-block capacitor, and f_C is the cutoff frequency.

$$f_c = \frac{1}{2\pi R_L C_O} \tag{1}$$

For a given high-pass cutoff frequency and load impedance, the required dc-blocking capacitor is found as:

$$C_O = \frac{1}{2\pi f_C R_L} \tag{2}$$

Reducing f_C improves low frequency fidelity and requires a larger dc-blocking capacitor. To achieve a 20 Hz cutoff with 16 Ω headphones, C_O must be at least 500 µF. Large capacitor values require large packages, consuming PCB area, increasing height, and increasing cost of assembly. During start-up or shutdown the dc-blocking capacitor has to be charged or discharged. This causes an audible pop on start-up and power-down. Large dc-blocking capacitors also reduce audio output signal fidelity.

Two different headphone amplifier architectures are available to eliminate the need for dc-blocking capacitors. The Capless amplifier architecture provides a reference voltage to the headphone connector shield pin as shown in the middle drawing of Figure 27. The audio output signals are centered around this reference voltage, which is typically half of the supply voltage to allow symmetrical output voltage swing.

When using a Capless amplifier do not connect the headphone jack shield to any ground reference or large currents will result. This makes Capless amplifiers ineffective for plugging non-headphone accessories into the headphone connector. Capless amplifiers are useful only with floating GND headphones.

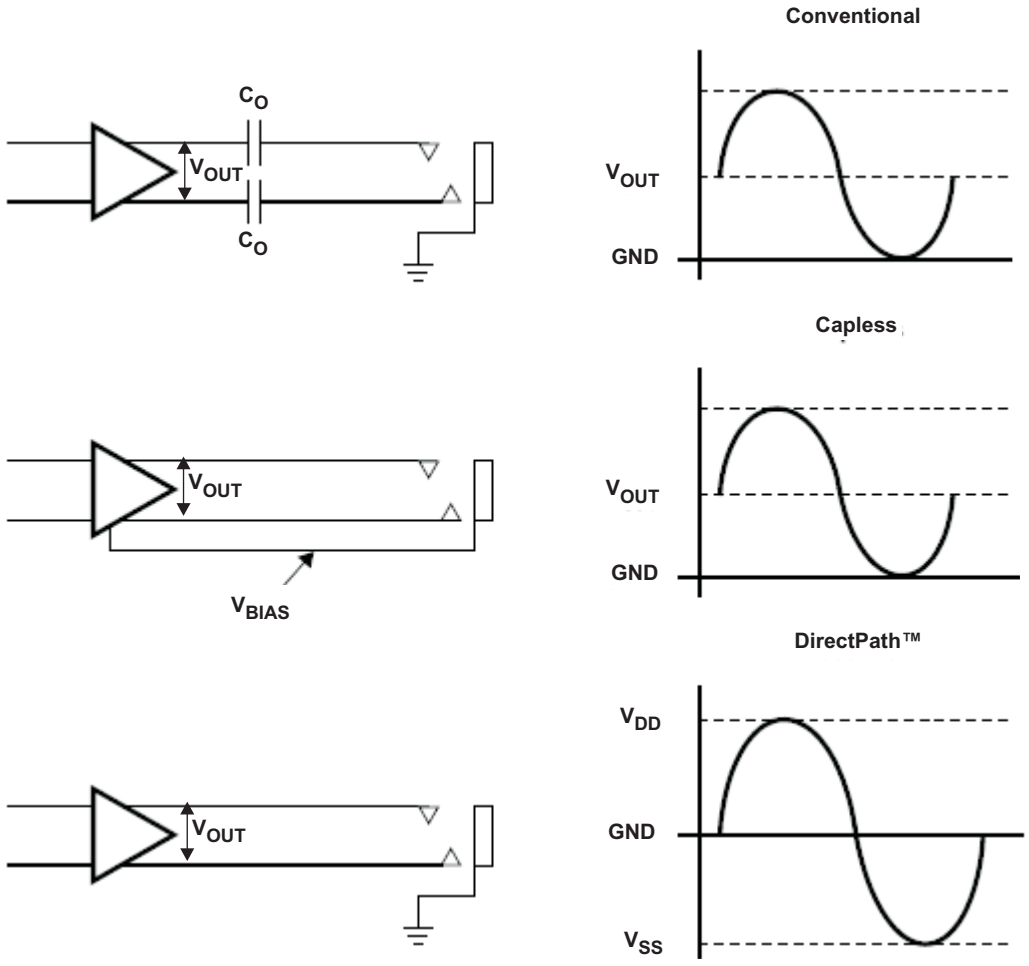


Figure 27. Amplifier Applications

The DirectPath™ amplifier architecture operates from a single supply voltage and uses an internal charge pump to generate a negative supply rail for the headphone amplifier. The output voltages are centered around 0 V and are capable of positive and negative voltage swings as shown in the bottom drawing of Figure 27. DirectPath amplifiers require no output dc-blocking capacitors. The headphone connector shield pin connects to ground and will interface with headphones and non-headphone accessories. The TPA6135A2 is a DirectPath amplifier.

ELIMINATING TURN-ON POP AND POWER SUPPLY SEQUENCING

The TPA6135A2 has excellent noise and turn-on / turn-off pop performance. It uses an integrated click-and-pop suppression circuit to allow fast start-up and shutdown without generating any voltage transients at the output pins. Typical start-up time from shutdown is 5 ms.

DirectPath technology keeps the output dc voltage at 0 V even when the amplifier is powered up. The DirectPath technology together with the active pop-and-click suppression circuit eliminates audible transients during start up and shutdown.

Use input coupling capacitors to ensure inaudible turn-on pop. Activate the TPA6135A2 after all audio sources have been activated and their output voltages have settled. On power-down, deactivate the TPA6135A2 before deactivating the audio input source. The EN pin controls device shutdown: Set to 0.6 V or lower to deactivate the TPA6135A2; set to 1.3 V or higher to activate.

RF AND POWER SUPPLY NOISE IMMUNITY

The TPA6135A2 employs a new differential amplifier architecture to achieve high power supply noise rejection and RF noise rejection. RF and power supply noise are common in modern electronics. Although RF frequencies are much higher than the 20 kHz audio band, signal modulation often falls in-band. This, in turn, modulates the supply voltage, allowing a coupling path into the audio amplifier. A common example is the 217 Hz GSM frame-rate buzz often heard from an active speaker when a cell phone is placed nearby during a phone call.

The TPA6135A2 has excellent rejection of power supply and RF noise, preventing audio signal degradation.

CONSTANT MAXIMUM OUTPUT POWER AND ACOUSTIC SHOCK PREVENTION

Typically the output power increases with increasing supply voltage on an unregulated headphone amplifier. The TPA6135A2 maintains a constant output power independent of the supply voltage. Thus the design for prevention of acoustic shock (hearing damage due to exposure to a loud sound) is simplified since the output power will remain constant, independent of the supply voltage. This feature allows maximizing the audio signal at the lowest supply voltage.

INPUT COUPLING CAPACITORS

Input coupling capacitors block any dc bias from the audio source and ensure maximum dynamic range. Input coupling capacitors also minimize TPA6135A2 turn-on pop to an inaudible level.

The input capacitors are in series with TPA6135A2 internal input resistors, creating a high-pass filter. Equation 3 calculates the high-pass filter corner frequency. The input impedance, RIN, is dependent on device gain. Larger input capacitors decrease the corner frequency. See the Operating Characteristics table for input impedance values.

$$f_C = \frac{1}{2\pi R_{IN} C_{IN}} \tag{3}$$

For a given high-pass cutoff frequency, the minimum input coupling capacitor is found as:

$$C_{IN} = \frac{1}{2\pi f_C R_{IN}} \tag{4}$$

Example: Design for a 20 Hz corner frequency with a TPA6135A2 gain of +6 dB. The Operating Characteristics table gives RIN as 13.2 kΩ. Equation 4 shows the input coupling capacitors must be at least 0.6 µF to achieve a 20 Hz high-pass corner frequency. Choose a 0.68 µF standard value capacitor for each TPA6135A2 input (X5R material or better is required for best performance).

Input capacitors can be removed provided the TPA6135A2 inputs are driven differentially with less than ±1 V_{RMS} and the common-mode voltage is within the input common-mode range of the amplifier. Without input capacitors turn-on pop performance may be degraded and should be evaluated in the system.

CHARGE PUMP FLYING CAPACITOR AND HPVSS CAPACITOR

The TPA6135A2 uses a built-in charge pump to generate a negative voltage supply for the headphone amplifiers. The charge pump flying capacitor connects between CPP and CPN. It transfers charge to generate the negative supply voltage. The HPVSS capacitor must be at least equal in value to the flying capacitor to allow maximum charge transfer. Use low equivalent-series-resistance (ESR) ceramic capacitors (X5R material or better is required for best performance) to maximize charge pump efficiency. Typical values are 1 µF to 2.2 µF for the HPVSS and flying capacitors. Although values down to 0.47 µF can be used, total harmonic distortion (THD) will increase.

POWER SUPPLY AND HPVDD DECOUPLING CAPACITORS AND CONNECTIONS

The TPA6135A2 DirectPath headphone amplifier requires adequate power supply decoupling to ensure that output noise and total harmonic distortion (THD) remain low. Use good low equivalent-series-resistance (ESR) ceramic capacitors (X5R material or better is required for best performance). Place a 2.2 μF capacitor within 5 mm of the VDD pin. Reducing the distance between the decoupling capacitor and VDD minimizes parasitic inductance and resistance, improving TPA6135A2 supply rejection performance. Use 0402 or smaller size capacitors if possible. Ensure that the ground connection of each of the capacitors has a minimum length return path to the device. Failure to properly decouple the TPA6135A2 may degrade audio or EMC performance.

For additional supply rejection, connect an additional 10 μF or higher value capacitor between VDD and ground. This will help filter lower frequency power supply noise. The high power supply rejection ratio (PSRR) of the TPA6135A2 makes the 10 μF capacitor unnecessary in most applications.

Connect a 2.2 μF capacitor between HPVDD and ground. This ensures the amplifier internal bias supply remains stable and maximizes headphone amplifier performance.

WARNING:

DO NOT connect HPVDD directly to VDD or an external supply voltage. The voltage at HPVDD is generated internally. Connecting HPVDD to an external voltage can damage the device.

LAYOUT RECOMMENDATIONS

EXPOSED PAD ON TPA6135A2RTE

Solder the exposed metal pad on the TPA6135A2RTE QFN package to the landing pad on the PCB. Connect the landing pad to ground or leave it electrically unconnected (floating). *Do not connect the landing pad to VDD or to any other power supply voltage*.

If the pad is grounded, it must be connected to the same ground as the PGND pin (10). See the layout and mechanical drawings at the end of the data sheet for proper sizing. Soldering the thermal pad is required for mechanical reliability and enhances thermal conductivity of the package.

WARNING:

DO NOT connect the TPA6135A2RTE exposed metal pad to VDD or any other power supply voltage.

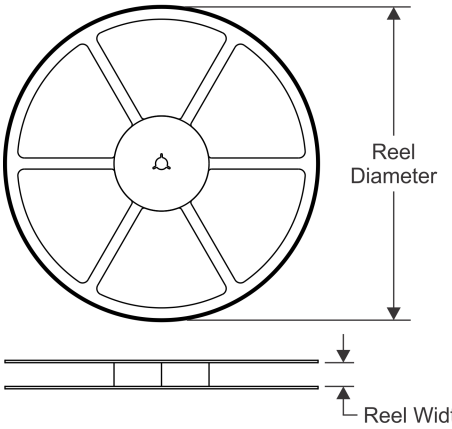
GND CONNECTIONS

The SGND pin is an input reference and must be connected to the headphone ground connector pin. This ensures no turn-on pop and minimizes output offset voltage. Do not connect more than ±0.3 V to SGND.

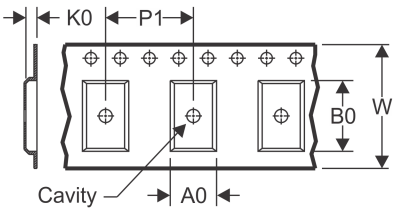
PGND is a power ground. Connect supply decoupling capacitors for VDD, HPVDD, and HPVSS to PGND.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

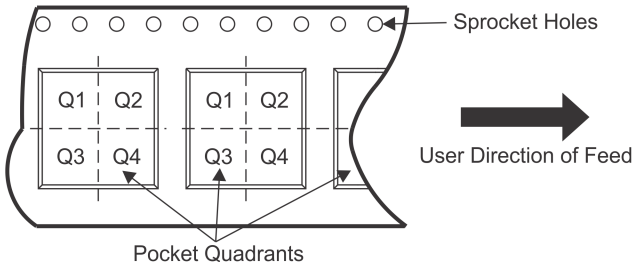


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

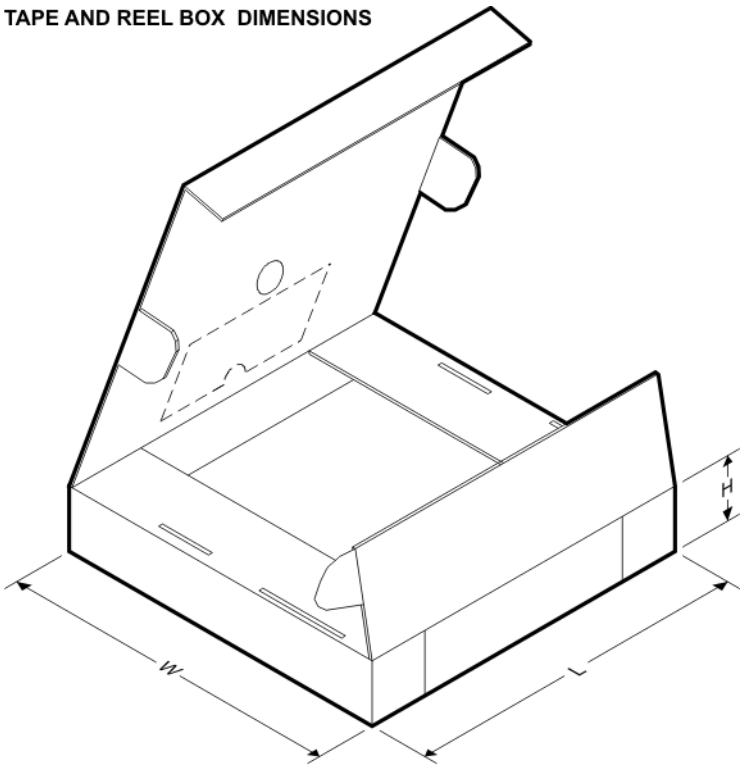
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA6135A2RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TPA6135A2RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPA6135A2RTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TPA6135A2RTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

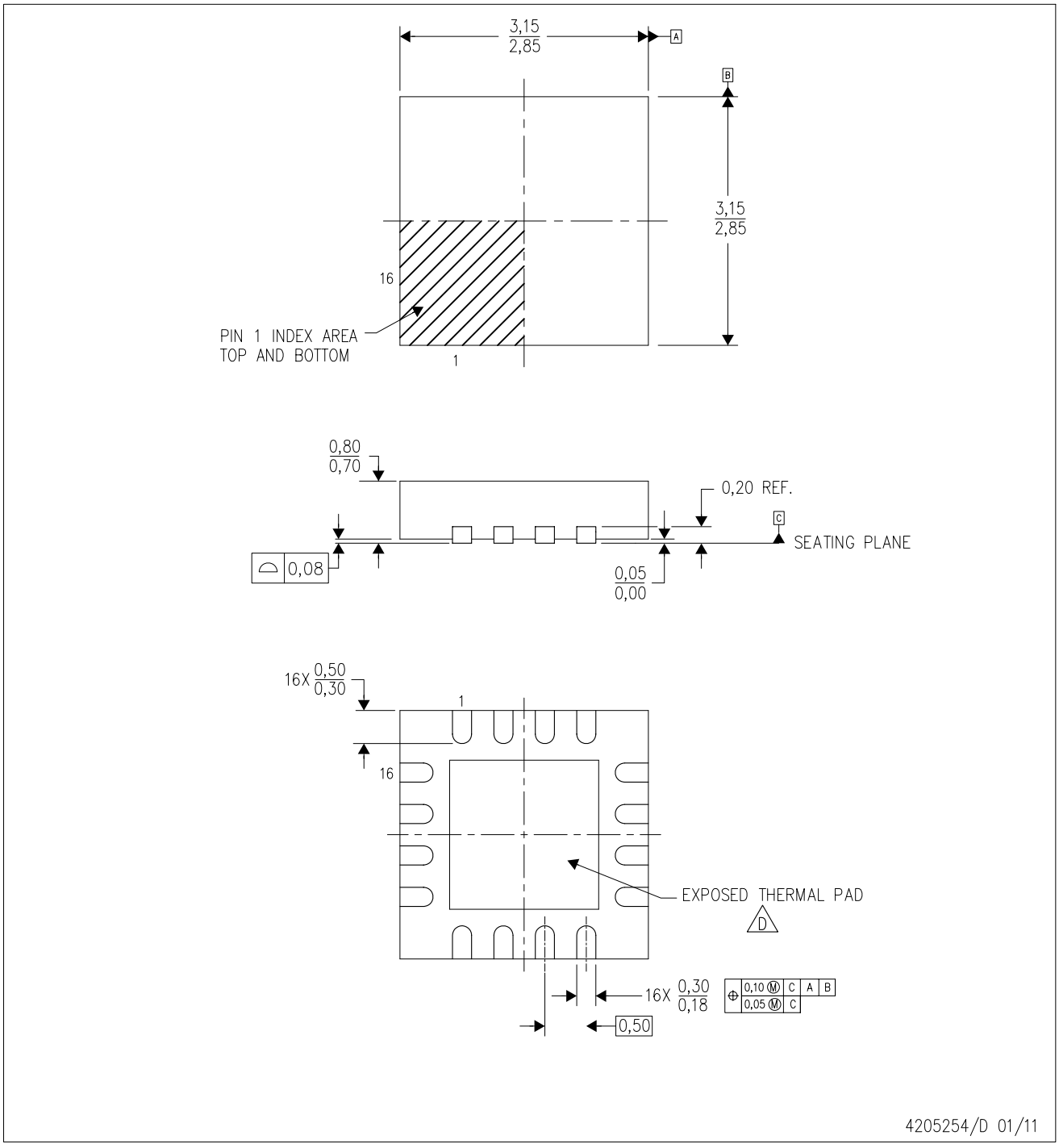
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA6135A2RTER	WQFN	RTE	16	3000	370.0	355.0	55.0
TPA6135A2RTER	WQFN	RTE	16	3000	367.0	367.0	35.0
TPA6135A2RTET	WQFN	RTE	16	250	195.0	200.0	45.0
TPA6135A2RTET	WQFN	RTE	16	250	210.0	185.0	35.0

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

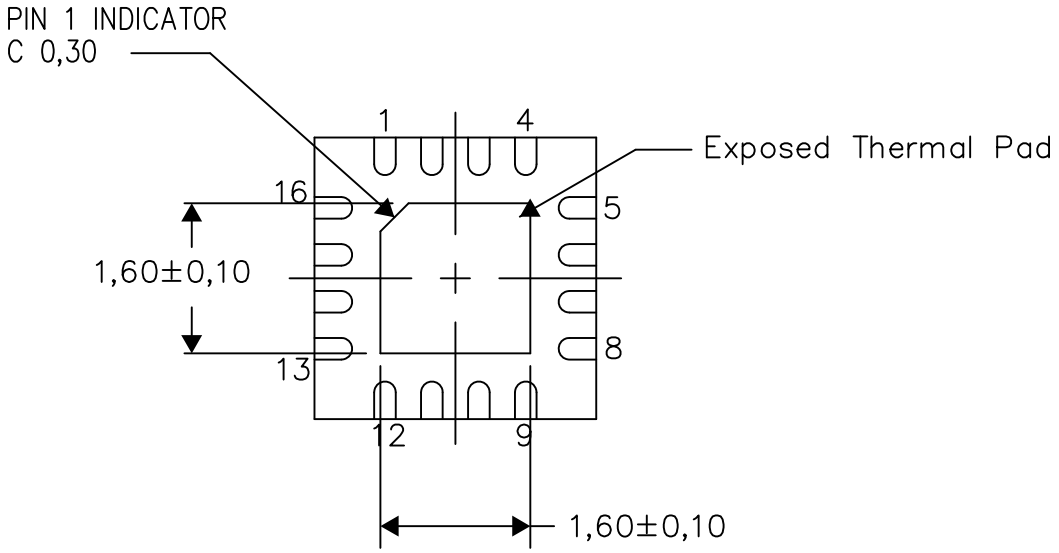
RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206446–2/N 07/13

NOTE: A. All linear dimensions are in millimeters

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

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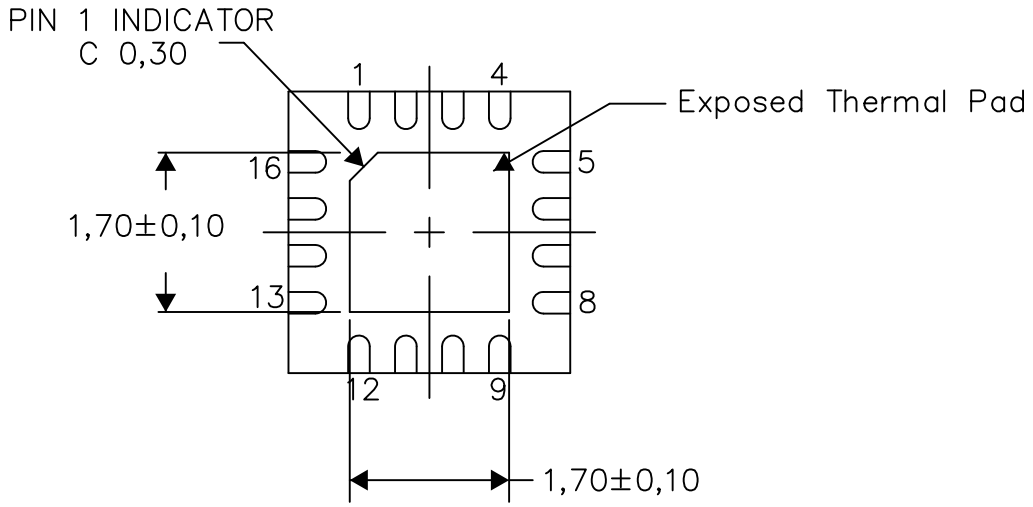
The exposed thermal pad dimensions for this package are shown in the following illustration.



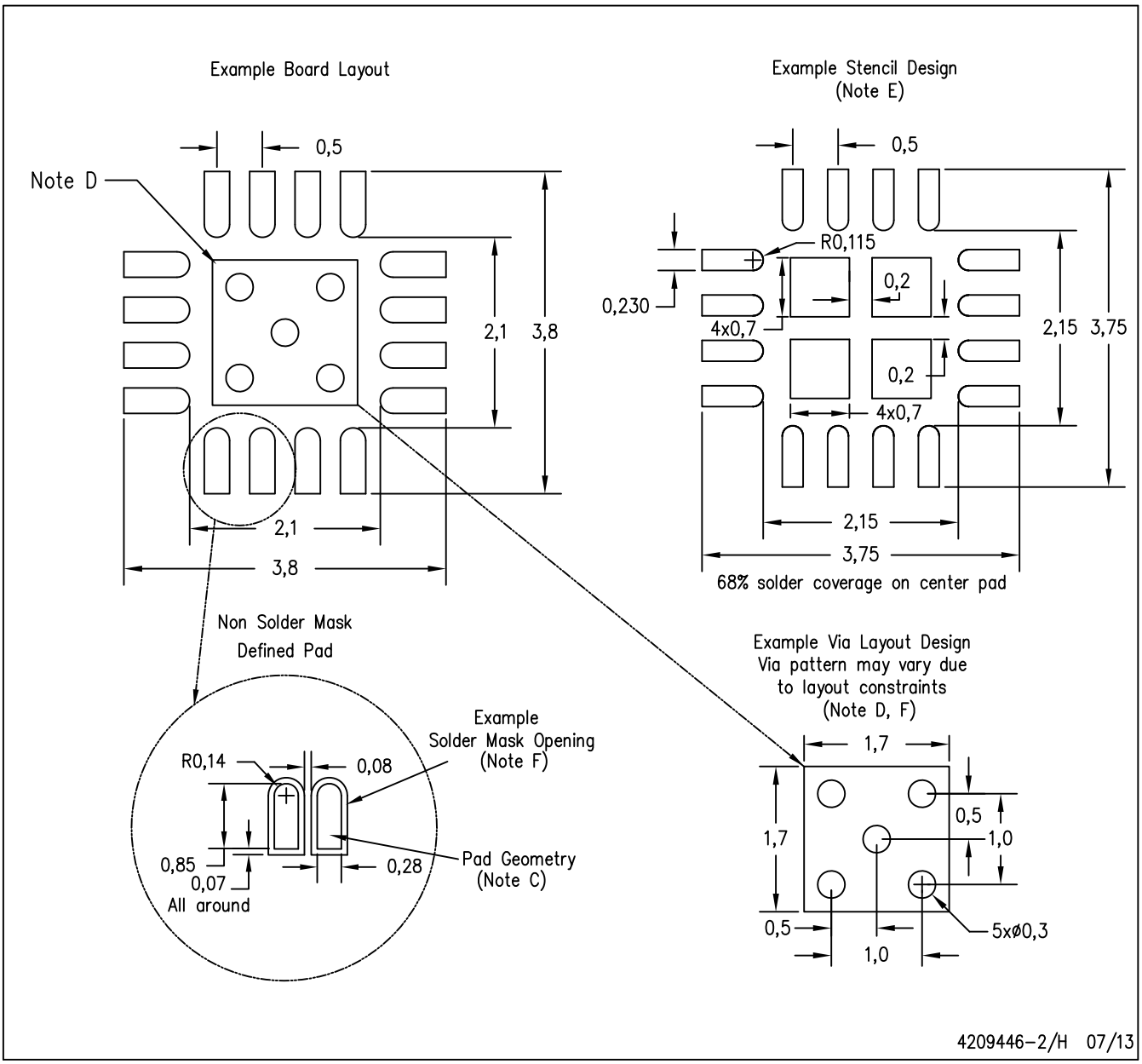
Bottom View

Exposed Thermal Pad Dimensions

4206446–3/N 07/13

NOTE: A. All linear dimensions are in millimeters

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

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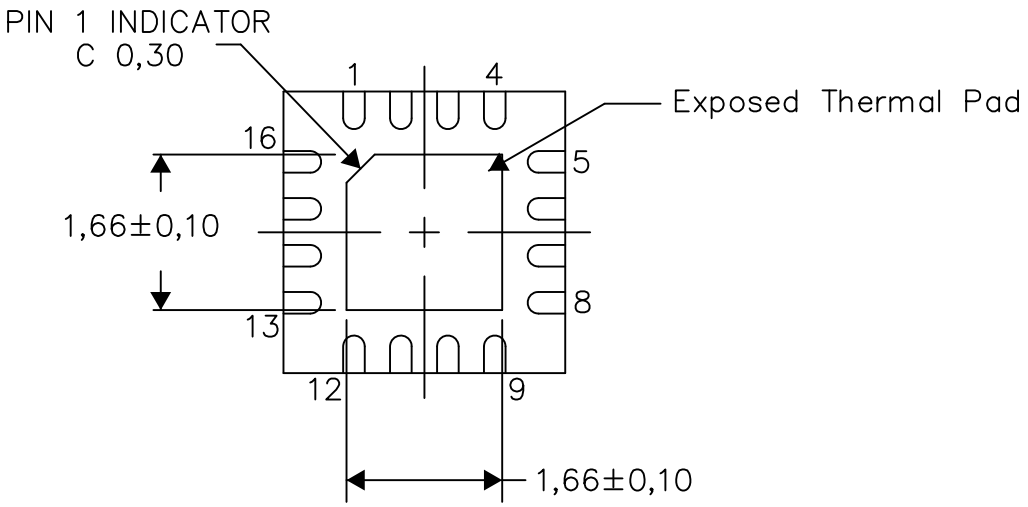
The exposed thermal pad dimensions for this package are shown in the following illustration.



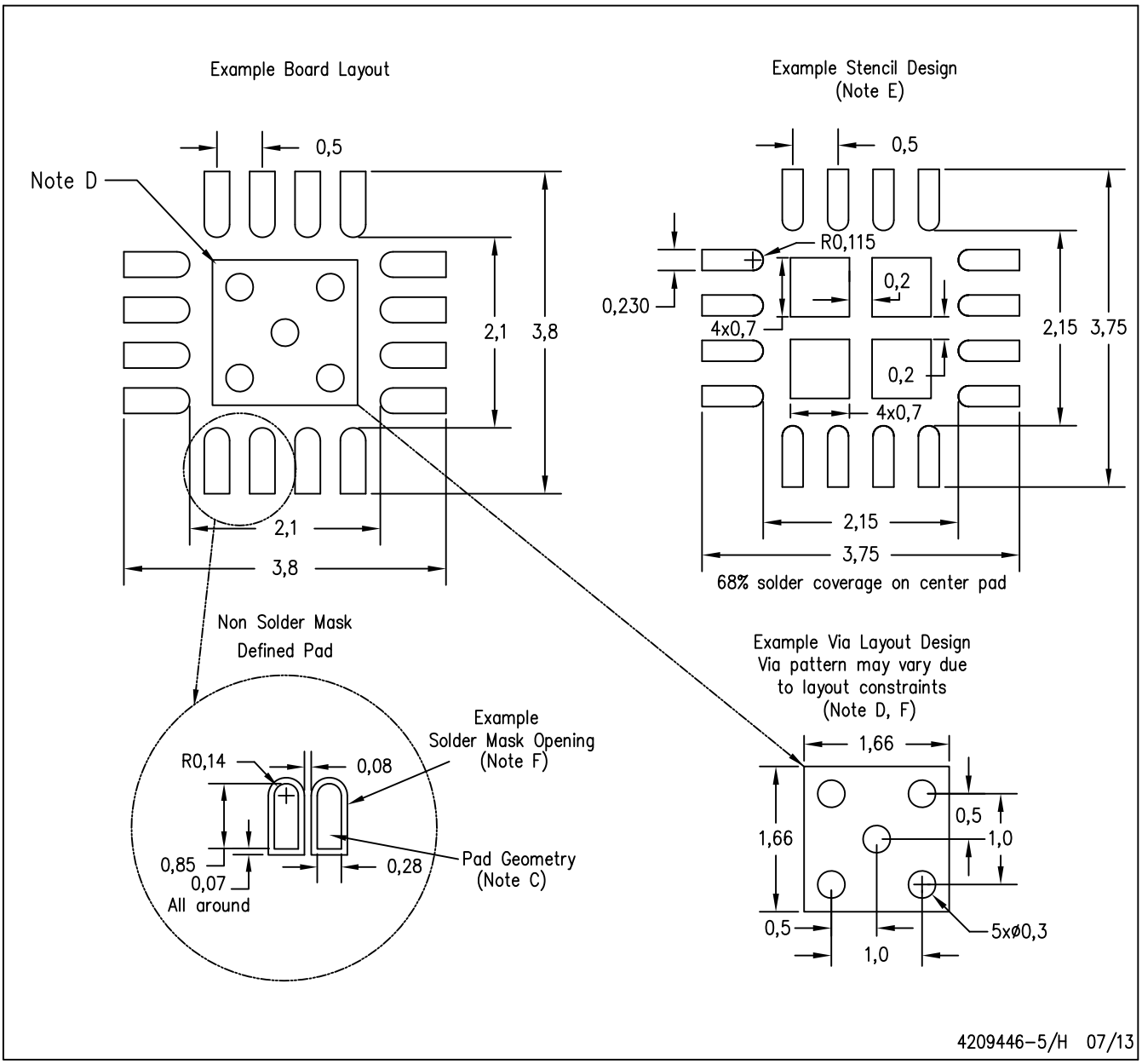
Bottom View

Exposed Thermal Pad Dimensions

4206446–5/N 07/13

NOTE: A. All linear dimensions are in millimeters

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



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