

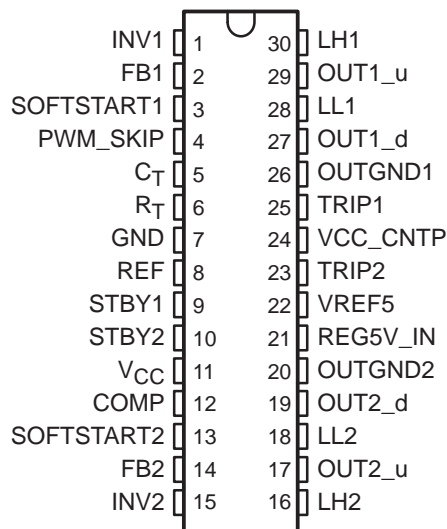
TPS5102

DUAL, HIGH-EFFICIENCY CONTROLLER FOR NOTEBOOK PC POWER

SLVS239 - SEPTEMBER 1999

- Dual, Step-Down for Notebook System Power
- 4.5 V to 25 V Input Voltage Range
- Adjustable Output Voltage
- 95% Efficiency Achievable
- PWM/Skip Mode Control Maintains High Efficiency Under Light Load Conditions
- Fixed-Frequency Operation
- Resistorless Current Protection
- Fixed High-Side Driver Voltage
- Low Quiescent Current (0.6 mA, <1 μ A for Standby)
- Small 30-Pin TSSOP
- EVM Available (TPS5102EVM-135)

**DBT PACKAGE
(TOP VIEW)**

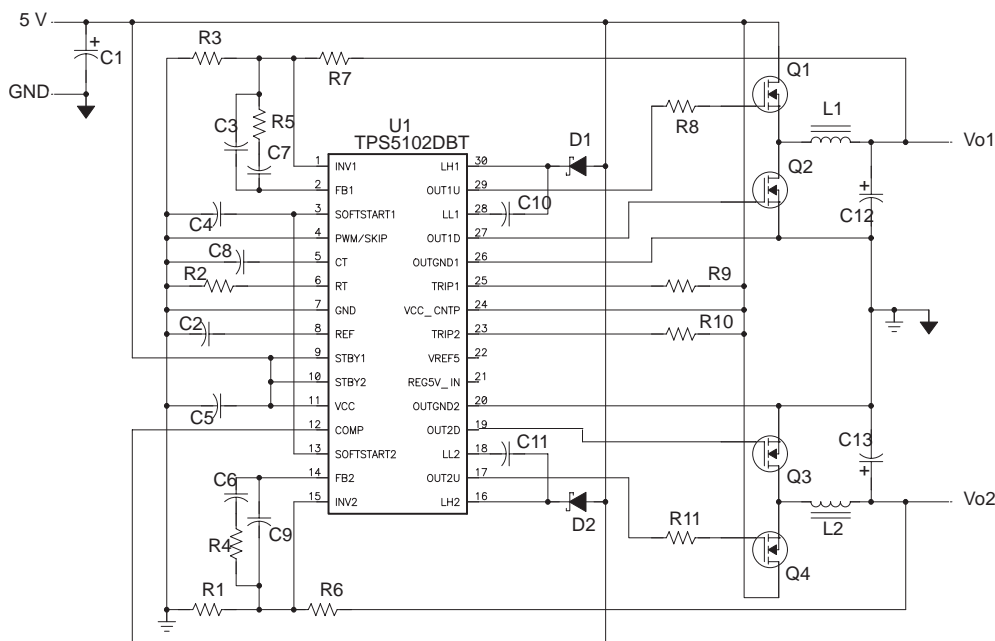


description

The TPS5102 is a dual, high efficiency controller designed for notebook system power requirements. Under light load conditions, high efficiency is maintained as the controller switches from the PWM mode to the lower frequency Skip mode.

These two operating modes, along with the synchronous-rectifier drivers, dead-time, and very low quiescent current, allow power to be conserved and the battery life extended, under all load conditions.

The resistor-less current protection and fixed high-side driver voltage simplify the system design and reduce the external parts count. The wide input voltage range and adjustable output voltages allow flexibility for using the TPS5102 in notebook power supply applications.



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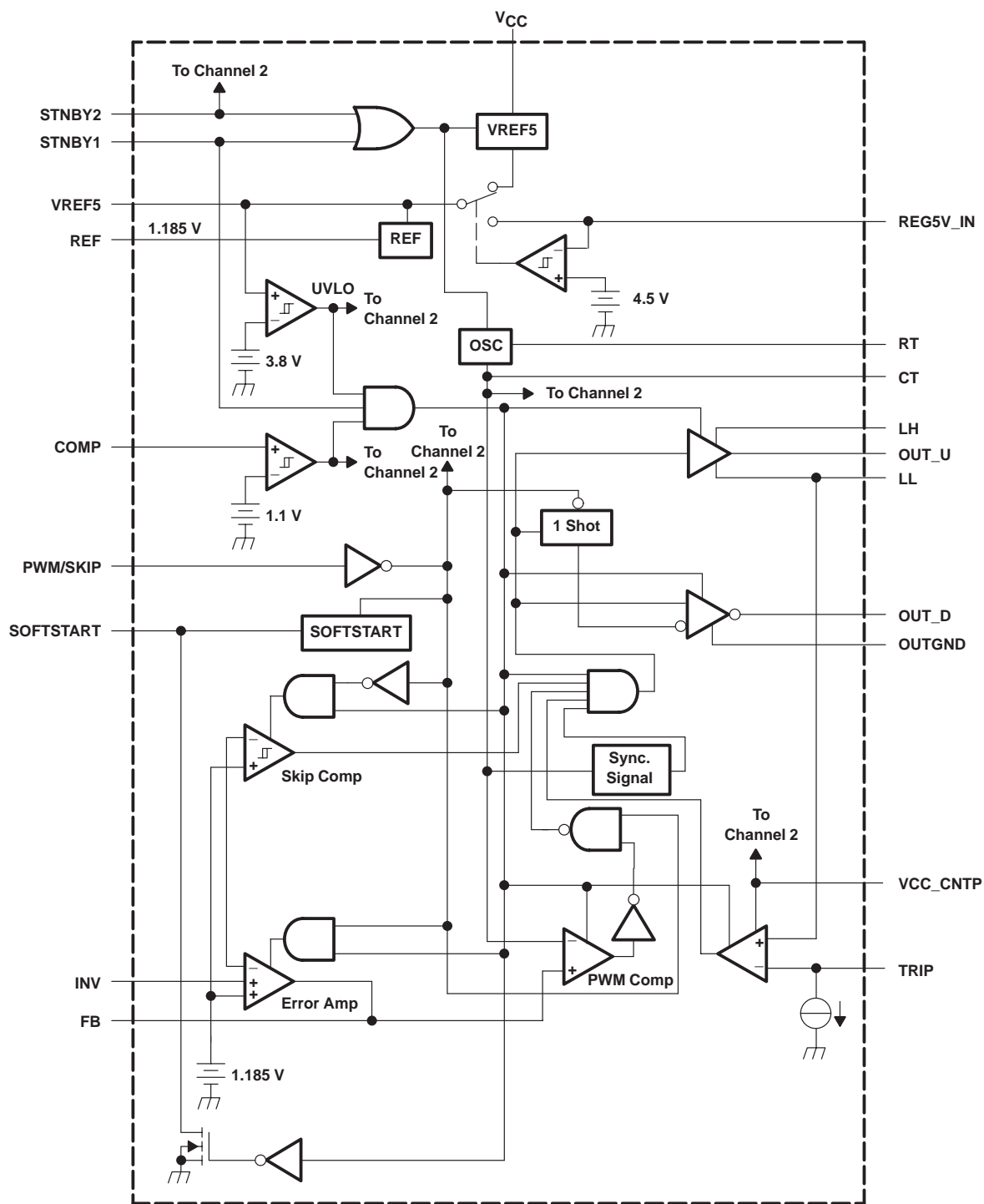
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TPS5102 DUAL, HIGH-EFFICIENCY CONTROLLER FOR NOTEBOOK PC POWER

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functional block diagram



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AVAILABLE OPTIONS

| T _A | PACKAGE | EVM |
|----------------|--------------|----------------|
| | TSSOP(DBT) | |
| -40°C to 85°C | TPS5102IDBT | TPS5102EVM-135 |
| | TPS5102IDBTR | |

Terminal Functions

| TERMINAL NAME | NO. | I/O | DESCRIPTION |
|-------------------|-----|-----|--|
| COMP | 12 | I/O | Voltage monitor comparator input |
| C _T | 5 | I/O | External capacitor connection for switching frequency adjustment |
| FB1 | 2 | O | CH1 error amp output |
| FB2 | 14 | O | CH2 error amp output |
| GND | 7 | | Control GND |
| INV1 | 1 | I | CH1 inverting input |
| INV2 | 15 | I | CH2 inverting input |
| LH1 | 30 | I/O | CH1 boost capacitor connection |
| LH2 | 16 | I/O | CH2 boost capacitor connection |
| LL1 | 28 | I/O | CH1 boost circuit connection |
| LL2 | 18 | I/O | CH2 boost circuit connection |
| OUT1_d | 27 | I/O | CH1 low-side gate-drive output |
| OUT2_d | 19 | O | CH2 low-side gate-drive output |
| OUT1_u | 29 | O | CH1 high-side drive output |
| OUT2_u | 17 | O | CH2 high-side drive output |
| OUTGND1 | 26 | | Output GND 1 |
| OUTGND2 | 20 | | Output GND 2 |
| PWM_SKIP | 4 | I | PWM/SKIP mode select L:PWM mode H:SKIP mode |
| REF | 8 | O | 1.185-V reference voltage output |
| REG5V_IN | 21 | I | External 5-V input |
| R _T | 6 | I/O | External resistor connection for switching frequency adjustment |
| SOFTSTART1 | 3 | I/O | External capacitor connection for CH1 soft start timing. |
| SOFTSTART2 | 13 | I/O | External capacitor connection for CH2 soft start timing. |
| STBY1 | 9 | I | CH1 stand-by control |
| STBY2 | 10 | I | CH2 stand-by control |
| TRIP2 | 23 | I | External resistor connection for CH2 over current protection. |
| TRIP1 | 25 | I | External resistor connection for CH1 over current protection. |
| V _{CC} | 11 | | Supply voltage input |
| V _{ref5} | 22 | O | 5-V internal regulator output |
| VCC_CNTP | 24 | I | Supply voltage sense input |



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detailed description

Vref (1.185 V)

The reference voltage is used to set the output voltage and the overvoltage protection (COMP).

Vref5 (5 V)

The internal linear voltage regulator is used for the high-side driver bootstrap voltage. Since the input voltage range is from 4.5 V to 25 V, this feature offers a fixed voltage for the bootstrap voltage greatly simplifying the drive design. It is also used for powering the low side driver. The tolerance is 6%.

5-V Switch

If the internal 5 V switch senses a 5-V input from REG5V_IN pin, the internal 5-V linear regulator will be disconnected from the MOSFET drivers. The external 5 V will be used for both the low-side driver and the high side bootstrap, thus increasing the efficiency.

PWM/SKIP

This pin is used to change between PWM and Skip mode. If the pin is lower than 0.5-V, the IC is in regular PWM mode; if a minimum 2-V is applied to this pin, the IC works in Skip mode. In light load condition (<0.2 A), the skip mode gives a short pulse to the low-side FET instead of a full pulse. By this control, switching frequency is lowered, reducing switching loss; also the output capacitor energy discharging through the output inductor and the low-side FET is prevented. Therefore, the IC can achieve high efficiency at light load conditions (< 0.2 A).

err-amp

Each channel has its own error amplifier to regulate the output voltage of the synchronous-buck converter. It is used in the PWM mode for the high output current condition (>0.2A). Voltage mode control is applied.

skip comparator

In Skip mode, each channel has its own hysteretic comparator to regulate the output voltage of the synchronous-buck converter. The hysteresis is set internally and typically at 8.5 mV. The delay from the comparator input to the driver output is typically 1.2 μ s.

low-side driver

The low-side driver is designed to drive low-Rds(on) n-channel MOSFETs. The maximum drive voltage is 5 V from Vref5. The current rating of the driver is typically 1 A, source and sink.

high-side driver

The high side driver is designed to drive low-Rds(on) n-channel MOSFETs. The current rating of the driver is 1 A, source and sink. When configured as a floating driver, the bias voltage to the driver is developed from Vref5, limiting the maximum drive voltage between OUT_u and LL to 5 V. The maximum voltage that can be applied between LHx and OUTGND is 30 V.

deadtime control

Deadtime prevents shoot-through current from flowing through the main power FETs during switching transitions by actively controlling the turn-on time of the MOSFETs drivers. The typical deadtime from low-side-driver-off to high-side-driver-on is 70 ns, and 85 ns from high-side-driver-off to low-side-driver-on.



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detailed description (continued)

current protection

Current protection is achieved by sensing the high-side power MOSFET drain-to-source voltage drop during on-time at VCC_CNTP and LL. An external resistor between Vin and TRIP pin in serial with the internal current source adjusts the current limit. When the voltage drop during the on-time is high enough, the current comparator triggers the current protection and the circuit is reset. The reset repeats until the over-current condition is removed.

COMP

COMP is an internal comparator used for any voltage protection such as the output under-voltage protection for notebook power applications. If the core voltage is lower than the setpoint, the comparator turns off both channels to prevent the notebook from damage.

SOFT1, SOFT2

Separate softstart terminals make it possible to set the start-up time of each output for any possibility.

STBY1, STBY2

Both channels can be switched into standby mode separately by grounding the STBY pin. The standby current is as low as 1 μ A.

ULVO

When the input voltage goes up to about 4 V, the IC is turned on, ready to function. When the input voltage is lower than the turn-on value, the IC is turned off. The typical hysteresis is 40 mV.

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absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

| | |
|--|----------------|
| Supply voltage, V _{CC} (see Note 1) | -0.3 V to 27 V |
| Input voltage, INV | -0.3 V to 7 V |
| SOFTSTART | -0.3 V to 7 V |
| COMP | -0.3 V to 6 V |
| REG5_IN | -0.3 V to 6 V |
| STBY | -0.3 V to 15 V |
| Driver current | 3 A |
| TRIP | -0.3 V to 27 V |
| C _T | -0.3 V to 7 V |
| R _T | -0.3 V to 7 V |
| LL | -0.3 V to 27 V |
| LH | -0.3 V to 32 V |
| OUT_u | -0.3 V to 32 V |
| OUT_d | -0.3 V to 7 V |
| PWM/SKIP | -0.3 V to 7 V |
| VCC_Sense | -0.3 V to 27 V |
| Power dissipation (T _A = 25°C) | 874 mW |
| Operating temperature (T _A) | -40°C to 85°C |
| Operating temperature (T _J) | -40°C to 125°C |
| Storage temperature (T _{STG}) | -55°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values are with respect to the network ground terminal.
 2. This rating is specified at duty ≤ 10% on output rise and fall each pulse. Each pulse width (rise and fall) for the peak current should not exceed 2 μs.
 3. See Dissipation Rating Table for free-air temperature range above 25°C.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE T _A = 25°C | T _A = 85°C POWER RATING |
|---------|---------------------------------------|--|---------------------------------------|
| DBT | 874 mW | 6.993 mW/°C | 454 mW |

recommended operating conditions

| PARAMETERS | | MIN | NOM | MAX | UNIT |
|---|--|------|-----|-----|------|
| Supply voltage, V _{CC} | | 4.5 | | 25 | V |
| Input voltage, V _I | INV1/2 C _T R _T , PWM/SKIP, SOFTSTART | | | 6 | V |
| | 5 V_IN | -0.1 | | 5.5 | |
| | STBY1, STBY2 | | | 12 | |
| | TRIP1/2 VCC_SENSE | -0.1 | | 25 | |
| Oscillator frequency | C _T | | 100 | | pF |
| | R _T | | 82 | | kΩ |
| | f _{osc} PWM | | 200 | | KHz |
| Operation temperature range, T _A | | -40 | | 85 | °C |



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electrical characteristics over recommended operating free-air temperature range, $V_{CC} = 7\text{ V}$ (unless otherwise noted)

reference voltage

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|-------------------|---|-------|-------|-------|------|
| Vref | Reference voltage | $T_A = 25^\circ\text{C}$, $I_{Vref} = 50\ \mu\text{A}$ | 1.167 | 1.185 | 1.203 | V |
| | | $I_{Vref} = 50\ \mu\text{A}$ | 1.155 | | 1.215 | |
| Regin | Line regulation | $V_{CC} = 4.5, 25\text{V}$, $I = 50\ \mu\text{A}$ | | 0.2 | 12 | mV |
| Regl | Load regulation | $I = 0.1\ \mu\text{A}$ to $1\ \text{mA}$ | | 0.5 | 10 | mV |

quiescent current

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|-------------------------------------|---|-----|-----|------|------|
| Icc | Operating current without switching | Both STBY > 2.5 V, No switching, $V_{in} = 4.5 - 25\ \text{V}$ | | 0.6 | 1.5 | mA |
| Iccs | Stand-by current | Both STBY < 0.5 V, $V_{in} = 4.5 - 25\ \text{V}$ | | 1 | 1000 | nA |

oscillator

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------|------------------------|--|-----|------|-----|------------|
| fosc | Frequency | PWM operation | | | 500 | kHz |
| R_T | Timing resistor | | 56 | | | k Ω |
| fdv | fosc change | $V_{CC} = 4.5\ \text{V}$ to $25\ \text{V}$ | | 0.1% | | |
| fdt | | $T_A = -40^\circ\text{C}$ to 85°C | | 2% | | |
| V _{oscH} | H-level output voltage | DC, includes internal comparator error | 1 | 1.1 | 1.2 | V |
| | | Fosc = 200 kHz, Includes internal comparator error | | 1.17 | | |
| V _{oscL} | L-level output voltage | Includes internal comparator error | 0.4 | 0.5 | 0.6 | V |
| | | Fosc = 200 kHz, Includes internal comparator error | | 0.43 | | |

error amp

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|------------------------|--------------------------|-----|---------|----------|---------------|
| Vio | Input offset voltage | $T_A = 25^\circ\text{C}$ | | ± 2 | ± 10 | mV |
| Av | Open-loop voltage gain | | 50 | | | dB |
| GB | Unity-gain bandwidth | | | 0.8 | | MHz |
| I _{snk} | Output sink current | $V_o = 0.4\ \text{V}$ | 30 | 45 | | μA |
| I _{src} | Output source current | $V_o = 1\ \text{V}$ | | 300 | | μA |

skip comparator

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------|--|---|-----|-----|-----|---------------|
| V _{hys} [†] | Hysteresis window | | 6 | 9.5 | 13 | mV |
| V _{hoff} | Offset voltage | | | 2 | | mV |
| I _{hbias} | Bias current | | | 10 | | μA |
| T _{LHT} | Propagation delay [‡] from INV to OUTxU | TTL input signal | | 0.7 | | μs |
| T _{LH} | | 10 mV overdrive on hysteresis band signal | | 1.2 | | μs |

[†] V_{hys} is assured by design.

[‡] The total delay in the table includes the driver delay.



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electrical characteristics over recommended operating free-air temperature range, $V_{CC} = 7\text{ V}$ (unless otherwise noted) (continued)

driver deadtime

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------------------|-----------------|-----|-----|-----|------|
| T_{DRVLH} Low side to high side | | | 70 | | nS |
| T_{DRVHL} High side to low side | | | 85 | | nS |

standby

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------|-----------------------|-----|-----|-----|---------------|
| V_{IH} H-level input voltage | STBY1, STBY2 | 2.5 | | | V |
| V_{IL} L-level input voltage | | | | 0.5 | |
| T_{turnon} Propagation delay | STBY to driver output | | 1.5 | | μs |
| $T_{turnoff}$ Propagation delay | | | 1.8 | | |

5V regulator

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------------|--|-----|-----|-----|------|
| V_O Output voltage | $I = 10\text{ mA}$ | 4.7 | | 5.3 | V |
| Regin Line regulation | $V_{CC} = 5.5\text{ V}, 25\text{ V}, I = 10\text{ mA}$ | | | 20 | mV |
| Regl Load regulation | $I = 1\text{ V}, 10\text{ mA}, V_{CC} = 5.5\text{ V}$ | | | 40 | mV |
| Ios Short-circuit output current | $V_{ref} = 0\text{ V}$ | | 80 | | mA |

5-V internal switch

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------|-------------------|-----|-----|-----|------|
| V_{TLH} | Threshold voltage | 4.2 | | 4.8 | V |
| V_{THL} | | 4.1 | | 4.7 | |
| V_{hys} Hysteresis | | 30 | | 150 | mV |

UVLO

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------|-------------------|-----|-----|-----|------|
| V_{TLH} | Threshold voltage | 3.7 | | 4.2 | V |
| V_{THL} | | 3.6 | | 4.1 | |
| V_{hys} Hysteresis | | 10 | 40 | 150 | mV |

current limit

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------|-----------------|-----|-----|-----|---------------|
| Internal current source | PWM mode | 10 | 15 | 20 | μA |
| | Skip mode | 3 | 5 | 7 | |
| Input offset voltage | | | 2.5 | | mV |

driver output

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------|--------------------|-----|------|-----|------|
| OUT_u sink current | $V_o = 3\text{ V}$ | 0.5 | 1.2 | | A |
| OUT_d sink current | | 0.5 | 1.2 | | |
| OUT_u source current | $V_o = 3\text{ V}$ | -1 | -1.7 | | A |
| OUT_d source current | | -1 | -1.5 | | |



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electrical characteristics over recommended operating free-air temperature range, $V_{CC} = 7\text{ V}$ (unless otherwise noted) (continued)

softstart

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------|-------------------------------|-----------------|-----|------|-----|---------------|
| I_{CTRL} | Soft-start current | | 1.8 | 2.5 | 3 | μA |
| | Maximum discharge current | | | 0.92 | | mA |
| V_{TLH} | Threshold voltage (skip mode) | | 3.4 | 3.9 | 4.7 | V |
| V_{THL} | | | 1.8 | 2.6 | 3.4 | |

output voltage protection (COMP)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|---|---------------------------|-----|-----|-----|------|
| | Threshold voltage | | 0.9 | 1.1 | 1.3 | V |
| | Propagation delay [†] , 50% duty cycle, No capacitor on COMP or OUT_u pin, Frequency = 200 kHz | Turnon | | 900 | | ns |
| | | Turnoff (with channel on) | | 400 | | ns |

[†] The delay time in the table includes the driver delay.

PWM/SKIP

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|--|-----------------|-----|-----|-----|------|
| Threshold | | High to low | | | 0.5 | V |
| | | Low to high | 2 | | | |
| Delay | | High to low | | 550 | | ns |
| | | Low to high | | 400 | | |



TYPICAL CHARACTERISTICS

QUIESCENT CURRENT (BOTH CHANNELS ON)
 vs
 INPUT VOLTAGE

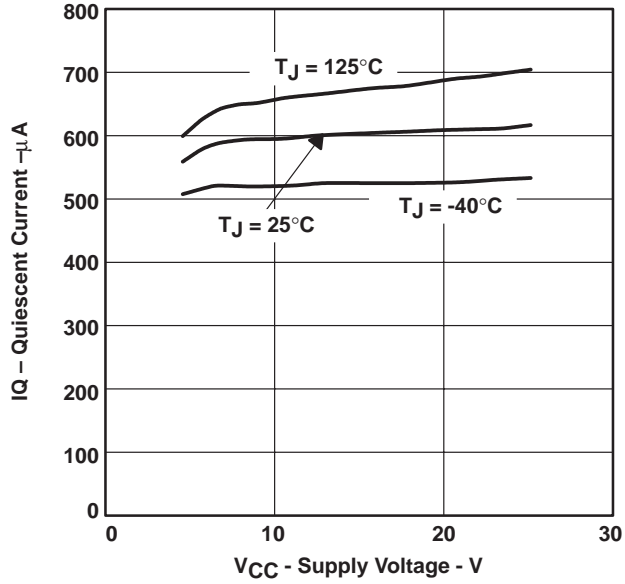


Figure 1

QUIESCENT CURRENT (BOTH CHANNELS STANDBY)
 vs
 INPUT VOLTAGE

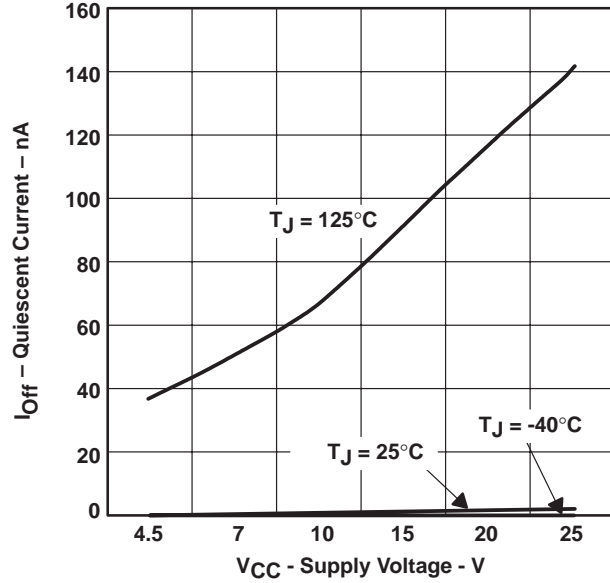


Figure 2

DRIVE CURRENT (SOURCE)
 vs
 DRIVE VOLTAGE

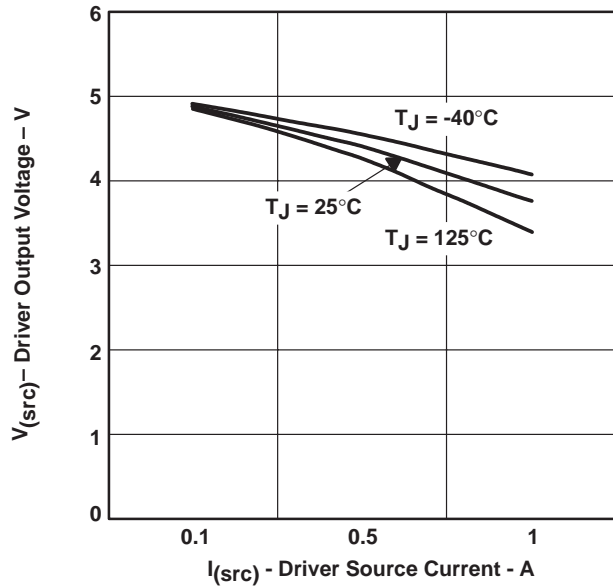


Figure 3

DRIVE CURRENT (SINK)
 vs
 DRIVE VOLTAGE

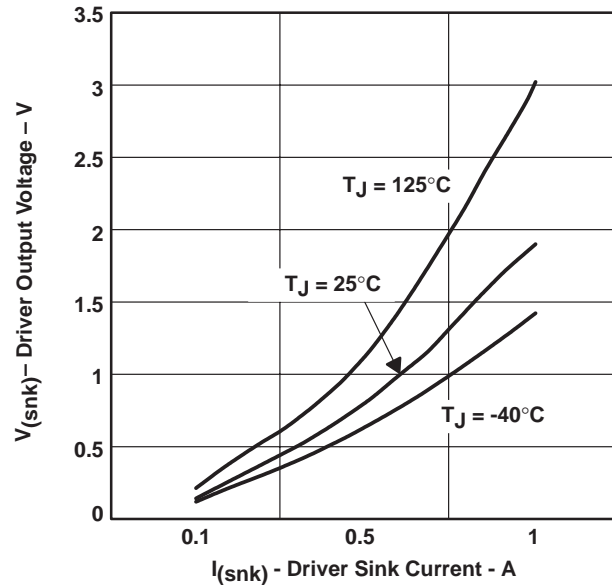


Figure 4

TYPICAL CHARACTERISTICS

CURRENT PROTECTION SOURCE CURRENT
 (SKIP MODE)
 vs
 INPUT VOLTAGE

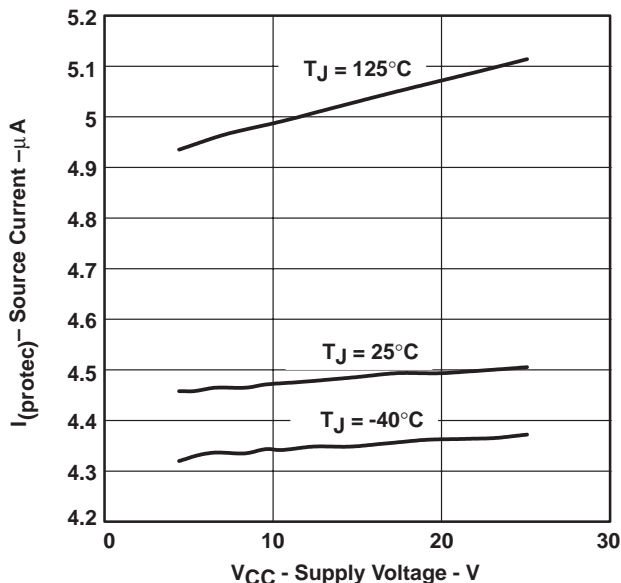


Figure 5

CURRENT PROTECTION SOURCE CURRENT
 (PWM MODE)
 vs
 INPUT VOLTAGE

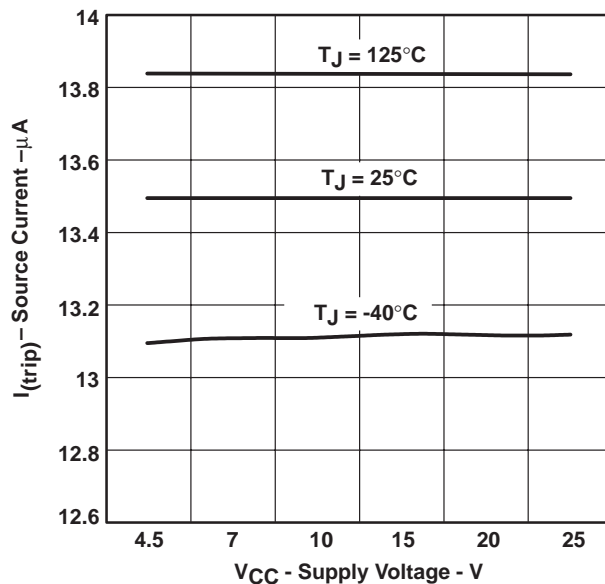


Figure 6

PWM/SKIP THRESHOLD VOLTAGE
 vs
 INPUT VOLTAGE

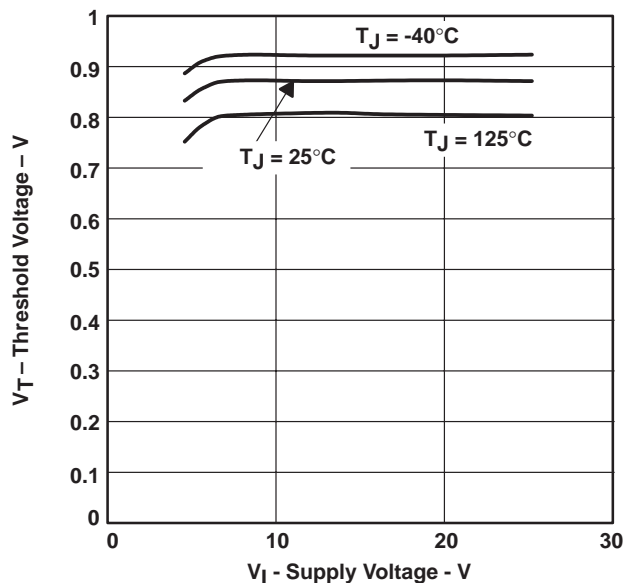


Figure 7

V_{ref5} VOLTAGE
 vs
 CURRENT

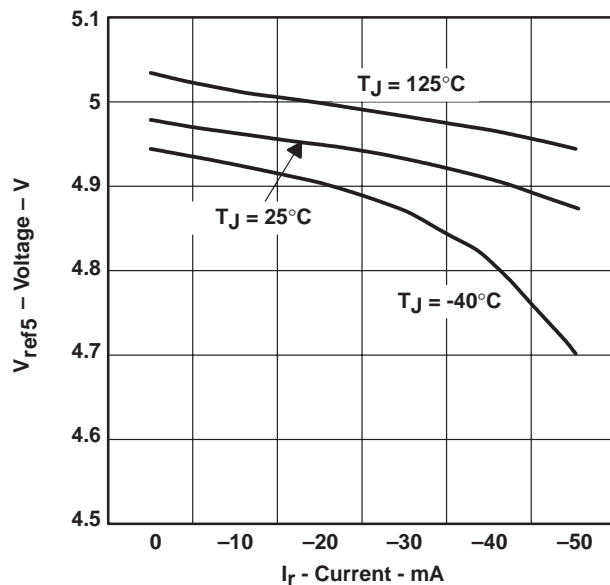


Figure 8

TYPICAL CHARACTERISTICS

MAXIMUM OUTPUT VOLTAGE
 VS
 SWITCHING FREQUENCY

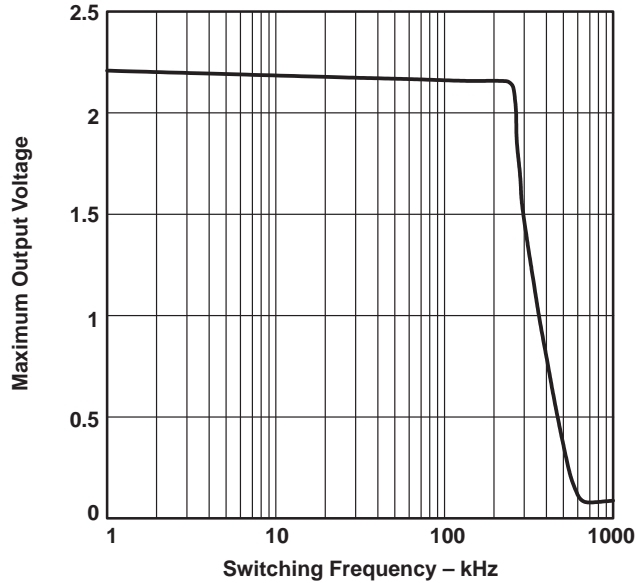


Figure 9

SOFT START CHARGE CURRENT
 VS
 JUNCTION TEMPERATURE

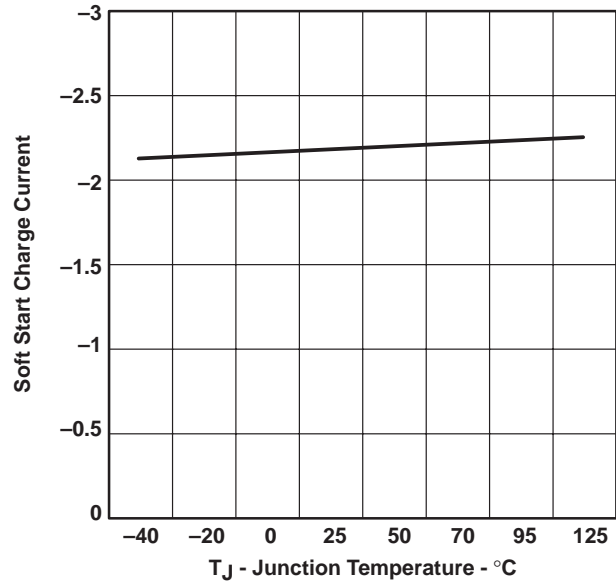


Figure 10

SWITCHING FREQUENCY
 VS
 TIMING RESISTOR

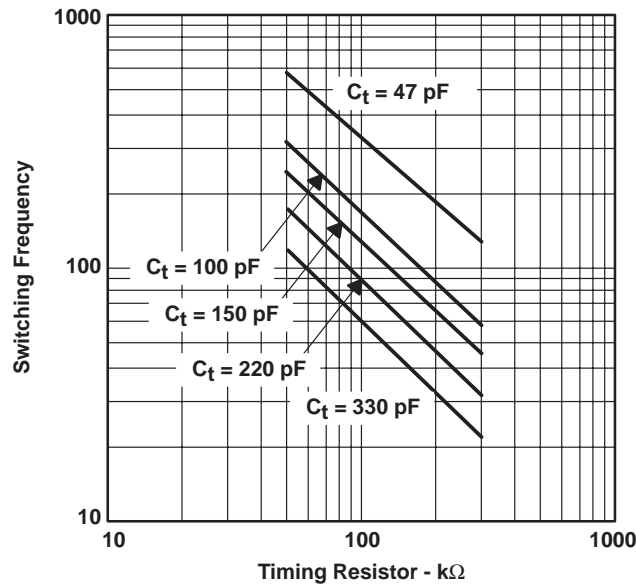
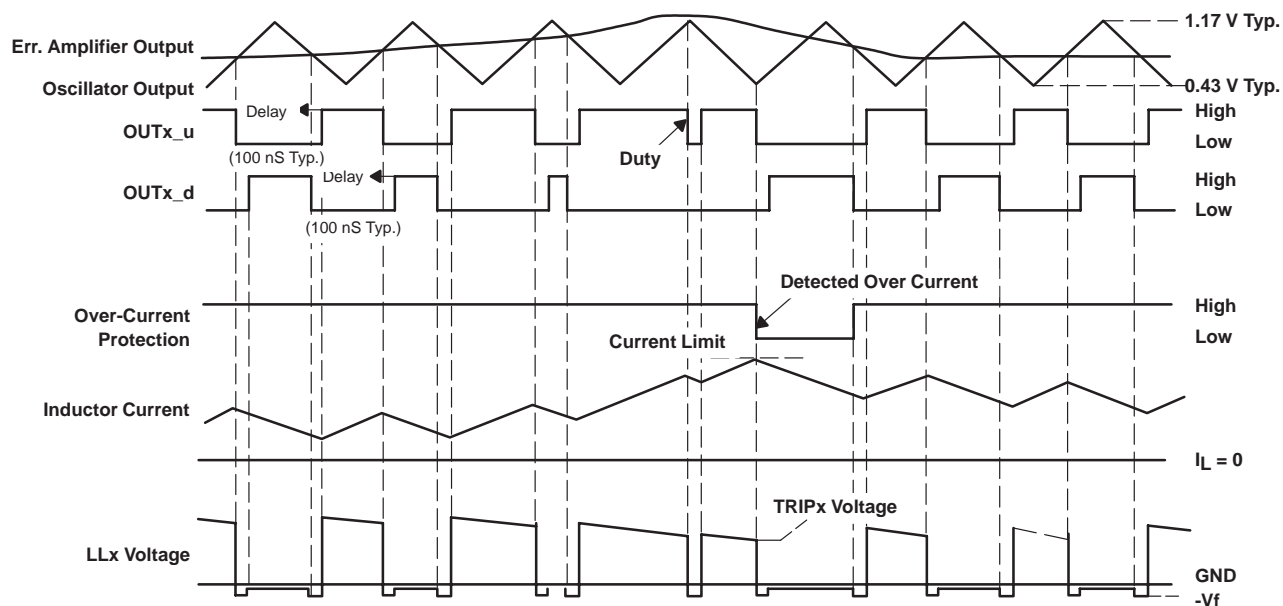


Figure 11

TYPICAL CHARACTERISTICS

timing diagram



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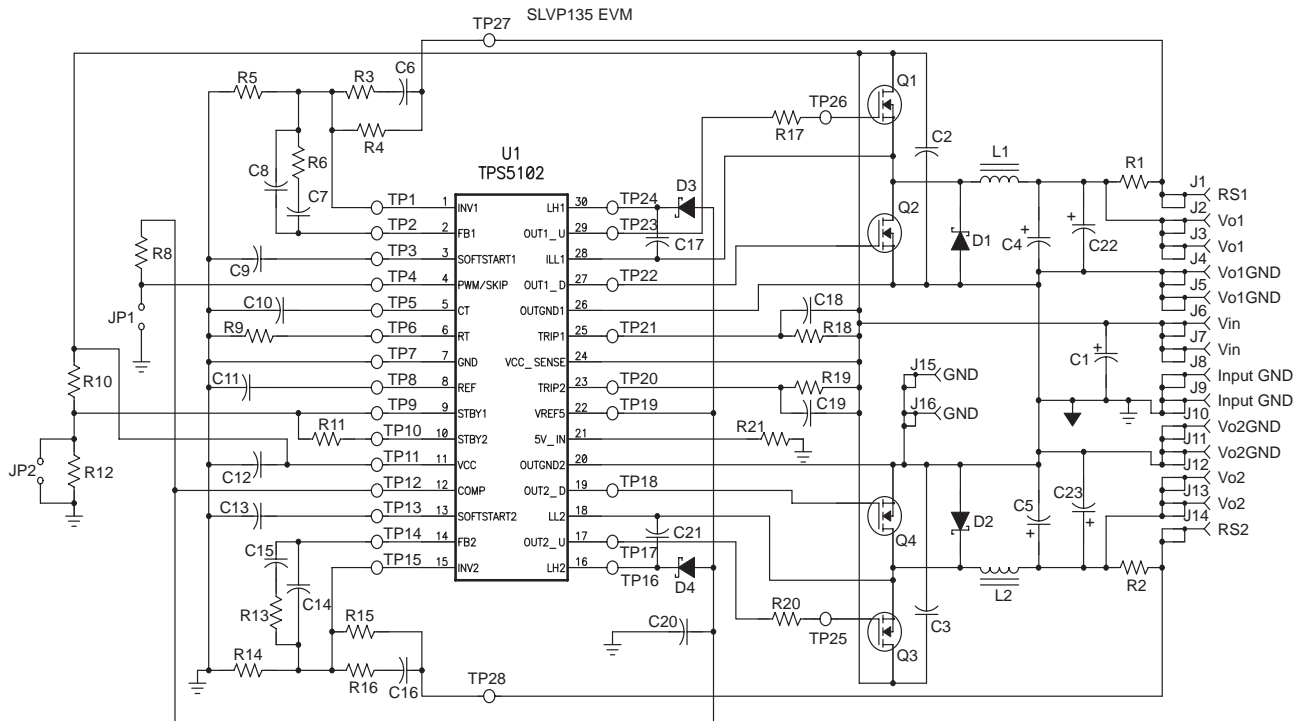
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APPLICATION INFORMATION

The design shown in this application report is a reference design for notebook applications. An evaluation module (EVM), TPS5102EVM-135 (SLVP135), is available for customer testing and evaluation. The intent is to allow a customer to fully evaluate the given design using the plug-in EVM supply shown here. For subsequent customer board revisions, the EVM design can be copied onto the users' PCB to shorten design cycle.

The following key design procedures will aid in the design of the notebook power supply using the TPS5102:



| Vin | Iin | Vo1 | Io1 | Vo2 | Io2 |
|--------------|-----|-------|-------|-----|-------|
| 6 V to 15 V | 6 A | 3.3 V | 4 A | 5 V | 4 A |
| 16 V to 25 V | | 3.3 V | 2.5 A | 5 V | 2.5 A |

output voltage setpoint calculation

The output voltage is set by the reference voltage and the voltage divider. In the TPS5102, the reference voltage is 1.185-V, and the divider is composed of two resistors in the EVM design that are R4 and R5, or R14 and R15. The equation for the setpoint is:

$$R2 = \frac{R1 \times Vr}{Vo - Vr}$$

Where R1 is the top resistor (kΩ) (R4 or R15); R2 is the bottom resistor (kΩ) (R5 or R14); Vo is the required output voltage (V); Vr is the reference voltage (1.185 V in TPS5102).

Example: R1 = 1 kΩ; Vr = 1.185 V; Vo = 3.3 V, then R2 = 560 Ω.

Some of the most popular output voltage setpoints are calculated in the table below:

| Vo | 1.3 V | 1.5 V | 1.8 V | 2.5 V | 3.3 V | 5 V |
|------------------|-------|-------|-------|-------|--------|--------|
| R1 (top) (kΩ) | 1 V | 1 V | 1 V | 1 V | 1 V | 1 V |
| R2 (bottom) (kΩ) | 10 V | 3.7 V | 1.9 V | 0.9 V | 0.56 V | 0.31 V |



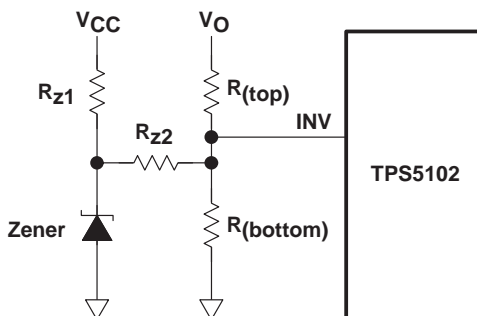
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APPLICATION INFORMATION

output voltage setpoint calculation (continued)

If a higher precision resistor is used, the voltage setup can be more accurate.

In some applications, the output voltage is required to be lower than the reference voltage. With a few extra components, the lower voltage can be easily achieved. The drawing below shows the method.



In the schematic, the R_{z1} , the R_{z2} , and the zener are the extra components. R_{z1} is used to give the zener enough current to build up the zener voltage. The zener voltage is added to INV through R_{z2} . Therefore, the voltage on the INV is still equal to the IC internal voltage (1.185 V) even if the output voltage is regulated at a lower setpoint. The equation for setting up the output voltage is shown below:

$$R_{z2} = \frac{(V_z - V_r)}{\frac{(V_r - V_o)}{R_{top}} + \frac{V_r}{R_{bottom}}}$$

When R_{z2} is the adjusting resistor for low output voltage; V_z is the zener voltage; V_r is the internal reference voltage; R_{top} is the resistor of the voltage sensing network; R_{bottom} is the bottom resistor of the sensing network; V_o is the required output voltage setpoint.

Example: Assuming the required output voltage setpoint is $V_o = 0.8$ V, $V_z = 5$ V; $R_{top} = 1$ k Ω ; $R_{bottom} = 1$ k Ω , Then the $R_{z2} = 2.43$ k Ω .

output inductor ripple current

The output inductor current ripple can affect not only the efficiency, but also the output voltage ripple. The equation is exhibited below:

$$I_{ripple} = \frac{V_{in} - V_{out} - I_{out} \times (R_{dson} + R_L)}{L_{out}} \times D \times T_s$$

Where I_{ripple} is the peak-to-peak ripple current (A) through the inductor; V_{in} is the input voltage (V); V_{out} is the output voltage (V); I_{out} is the output current; R_{dson} is the on-time resistance of MOSFET (Ω); D is the duty cycle; and T_s is the switching cycle (S). From the equation, it can be seen that the current ripple can be adjusted by changing the output inductor value.

Example: $V_{in} = 5$ V; $V_{out} = 1.8$ V; $I_{out} = 5$ A; $R_{dson} = 10$ m Ω ; $R_L = 5$ m Ω ; $D = 0.36$; $T_s = 10$ μ S; $L_{out} = 6$ μ H

Then, the ripple $I_{ripple} = 2$ A.

APPLICATION INFORMATION

output capacitor RMS current

Assuming the inductor ripple current totally goes through the output capacitor to ground, the RMS current in the output capacitor can be calculated as:

$$I_{orms} = \frac{\Delta I}{\sqrt{12}}$$

Where $I_{o(rms)}$ is the maximum RMS current in the output capacitor (A); ΔI is the peak-to-peak inductor ripple current (A).

Example: $\Delta I = 2$ A, so $I_{o(rms)} = 0.58$ A

input capacitor RMS current

Assuming the input ripple current totally goes into the input capacitor to the power ground, the RMS current in the input capacitor can be calculated as:

$$I_{irms} = \sqrt{I_o^2 \times D \times (1-D) + \frac{1}{12} D \times I_{ripple}^2}$$

Where $I_{i(rms)}$ is the input RMS current in the input capacitor (A); I_o is the output current (A); I_{ripple} is the peak-to-peak output inductor ripple current; D is the duty cycle. From the equation, it can be seen that the highest input RMS current usually occurs at the lowest input voltage, so it is the worst case design for input capacitor ripple current.

Example: $I_o = 5$ A; $D = 0.36$; $I_{ripple} = 2$ A,

Then, $I_{i(rms)} = 2.42$ A

soft-start

The soft-start timing can be adjusted by selecting the soft-start capacitor value. The equation is

$$C_{soft} = 2 \times T_{soft}$$

Where C_{soft} is the soft-start capacitance (μ F) (C9 or C13 in EVM design); T_{soft} is the start-up time (S).

Example: $T_{soft} = 5$ mS, so $C_{soft} = 0.01$ μ F.

APPLICATION INFORMATION

current protection

The current limit in TPS5102 on each channel is set using an internal current source and an external resistor (R18 or R19). The sensed high side MOSFET drain-to-source voltage drop is compared to the set point, if the voltage drop exceeds the limit, the internal oscillator is activated, and it continuously reset the current limit until the over-current condition is removed. The equation below should be used for calculating the external resistor value for current protection setpoint:

$$R_{cl} = \frac{R_{ds(on)} \times (I_{trip} + I_{ind(p-p)}/2)}{0.000015}$$

In skip mode,

$$R_{cl} = \frac{R_{ds(on)} \times (I_{trip} + I_{ind(p-p)}/2)}{0.000005}$$

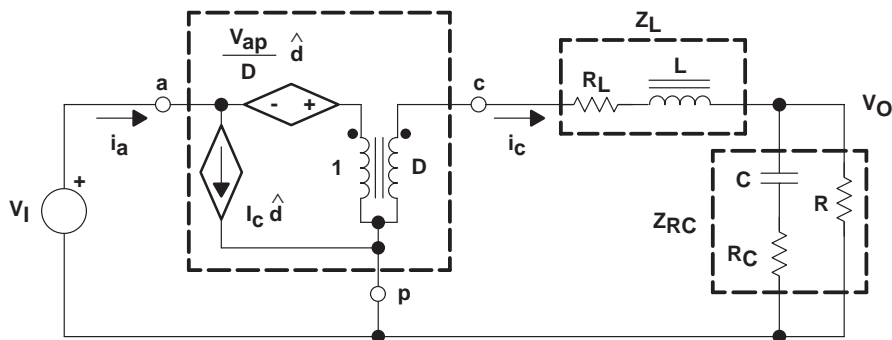
Where Rcl is the external current limit resistor (R10 or R11); Rds(on) is the high side MOSFET (Q1 or Q3) on-time resistance. Itrip is the required current limit; Iind(p-p) is the peak-to-peak output inductor current.

Example for voltage mode: Rds(on) = 10 mΩ, Itrip = 5 A, Iind = 2 A, so Rcl = 4 kΩ.

loop-gain compensation

Voltage mode control is used in this controller for the output voltage regulation. To achieve fast, stabilized control, two parts are discussed in this section: the power stage small signal modeling and the compensation circuit design.

For the buck converter, the small signal modeling circuit is shown below:



From this equivalent circuit, several control transfer functions can be derived: input-to-output, output impedance, and control-to-output. Typically the control-to-output transfer function is used for the feedback control design.

Assuming R_c and R_L are much smaller than R, the simplified small signal control-to-output transfer function is:

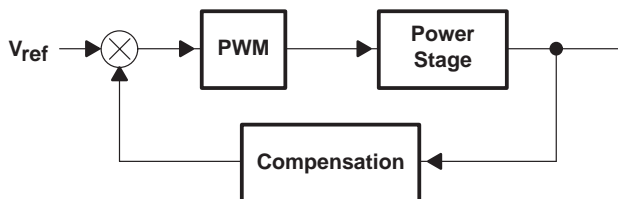
$$V_{od} = \frac{\hat{V}_O}{\hat{d}} = \frac{(1 + sCR_c)}{1 + s\left[C \times (R_c + R_L) + \frac{L}{R}\right] + s^2LC}$$

Where C is the output capacitance; R_c is the equivalent serial resistance (ESR) in the output capacitor; L is the output inductor; R_L is the equivalent serial resistance (DCR) in the output inductor; R is the load resistance.

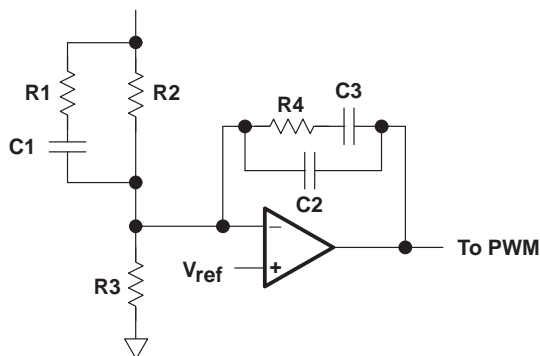
APPLICATION INFORMATION

loop-gain compensation (continued)

To achieve fast transient response and the better output voltage regulation, a compensation circuit is added to improve the feedback control. The whole system is shown:



The typical compensation circuit used as an option in the EVM design is a part of the output feedback circuit. The circuitry is displayed below:



This circuit is composed of one integrator, two poles, and two zeros:

Assuming $R1 \ll R2$ and $C2 \ll C3$, the equation is:

$$Comp = \frac{(1 + sC3R4) \times (1 + sC2R2)}{sC3R2(1 + sC2R4) (1 + sC1R1)}$$

Therefore,

$$Pole1 = \frac{1}{2\pi C1R1}$$

$$Zero1 = \frac{1}{2\pi C2R2}$$

$$Pole2 = \frac{1}{2\pi C2R4}$$

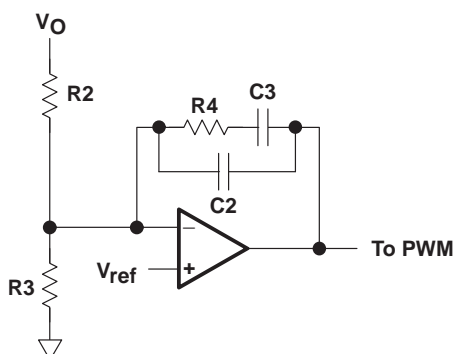
$$Zero2 = \frac{1}{2\pi C3R4}$$

$$Integrator = \frac{1}{2\pi C3R2}$$

A simplified version used in the EVM design is exhibited below:

APPLICATION INFORMATION

loop-gain compensation (continued)



Assuming $C2 \ll C3$, the equation is:

$$Comp = \frac{(1 + sC3R4)}{sC3R2(1 + sC2R4)}$$

There is one pole, one zero and one integrator:

$$Zero = \frac{1}{2\pi C3R4} \quad Integrator = \frac{1}{2\pi f C3R2} \quad Pole = \frac{1}{2\pi C2R4}$$

The loop-gain concept is used to design a stable and fast feedback control. The loop-gain equation is derived by the control-to-output transfer function times the compensation:

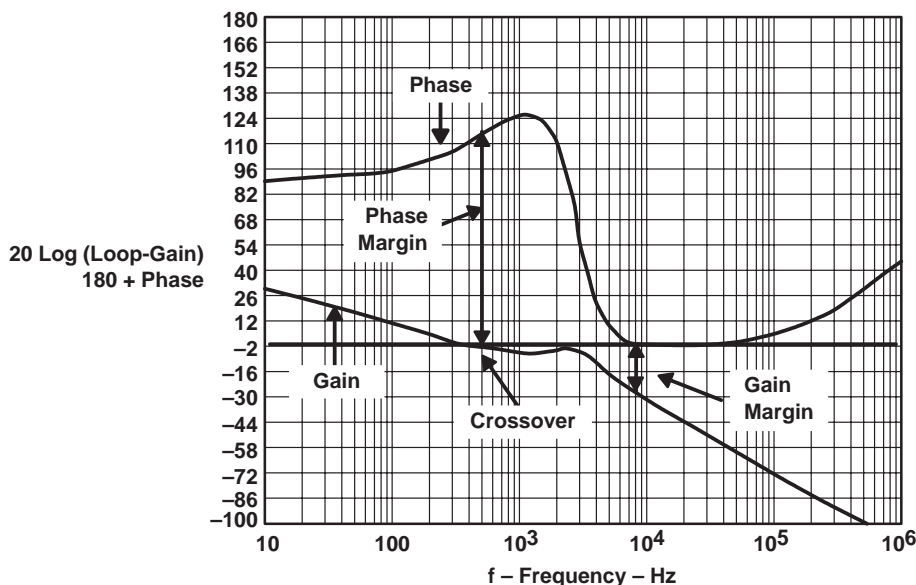
$$Loop-gain = Vod \times Comp$$

The amplitude and the phase of this equation can be drawn with software such as MathCad. In turn, the stability can be easily designed by adjusting the compensation parameters. The sample bode plot is shown below to explain the phase margin, gain margin, and the crossover frequency.

The gain is drawn as $20 \log(\text{loop-gain})$, and the phase is in degrees. To explain them clearer, 180 degrees is added to the phase, so that the gain and phase share the same zero.

The crossover frequency is the point at which the gain curve touches zero. The higher this frequency, the faster the transient response, since the transient recovery time is $1/(\text{crossover frequency})$. The phase is the phase margin. The phase margin should be at least 60 degrees to cover all changes such as temperature. The gain margin is the gap between the gain curve and the zero when the phase curve touches zero. This margin should be at least 20 dB to guarantee stability over all conditions.

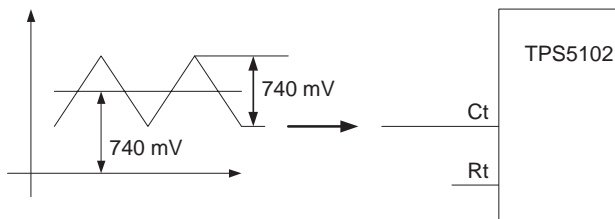
APPLICATION INFORMATION



synchronization

Some applications require switching clock synchronization. There are two methods that can be used for synchronization: the triangle wave synchronization and the square wave synchronization.

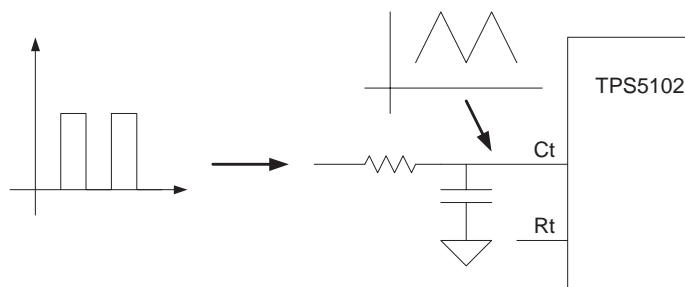
The triangle wave synchronization is displayed below:



It can be seen that both Rt and Ct are removed from the circuit. Therefore, two components are saved. This method is good for the synchronization between two controllers. If the controller needs to be synchronized with a digital circuit such as DSP, the square-type clock signal is usually used. The configuration exhibited below is for this type of application:

APPLICATION INFORMATION

synchronization (continued)



An external resistor is added into the circuit, but R_t is still removed. C_t is kept to be a part of RC circuit generating triangle waveform for the controller. Assuming the peak value of the square is known, the resistor and the capacitor can be adjusted to achieve the correct peak-to-peak value and the offset value.

layout guidelines

Good power supply results will only occur when care is given to proper design and layout. Layout will affect noise pickup and generation and can cause a good design to perform with less than expected results. With a range of currents from milliamps to tens or even hundreds of amps, good power supply layout is much more difficult than most general PCB designs. The general design should proceed from the switching node to the output, then back to the driver section and, finally, parallel the low-level components. Below are several specific points to consider *before* the layout of a TPS5102 design begins.

- All sensitive analog components should be referenced to ANAGND. These include components connected to V_{ref5} , V_{ref} , INV, LH, and COMP.
- Analog ground and drive ground should be isolated as much as possible. Ideally, analog ground will connect to the ground side of the bulk storage capacitors on V_O , and drive ground will connect to the main ground plane close to the source of the low-side FET.
- Connections from the drivers to the gate of the power FETs should be as short and wide as possible to reduce stray inductance. This becomes more critical if external gate resistors are not being used.
- The bypass capacitor for V_{CC} should be placed close to the TPS5102.
- When configuring the high-side driver as a floating driver, the connection from LL to the power FETs should be as short and as wide as possible.
- When configuring the high-side driver as a floating driver, the bootstrap capacitor (connected from LH to LL) should be placed close to the TPS5102.
- When configuring the high-side driver as a ground-referenced driver, LL should be connected to DRVGND.
- The bulk storage capacitors across V_{IN} should be placed close to the power FETS. High-frequency bypass capacitors should be placed in parallel with the bulk capacitors and connected close to the drain of the high-side FET and to the source of the low-side FET.
- High-frequency bypass capacitors should be placed across the bulk storage capacitors on V_O .
- LH and LL should be connected very close to the drain and source, respectively, of the high-side FET. LH and LL should be routed very close to each other to minimize differential-mode noise coupling to these traces.
- The output voltage sensing trace should be isolated by either ground trace or V_{cc} trace.

APPLICATION INFORMATION

PWM AND SKIP MODE EFFICIENCY
 COMPARISON

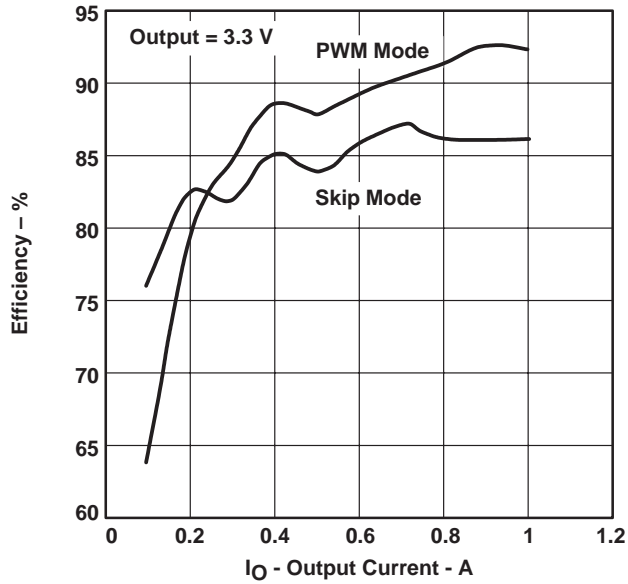


Figure 12

PWM AND SKIP MODE EFFICIENCY
 COMPARISON

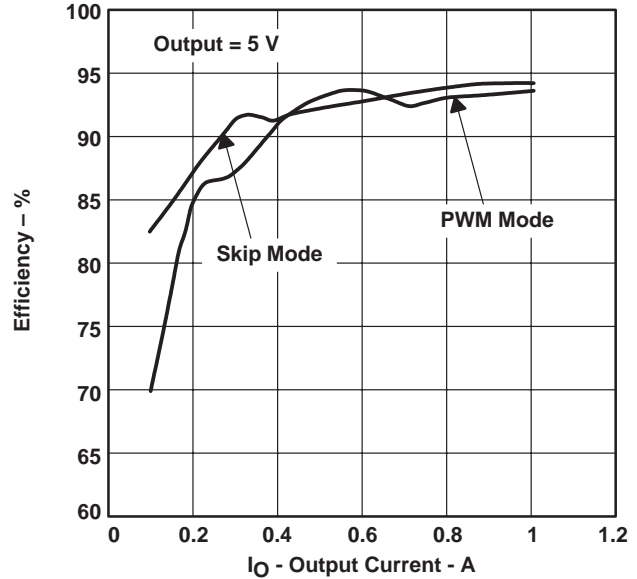


Figure 13

EFFICIENCY
 vs
 OUTPUT CURRENT

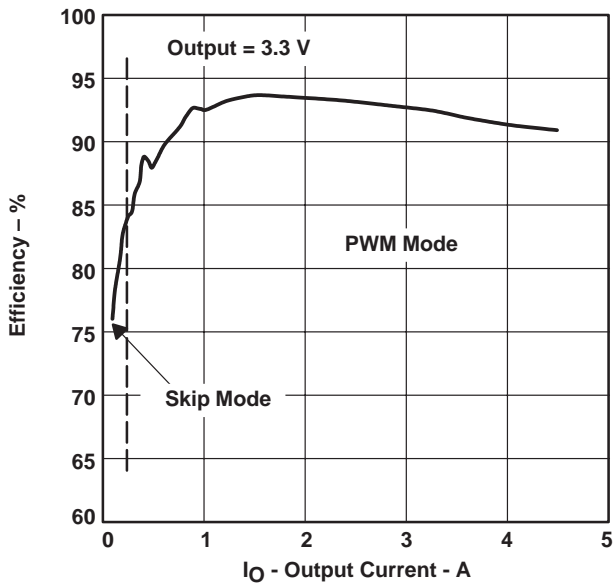


Figure 14

EFFICIENCY
 vs
 OUTPUT CURRENT

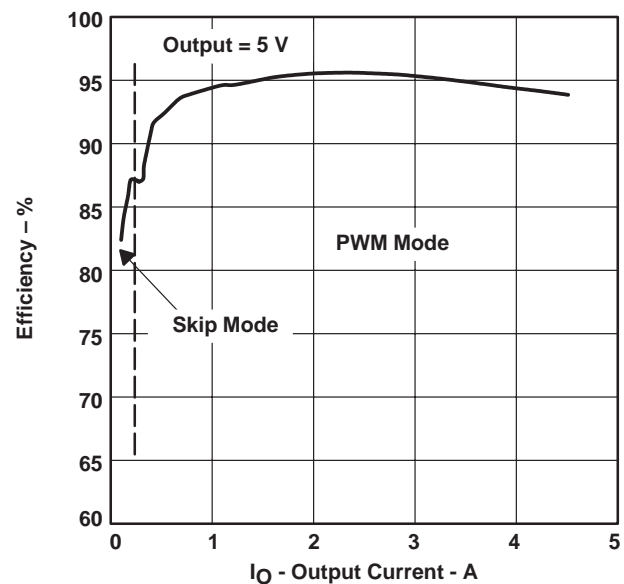


Figure 15

APPLICATION INFORMATION

EFFICIENCY
 VS
 OUTPUT CURRENT

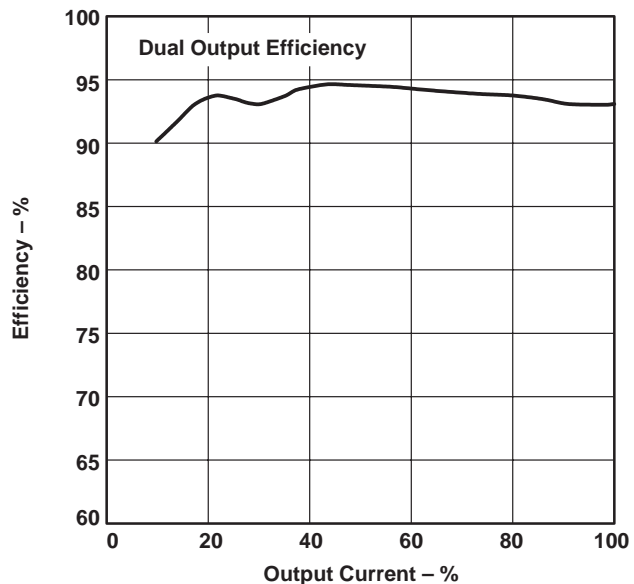


Figure 16

OUTPUT LOAD REGULATION

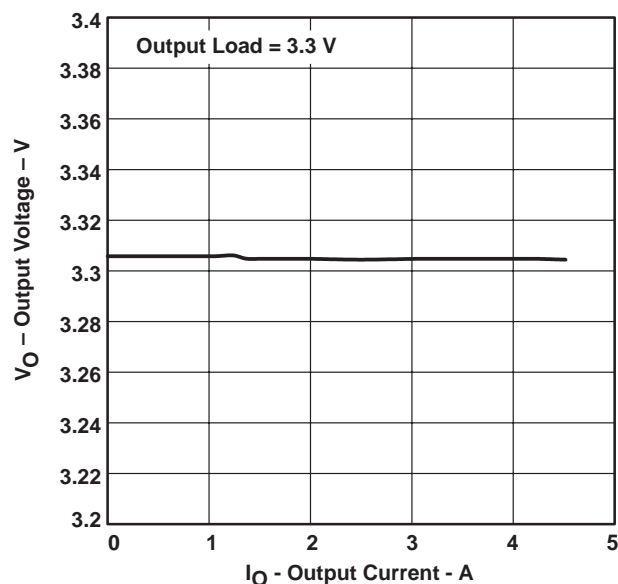


Figure 17

OUTPUT LOAD REGULATION

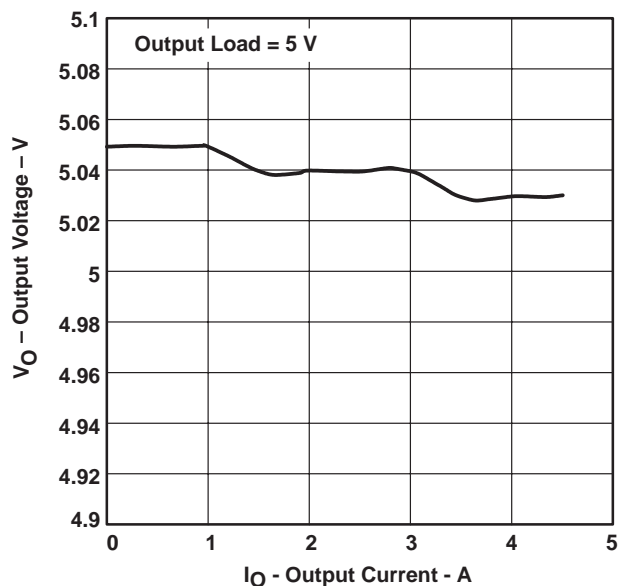


Figure 18

OUTPUT LINE REGULATION

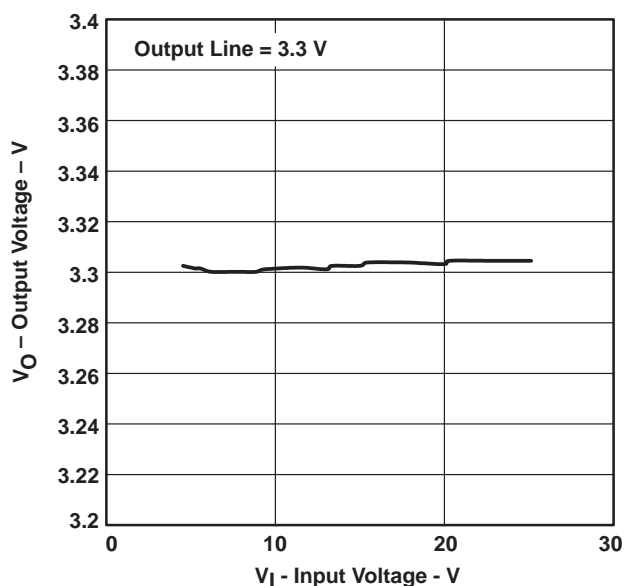


Figure 19

APPLICATION INFORMATION

OUTPUT LINE REGULATION

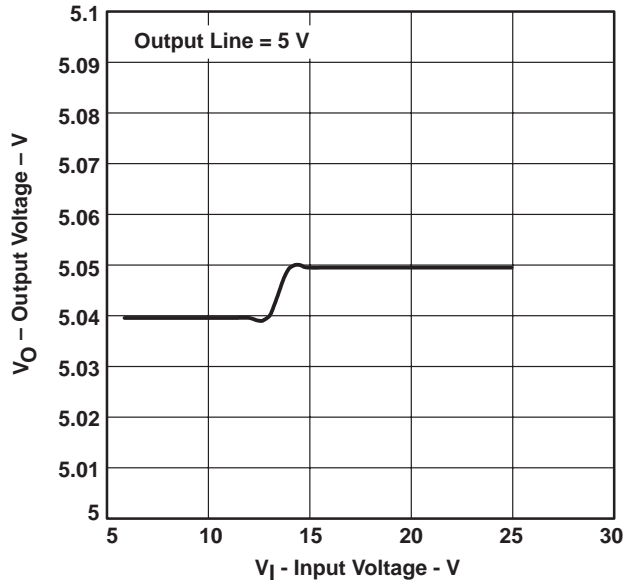


Figure 20

DIODE VERSION EFFICIENCY

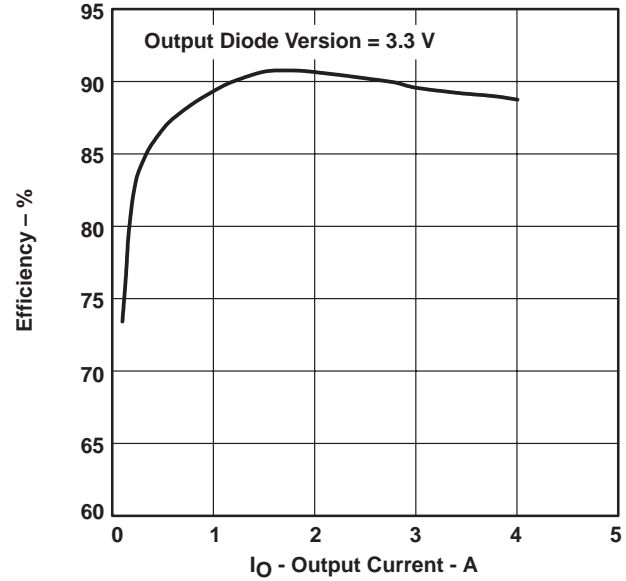


Figure 21

3.3-V OUTPUT VOLTAGE RIPPLE

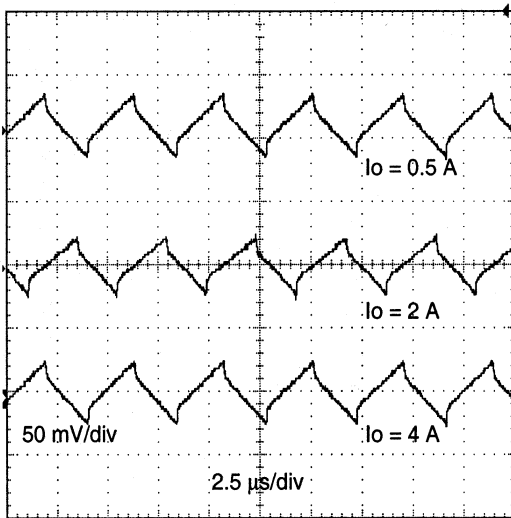


Figure 22

5-V OUTPUT VOLTAGE RIPPLE

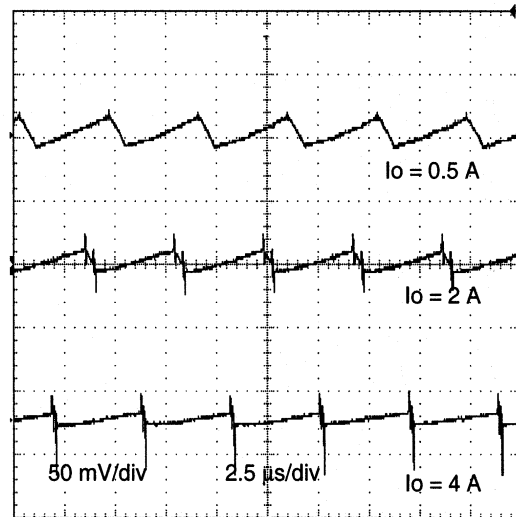


Figure 23

TPS5102

DUAL, HIGH-EFFICIENCY CONTROLLER FOR NOTEBOOK PC POWER

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APPLICATION INFORMATION

Table 1. Bill of Materials

| REF. | PN | DESCRIPTION | MANUFACTURER | SIZE |
|-----------|-----------------|--|---------------|------------------------|
| C1 | RV-35V221MH10-R | Capacitor, electrolytic, 220 μ F, 35 V | ELNA | 10x10mm |
| C1†opt | 10TPB220M | Capacitor, POSCAP, 220 μ F, 10 V | Sanyo | 7.3x4.3mm |
| C2 | GMK325F106ZH | Capacitor, ceramic, 10 μ F, 35 V | Taiyo Yuden | 1210 |
| C3 | GMK325F106ZH | Capacitor, ceramic, 10 μ F, 35 V | Taiyo Yuden | 1210 |
| C4 | 4TPB470M | Capacitor, POSCAP, 470 μ F, 4 V | Sanyo | 7.3x4.3mm |
| C5 | 10TPB220M | Capacitor, POSCAP, 220 μ F, 10 V | Sanyo | 7.3x4.3mm |
| C5†opt | 6TPB330M | Capacitor, POSCAP, 330 μ F, 6.3 V | Sanyo | 7.3x4.3mm |
| C6† | Standard | Open, capacitor, ceramic, 0.22 μ F, 16 V | | 805 |
| C7 | Standard | Capacitor, ceramic, 0.01 μ F, 16 V | | 805 |
| C8 | Standard | Capacitor, ceramic, 220 pF, 16 V | | 805 |
| C9 | Standard | Capacitor, ceramic, 0.01 μ F, 16 V | | 805 |
| C10 | Standard | Capacitor, ceramic, 100 pF, 16 V | | 805 |
| C11 | Standard | Capacitor, ceramic, 1 μ F, 16 V | muRata | 805 |
| C12 | GMK316F225ZG | Capacitor, ceramic, 2.2 μ F, 35 V | Taiyo Yuden | 1206 |
| C13 | Standard | Capacitor, ceramic, 0.01 μ F, 16 V | | 805 |
| C14 | Standard | Capacitor, ceramic, 220 pF, 16 V | | 805 |
| C15 | Standard | Capacitor, ceramic, 0.1 μ F, 16 V | | 805 |
| C16† | Standard | Open, capacitor, ceramic, 0.1 μ F, 16 V | | 805 |
| C17 | GMK316F225ZG | Capacitor, ceramic, 2.2 μ F, 35 V | Taiyo Yuden | 1206 |
| C18 | Standard | Open | | 805 |
| C19 | Standard | Open | | 805 |
| C20 | GMK325F106ZH | Capacitor, ceramic, 10 μ F, 35 V | Taiyo Yuden | 1210 |
| C21 | GMK316F225ZG | Capacitor, ceramic, 2.2 μ F, 35 V | Taiyo Yuden | 1206 |
| C22† | | | | 7.3x4.3mm |
| C23† | | | | 7.3x4.3mm |
| D1 | MBRS340T3 | Diode, Schottky, 40 V, 3 A | Motorola | SMC |
| D2 | MBRS340T3 | Diode, Schottky, 40 V, 3 A | Motorola | SMC |
| D3 | SD103-AWDICT-ND | Diode, Schottky, 40 V, 200 mA | Digikey | 3.5x1.5mm |
| D4 | SD103-AWDICT-ND | Diode, Schottky, 40 V, 200 mA | Digikey | 3.5x1.5mm |
| L1 | DO3316P-682 | Inductor, 6.8 μ H, 4.4 A | Coilcraft | 0.5x0.37in |
| L2 | DO3316P-682 | Inductor, 6.8 μ H, 4.4 A | Coilcraft | 0.5x0.37in |
| J1-J16 | CA26DA-D36W-OFC | Edge connector, surface mount, 0.040" board, 0.090" standoff | NAS Interplex | 0.040in |
| JP1 | S1132-2-ND | Header, straight, 2-pin, 0.1 ctrs, 0.3" pins | Sullins | DigiKey # 1132-2-ND |
| JP1 shunt | S1132-14-ND | Shunt, jumper, 0.1" | Sullins | DigiKey # 929950-00-ND |
| JP2 | S1132-14-ND | Header, straight, 2-pin, 0.1 ctrs, 0.3" pins | Sullins | DigiKey # 1132-2-ND |
| R1 | Standard | Resistor, 5.1 Ω , 5% | | 805 |
| R2 | Standard | Resistor, 5.1 Ω , 5% | | 805 |
| R3† | Standard | Open | | 805 |
| R4 | Standard | Resistor, 1.21 k Ω , 1% | | 805 |
| R5 | Standard | Resistor, 680 Ω , 1% | | 805 |
| R6 | Standard | Resistor, 5.1 k Ω , 5% | | 805 |
| R8 | Standard | Resistor, 1 k Ω , 5% | | 805 |

† Option table



TPS5102

DUAL, HIGH-EFFICIENCY CONTROLLER FOR NOTEBOOK PC POWER

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APPLICATION INFORMATION

Table 1. Bill of Materials (continued)

| REF. | PN | DESCRIPTION | MANUFACTURER | SIZE |
|------|----------|--|--------------|-------|
| R9 | Standard | Resistor, 82 kΩ, 5% | | 805 |
| R10 | Standard | Resistor, 1 kΩ, 5% | | 805 |
| R11 | Standard | Resistor, 0 Ω, 5% | | 805 |
| R12 | Standard | Resistor, 1 kΩ, 5% | | 805 |
| R13 | Standard | Resistor, 1 kΩ, 5% | | 805 |
| R14 | Standard | Resistor, 310 kΩ, 1% | | 805 |
| R15 | Standard | Resistor, 1 kΩ, 1% | | 805 |
| R16† | Standard | Open resistor, 5.1 Ω, 5% | | 805 |
| R17 | Standard | Resistor, 15 Ω, 5% | | 805 |
| R18 | Standard | Resistor, 7.5 kΩ, 5% | | 805 |
| R19 | Standard | Resistor, 7.5 kΩ, 5% | | 805 |
| R20 | Standard | Resistor, 15 Ω, 5% | | 805 |
| R21 | Standard | Open | | 805 |
| Q1 | Si4410DY | Transistor, MOSFET, n-ch, 30 V, 10 A, 13 mΩ, | Siliconix | SO-8 |
| Q2 | Si4410DY | Transistor, MOSFET, n-ch, 30 V, 10 A, 13 mΩ, | Siliconix | SO-8 |
| Q3 | Si4410DY | Transistor, MOSFET, n-ch, 30 V, 10 A, 13 mΩ, | Siliconix | SO-8 |
| Q4 | Si4410DY | Transistor, MOSFET, n-ch, 30 V, 10 A, 13 mΩ, | Siliconix | SO-8 |
| U1 | TPS5102 | IC, Dual Controller | TI | TSSOP |

† Option table

This EVM is designed to cover as many applications as possible. For some more specific applications, the circuit can be simpler. The table below gives some recommendations.

Table 2. EVM Application Recommendations

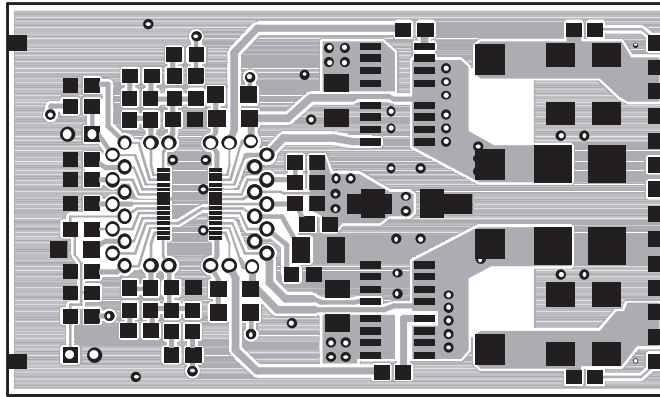
| 5V INPUT VOLTAGE | <3-A OUTPUT CURRENT | DIODE VERSION |
|---|--|--------------------------------------|
| Change C1 to low profile capacitor Sanyo 10TPB220M (220 μF, 10 V) Or 6TPB330M (330 μF, 6.3 V) | Change Q1/Q2 and Q3/Q4 to dual pack MOS-FET, IRF7311 to reduce the cost. | Remove Q2 and Q4 to reduce the cost. |
| Remove R12 | | |

Table 3. Vendor and Source Information

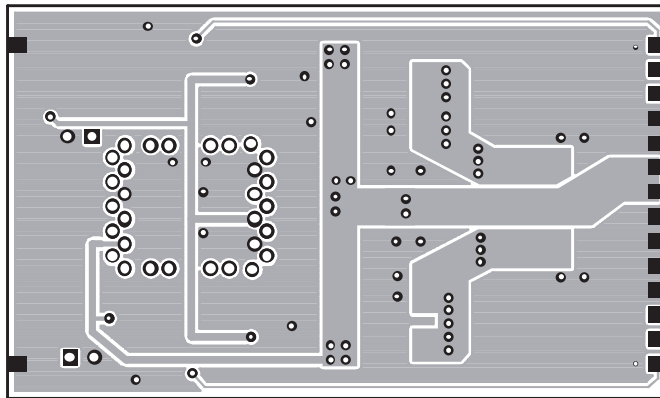
| MATERIAL | SOURCE | PART NUMBER | DISTRIBUTORS |
|---|-----------------------------|------------------------------------|------------------------------------|
| MOSFETS (Q1–Q4) | In EVM Design | Si4410DY (SILICONIX) | Local Distributor |
| | Second Source | IRF7811 (International Rectifier) | |
| INPUT CAPACITORS (C1) | In EVM Design | RV–35V221MH10–R (ELNA) | Bell Microproducts 972–783–4191 |
| | Second Source | 35CV330AX/GX (Sanyo) | 870–633–5030 |
| | | UUR1V221MNR1GS (Nichicon) | Future Electronics (Local Office) |
| MAIN DIODES (D1 – D2) | In EVM Design | MBRS340T3 (Motorola) | Local Distributors |
| | Second Source | U3FWJ44N (Toshiba) | |
| INDUCTORS (L1 – L2) | In EVM Design | DO3316P–682 (Coilcraft) | 972–248–3575 |
| | Second Source | CTDO3316P–682 (Inductor Warehouse) | 800–533–8295 |
| CERAMIC CAPACITORS (C2, C3) (C12, C17, C21) | IN EVM Design | GMK325F106ZH | SMEC 512–331–1877 |
| | | GMK316F225ZG (Taiyo Yuden) | |
| | Taiyo Yuden, Representative | | e-mail: mike@millsales.com |



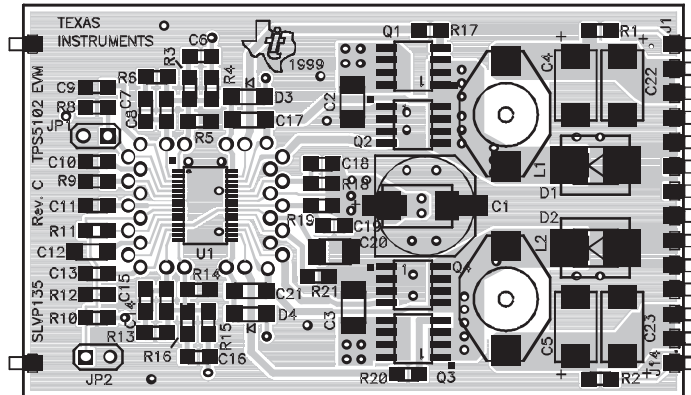
APPLICATION INFORMATION



Top Layer



Bottom Layer (Top View)

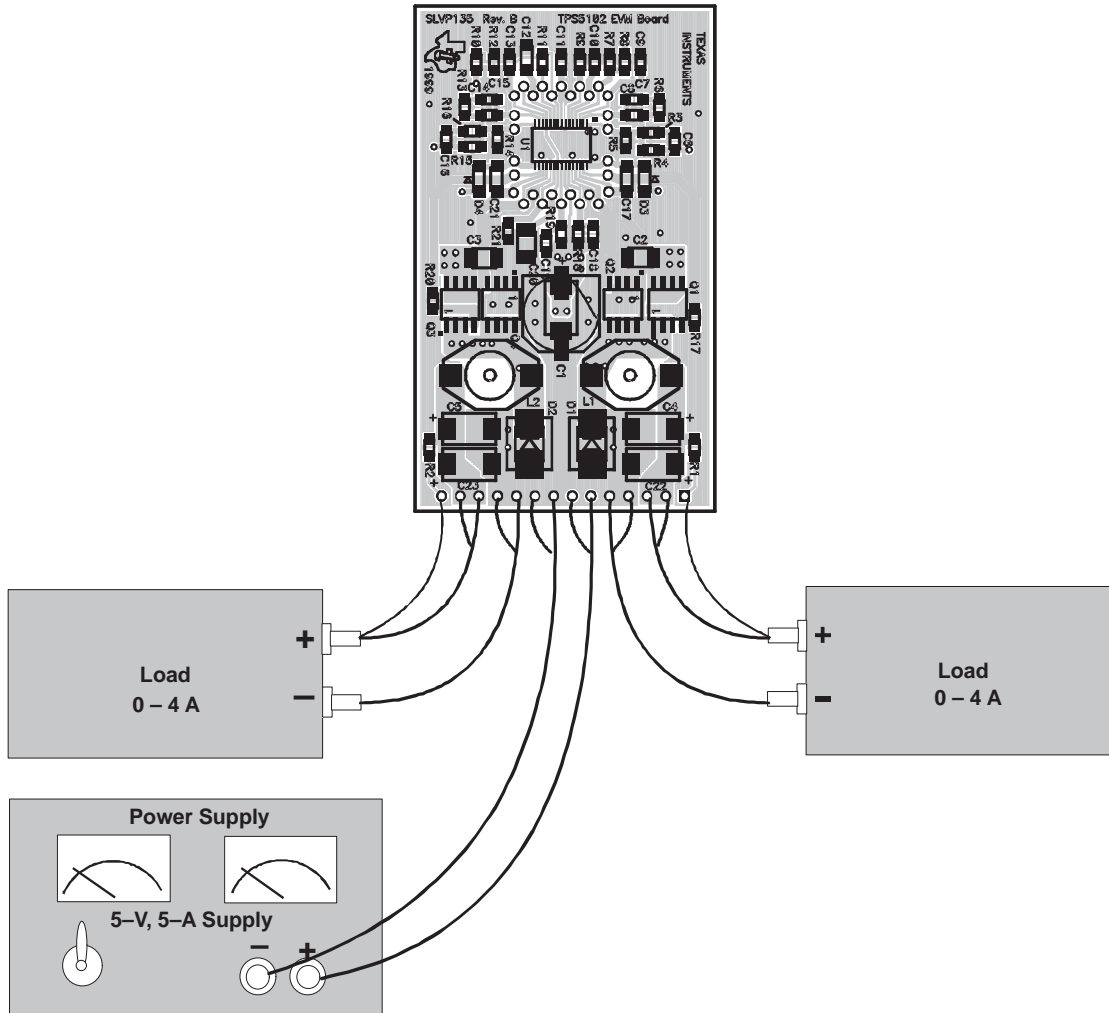


Top Assembly

TPS5102 DUAL, HIGH-EFFICIENCY CONTROLLER FOR NOTEBOOK PC POWER

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APPLICATION INFORMATION



NOTE: All wire pairs should be twisted.

Test Setup

TPS5102

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APPLICATION INFORMATION

High current applications are described in table . The values are recommendations based on actual test circuits. Many variations are possible based on the requirements of the user. Performance of the circuit is dependent upon the layout rather than the on specific components, if the device parameters are not exceeded. The power stage, having the highest current levels and greatest dv/dt rates, should be given the most attention, as both the supply and load can be severely affected by the power levels and edge rates.

Table 4. High Current Applications

| REFERENCE DESIGNATIONS | FUNCTION | 8-A OUTPUT | 12-A OUTPUT | 16-A OUTPUT |
|------------------------|-------------------------|--|--|---|
| C1 | Input Bulk Capacitor | 2x ELNA RV-35V221MH10-R 220 μ F, 35 V | 3x ELNA RV-35V221MH10-R 220 μ F, 35 V | 4x ELNA RV-35V221MH10-R 220 μ F, 35 V |
| C2 (C3) | Input Bypass Capacitor | 2x Taiyo Yuden GMK325F106ZH 10 μ F, 35 V | 3x Taiyo Yuden GMK325F106ZH 10 μ F, 35 V | 4x Taiyo Yuden GMK325F106ZH 10 μ F, 35 V |
| L1 (L2) | Output Filter Inductor | Coiltronics UP3B-2R2 2.2 μ H, 9.2 A | Coiltronics UP4B-1R5 1.5 μ H, 13.4 A | MicorMetals T68-8/90 Core w/7T, #16 1.0 μ H, 25 A |
| C4 (C22) | Output Filter Capacitor | 2x Sanyo 4TPB470M 470 μ F, 4 V | 3x Sanyo 4TPB470M 470 μ F, 4 V | 4x Sanyo 4TPB470M 470 μ F, 4 V |
| C5 (C23) | Output Filter Capacitor | 2x Sanyo 6TPB330M 330 μ F, 6.3 V | 3x Sanyo 6TPB330M 330 μ F, 6.3 V | 4x Sanyo 6TPB330M 330 μ F, 6.3 V |
| Q1 (Q3) | Power Switch | 2x Siliconix Si4410DY 30 V, 10 A, 13 m Ω | 3x Siliconix Si4410DY 30 V, 10 A, 13 m Ω | 4x Siliconix Si4410DY 30 V, 10 A, 13 m Ω |
| Q2 (Q4) | Power Switch | 2x Siliconix Si4410DY 30 V, 10 A, 13 m Ω | 3x Siliconix Si4410DY 30 V, 10 A, 13 m Ω | 4x Siliconix Si4410DY 30 V, 10 A, 13 m Ω |
| R17 (R20) | Gate Drive Resistor | 7 Ω | 5 Ω | 4 Ω |
| R18 (R19) | Current Limit Resistor | 10 k Ω | 15 k Ω | 20 k Ω |
| Switching Frequency | | 200 kHz | 150 kHz | 100 kHz |

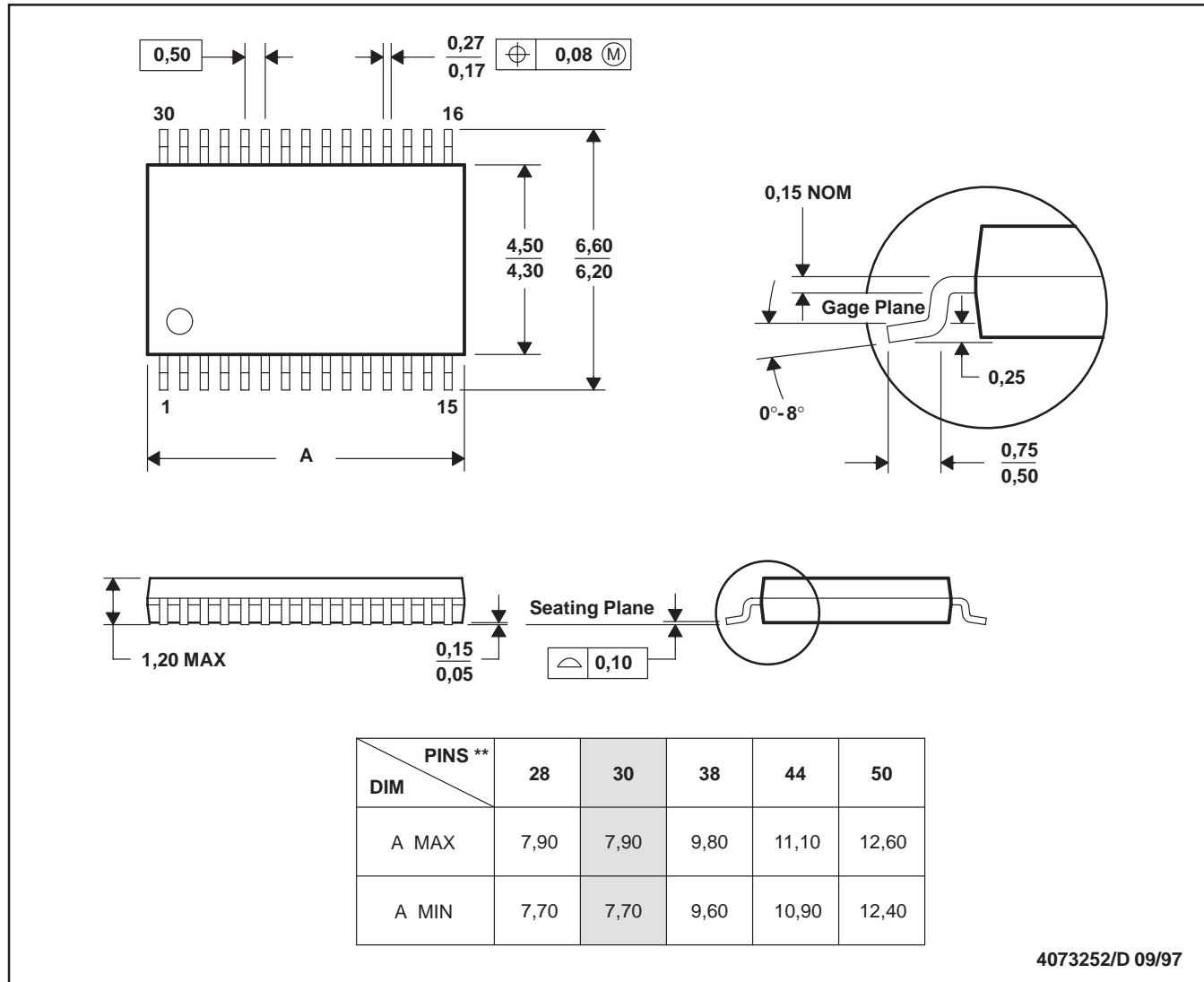
TPS5102 DUAL, HIGH-EFFICIENCY CONTROLLER FOR NOTEBOOK PC POWER

SLVS239 - SEPTEMBER 1999

DBT (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

30 PINS SHOWN



4073252/D 09/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion.
 D. Falls within JEDEC MO-153

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| TPS5102IDBT | ACTIVE | TSSOP | DBT | 30 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS5102IDBTG4 | ACTIVE | TSSOP | DBT | 30 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS5102IDBTR | ACTIVE | TSSOP | DBT | 30 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS5102IDBTRG4 | ACTIVE | TSSOP | DBT | 30 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

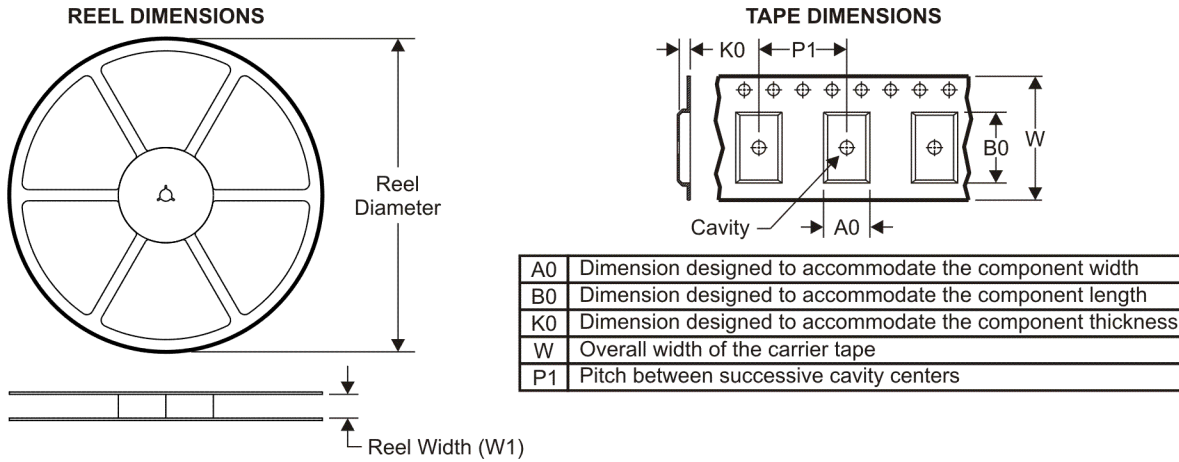
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

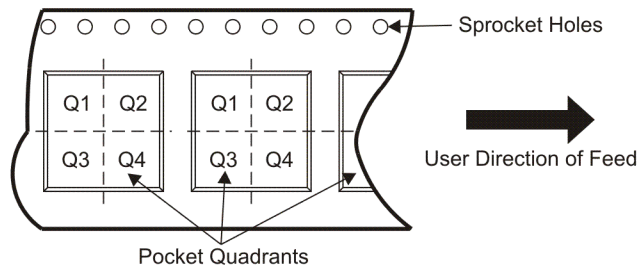
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TAPE AND REEL INFORMATION



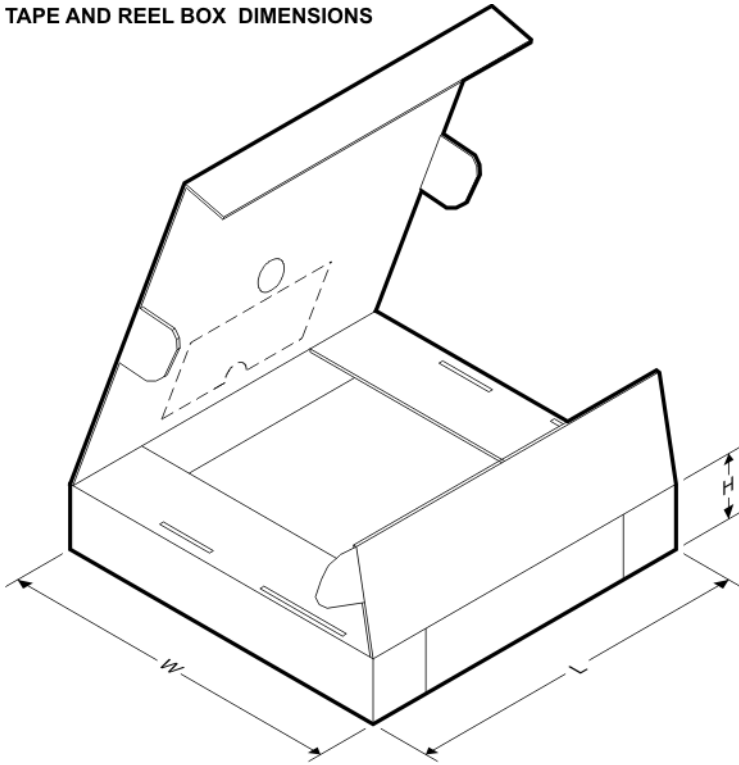
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS5102IDBTR | TSSOP | DBT | 30 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS5102IDBTR | TSSOP | DBT | 30 | 2000 | 346.0 | 346.0 | 33.0 |

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