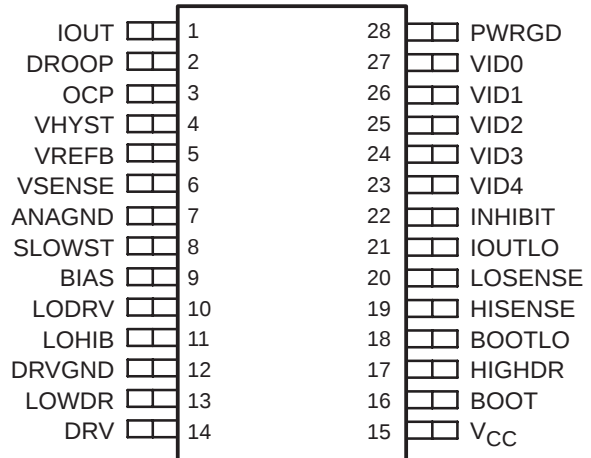


# TPS5210 PROGRAMMABLE SYNCHRONOUS-BUCK REGULATOR CONTROLLER

SLVS171A – SEPTEMBER 1998 – REVISED MAY 1999

- **±1% Reference Over Full Operating Temperature Range**
- **Synchronous Rectifier Driver for Greater Than 90% Efficiency**
- **Programmable Reference Voltage Range of 1.3 V to 3.5 V**
- **User-Selectable Hysteretic Type Control**
- **Droop Compensation for Improved Load Transient Regulation**
- **Adjustable Overcurrent Protection**
- **Programmable Softstart**
- **Overvoltage Protection**
- **Active Deadtime Control**
- **Power Good Output**
- **Internal Bootstrap Schottky Diode**
- **Low Supply Current . . . 3-mA Typ**

**DW OR PWP PACKAGE  
(TOP VIEW)**



## description

The TPS5210 is a synchronous-buck regulator controller which provides an accurate, programmable supply voltage to microprocessors. An internal 5-bit DAC is used to program the reference voltage to within a range of 1.3 V to 3.5 V. The output voltage can be set to be equal to the reference voltage or to some multiple of the reference voltage. A hysteretic controller with user-selectable hysteresis and programmable droop compensation is used to dramatically reduce overshoot and undershoot caused by load transients. Propagation delay from the comparator inputs to the output drivers is less than 250 ns. Overcurrent shutdown and crossover protection for the output drivers combine to eliminate destructive faults in the output FETs. The softstart current source is proportional to the reference voltage, thereby eliminating variation of the softstart timing when changes are made to the output voltage. PWRGD monitors the output voltage and pulls the open-collector output low when the output drops 7% below the nominal output voltage. An overvoltage circuit disables the output drivers if the output voltage rises 15% above the nominal value. The inhibit pin can be used to control power sequencing. Inhibit and undervoltage lockout assures the 12-V supply voltage and system supply voltage (5 V or 3.3 V) are within proper operating limits before the controller starts. Single-supply (12 V) operation is easily accomplished using a low-current divider for the required 5-V signals. The output driver circuits include 2-A drivers with internal 8-V gate-voltage regulators. The high-side driver can be configured either as a ground-referenced driver or as a floating bootstrap driver. The TPS5210 is available in a 28-pin SOIC package and a 28-pin TSSOP PowerPAD™ package. It operates over a junction temperature range of 0°C to 125°C.

**AVAILABLE OPTIONS**

| T <sub>J</sub> | PACKAGES  |             |
|----------------|-----------|-------------|
|                | SOIC (DW) | TSSOP (PWP) |
| 0°C to 125°C   | TPS5210DW | TPS5210PWPR |

The DW package is available taped and reeled. Add R suffix to device type (e.g., TPS5210DWR).



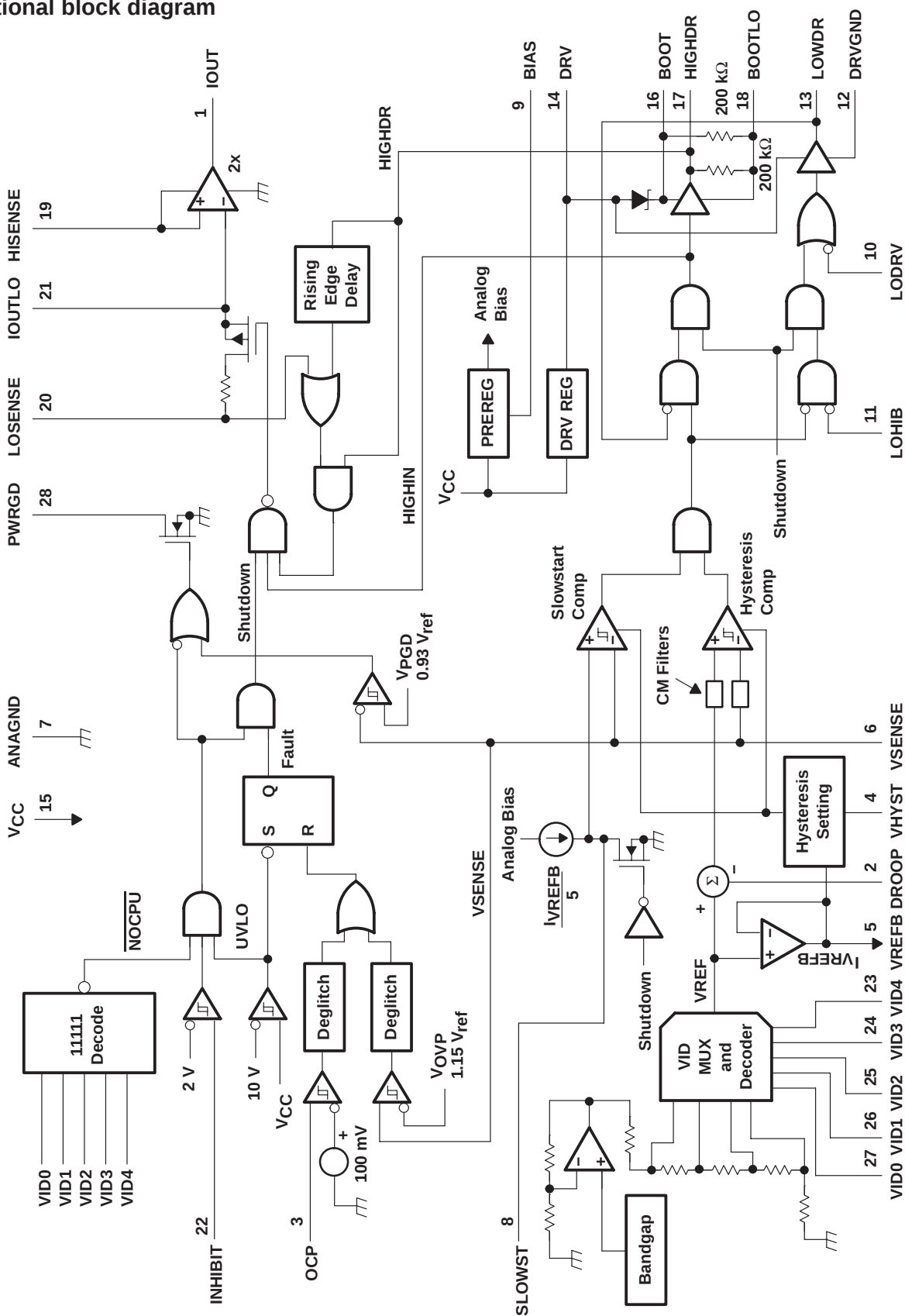
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1999, Texas Instruments Incorporated



# TPS5210

## PROGRAMMABLE SYNCHRONOUS BUCK REGULATOR CONTROLLER

SLVS171A – SEPTEMBER 1998 – REVISED MAY 1999

### Terminal Functions

| TERMINAL |     | I/O | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                 |
|----------|-----|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME     | NO. |     |                                                                                                                                                                                                                                                                                                                                                                             |
| ANAGND   | 7   |     | Analog ground                                                                                                                                                                                                                                                                                                                                                               |
| BIAS     | 9   | O   | Analog BIAS pin. A 1-μF ceramic capacitor should be connected from BIAS to ANAGND.                                                                                                                                                                                                                                                                                          |
| BOOT     | 16  | I   | Bootstrap. Connect a 1-μF low-ESR capacitor from BOOT to BOOTLO.                                                                                                                                                                                                                                                                                                            |
| BOOTLO   | 18  | O   | Bootstrap low. Connect BOOTLO to the junction of the high-side and low-side FETs for floating drive configuration. Connect BOOTLO to PGND for ground reference drive configuration.                                                                                                                                                                                         |
| DROOP    | 2   | I   | Droop voltage. Voltage input used to set the amount of output-voltage set-point droop as a function of load current. The amount of droop compensation is set with a resistor divider between IOUT and ANAGND.                                                                                                                                                               |
| DRV      | 14  | O   | Drive regulator for the FET drivers. A 1-μF ceramic capacitor should be connected from DRV to DRVGNL.                                                                                                                                                                                                                                                                       |
| DRVGNL   | 12  |     | Drive ground. Ground for FET drivers. Connect to FET PWRGNL.                                                                                                                                                                                                                                                                                                                |
| HIGHDR   | 17  | O   | High drive. Output drive to high-side power switching FETs                                                                                                                                                                                                                                                                                                                  |
| HISENSE  | 19  | I   | High current sense. For current sensing across high-side FETs, connect to the drain of the high-side FETs; for optional resistor sensing scheme, connect to power supply side of current-sense resistor placed in series with high-side FET drain.                                                                                                                          |
| INHIBIT  | 22  | I   | Disables the drive signals to the MOSFET drivers. Can also serve as UVLO for system logic supply (either 3.3 V or 5 V).                                                                                                                                                                                                                                                     |
| IOUT     | 1   | O   | Current out. Output voltage on this pin is proportional to the load current as measured across the Rds(on) of the high-side FETs. The voltage on this pin equals $2 \times R_{ds(on)} \times I_{OUT}$ . In applications where very accurate current sensing is required, a sense resistor should be connected between the input supply and the drain of the high-side FETs. |
| IOUTLO   | 21  | O   | Current sense low output. This is the voltage on the LOSENSE pin when the high-side FETs are on. A ceramic capacitor should be connected from IOUTLO to HISENSE to hold the sensed voltage while the high-side FETs are off. Capacitance range should be between 0.033 μF and 0.1 μF.                                                                                       |
| LODRV    | 10  | I   | Low drive enable. Normally tied to 5 V. To activate the low-side FETs as a crowbar, pull LODRV low.                                                                                                                                                                                                                                                                         |
| LOHIB    | 11  | I   | Low side inhibit. Connect to the junction of the high and low side FETs to control the anti-cross-conduction and eliminate shoot-through current. Disabled when configured in crowbar mode.                                                                                                                                                                                 |
| LOSENSE  | 20  | I   | Low current sense. For current sensing across high-side FETs, connect to the source of the high-side FETs; for optional resistor sensing scheme, connect to high-side FET drain side of current-sense resistor placed in series with high-side FET drain.                                                                                                                   |
| LOWDR    | 13  | O   | Low drive. Output drive to synchronous rectifier FETs                                                                                                                                                                                                                                                                                                                       |
| OCF      | 3   | I   | Over current protection. Current limit trip point is set with a resistor divider between IOUT and ANAGND.                                                                                                                                                                                                                                                                   |
| PWRGD    | 28  | O   | Power good. Power Good signal goes high when output voltage is within 7% of voltage set by VID pins. Open-drain output.                                                                                                                                                                                                                                                     |
| SLOWST   | 8   | O   | Slow Start (soft start). A capacitor from SLOWST to ANAGND sets the slowstart time. Slowstart current = $I_{VREFB}/5$                                                                                                                                                                                                                                                       |
| VCC      | 15  |     | 12-V supply. A 1-μF ceramic capacitor should be connected from VCC to DRVGNL.                                                                                                                                                                                                                                                                                               |
| VHYSF    | 4   | I   | HYSTERESIS set pin. The hysteresis is set with a resistor divider from VREFB to ANAGND. The hysteresis window = $2 \times (V_{REFB} - V_{HYSF})$                                                                                                                                                                                                                            |
| VID0     | 27  | I   | Voltage Identification input 0                                                                                                                                                                                                                                                                                                                                              |
| VID1     | 26  | I   | Voltage Identification input 1                                                                                                                                                                                                                                                                                                                                              |
| VID2     | 25  | I   | Voltage Identification input 2                                                                                                                                                                                                                                                                                                                                              |
| VID3     | 24  | I   | Voltage Identification input 3                                                                                                                                                                                                                                                                                                                                              |
| VID4     | 23  | I   | Voltage Identification input 4. Digital inputs that set the output voltage of the converter. The code pattern for setting the output voltage is located in Table 1. Internally pulled up to 5 V with a resistor divider biased from VCC.                                                                                                                                    |
| VREFB    | 5   | O   | Buffered reference voltage from VID network                                                                                                                                                                                                                                                                                                                                 |
| VSENSE   | 6   | I   | Voltage sense Input. To be connected to converter output voltage bus to sense and control output voltage. It is recommended an RC low pass filter be connected at this pin to filter noise.                                                                                                                                                                                 |



# TPS5210

## PROGRAMMABLE SYNCHRONOUS BUCK REGULATOR CONTROLLER

SLVS171A – SEPTEMBER 1998 – REVISED MAY 1999

---

### detailed description

#### $V_{REF}$

The reference/voltage identification (VID) section consists of a temperature-compensated bandgap reference and a 5-bit voltage selection network. The 5 VID terminals are inputs to the VID selection network and are TTL-compatible inputs internally pulled up to 5 V by a resistor divider connected to  $V_{CC}$ . The VID codes conform to the Intel *VRM 8.3 DC-DC Converter Specification* for voltage settings between 1.8 V and 3.5 V, and they are decremented by 50 mV, down to 1.3 V, for the lower VID settings. Voltages higher than  $V_{REF}$  can be implemented using an external divider. Refer to Table 1 for the VID code settings. The output voltage of the VID network,  $V_{REF}$ , is within  $\pm 1\%$  of the nominal setting over the VID range of 1.3 V to 2.5 V, including a junction temperature range of  $5^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , and a  $V_{CC}$  supply voltage range of 11.4 V to 12.6 V. The output of the reference/VID network is indirectly brought out through a buffer to the  $V_{REFB}$  pin. The voltage on this pin will be within 2% of  $V_{REF}$ . It is not recommended to drive loads with  $V_{REFB}$ , other than setting the hysteresis of the hysteretic comparator, because the current drawn from  $V_{REFB}$  sets the charging current for the slowstart capacitor. Refer to the slowstart section for additional information.

#### hysteretic comparator

The hysteretic comparator regulates the output voltage of the synchronous-buck converter. The hysteresis is set by 2 external resistors and is centered on  $V_{REF}$ . The 2 external resistors form a resistor divider from  $V_{REFB}$  to ANAGND, with the output voltage connecting to the  $V_{HYST}$  pin. The hysteresis of the comparator will be equal to twice the voltage *difference* between the  $V_{REFB}$  and  $V_{HYST}$  pins. The propagation delay from the comparator inputs to the driver outputs is 250 ns (maximum). The maximum hysteresis setting is 60 mV.

#### low-side driver

The low-side driver is designed to drive low- $R_{ds(on)}$  n-channel MOSFETs. The current rating of the driver is 2 A, source and sink. The bias to the low-side driver is internally connected to the DRV regulator.

#### high-side driver

The high-side driver is designed to drive low- $R_{ds(on)}$  n-channel MOSFETs. The current rating of the driver is 2 A, source and sink. The high-side driver can be configured either as a ground-referenced driver or as a floating bootstrap driver. When configured as a floating driver, the bias voltage to the driver is developed from the DRV regulator. The internal bootstrap diode, connected between the DRV and BOOT pins, is a Schottky for improved drive efficiency. The maximum voltage that can be applied between BOOT and DRVGNDA is 30 V. The driver can be referenced to ground by connecting BOOTLO to DRVGNDA, and connecting BOOT to either DRV or  $V_{CC}$ .

#### deadtime control

Deadtime control prevents shoot-through current from flowing through the main power FETs during switching transitions by actively controlling the turn-on times of the MOSFET drivers. The high-side driver is not allowed to turn on until the gate-drive voltage to the low-side FETs is below 2 V; the low-side driver is not allowed to turn on until the voltage at the junction of the high-side and low-side FETs ( $V_{phase}$ ) is below 2 V.

#### current sensing

Current sensing is achieved by sampling and holding the voltage across the high-side power FETs while the high-side FETs are on. The sampling network consists of an internal  $60\text{-}\Omega$  switch and an external ceramic hold capacitor. Recommended value of the hold capacitor is between  $0.033\text{ }\mu\text{F}$  and  $0.1\text{ }\mu\text{F}$ . Internal logic controls the turn-on and turn-off of the sample/hold switch such that the switch does not turn on until the  $V_{phase}$  voltage transitions high, and the switch turns off when the input to the high-side driver goes low. The sampling will occur only when the high-side FETs are conducting current. The voltage on the IOUT pin equals 2 times the sensed high-side voltage. In applications where a higher accuracy in current sensing is required, a sense resistor can be placed in series with the high-side FETs, and the voltage across the sense resistor can be sampled by the current sensing circuit.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

## **detailed description (continued)**

### **droop compensation**

The droop compensation network reduces the load transient overshoot/undershoot on  $V_O$ , relative to  $V_{REF}$ .  $V_O$  is programmed to a voltage greater than  $V_{REF}$  by an external resistor divider from  $V_O$  to  $V_{SENSE}$  to reduce the undershoot on  $V_O$  during a low-to-high load transient. The overshoot during a high-to-low load transient is reduced by subtracting the voltage on  $DROOP$  from  $V_{REF}$ . The voltage on  $IOUT$  is divided with an external resistor divider, and connected to  $DROOP$ .

### **inhibit**

$INHIBIT$  is a TTL-compatible digital input used to enable the controller. When  $INHIBIT$  is low, the output drivers are low and the slowstart capacitor is discharged. When  $INHIBIT$  goes high, the short across the slowstart capacitor is released and normal converter operation begins. When the system-logic supply is connected to  $INHIBIT$ , it also controls power sequencing by locking out controller operation until the system-logic supply exceeds the input threshold voltage of the inhibit circuit. The 12-V supply and the system logic supply (either 5 V or 3.3 V) must be above  $UVLO$  thresholds before the controller is allowed to start up. The start threshold is 2.1 V and the hysteresis is 100 mV for the  $INHIBIT$  comparator.

### **$V_{CC}$ undervoltage lockout (UVLO)**

The undervoltage lockout circuit disables the controller while the  $V_{CC}$  supply is below the 10-V start threshold during power up. When the controller is disabled, the output drivers will be low and the slowstart capacitor is discharged. When  $V_{CC}$  exceeds the start threshold, the short across the slowstart capacitor is released and normal converter operation begins. There is a 2-V hysteresis in the undervoltage lockout circuit for noise immunity.

### **slowstart**

The slowstart circuit controls the rate at which  $V_O$  powers up. A capacitor is connected between  $SLOWST$  and  $ANAGND$  and is charged by an internal current source. The current source is proportional to the reference voltage, so that the charging rate of  $C_{SLOWST}$  is proportional to the reference voltage. By making the charging current proportional to  $V_{REF}$ , the power-up time for  $V_O$  will be independent of  $V_{REF}$ . Thus,  $C_{SLOWST}$  can remain the same value for all  $VID$  settings. The slowstart charging current is determined by the following equation:

$$I_{slowstart} = I(V_{REFB}) / 5 \quad (\text{amps})$$

Where  $I(V_{REFB})$  is the current flowing out of  $V_{REFB}$ .

It is recommended that no additional loads be connected to  $V_{REFB}$ , other than the resistor divider for setting the hysteresis voltage. The maximum current that can be sourced by the  $V_{REFB}$  circuit is 500  $\mu\text{A}$ . The equation for setting the slowstart time is:

$$t_{SLOWST} = 5 \times C_{SLOWST} \times R_{VREFB} \quad (\text{seconds})$$

Where  $R_{VREFB}$  is the total external resistance from  $V_{REFB}$  to  $ANAGND$ .

### **power good**

The power-good circuit monitors for an undervoltage condition on  $V_O$ . If  $V_O$  is 7% below  $V_{REF}$ , then the  $PWRGD$  pin is pulled low.  $PWRGD$  is an open-drain output.

### **overvoltage protection**

The overvoltage protection (OVP) circuit monitors  $V_O$  for an overvoltage condition. If  $V_O$  is 15% above  $V_{REF}$ , then a fault latch is set and both output drivers are turned off. The latch will remain set until  $V_{CC}$  goes below the undervoltage lockout value. A 3- $\mu\text{s}$  deglitch timer is included for noise immunity. Refer to the  $LODRV$  section for information on how to protect the microprocessor against overvoltages due to a shorted fault across the high-side power FET.

# TPS5210

## PROGRAMMABLE SYNCHRONOUS BUCK REGULATOR CONTROLLER

SLVS171A – SEPTEMBER 1998 – REVISED MAY 1999

### detailed description (continued)

#### overcurrent protection

The overcurrent protection (OCP) circuit monitors the current through the high-side FET. The overcurrent threshold is adjustable with an external resistor divider between IOUT and ANAGND, with the divider voltage connected to the OCP pin. If the voltage on OCP exceeds 100 mV, then a fault latch is set and the output drivers are turned off. The latch will remain set until  $V_{CC}$  goes below the undervoltage lockout value. A 3- $\mu$ s deglitch timer is included for noise immunity. The OCP circuit is also designed to protect the high-side power FET against a short-to-ground fault on the terminal common to both power FETs.

#### drive regulator

The drive regulator provides drive voltage to the output drivers. The minimum drive voltage is 7 V. The minimum short circuit current is 100 mA. Connect a 1- $\mu$ F ceramic capacitor from DRV to DRVND.

#### LODRV

The LODRV circuit is designed to protect the microprocessor against overvoltages that can occur if the high-side power FETs become shorted. External components to sense an overvoltage condition are required to use this feature. When an overvoltage fault occurs, the low-side FETs are used as a crowbar. LODRV is pulled low and the low-side FET will be turned on, overriding all control signals inside the TPS5210 controller. The crowbar action will short the input supply to ground through the faulted high-side FETs and the low-side FETs. A fuse in series with  $V_{in}$  should be added to disconnect the short-circuit.

**Table 1. Voltage Identification Codes**

| VID TERMINALS<br>(0 = GND, 1 = floating or pull-up to 5 V) |      |      |      |      | $V_{REF}$ |
|------------------------------------------------------------|------|------|------|------|-----------|
| VID4                                                       | VID3 | VID2 | VID1 | VID0 | (Vdc)     |
| 0                                                          | 1    | 1    | 1    | 1    | 1.30      |
| 0                                                          | 1    | 1    | 1    | 0    | 1.35      |
| 0                                                          | 1    | 1    | 0    | 1    | 1.40      |
| 0                                                          | 1    | 1    | 0    | 0    | 1.45      |
| 0                                                          | 1    | 0    | 1    | 1    | 1.50      |
| 0                                                          | 1    | 0    | 1    | 0    | 1.55      |
| 0                                                          | 1    | 0    | 0    | 1    | 1.60      |
| 0                                                          | 1    | 0    | 0    | 0    | 1.65      |
| 0                                                          | 0    | 1    | 1    | 1    | 1.70      |
| 0                                                          | 0    | 1    | 1    | 0    | 1.75      |
| 0                                                          | 0    | 1    | 0    | 1    | 1.80      |
| 0                                                          | 0    | 1    | 0    | 0    | 1.85      |
| 0                                                          | 0    | 0    | 1    | 1    | 1.90      |
| 0                                                          | 0    | 0    | 1    | 0    | 1.95      |
| 0                                                          | 0    | 0    | 0    | 1    | 2.00      |
| 0                                                          | 0    | 0    | 0    | 0    | 2.05      |
| 1                                                          | 1    | 1    | 1    | 1    | No CPU    |
| 1                                                          | 1    | 1    | 1    | 0    | 2.10      |
| 1                                                          | 1    | 1    | 0    | 1    | 2.20      |
| 1                                                          | 1    | 1    | 0    | 0    | 2.30      |
| 1                                                          | 1    | 0    | 1    | 1    | 2.40      |
| 1                                                          | 1    | 0    | 1    | 0    | 2.50      |
| 1                                                          | 1    | 0    | 0    | 1    | 2.60      |

# TPS5210

## PROGRAMMABLE SYNCHRONOUS BUCK REGULATOR CONTROLLER

SLVS171A – SEPTEMBER 1998 – REVISED MAY 1999

**Table 1. Voltage Identification Codes (Continued)**

| VID TERMINALS<br>(0 = GND, 1 = floating or pull-up to 5 V) |      |      |      |      | V <sub>REF</sub>   |
|------------------------------------------------------------|------|------|------|------|--------------------|
| VID4                                                       | VID3 | VID2 | VID1 | VID0 | (V <sub>dc</sub> ) |
| 1                                                          | 1    | 0    | 0    | 0    | 2.70               |
| 1                                                          | 0    | 1    | 1    | 1    | 2.80               |
| 1                                                          | 0    | 1    | 1    | 0    | 2.90               |
| 1                                                          | 0    | 1    | 0    | 1    | 3.00               |
| 1                                                          | 0    | 1    | 0    | 0    | 3.10               |
| 1                                                          | 0    | 0    | 1    | 1    | 3.20               |
| 1                                                          | 0    | 0    | 1    | 0    | 3.30               |
| 1                                                          | 0    | 0    | 0    | 1    | 3.40               |
| 1                                                          | 0    | 0    | 0    | 0    | 3.50               |

**absolute maximum ratings over operating virtual junction temperature (unless otherwise noted)<sup>†</sup>**

|                                                                        |                              |
|------------------------------------------------------------------------|------------------------------|
| Supply voltage range, V <sub>CC</sub> (see Note1)                      | –0.3 V to 14 V               |
| Input voltage range: BOOT to DRV <sub>GND</sub> (High-side Driver ON)  | –0.3 V to 30 V               |
| BOOT to HIGH <sub>DRV</sub>                                            | –0.3 V to 15 V               |
| BOOT to BOOT <sub>LO</sub>                                             | –0.3 V to 15 V               |
| INHIBIT, VID <sub>x</sub> , LOD <sub>RV</sub>                          | –0.3 V to 7.3 V              |
| PWR <sub>GD</sub> , OCP, DROOP                                         | –0.3 V to 7 V                |
| LOHIB, LOSENSE, IOUT <sub>LO</sub> , HISENSE                           | –0.3 V to 14 V               |
| VSENSE                                                                 | –0.3 V to 5 V                |
| Voltage difference between ANA <sub>GND</sub> and DRV <sub>GND</sub>   | ±0.5 V                       |
| Output current, V <sub>REFB</sub>                                      | 0.5 mA                       |
| Short circuit duration, DRV                                            | Continuous                   |
| Continuous total power dissipation                                     | See Dissipation Rating Table |
| Operating virtual junction temperature range, T <sub>J</sub>           | 0°C to 125°C                 |
| Storage temperature range, T <sub>stg</sub>                            | –65°C to 150°C               |
| Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds | 260°C                        |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Unless otherwise specified, all voltages are with respect to ANA<sub>GND</sub>.

**DISSIPATION RATING TABLE**

| PACKAGE | T <sub>A</sub> ≤ 25°C<br>POWER RATING | DERATING FACTOR<br>ABOVE T <sub>A</sub> = 25°C | T <sub>A</sub> = 70°C<br>POWER RATING | T <sub>A</sub> = 85°C<br>POWER RATING |
|---------|---------------------------------------|------------------------------------------------|---------------------------------------|---------------------------------------|
| DW      | 1200 mW                               | 12 mW/°C                                       | 660 mW                                | 480 mW                                |
| PWP     | 1150 mW                               | 11.5 mW/°C                                     | 630 mW                                | 460 mW                                |



# TPS5210

## PROGRAMMABLE SYNCHRONOUS BUCK REGULATOR CONTROLLER

SLVS171A – SEPTEMBER 1998 – REVISED MAY 1999

### recommended operating conditions

|                                                        | MIN  | MAX  | UNIT |
|--------------------------------------------------------|------|------|------|
| Supply voltage, $V_{CC}$                               | 11.4 | 13   | V    |
| Input voltage, BOOT to DRVGN                           | 0    | 28   | V    |
| Input voltage, BOOT to BOOTLO                          | 0    | 13   | V    |
| Input voltage, INHIBIT, VIDx, LODRV, PWRGD, OCP, DROOP | 0    | 6    | V    |
| Input voltage, LOHIB, LOSENSE, IOUTLO, HISENSE         | 0    | 13   | V    |
| Input voltage, VSENSE                                  | 0    | 4.5  | V    |
| Voltage difference between ANAGND and DRVGN            | 0    | ±0.2 | V    |
| Output current, $V_{REFB}^{\dagger}$                   | 0    | 0.4  | mA   |

$\dagger$  Not recommended to load  $V_{REFB}$  other than to set hysteresis since  $I_{VREFB}$  sets slowstart time.

### electrical characteristics over recommended operating virtual junction temperature range, $V_{CC} = 12$ V, $I_{DRV} = 0$ A (unless otherwise noted)

#### reference/voltage identification

| PARAMETER  |                                                                             | TEST CONDITIONS                                                                     | MIN           | TYP       | MAX           | UNIT       |
|------------|-----------------------------------------------------------------------------|-------------------------------------------------------------------------------------|---------------|-----------|---------------|------------|
| $V_{REF}$  | Reference voltage accuracy, (Includes offset of droop compensation network) | $V_{CC} = 11.4$ to $12.6$ V, $1.3$ V $\leq V_{REF} \leq 2.5$ V                      | -0.01         |           | 0.01          | V/V        |
|            |                                                                             | $V_{CC} = 11.4$ to $12.6$ V, $V_{REF} = 2.6$ V                                      | -0.0104       |           | 0.0104        | V/V        |
|            |                                                                             | $V_{CC} = 11.4$ to $12.6$ V, $V_{REF} = 2.7$ V                                      | -0.0108       |           | 0.0108        | V/V        |
|            |                                                                             | $V_{CC} = 11.4$ to $12.6$ V, $V_{REF} = 2.8$ V                                      | -0.0112       |           | 0.0112        | V/V        |
|            |                                                                             | $V_{CC} = 11.4$ to $12.6$ V, $V_{REF} = 2.9$ V                                      | -0.0116       |           | 0.0116        | V/V        |
|            |                                                                             | $V_{CC} = 11.4$ to $12.6$ V, $V_{REF} = 3$ V                                        | -0.0120       |           | 0.0120        | V/V        |
|            |                                                                             | $V_{CC} = 11.4$ to $12.6$ V, $V_{REF} = 3.1$ V                                      | -0.0124       |           | 0.0124        | V/V        |
|            |                                                                             | $V_{CC} = 11.4$ to $12.6$ V, $V_{REF} = 3.2$ V                                      | -0.0128       |           | 0.0128        | V/V        |
|            |                                                                             | $V_{CC} = 11.4$ to $12.6$ V, $V_{REF} = 3.3$ V                                      | -0.0132       |           | 0.0132        | V/V        |
|            |                                                                             | $V_{CC} = 11.4$ to $12.6$ V, $V_{REF} = 3.4$ V                                      | -0.0136       |           | 0.0136        | V/V        |
|            |                                                                             | $V_{CC} = 11.4$ to $12.6$ V, $V_{REF} = 3.5$ V                                      | -0.0140       |           | 0.0140        | V/V        |
|            | Cumulative reference accuracy (see Note 2)                                  | $V_{REF} = 1.3$ V, Hysteresis window = 30 mV                                        | -0.011        |           | 0.011         | V/V        |
|            |                                                                             | $V_{REF} = 1.3$ V, Hysteresis, $T_J = 60^\circ\text{C}$ window = 30 mV (see Note 3) | -0.008        |           | 0.008         |            |
|            |                                                                             | $V_{REF} = 1.9$ V, Hysteresis, $T_J = 60^\circ\text{C}$ window = 30 mV (see Note 3) | -0.0090       |           | 0.0090        |            |
|            |                                                                             | $V_{REF} = 3.5$ V, Hysteresis, $T_J = 60^\circ\text{C}$ window = 30 mV (see Note 3) | -0.0115       |           | 0.0115        |            |
| VIDx       | High-level input voltage                                                    |                                                                                     | 2.25          |           |               | V          |
| VIDx       | Low-level input voltage                                                     |                                                                                     |               |           | 1             | V          |
| $V_{REFB}$ | Output voltage                                                              | $I_{VREFB} = 50$ $\mu\text{A}$                                                      | $V_{REF}-2\%$ | $V_{REF}$ | $V_{REF}+2\%$ | V          |
|            | Output regulation                                                           | $10$ $\mu\text{A} \leq I_O \leq 500$ $\mu\text{A}$                                  |               | 2         |               | mV         |
| VIDx       | Input resistance                                                            | $VIDx = 0$ V                                                                        | 36            | 73        | 95            | k $\Omega$ |
|            | Input pull-up voltage divider                                               |                                                                                     | 4.8           | 4.9       | 5             | V          |

NOTES: 2. Cumulative reference accuracy is the combined accuracy of the reference voltage and the input offset voltage of the hysteretic comparator. Cumulative accuracy equals the average of the high-level and low-level thresholds of the hysteretic comparator.  
3. This parameter is ensured by design and is not production tested.



# TPS5210

## PROGRAMMABLE SYNCHRONOUS BUCK REGULATOR CONTROLLER

SLVS171A – SEPTEMBER 1998 – REVISED MAY 1999

electrical characteristics over recommended operating virtual junction temperature range,  
 $V_{CC} = 12\text{ V}$ ,  $I_{DRV} = 0\text{ A}$  (unless otherwise noted) (continued)

### power good

| PARAMETER                   |                          | TEST CONDITIONS          | MIN | TYP | MAX  | UNIT          |
|-----------------------------|--------------------------|--------------------------|-----|-----|------|---------------|
| Undervoltage trip threshold |                          |                          | 90  | 93  | 95   | % $V_{REF}$   |
| $V_{OL}$                    | Low-level output voltage | $I_O = 5\text{ mA}$      |     | 0.5 | 0.75 | V             |
| $I_{OH}$                    | High-level input current | $V_{PWRGD} = 6\text{ V}$ |     | 1   |      | $\mu\text{A}$ |
| $V_{hys}$                   | Hysteresis voltage       |                          | 1.3 | 2.9 | 4.5  | % $V_{REF}$   |

### slowstart

| PARAMETER                       | TEST CONDITIONS                                                                                   | MIN  | TYP | MAX  | UNIT          |
|---------------------------------|---------------------------------------------------------------------------------------------------|------|-----|------|---------------|
| Charge current                  | $V_{SLOWST} = 0.5\text{ V}$ , $V_{VREFB} = 1.3\text{ V}$ ,<br>$I_{VREFB} = 65\text{ }\mu\text{A}$ | 10.4 | 13  | 15.6 | $\mu\text{A}$ |
| Discharge current               | $V_{SLOWST} = 1\text{ V}$                                                                         |      | 3   |      | mA            |
| Comparator input offset voltage |                                                                                                   |      |     | 10   | mV            |
| Comparator input bias current   | See Note 3                                                                                        |      | 10  | 100  | nA            |
| Comparator hysteresis           |                                                                                                   | -7.5 |     | 7.5  | mV            |

NOTE 3: This parameter is ensured by design and is not production tested.

### hysteretic comparator

| PARAMETER                  | TEST CONDITIONS                                                     | MIN  | TYP | MAX | UNIT |
|----------------------------|---------------------------------------------------------------------|------|-----|-----|------|
| Input offset voltage       | $V_{DROOP} = 0\text{ V}$ (see Note 3)                               | -2.5 |     | 2.5 | mV   |
| Input bias current         | See Note 3                                                          |      |     | 500 | nA   |
| Hysteresis accuracy        | $V_{REFB} - V_{HYST} = 15\text{ mV}$<br>(Hysteresis window = 30 mV) | -3.5 |     | 3.5 | mV   |
| Maximum hysteresis setting | $V_{REFB} - V_{HYST} = 30\text{ mV}$                                |      | 60  |     | mV   |

NOTE 3: This parameter is ensured by design and is not production tested.



# TPS5210

## PROGRAMMABLE SYNCHRONOUS BUCK REGULATOR CONTROLLER

SLVS171A – SEPTEMBER 1998 – REVISED MAY 1999

electrical characteristics over recommended operating virtual junction temperature range,  
 $V_{CC} = 12\text{ V}$ ,  $I_{DRV} = 0\text{ A}$  (unless otherwise noted) (continued)

### high-side VDS sensing

| PARAMETER              |                          | TEST CONDITIONS                                                                                                                      | MIN  | TYP | MAX  | UNIT          |
|------------------------|--------------------------|--------------------------------------------------------------------------------------------------------------------------------------|------|-----|------|---------------|
| Gain                   |                          |                                                                                                                                      |      | 2   |      | V/V           |
| Initial accuracy       |                          | $V_{HISENSE} = 12\text{ V}$ , $V_{LOSENSE} = 11.9\text{ V}$ ,<br>Differential input to $V_{DS}$ sensing amp = 100 mV                 | 194  |     | 206  | mV            |
| IOUTLO                 | Sink current             | $5\text{ V} \leq V_{IOUTLO} \leq 13\text{ V}$                                                                                        |      |     | 250  | nA            |
| IOUT                   | Source current           | $V_{IOUT} = 0.5\text{ V}$ , $V_{HISENSE} = 12\text{ V}$ ,<br>$V_{IOUTLO} = 11.5\text{ V}$                                            | 500  |     |      | $\mu\text{A}$ |
| IOUT                   | Sink current             | $V_{IOUT} = 0.05\text{ V}$ , $V_{HISENSE} = 12\text{ V}$ ,<br>$V_{IOUTLO} = 12\text{ V}$                                             | 50   |     |      | $\mu\text{A}$ |
| Output voltage swing   |                          | $V_{HISENSE} = 11\text{ V}$ , $R_{IOUT} = 10\text{ k}\Omega$                                                                         | 0    |     | 2    | V             |
|                        |                          | $V_{HISENSE} = 4.5\text{ V}$ , $R_{IOUT} = 10\text{ k}\Omega$                                                                        | 0    |     | 1.5  | V             |
|                        |                          | $V_{HISENSE} = 3\text{ V}$ , $R_{IOUT} = 10\text{ k}\Omega$                                                                          | 0    |     | 0.75 | V             |
| LOSENSE                | High-level input voltage | $V_{HISENSE} = 4.5\text{ V}$ (see Note 3)                                                                                            | 2.85 |     |      | V             |
|                        | Low-level input voltage  |                                                                                                                                      | 2.4  |     |      | V             |
| Sample/hold resistance |                          | $11.4\text{ V} \leq V_{HISENSE} \leq 12.6\text{ V}$ ,<br>LOSENSE connected to HISENSE,<br>$V_{HISENSE} - V_{IOUTLO} = 0.15\text{ V}$ | 50   | 60  | 80   | $\Omega$      |
|                        |                          | $4.5\text{ V} \leq V_{HISENSE} \leq 5.5\text{ V}$ ,<br>LOSENSE connected to HISENSE,<br>$V_{HISENSE} - V_{IOUTLO} = 0.15\text{ V}$   | 62   | 85  | 123  |               |
|                        |                          | $3\text{ V} \leq V_{HISENSE} \leq 3.6\text{ V}$ ,<br>LOSENSE connected to HISENSE,<br>$V_{HISENSE} - V_{IOUTLO} = 0.15\text{ V}$     | 67   | 95  | 144  |               |
| CMRR                   |                          | $V_{HISENSE} = 12.6\text{ V}$ to $3\text{ V}$ ,<br>$V_{HISENSE} - V_{IOUTLO} = 100\text{ mV}$                                        | 69   | 75  |      | dB            |

NOTE 3. This parameter is ensured by design and is not production tested.

### inhibit

| PARAMETER       | TEST CONDITIONS | MIN  | TYP | MAX  | UNIT |
|-----------------|-----------------|------|-----|------|------|
| Start threshold |                 | 1.9  | 2.1 | 2.35 | V    |
| Hysteresis      |                 | 0.08 | 0.1 | 0.12 | V    |
| Stop threshold  |                 | 1.85 |     |      | V    |

### overvoltage protection

| PARAMETER                  | TEST CONDITIONS | MIN | TYP | MAX | UNIT        |
|----------------------------|-----------------|-----|-----|-----|-------------|
| Overvoltage trip threshold |                 | 112 | 115 | 120 | $\%V_{REF}$ |
| Hysteresis                 | See Note 3      |     | 10  |     | mV          |

NOTE 3: This parameter is ensured by design and is not production tested.

### overcurrent protection

| PARAMETER          | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------|-----------------|-----|-----|-----|------|
| OCP trip threshold |                 | 90  | 100 | 110 | mV   |
| Input bias current |                 |     |     | 100 | nA   |



# TPS5210

## PROGRAMMABLE SYNCHRONOUS BUCK REGULATOR CONTROLLER

SLVS171A – SEPTEMBER 1998 – REVISED MAY 1999

electrical characteristics over recommended operating virtual junction temperature range,  
 $V_{CC} = 12\text{ V}$ ,  $I_{DRV} = 0\text{ A}$  (unless otherwise noted) (continued)

### deadtime

| PARAMETER |                          | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|--------------------------|-----------------|-----|-----|-----|------|
| LOHIB     | High-level input voltage |                 | 2.4 |     |     | V    |
|           | Low-level input voltage  |                 |     |     | 1.4 |      |
| LOWDR     | High-level input voltage | See Note 3      | 3   |     |     | V    |
|           | Low-level input voltage  | See Note 3      |     |     | 1.7 |      |

NOTE 3: This parameter is ensured by design and is not production tested.

### LODRV

| PARAMETER |                          | TEST CONDITIONS | MIN  | TYP | MAX  | UNIT |
|-----------|--------------------------|-----------------|------|-----|------|------|
| LODRV     | High-level input voltage |                 | 1.85 |     |      | V    |
|           | Low-level input voltage  |                 |      |     | 0.95 |      |

### droop compensation

| PARAMETER        |  | TEST CONDITIONS            | MIN | TYP | MAX | UNIT |
|------------------|--|----------------------------|-----|-----|-----|------|
| Initial accuracy |  | $V_{DROOP} = 50\text{ mV}$ | 46  |     | 54  | mV   |

### drive regulator

| PARAMETER             | TEST CONDITIONS                                                           | MIN | TYP | MAX | UNIT |
|-----------------------|---------------------------------------------------------------------------|-----|-----|-----|------|
| Output voltage        | $11.4\text{ V} \leq V_{CC} \leq 12.6\text{ V}$ , $I_{DRV} = 50\text{ mA}$ | 7   |     | 9   | V    |
| Output regulation     | $1\text{ mA} \leq I_{DRV} \leq 50\text{ mA}$                              |     | 100 |     | mV   |
| Short-circuit current |                                                                           | 100 |     |     | mA   |

### bias regulator

| PARAMETER      | TEST CONDITIONS                                             | MIN | TYP | MAX | UNIT |
|----------------|-------------------------------------------------------------|-----|-----|-----|------|
| Output voltage | $11.4\text{ V} \leq V_{CC} \leq 12.6\text{ V}$ , See Note 4 | 6   |     |     | V    |

NOTE 4: The bias regulator is designed to provide a quiet bias supply for the TPS5210 controller. External loads should not be driven by the bias regulator.

### input undervoltage lockout

| PARAMETER       | TEST CONDITIONS | MIN  | TYP | MAX   | UNIT |
|-----------------|-----------------|------|-----|-------|------|
| Start threshold |                 | 9.25 | 10  | 10.75 | V    |
| Hysteresis      |                 | 1.9  | 2   | 2.2   | V    |
| Stop threshold  |                 | 7.5  |     |       | V    |



# TPS5210

## PROGRAMMABLE SYNCHRONOUS BUCK REGULATOR CONTROLLER

SLVS171A – SEPTEMBER 1998 – REVISED MAY 1999

electrical characteristics over recommended operating virtual junction temperature range,  
 $V_{CC} = 12\text{ V}$ ,  $I_{DRV} = 0\text{ A}$  (unless otherwise noted) (continued)

### output drivers

| PARAMETER                           |                  | TEST CONDITIONS                                                                                                              | MIN | TYP | MAX | UNIT     |
|-------------------------------------|------------------|------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|----------|
| Peak output current<br>(see Note 5) | High-side sink   | Duty cycle < 2%, $t_{pw} < 100\text{ }\mu\text{s}$ ,<br>$T_J = 125^\circ\text{C}$ , $V_{BOOT} - V_{BOOTLO} = 6.5\text{ V}$ , | 2   |     |     | A        |
|                                     | High-side source | $V_{HIGHDR} = 1.5\text{ V}$ (source) or $6\text{ V}$ (sink),<br>See Note 3                                                   | 2   |     |     |          |
|                                     | Low-side sink    | Duty Cycle < 2%, $t_{pw} < 100\text{ }\mu\text{s}$ ,<br>$T_J = 125^\circ\text{C}$ , $V_{DRV} = 6.5\text{ V}$ ,               | 2   |     |     |          |
|                                     | Low-side source  | $V_{LOWDR} = 1.5\text{ V}$ (source) or $5\text{ V}$ (sink),<br>See Note 3                                                    | 2   |     |     |          |
| Output resistance<br>(see Note 5)   | High-side sink   | $T_J = 125^\circ\text{C}$ , $V_{BOOT} - V_{BOOTLO} = 6.5\text{ V}$ ,                                                         |     |     | 3   | $\Omega$ |
|                                     | High-side source | $V_{HIGHDR} = 6\text{ V}$ (source) or $0.5\text{ V}$ (sink)                                                                  |     |     | 45  |          |
|                                     | Low-side sink    | $T_J = 125^\circ\text{C}$ , $V_{DRV} = 6.5\text{ V}$ ,                                                                       |     |     | 5.7 |          |
|                                     | Low-side source  | $V_{LOWDR} = 6\text{ V}$ (source) or $0.5\text{ V}$ (sink)                                                                   |     |     | 45  |          |

NOTES: 3. This parameter is ensured by design and is not production tested.

5. The pull-up/pull-down circuits of the drivers are bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors. The output resistance is the  $R_{ds(on)}$  of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor.

### supply current

| PARAMETER |                                    | TEST CONDITIONS                                                                                                                                                                                                                                | MIN  | TYP | MAX | UNIT          |
|-----------|------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|-----|-----|---------------|
| $V_{CC}$  | Supply voltage range               |                                                                                                                                                                                                                                                | 11.4 | 12  | 13  | V             |
| $V_{CC}$  | Quiescent current                  | $V_{INHIBIT} = 5\text{ V}$ ,<br>$V_{CC} > 10.75\text{ V}$ at startup,<br>VID code $\neq 11111$ ,<br>$V_{BOOTLO} = 0\text{ V}$                                                                                                                  |      | 3   | 10  | mA            |
|           |                                    | $V_{INHIBIT} = 5\text{ V}$ ,<br>$V_{CC} > 10.75\text{ V}$ at startup,<br>$C_{HIGHDR} = 50\text{ pF}$ ,<br>$f_{SWX} = 200\text{ kHz}$ ,<br>VID code $\neq 11111$ ,<br>$V_{BOOTLO} = 0\text{ V}$ ,<br>$C_{LOWDR} = 50\text{ pF}$ ,<br>See Note 3 |      | 5   |     |               |
|           | High-side driver quiescent current | $V_{INHIBIT} = 0\text{ V}$ or VID code = 11111 or $V_{CC} < 9.25\text{ V}$ at startup,<br>$V_{BOOT} = 13\text{ V}$ , $V_{BOOTLO} = 0\text{ V}$                                                                                                 |      |     | 80  | $\mu\text{A}$ |
|           |                                    | $V_{INHIBIT} = 5\text{ V}$ ,<br>$V_{BOOT} = 13\text{ V}$ ,<br>$C_{HIGHDR} = 50\text{ pF}$ ,<br>VID code $\neq 11111$ , $V_{CC} > 10.75\text{ V}$ at startup,<br>$V_{BOOTLO} = 0\text{ V}$ ,<br>$f_{SWX} = 200\text{ kHz}$ (see Note 3)         |      | 2   |     | mA            |

NOTE 3: This parameter is ensured by design and is not production tested.

# TPS5210

## PROGRAMMABLE SYNCHRONOUS BUCK REGULATOR CONTROLLER

SLVS171A – SEPTEMBER 1998 – REVISED MAY 1999

**switching characteristics over recommended operating virtual-junction temperature range,  $V_{CC} = 12\text{ V}$ ,  $I_{DRV} = 0\text{ A}$  (unless otherwise noted)**

| PARAMETER                                             |                                                 | TEST CONDITIONS                                                                                             | MIN | TYP | MAX | UNIT          |
|-------------------------------------------------------|-------------------------------------------------|-------------------------------------------------------------------------------------------------------------|-----|-----|-----|---------------|
| Propagation delay                                     | VSENSE to HIGHDR or LOWDR (excluding dead-time) | $1.3\text{ V} \leq V_{VREF} \leq 3.5\text{ V}$ , 10 mV overdrive (see Note 3)                               |     | 150 | 250 | ns            |
|                                                       | OCP comparator                                  | See Note 3                                                                                                  |     | 1   |     | $\mu\text{s}$ |
|                                                       | OVP comparator                                  |                                                                                                             |     | 1   |     |               |
|                                                       | PWRGD comparator                                |                                                                                                             |     | 1   |     |               |
|                                                       | SLOWST comparator                               | Overdrive = 10 mV (see Note 3)                                                                              |     | 560 | 900 | ns            |
| Rise time                                             | HIGHDR output                                   | $C_L = 9\text{ nF}$ , $V_{BOOT} = 6.5\text{ V}$ , $V_{BOOTLO} = 0\text{ V}$ , $T_J = 125^\circ\text{C}$     |     |     | 60  | ns            |
|                                                       | LOWDR output                                    | $C_L = 9\text{ nF}$ , $T_J = 125^\circ\text{C}$ , $V_{DRV} = 6.5\text{ V}$                                  |     |     | 60  |               |
| Fall time                                             | HIGHDR output                                   | $C_L = 9\text{ nF}$ , $V_{BOOT} = 6.5\text{ V}$ , $V_{BOOTLO} = 0\text{ V}$ , $T_J = 125^\circ\text{C}$     |     |     | 60  | ns            |
|                                                       | LOWDR output                                    | $C_L = 9\text{ nF}$ , $T_J = 125^\circ\text{C}$ , $V_{DRV} = 6.5\text{ V}$                                  |     |     | 60  |               |
| Deglitch time (Includes comparator propagation delay) | OCP                                             | See Note 3                                                                                                  | 2   |     | 5   | $\mu\text{s}$ |
|                                                       | OVP                                             |                                                                                                             | 2   |     | 5   |               |
| Response time                                         | High-side VDS sensing                           | $V_{HISENSE} = 12\text{ V}$ , $V_{IOUTLO}$ pulsed from 12 V to 11.9 V, 100 ns rise/fall times (see Note 3)  |     |     | 2   | $\mu\text{s}$ |
|                                                       |                                                 | $V_{HISENSE} = 4.5\text{ V}$ , $V_{IOUTLO}$ pulsed from 4.5 V to 4.4 V, 100 ns rise/fall times (see Note 3) |     |     | 3   |               |
|                                                       |                                                 | $V_{HISENSE} = 3\text{ V}$ , $V_{IOUTLO}$ pulsed from 3 V to 2.9 V, 100 ns rise/fall times (see Note 3)     |     |     | 3   |               |
| Short-circuit protection rising-edge delay            | SCP                                             | $LOSENSE = 0\text{ V}$ (see Note 3)                                                                         | 300 |     | 500 | ns            |
| Turn-on/turn-off delay                                | VDS sensing sample/hold switch                  | $3\text{ V} \leq V_{HISENSE} \leq 11\text{ V}$ , $V_{LOSENSE} = V_{HISENSE}$ (see Note 3)                   | 30  |     | 100 | ns            |
| Crossover delay time                                  | LOWDR to HIGHDRV, and LOHIB to LOWDR            | See Note 3                                                                                                  | 30  |     | 100 | ns            |
| Prefilter pole frequency                              | Hysteretic comparator                           | See Note 3                                                                                                  |     | 5   |     | MHz           |
| Propagation delay                                     | LODRV                                           | See Note 3                                                                                                  |     |     | 400 | ns            |

NOTE 3: This parameter is ensured by design and is not production tested.



# TPS5210

## PROGRAMMABLE SYNCHRONOUS BUCK REGULATOR CONTROLLER

SLVS171A – SEPTEMBER 1998 – REVISED MAY 1999

### TYPICAL CHARACTERISTICS

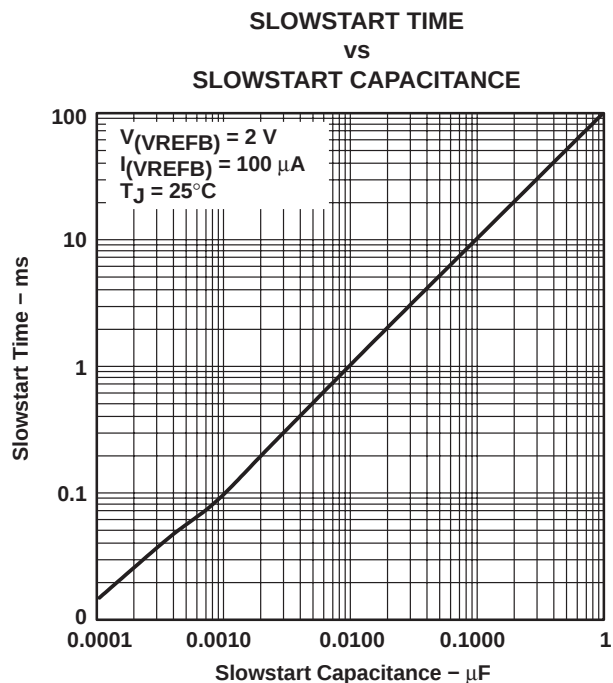


Figure 1

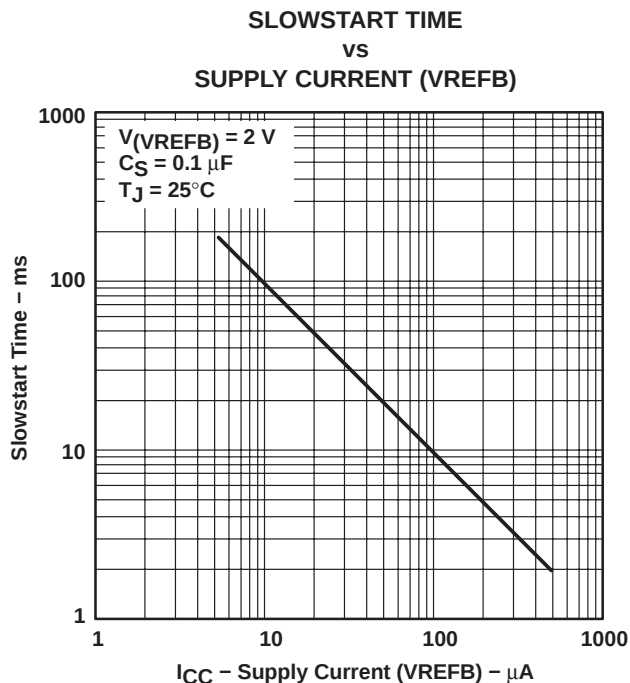


Figure 2

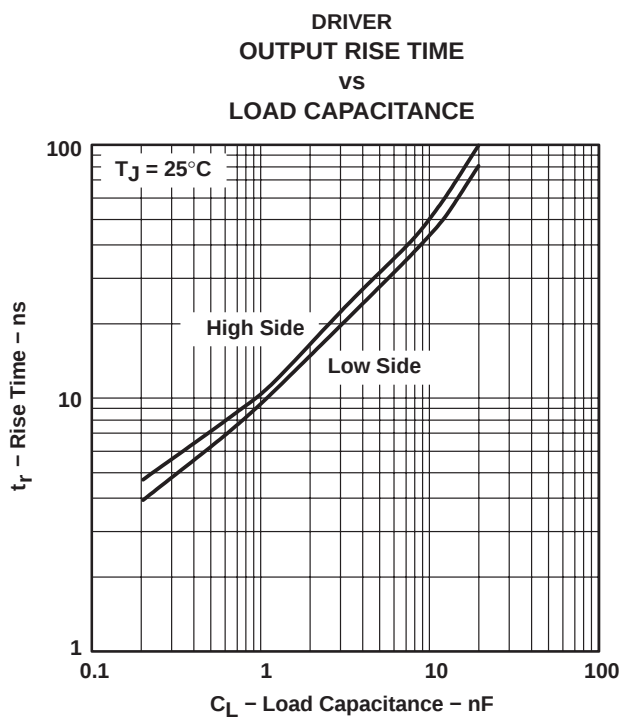


Figure 3

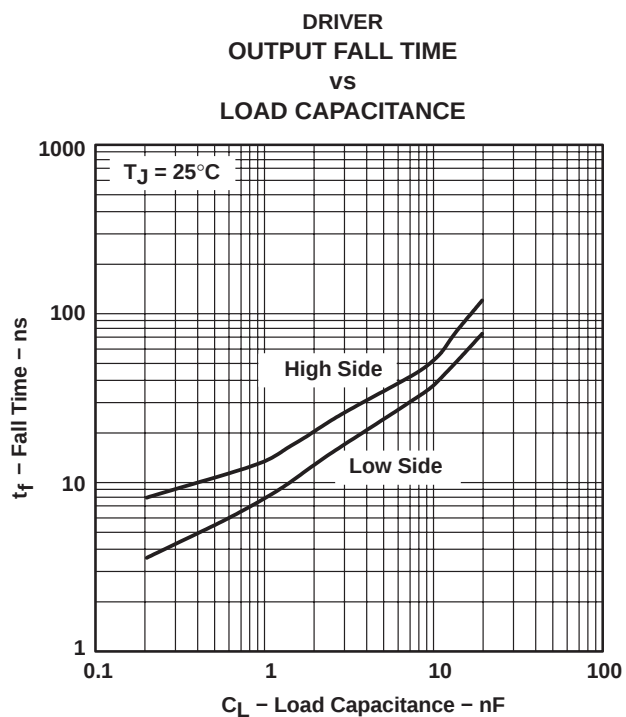
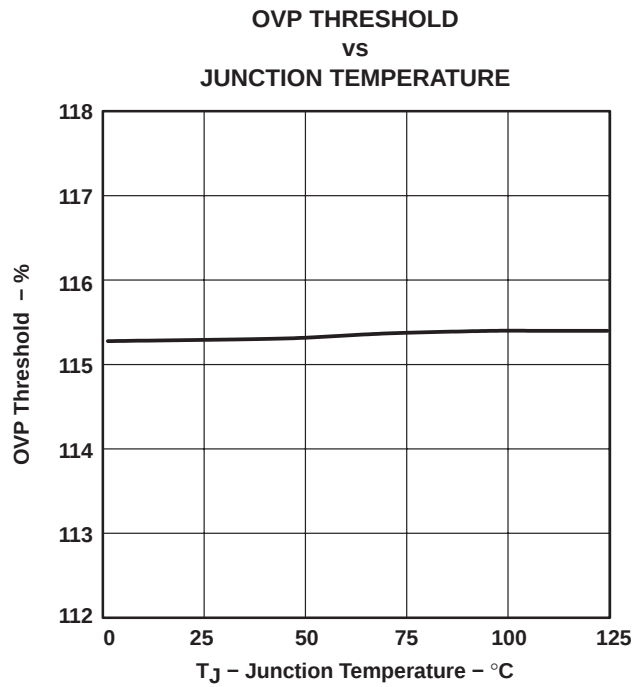
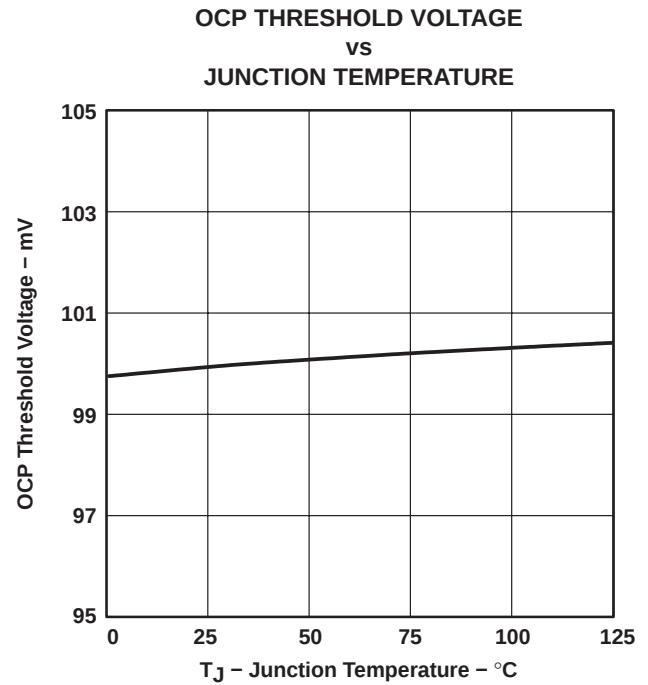


Figure 4

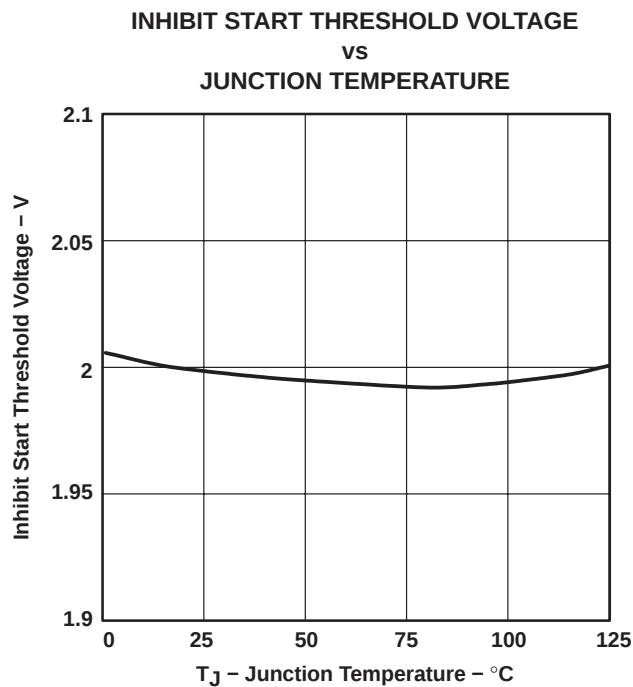
## TYPICAL CHARACTERISTICS



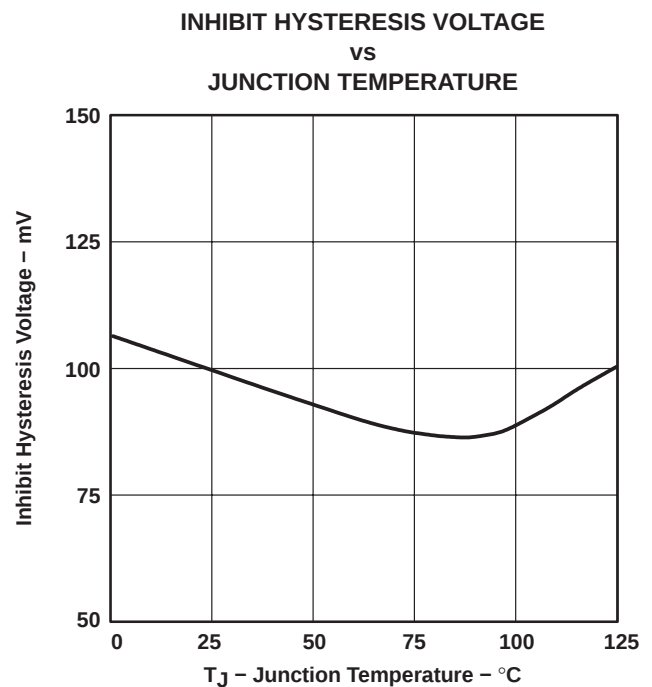
**Figure 5**



**Figure 6**



**Figure 7**



**Figure 8**

# TPS5210

## PROGRAMMABLE SYNCHRONOUS BUCK REGULATOR CONTROLLER

SLVS171A – SEPTEMBER 1998 – REVISED MAY 1999

### TYPICAL CHARACTERISTICS

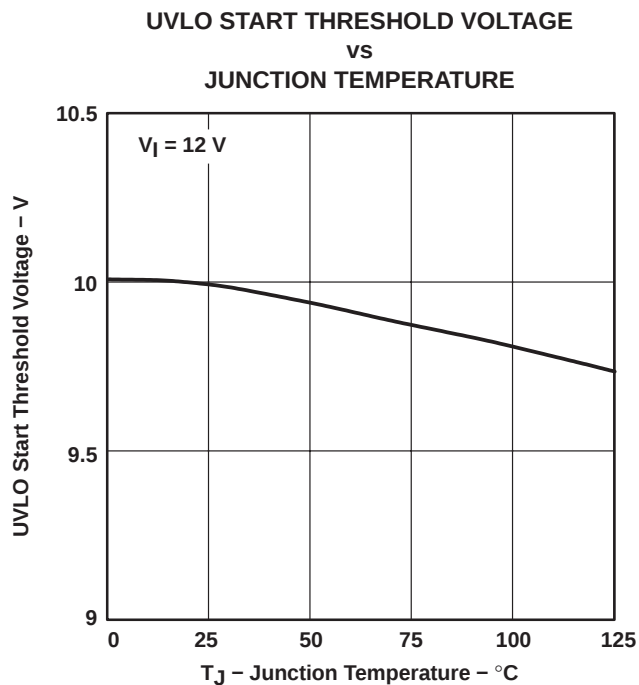


Figure 9

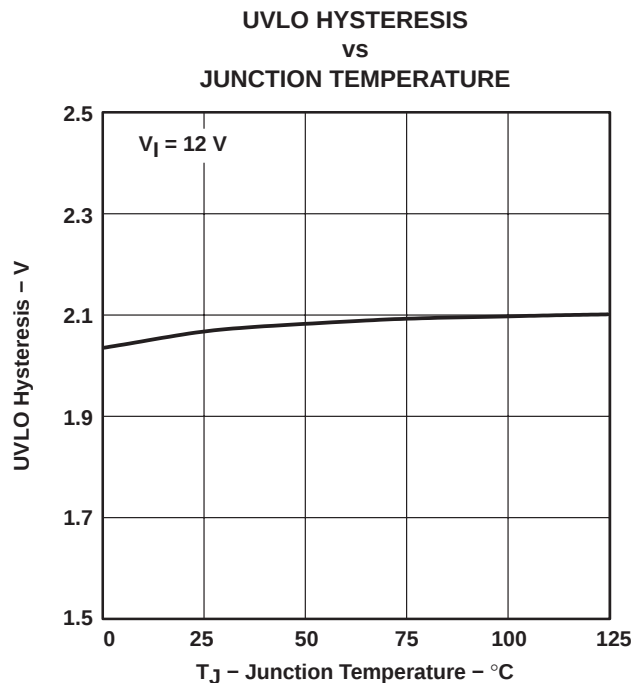


Figure 10

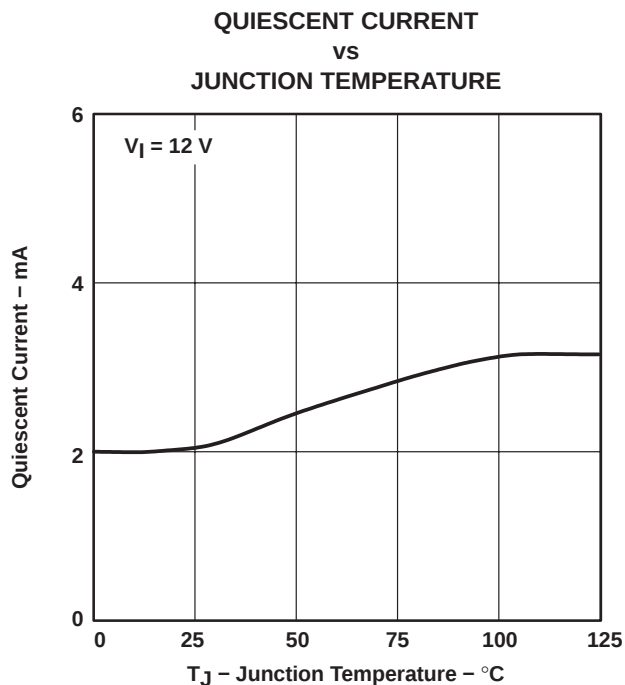


Figure 11

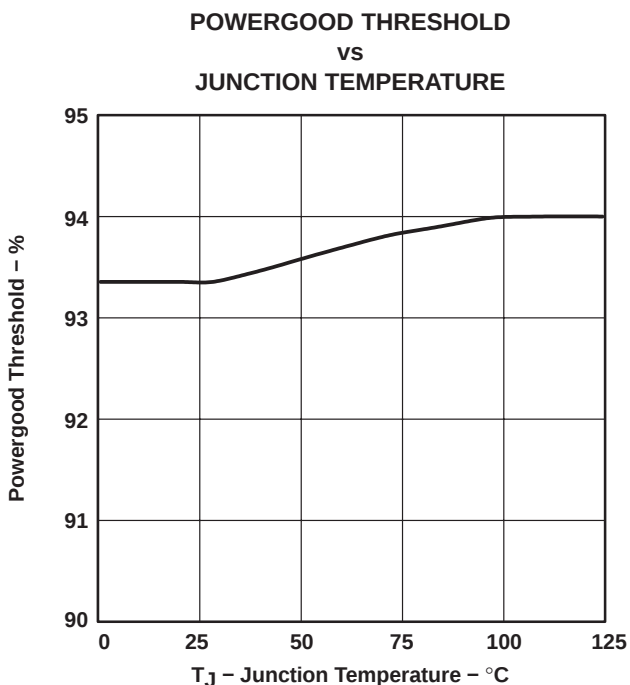


Figure 12

## TYPICAL CHARACTERISTICS

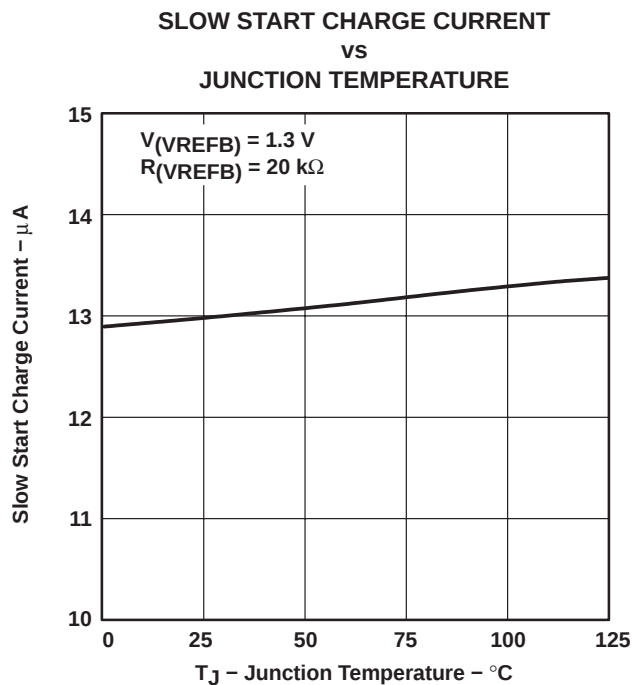


Figure 13

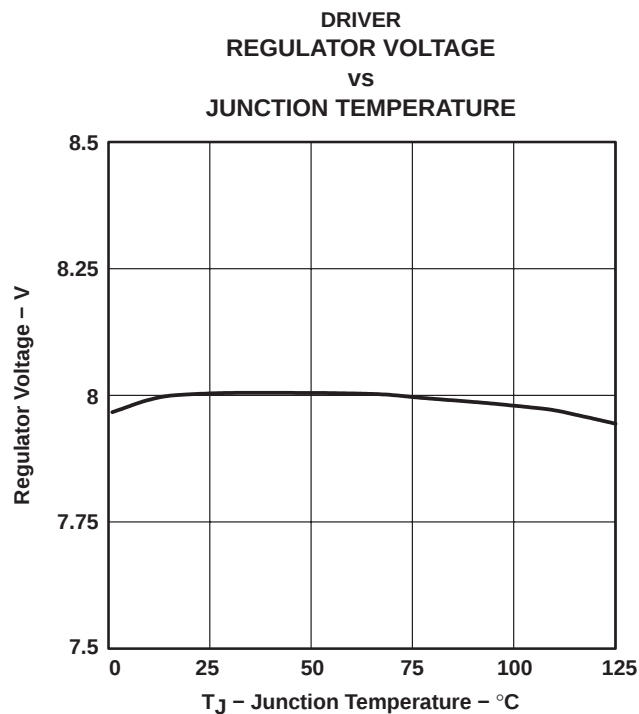


Figure 14

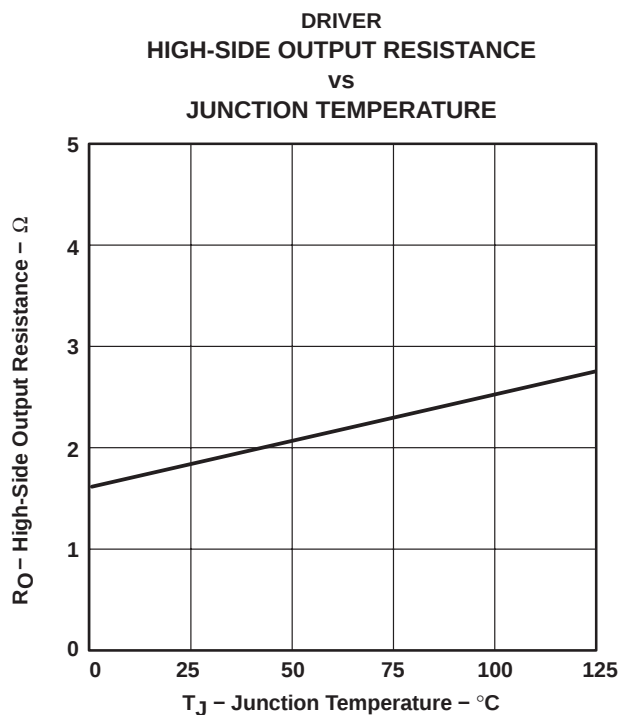


Figure 15

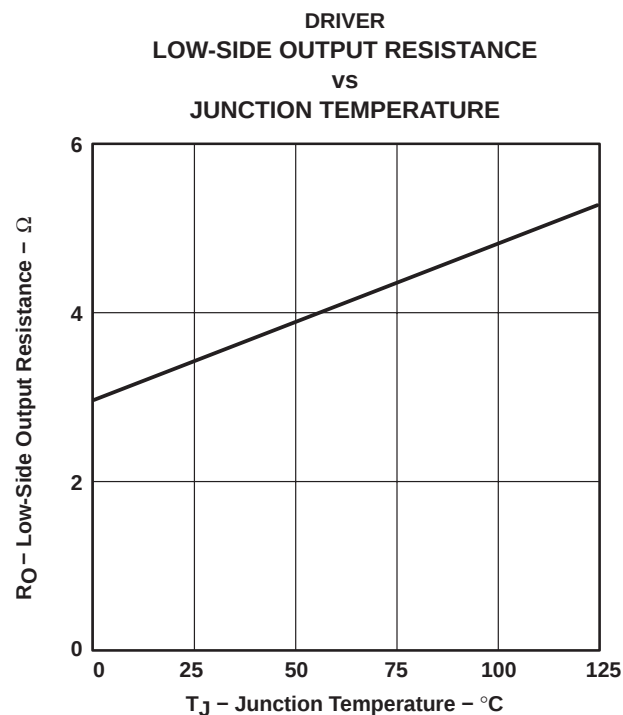


Figure 16

# TPS5210

## PROGRAMMABLE SYNCHRONOUS BUCK REGULATOR CONTROLLER

SLVS171A – SEPTEMBER 1998 – REVISED MAY 1999

### TYPICAL CHARACTERISTICS

SENSING SAMPLE/HOLD RESISTANCE  
vs  
JUNCTION TEMPERATURE

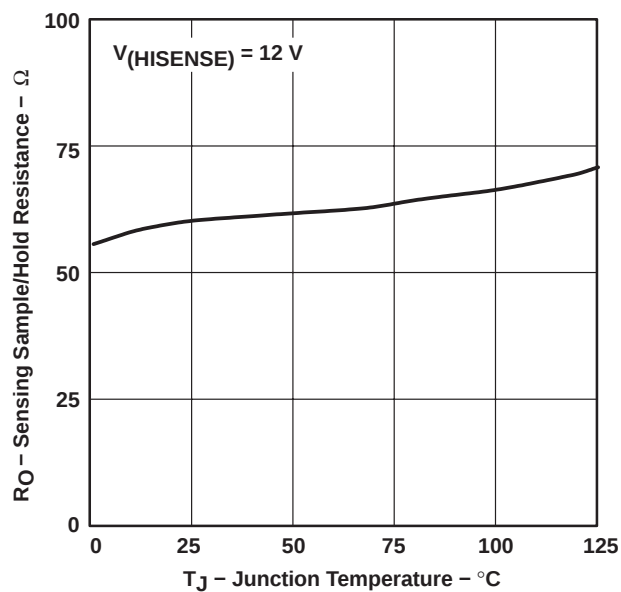


Figure 17

# TPS5210

## PROGRAMMABLE SYNCHRONOUS BUCK REGULATOR CONTROLLER

SLVS171A – SEPTEMBER 1998 – REVISED MAY 1999

### APPLICATION INFORMATION

The following figure is a typical application schematic. The circuit can be divided into the power-stage section and the control-circuit section. The power stage must be tailored to the input/output requirements of the application. The control circuit is basically the same for all applications with some minor tweaking of specific values. Table 2 shows the values of the power stage components for various output-current options.

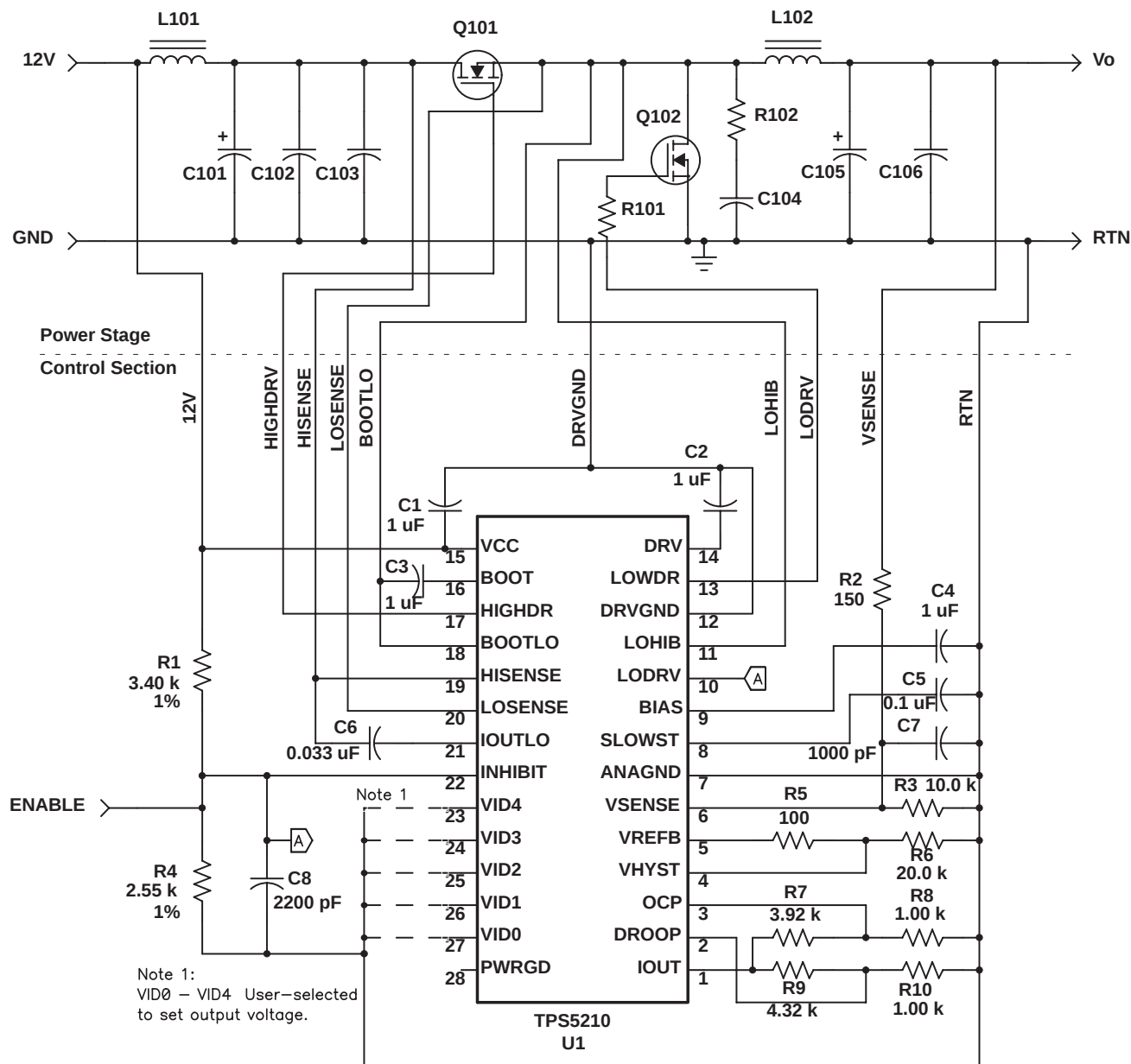


Figure 18. Standard Application Schematic

# TPS5210

## PROGRAMMABLE SYNCHRONOUS BUCK REGULATOR CONTROLLER

SLVS171A – SEPTEMBER 1998 – REVISED MAY 1999

### APPLICATION INFORMATION

**Table 2. Power Stage Components**

| Ref Des                        | Function                        | 12-V-Input Power Stage Components                            |                                                              |                                                              |                                                                  |                                                                  |
|--------------------------------|---------------------------------|--------------------------------------------------------------|--------------------------------------------------------------|--------------------------------------------------------------|------------------------------------------------------------------|------------------------------------------------------------------|
|                                |                                 | 4-A Out                                                      | 8-A Out                                                      | 12-A Out                                                     | 20-A Out                                                         | 40-A Out                                                         |
| C101                           | Input Bulk Capacitor            | Sanyo, 16SV100M, 100- $\mu$ F, 16-V, 20%                     | Sanyo, 16SA470M, 2 x 470- $\mu$ F, 16-V, 20%                 | Sanyo, 16SA470M, 2 x 470- $\mu$ F, 16-V, 20%                 | Sanyo, 16SA470M, 3 x 470- $\mu$ F, 16-V, 20%                     | Sanyo, 16SA470M, 4 x 470- $\mu$ F, 16-V, 20%                     |
| C102                           | Input Mid-Freq Capacitor        | muRata, GRM42-6Y5V105Z025A 1.0- $\mu$ F, 25-V, +80%-20%, Y5V | muRata, GRM42-6Y5V225Z016A 2.2- $\mu$ F, 16-V, +80%-20%, Y5V | muRata, GRM42-6Y5V225Z016A 2.2- $\mu$ F, 16-V, +80%-20%, Y5V | muRata, GRM42-6Y5V105Z025A 3 x 1.0- $\mu$ F, 25-V, +80%-20%, Y5V | muRata, GRM42-6Y5V105Z025A 4 x 1.0- $\mu$ F, 25-V, +80%-20%, Y5V |
| C103                           | Input Hi-Freq Bypass Capacitor  | muRata, GRM39X7R104K016A 0.1- $\mu$ F, 16-V, X7R             | muRata, GRM39X7R104K016A, 0.1- $\mu$ F, 16-V, X7R            | muRata, GRM39X7R104K016A, 2 x 0.1- $\mu$ F, 16-V, X7R        | muRata, GRM39X7R104K016A, 3 x 0.1- $\mu$ F, 16-V, X7R            | muRata, GRM39X7R104K016A, 4 x 0.1- $\mu$ F, 16-V, X7R            |
| C104                           | Snubber Capacitor               | muRata, GRM39X7R102K050A, 1000-pF, 50-V, X7R                 | muRata, GRM39X7R102K050A, 1000-pF, 50-V, X7R                 | muRata, GRM39X7R102K050A, 2 x 1000-pF, 50-V, X7R             | muRata, GRM39X7R102K050A, 3 x 1000-pF, 50-V, X7R                 | muRata, GRM39X7R102K050A, 4 x 1000-pF, 50-V, X7R                 |
| C105                           | Output Bulk Capacitor           | Sanyo, 6TPB150M, 3 x 150- $\mu$ F, 6.3-V, 20%                | Sanyo, 4SP820M, 820- $\mu$ F, 4-V, 20%                       | Sanyo, 4SP820M, 2 x 820- $\mu$ F, 4-V, 20%                   | Sanyo, 4SP820M, 3 x 820- $\mu$ F, 4-V, 20%                       | Sanyo, 4SP820M, 4 x 820- $\mu$ F, 4-V, 20%                       |
| C106                           | Output Hi-Freq Bypass Capacitor | muRata, GRM39X7R104K016A, 0.1- $\mu$ F, 16-V, X7R            | muRata, GRM39X7R104K016A, 0.1- $\mu$ F, 16-V, X7R            | muRata, GRM39X7R104K016A, 2 x 0.1- $\mu$ F, 16-V, X7R        | muRata, GRM39X7R104K016A, 3 x 0.1- $\mu$ F, 16-V, X7R            | muRata, GRM39X7R104K016A, 4 x 0.1- $\mu$ F, 16-V, X7R            |
| L101                           | Input Filter Inductor           | CoilCraft, DO1608C-332, 3.3- $\mu$ H, 2.0-A                  | Coiltronics, UP2B-2R2, 2.2- $\mu$ H, 7.2-A                   | Coiltronics, UP2B-2R2, 2.2- $\mu$ H, 7.2-A                   | Coiltronics, UP3B-1R0, 1- $\mu$ H, 12.5-A                        | Coiltronics, UP3B-1R0, 1- $\mu$ H, 12.5-A                        |
| L102                           | Output Filter Inductor          | CoilCraft, DO3316P-332, 3.3- $\mu$ H, 6.1-A                  | Coiltronics, UP3B-2R2, 2.2- $\mu$ H, 9.2-A                   | Coiltronics, UP4B-1R5, 1.5- $\mu$ H, 13.4-A                  | MicroMetals, T68-8/90 Core w/TT #16, 1.0- $\mu$ H, 25-A          | Pulse Engineering, P1605, 1.0- $\mu$ H, 50-A                     |
| R101                           | Lo-Side Gate Resistor           | 3.3- $\Omega$ , 1/16-W, 5%                                   | 3.3- $\Omega$ , 1/16-W, 5%                                   | 2 x 3.3- $\Omega$ , 1/16-W, 5%                               | 3 x 3.3- $\Omega$ , 1/16-W, 5%                                   | 4 x 3.3- $\Omega$ , 1/16-W, 5%                                   |
| R102                           | Snubber Resistor                | 2.7- $\Omega$ , 1/10-W, 5%                                   | 2.7- $\Omega$ , 1/10-W, 5%                                   | 2 x 2.7- $\Omega$ , 1/10-W, 5%                               | 3 x 2.7- $\Omega$ , 1/10-W, 5%                                   | 4 x 2.7- $\Omega$ , 1/10-W, 5%                                   |
| Q101                           | Power Switch                    | Siliconix, Si4410, NMOS, 13-m $\Omega$                       | Siliconix, Si4410, NMOS, 13-m $\Omega$                       | Siliconix, 2 x Si4410, NMOS, 13-m $\Omega$                   | Siliconix, 2 x Si4410, NMOS, 13-m $\Omega$                       | IR, 2 x IRF7811, NMOS, 11-m $\Omega$                             |
| Q102                           | Synchron-ous Switch             | Siliconix, Si4410, NMOS, 13-m $\Omega$                       | Siliconix, Si4410, NMOS, 13-m $\Omega$                       | Siliconix, 2 x Si4410, NMOS, 13-m $\Omega$                   | Siliconix, 3 x Si4410, NMOS, 13-m $\Omega$                       | IR, 4 x IRF7811, NMOS, 11-m $\Omega$                             |
| Nominal Frequency <sup>†</sup> |                                 | 220 KHz                                                      | 330 KHz                                                      | 240 KHz                                                      | 140 KHz                                                          | 168 KHz                                                          |
| Hysteresis Window              |                                 | 20 mV                                                        | 20 mV                                                        | 20 mV                                                        | 20 mV                                                            | 10 mV                                                            |

<sup>†</sup> Nominal frequency measured with Vo set to 2 V.

The values listed above are recommendations based on actual test circuits. Many variations of the above are possible based upon the desires and/or requirements of the user. Performance of the circuit is equally, if not more, dependent upon the layout than on the specific components, as long as the device parameters are not exceeded. Fast-response, low-noise circuits require critical attention to the layout details. Even though the operating frequencies of typical power supplies are relatively low compared to today's microprocessor circuits, the power levels and edge rates can cause severe problems both in the supply and the load. The power stage, having the highest current levels and greatest dv/dt rates, should be given the greatest attention.



## APPLICATION INFORMATION

### frequency calculation

A detailed derivation of frequency calculation is shown in the application report, “*Designing Fast Response Synchronous Buck Regulators Using the TPS5210*”, TI Literature number SLVA044. When less accurate results are acceptable, the simplified equation shown below can be used:

$$f_s \cong \frac{(V_O \times [V_I - V_O] \times \text{ESR})}{(V_I \times L \times \text{Hysteresis Window})}$$

### Control Section

Below are the equations needed to select the various components within the control section. Details and the derivations of the equations used in this section are available in the application report “*Designing Fast Response Synchronous Buck Regulators Using the TPS5210*”, TI Literature number SLVA044.

### output voltage selection

Of course the most important function of the power supply is to regulate the output voltage to a specific value. Values between 1.3 V and 3.5 V can be easily set by shorting the correct VID inputs to ground. Values above the maximum reference voltage (3.5 V) can be set by setting the reference voltage to any convenient voltage within its range and selecting values for R2 and R3 to give the correct output. Select R3:

$R3 \ll \text{than } V_{\text{REF}}/I_{\text{BIAS}}(V_{\text{SENSE}})$ ; a recommended value is 10 k $\Omega$

Then, calculate R2 using:

$$V_O = V_{\text{REF}} \left( 1 + \frac{R2}{R3} \right) \quad \text{or} \quad R2 = \frac{R3 \times (V_O - V_{\text{REF}})}{V_{\text{REF}}}$$

R2 and R3 can also be used to make small adjusts to the output voltage within the reference-voltage range and/or to adjust for load-current active droop compensation. If there is no need to adjust the output voltage, R3 can be eliminated. R2, R3 (if used), and C7 are used as a noise filter; calculate using:

$$C7 = \frac{150 \text{ ns}}{(R2 \parallel R3)}$$

### slowstart timing

Slowstart reduces the startup stresses on the power-stage components and reduces the input current surge. Slowstart timing is a function of the reference-voltage current (determined by R6) and is independent of the reference voltage. The first step in setting slowstart timing will be to determine R6:

R6 should be between 7 k $\Omega$  and 300 k $\Omega$ , a recommended value is 20 k $\Omega$ .

Set the slowstart timing using the formula:

$$C5 = \frac{t_{\text{SS}}}{(5 \times R_{\text{VREFB}})} \cong \frac{t_{\text{SS}}}{(5 \times R6)}$$

Where C5 = Slowstart capacitance in  $\mu\text{F}$

$t_{\text{SS}}$  = Slowstart timing in  $\mu\text{s}$

$R_{\text{VREFB}}$  = Resistance from VREFB to GND in ohms ( $\approx R6$ )

# TPS5210

## PROGRAMMABLE SYNCHRONOUS BUCK REGULATOR CONTROLLER

SLVS171A – SEPTEMBER 1998 – REVISED MAY 1999

### APPLICATION INFORMATION

#### hysteresis voltage

A hysteretic controller regulates by self-oscillation, thus requiring a small ripple voltage on the output which the input comparator uses for sensing. Once selected, the TPS5210 hysteresis is proportional to the reference voltage; programming Vref to a new value automatically adjusts the hysteresis to be the same percentage of Vref. The actual output ripple voltage is the combination of the hysteresis voltage, overshoot caused by internal delays, and the output capacitor characteristics. Figure 20 shows the hysteresis window voltage ( $V_{HI}$  to  $V_{LO}$ ) and the output voltage ripple ( $V_{MAX}$  to  $V_{MIN}$ ). Since the output current from VREFB should be less than 500  $\mu$ A, the total divider resistance ( $R5 + R6$ ) should be greater than 7 K $\Omega$ . The hysteresis voltage should be no greater than 60 mV so R6 will dominate the divider.

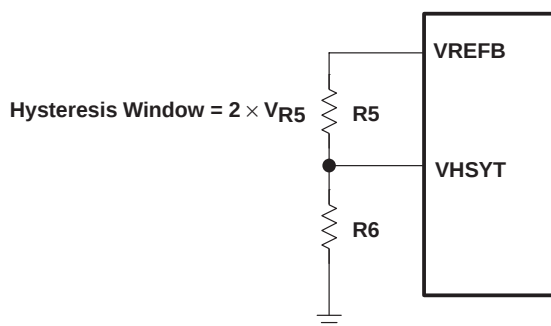


Figure 19. Hysteresis Divider Circuit

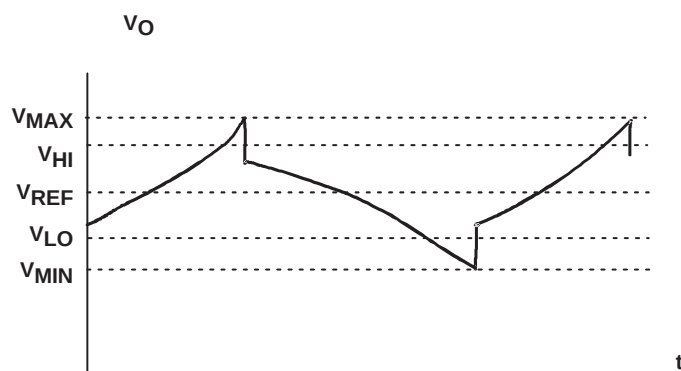


Figure 20. Output Ripple

The upper divider resistor, R5, is calculated using:

$$R5 = \frac{\text{Hysteresis Window}}{(2 \times V_{REFB} - \text{Hysteresis Window})} \times R6 \cong \frac{V_{HYST} (\%) }{(2 \times 100)} \times R6$$

Where Hysteresis Window = the desired peak-to-peak hysteresis voltage.

VREFB = selected reference voltage.

$$V_{HYST} (\%) = [(\text{Hysteresis Window}) / V_{REFB}] \times 100 < V_{O(\text{Ripple}) (P-P)} (\%)$$

## APPLICATION INFORMATION

### current limit

Current limit can be implemented using the on-resistance of the upper FETs as the sensing elements. Select R8:

$$R8 \ll \frac{V_{OCP}}{I_{Bias(OCF)}} \leq \frac{0.1V}{(100 \times 100 nA)} \leq 10 k\Omega \quad (\text{A recommended value is } 1 k\Omega)$$

The IOUT signal is used to drive the current limit and droop-circuit dividers. The voltage at IOUT at the output current trip point will be:

$$V_{IOUT(Trip)} = \frac{(2 \times R_{DS(ON)} \times TF)}{NumFETS} \times I_{O(Trip)}$$

Where NumFETS = Number of upper FETS in Parallel.

TF =  $R_{DS(ON)}$  temperature correction factor.

$I_{O(Trip)}$  = Desired output current trip level (A).

Calculate R7 using:

$$R7 = \left( \frac{V_{IOUT(Trip)}}{0.1 V} - 1 \right) \times R8$$

Note that since  $R_{DS(ON)}$  of MOSFETs can vary from lot to lot and with temperature, tight current-limit control (less than  $1.5 \times I_O$ ) using this method is not practical. If tight control is required, an external current-sense resistor in series with the drain of the upper FET can be used with HISENSE and LOSENSE connected across the resistor.

### droop compensation

Droop compensation is used to reduce the output voltage range during load transients by increasing the output voltage setpoint toward the upper tolerance limit during light loads and decreasing the voltage setpoint toward the lower tolerance limit during heavy loads. This allows the output voltage to swing a greater amount and still remain within the tolerance window. The maximum droop voltage is set with R9 and R10. Select R10:

$$R10 \ll \frac{V_{DROOP(Min)}}{I_{Bias(DROOP,Max)}} \leq \frac{0.01V}{(100 \times 100 nA)} \leq 1 k\Omega \quad (\text{Again, a value of } 1 k\Omega \text{ is recommended})$$

The voltage at IOUT during normal operation (0 to 100% load) will vary from 0 V up to:

$$V_{IOUT(Max)} = \frac{(2 \times R_{DS(ON)} \times TF)}{NumFETS} \times I_{O(Max)}$$

Where  $I_{O(Max)}$  = Maximum output load current (A).

# TPS5210

## PROGRAMMABLE SYNCHRONOUS BUCK REGULATOR CONTROLLER

SLVS171A – SEPTEMBER 1998 – REVISED MAY 1999

### APPLICATION INFORMATION

#### droop compensation (continued)

Then, calculate R9:

$$R9 = \left( \frac{V_{IOUT(Max)}}{V_{DROOP}} - 1 \right) \times R10$$

Where  $V_{DROOP}$  = Desired droop voltage

At full load, the output voltage will be:

$$V_O = V_{REF} \times \left( 1 + \frac{R2}{R3} \right) - V_{DROOP}$$

#### using the TPS5210 when both 12 V and 5 V are available

When both 12 V and 5 V are available, several components can be removed from the basic schematic shown above. R1, R4, and C9 are no longer required if 5 V is brought in directly to INHIBIT and LODRV. However, if undervoltage lockout for the 5-V input is desired, R1 and R4 can be used to set the startup setpoint. The INHIBIT pin trip level is 2.1 V. Select R4:

$$R4 \ll \frac{V_{INH}}{I_{INH(Max)}} \leq \frac{2.1V}{(100 \times 100 nA)} \leq 210 k\Omega$$

Then, set the 5-V UVLO trip level with R1:

$$R1 = \frac{(5V_{Trip} - 2V)}{2V} \times R4$$

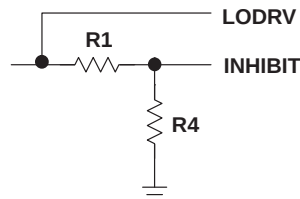


Figure 21. 5-V Input with UVLO

#### using the TPS5210 when only 5 V is available

The TPS5210 controller requires 12 V for internal control of the device. If an external source for 12 V is not available, a small on-board source must be included in the design. Total 12-V current is very small, typically about 20 mA, so even a small charge pump can be used to generate the supply voltage. The power stage is not voltage dependent, but component values must be selected for 5-V inputs and the frequency of operation is dependent upon the power stage input voltage.

# TPS5210 PROGRAMMABLE SYNCHRONOUS BUCK REGULATOR CONTROLLER

SLVS171A – SEPTEMBER 1998 – REVISED MAY 1999

## APPLICATION INFORMATION

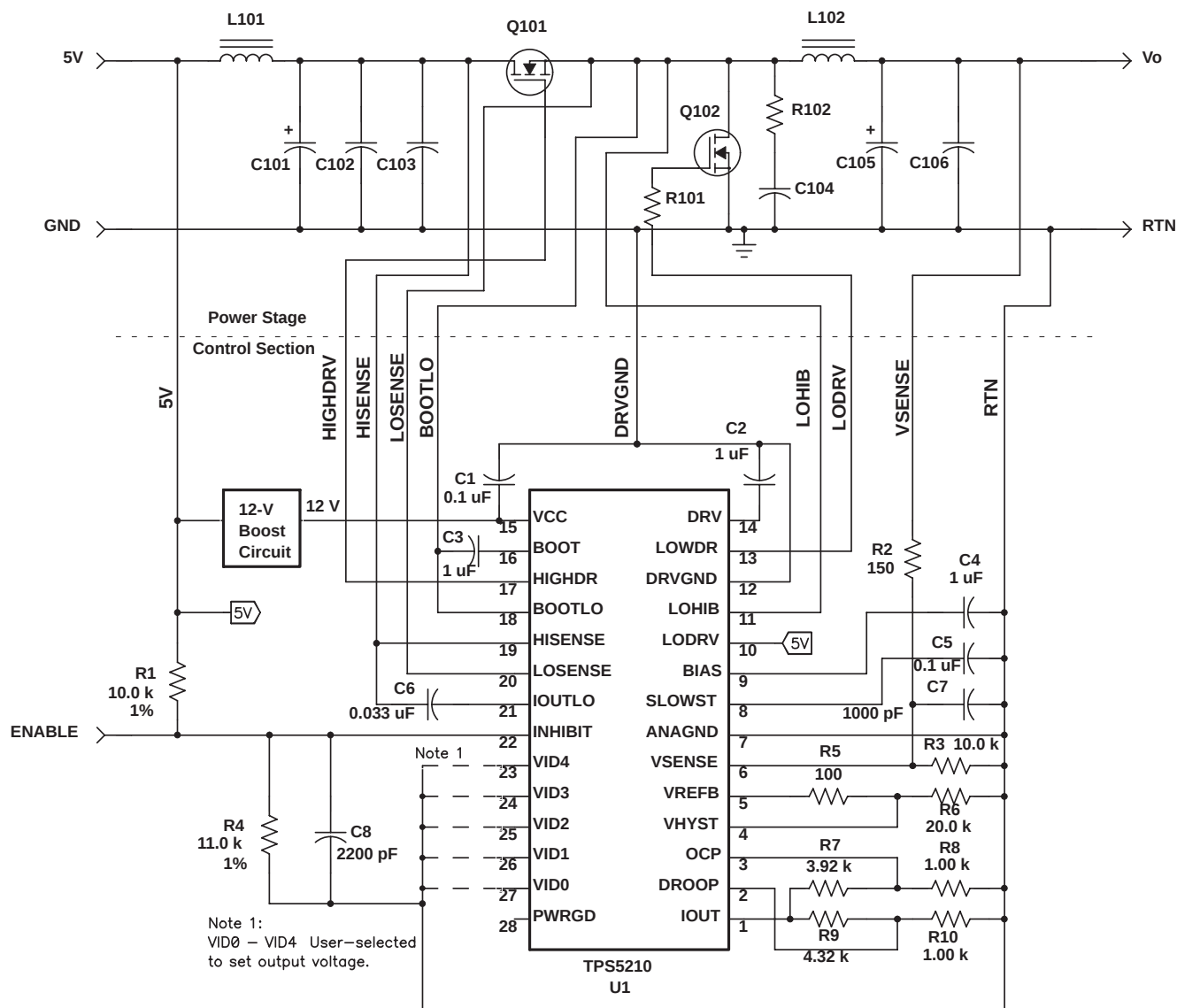


Figure 22. Typical 5-V-Only Application Circuit

## application examples

Various application and layout examples using the TPS5210 are available from Texas Instruments. This information can be downloaded from <http://www.ti.com/sc/docs/products/msp/pwrsply/default.htm> or received from your TI representative.

# TPS5210

## PROGRAMMABLE SYNCHRONOUS BUCK REGULATOR CONTROLLER

SLVS171A – SEPTEMBER 1998 – REVISED MAY 1999

---

### APPLICATION INFORMATION

#### layout guidelines

Good power supply results will only occur when care is given to proper design and layout. Layout will affect noise pickup and generation and can cause a good design to perform with less than expected results. With a range of currents from milliamps to tens or even hundreds of amps, good power supply layout is much more difficult than most general PCB design. The general design should proceed from the switching node to the output, then back to the driver section, and, finally, place the low-level components. Below are several specific points to consider *before* layout of a TPS5210 design begins.

1. All sensitive analog components should be referenced to ANAGND. These include components connected to SLOWST, DROOP, IOUT, OCP, VSENSE, VREFB, VHYST, BIAS, and LOHIB.
2. Analog ground and drive ground should be isolated as much as possible. Ideally, analog ground will connect to the ground side of the bulk storage capacitors on  $V_O$ , and drive ground will connect to the main ground plane close to the source of the low-side FET.
3. Connections from the drivers to the gate of the power FETs, should be as short and wide as possible to reduce stray inductance. This becomes more critical if external gate resistors are not being used.
4. The bypass capacitor for the DRV regulator should be placed close to the TPS5210 and be connected to DRVGNL.
5. The bypass capacitor for  $V_{CC}$  should be placed close to the TPS5210 and be connected to DRVGNL.
6. When configuring the high-side driver as a floating driver, the connection from BOOTLO to the power FETs should be as short and as wide as possible. The other pins that also connect to the power FETs, LOHIB and LOSENSE, should have a separate connection to the FETs since BOOTLO will have large peak currents flowing through it.
7. When configuring the high-side driver as a floating driver, the bootstrap capacitor (connected from BOOT to BOOTLO) should be placed close to the TPS5210.
8. When configuring the high-side driver as a ground-referenced driver, BOOTLO should be connected to DRVGNL.
9. The bulk storage capacitors across  $V_I$  should be placed close to the power FETs. High-frequency bypass capacitors should be placed in parallel with the bulk capacitors and connected close to the drain of the high-side FET and to the source of the low-side FET.
10. High-frequency bypass capacitors should be placed across the bulk storage capacitors on  $V_O$ .
11. HISENSE and LOSENSE should be connected very close to the drain and source, respectively, of the high-side FET. HISENSE and LOSENSE should be routed very close to each other to minimize differential-mode noise coupling to these traces. Ceramic decoupling capacitors should be placed close to where HISENSE connects to  $V_{in}$ , to reduce high-frequency noise coupling on HISENSE.



## PACKAGING INFORMATION

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| TPS5210DW        | ACTIVE                | SOIC         | DW              | 28   | 20          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| TPS5210DWG4      | ACTIVE                | SOIC         | DW              | 28   | 20          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| TPS5210DWR       | ACTIVE                | SOIC         | DW              | 28   | 1000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| TPS5210DWRG4     | ACTIVE                | SOIC         | DW              | 28   | 1000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| TPS5210PWP       | ACTIVE                | HTSSOP       | PWP             | 28   | 50          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| TPS5210PWPG4     | ACTIVE                | HTSSOP       | PWP             | 28   | 50          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| TPS5210PWPR      | ACTIVE                | HTSSOP       | PWP             | 28   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| TPS5210PWPRG4    | ACTIVE                | HTSSOP       | PWP             | 28   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

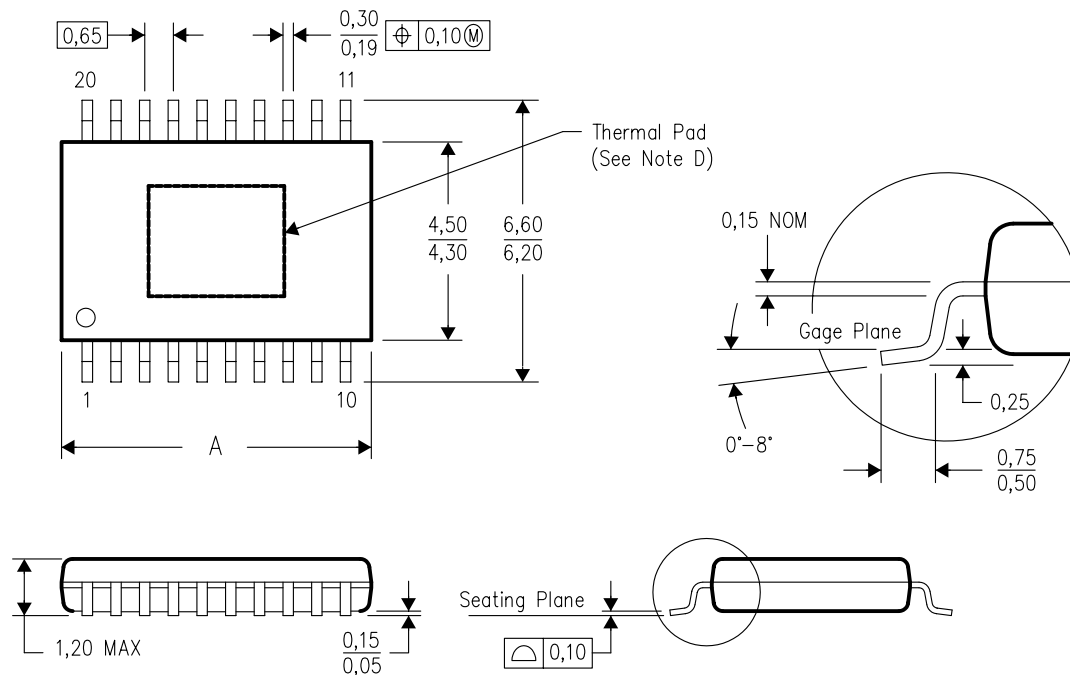
**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## PWP (R-PDSO-G\*\*)

## PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE

20 PIN SHOWN



| PINS ** | 14   | 16   | 20   | 24   | 28   |
|---------|------|------|------|------|------|
| DIM     |      |      |      |      |      |
| A MAX   | 5,10 | 5,10 | 6,60 | 7,90 | 9,80 |
| A MIN   | 4,90 | 4,90 | 6,40 | 7,70 | 9,60 |

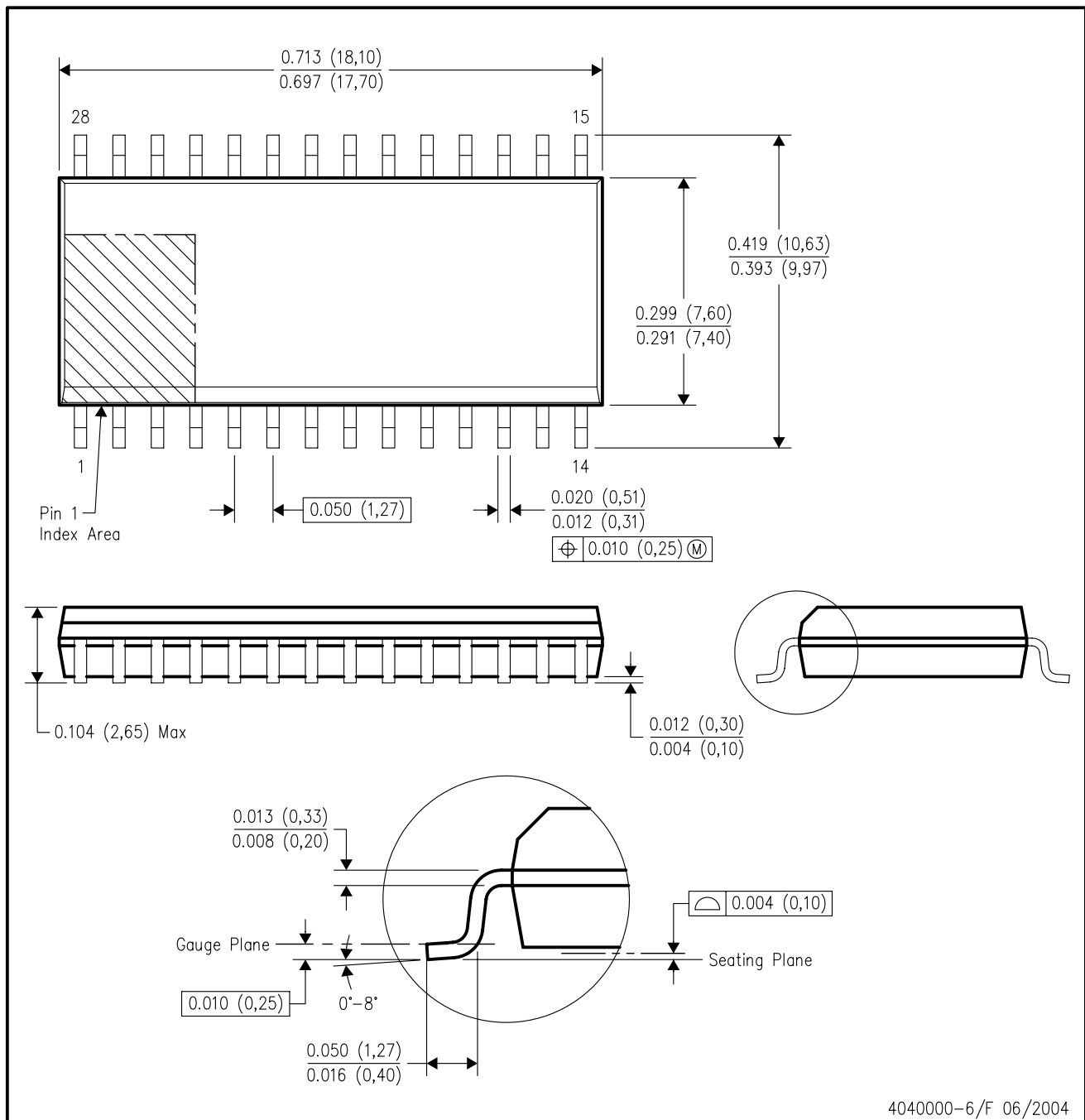
4073225/H 12/05

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

DW (R-PDSO-G28)

# PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
D. Falls within JEDEC MS-013 variation AE.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

### Products

|                    |                                                                    |
|--------------------|--------------------------------------------------------------------|
| Amplifiers         | <a href="http://amplifier.ti.com">amplifier.ti.com</a>             |
| Data Converters    | <a href="http://dataconverter.ti.com">dataconverter.ti.com</a>     |
| DSP                | <a href="http://dsp.ti.com">dsp.ti.com</a>                         |
| Interface          | <a href="http://interface.ti.com">interface.ti.com</a>             |
| Logic              | <a href="http://logic.ti.com">logic.ti.com</a>                     |
| Power Mgmt         | <a href="http://power.ti.com">power.ti.com</a>                     |
| Microcontrollers   | <a href="http://microcontroller.ti.com">microcontroller.ti.com</a> |
| Low Power Wireless | <a href="http://www.ti.com/lpw">www.ti.com/lpw</a>                 |

### Applications

|                    |                                                                          |
|--------------------|--------------------------------------------------------------------------|
| Audio              | <a href="http://www.ti.com/audio">www.ti.com/audio</a>                   |
| Automotive         | <a href="http://www.ti.com/automotive">www.ti.com/automotive</a>         |
| Broadband          | <a href="http://www.ti.com/broadband">www.ti.com/broadband</a>           |
| Digital Control    | <a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a> |
| Military           | <a href="http://www.ti.com/military">www.ti.com/military</a>             |
| Optical Networking | <a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a> |
| Security           | <a href="http://www.ti.com/security">www.ti.com/security</a>             |
| Telephony          | <a href="http://www.ti.com/telephony">www.ti.com/telephony</a>           |
| Video & Imaging    | <a href="http://www.ti.com/video">www.ti.com/video</a>                   |
| Wireless           | <a href="http://www.ti.com/wireless">www.ti.com/wireless</a>             |

Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265