200 mA, LOW QUIESCENT CURRENT, ULTRA-LOW NOISE, HIGH PSRR, LOW DROPOUT, LINEAR REGULATORS

Check for Samples: TPS79901-Q1, TPS79912-Q1, TPS79915-Q1, TPS79918-Q1, TPS79925-Q1, TPS79927-Q1, TPS79933-Q1

FEATURES

- **Qualified for Automotive Applications**
- **200-mA Low-Dropout (LDO) Regulator With Enable (EN)**
- **Low I_Q: 40 µA**
- **Multiple Output Voltage Versions Available:**
  - **Fixed Outputs of 1.2 V to 4.5 V Using Innovative Factory EEPROM Programming**
  - **Adjustable Outputs from 1.2 V to 6.5 V**
- **High PSRR: 66 dB at 1 kHz**
- **Ultralow Noise: 29.5 μV_{RMS}**
- **Fast Start-Up Time: 45 µs**
- **Stable With a Low ESR, 2-µF (Typ) Output Capacitance**
- **Excellent Load/Line Transient Response**
- **2% Overall Accuracy (Load/Line/Temperature)**
- **Very Low Dropout: 100 mV**
- **Thin SOT-23 and 2-mm × 2-mm SON-6 Packages**

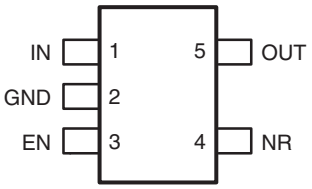
APPLICATIONS

- **Cellular Phones**
- **Wireless LANs, Bluetooth®**
- **VCOs, RF**
- **Handheld Organizers, PDAs**

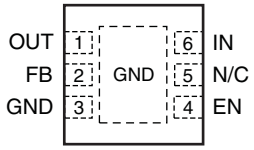
DESCRIPTION

The TPS799xx family of low-dropout (LDO) low-power linear regulators offers excellent ac performance with very low ground current. High power-supply rejection ratio (PSRR), low noise, fast start-up, and excellent line and load transient response are provided while consuming a very low 40-µA (typical) ground current. The TPS799xx is stable with ceramic capacitors and uses an advanced BiCMOS fabrication process to yield a dropout voltage of 100 mV (typ) at 200-mA output. The TPS799xx uses a precision voltage reference and feedback loop to achieve overall accuracy of 2% over all load, line, process, and temperature variations. It is fully specified from T_J = –40°C to 125°C and is offered in low profile ThinSOT-23 and 2-mm × 2-mm SON packages, ideal for wireless handsets and WLAN cards.

DDC (TSOT-23-5) PACKAGE (TOP VIEW)



DRV (SON-6) PACKAGE (TOP VIEW)



N/C – No internal connection

ORDERING INFORMATION(1)

T_J	V_{OUT}	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	1.2 V	SON-6 – DRV	Reel of 3000	TPS79912QDRVRQ1	DAV
	1.5 V	TSOT-23-5 – DDC	Reel of 3000	TPS79915QDDCRQ1	OFC
		SON-6 – DRV	Reel of 3000	TPS79915QDRVRQ1	RAQ
	1.8 V	TSOT-23-5 – DDC	Reel of 3000	TSP79918QDDCRQ1	CEW
	2.5 V	TSOT-23-5 – DDC	Reel of 3000	TPS79925QDDCRQ1	OFM
	2.7 V	TSOT-23-5 – DDC	Reel of 3000	TPS79927QDDCRQ1	OFD
		SON-6 – DRV	Reel of 3000	TPS79927QDRVRQ1	OFK
	3.3 V	TSOT-23-5 – DDC	Reel of 3000	TSP79933QDDCRQ1	PSEQ
	Adjustable(3)	SON-6 – DRV	Reel of 3000	TSP79901QDRVRQ1	CFA

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) For fixed 1.2-V operation, tie FB to OUT.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

over operating temperature range (unless otherwise noted)

V_{IN} range	–0.3 V to 7 V
V_{EN} range	–0.3 V to V_{IN} + 0.3 V
V_{OUT} range	–0.3 V to V_{IN} + 0.3 V
Peak output current	Internally limited
Continuous total power dissipation	See the Thermal Information table
Junction temperature range, T_J	–55°C to 150°C
Storage junction temperature range , T_{stg}	–55°C to 150°C
ESD rating, HBM	2000 V
ESD rating, CDM	1000 V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

THERMAL INFORMATION

THERMAL METRIC(1)(2)		TPS799xxQ1		UNITS
		DRV (6 PINS)	DDC (5 PINS)	
θ_{JA}	Junction-to-ambient thermal resistance	74.2	178.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	58.8	70.7	
θ_{JB}	Junction-to-board thermal resistance	145.9	73.4	
ψ_{JT}	Junction-to-top characterization parameter	0.2	2.5	
ψ_{JB}	Junction-to-board characterization parameter	54.4	74.1	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	7.2	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.

ELECTRICAL CHARACTERISTICS

over operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.3 V or 2.7 V, whichever is greater; I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{OUT} = 2.2 µF, C_{NR} = 0.01 µF (unless otherwise noted) For TPS79901, V_{OUT} = 3.0 V. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range(1)			2.7		6.5	V
V_{FB}	Internal reference (TPS79901)			1.169	1.193	1.217	V
V_{OUT}	Output voltage range (TPS79901)			V_{FB}		6.5 – V_{DO}	V
V_{OUT}	Output accuracy	Nominal, T_J = 25°C		–1.0		+1.0	%
V_{OUT}	Output accuracy(1)	Over V_{IN}, I_{OUT}, temperature, V_{OUT} + 0.3 V ≤ V_{IN} ≤ 6.5 V, 500 µA ≤ I_{OUT} ≤ 200 mA		–2.0	±1.0	+2.0	%
ΔV_{OUT}%/ ΔV_{IN}	Line regulation(1)	$V_{OUT(NOM)}$ + 0.3 V ≤ V_{IN} ≤ 6.5 V			0.02		%/V
ΔV_{OUT}%/ ΔI_{OUT}	Load regulation	500 µA ≤ I_{OUT} ≤ 200 mA			0.002		%/mA
V_{DO}	Dropout voltage(2) (V_{IN} = $V_{OUT(NOM)}$ – 0.1 V)	V_{OUT} < 3.3 V	I_{OUT} = 200 mA		100	175	mV
		V_{OUT} ≥ 3.3 V			90	160	
I_{CL}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(NOM)}$		200	400	600	mA
I_{GND}	Ground pin current	500 µA ≤ I_{OUT} ≤ 200 mA			40	60	µA
I_{SHDN}	Shutdown current (I_{GND})	V_{EN} ≤ 0.4 V, 2.7 V ≤ V_{IN} ≤ 6.5 V			0.15	1.0	µA
I_{FB}	Feedback pin current (TPS79901)			–0.5		0.5	µA
PSRR	Power-supply rejection ratio	V_{IN} = 3.85 V, V_{OUT} = 2.85 V, C_{NR} = 0.01 µF, I_{OUT} = 100 mA	f = 100 Hz		70		dB
			f = 1 kHz		66		
			f = 10 kHz		51		
			f = 100 kHz		38		
V_N	Output noise voltage BW = 10 Hz to 100 kHz, V_{OUT} = 2.8 V	C_{NR} = 0.01 µF			10.5 V_{OUT}		μV_{RMS}
		C_{NR} = none			94 V_{OUT}		
T_{STR}	Startup time	V_{OUT} = 2.85 V, R_L = 14 Ω, C_{OUT} = 2.2 µF	C_{NR} = 0.001 µF		45		µs
			C_{NR} = 0.047 µF		45		
			C_{NR} = 0.01 µF		50		
			C_{NR} = none		50		
$V_{EN(HI)}$	Enable high (enabled)			1.2		V_{IN}	V
$V_{EN(LO)}$	Enable low (shutdown)			0		0.4	V
$I_{EN(HI)}$	Enable pin current, enabled	V_{EN} = V_{IN} = 6.5 V			0.03	1.0	µA
TSD	Thermal shutdown temperature	Shutdown, temperature increasing			165		°C
		Reset, temperature decreasing			145		°C
T_J	Operating junction temperature			–40		125	°C
V_{UVLO}	Undervoltage lock-out	V_{IN} rising		1.90	2.20	2.65	V
$V_{UVLO,hys}$	Hysteresis	V_{IN} falling			70		mV

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or 2.7 V, whichever is greater.
(2) V_{DO} is not measured for devices with $V_{OUT(NOM)}$ < 2.8 V because minimum V_{IN} = 2.7 V.

DEVICE INFORMATION

FUNCTIONAL BLOCK DIAGRAMS

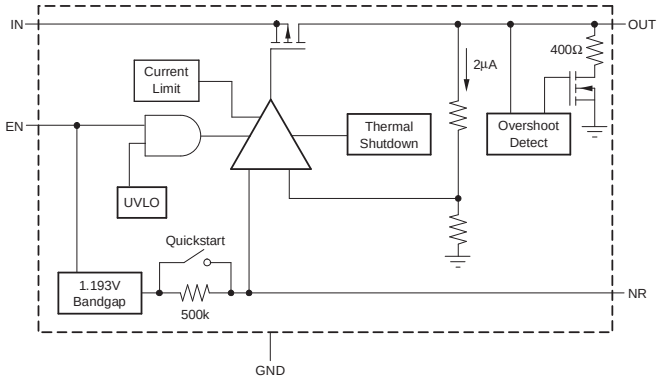


Figure 1. Fixed-Voltage Version

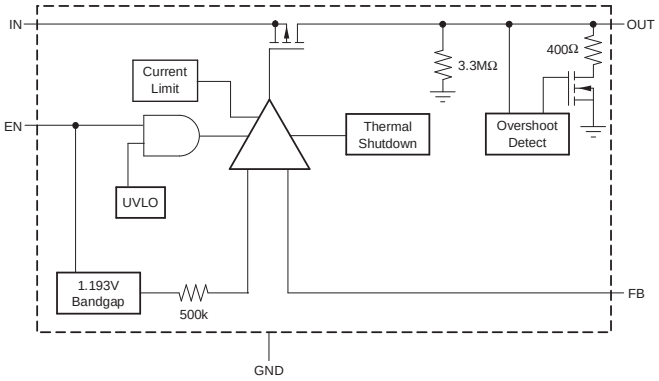
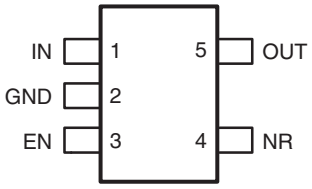


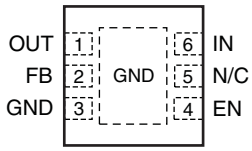
Figure 2. Adjustable-Voltage Version

PIN CONFIGURATIONS

DDC (TSOT-23-5) PACKAGE (TOP VIEW)



DRV (SON-6) PACKAGE (TOP VIEW)



N/C – No internal connection

Table 1. PIN DESCRIPTIONS

PIN			DESCRIPTION
NAME	NO.		
	DDC	DRV	
IN	1	6	Input supply
GND	2	3, Pad	Ground. The pad must be tied to GND.
EN	3	4	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. EN can be connected to IN if not used.
NR	4	2	Fixed-voltage versions only; connecting an external capacitor to this pin bypasses noise generated by the internal bandgap. This capacitor allows output noise to be reduced to very low levels.
FB	4	2	Adjustable version only; this pin is the input to the control loop error amplifier, and is used to set the output voltage of the device.
OUT	5	1	Output of the regulator. A small capacitor (total typical capacitance ≥ 2 µF ceramic) is needed from this pin to ground to ensure stability.
N/C	—	5	Not internally connected. This pin must either be left open or tied to GND.

TYPICAL CHARACTERISTICS

Over operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.3 V or 2.7 V, whichever is greater; I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{OUT} = 2.2 µF, C_{NR} = 0.01 µF (unless otherwise noted). For TPS79901, V_{OUT} = 3 V. Typical values are at T_J = 25°C.

LOAD REGULATION

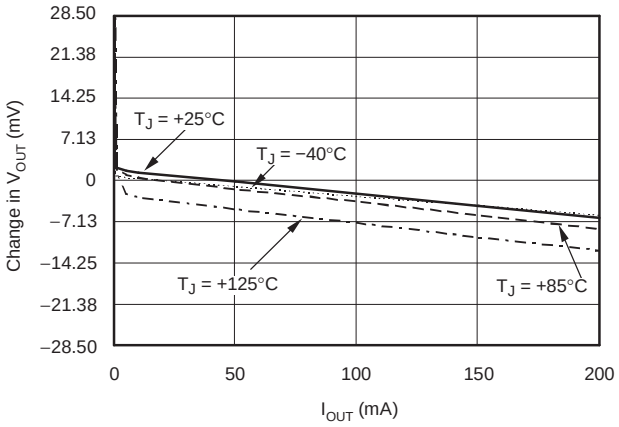


Figure 3.

LINE REGULATION

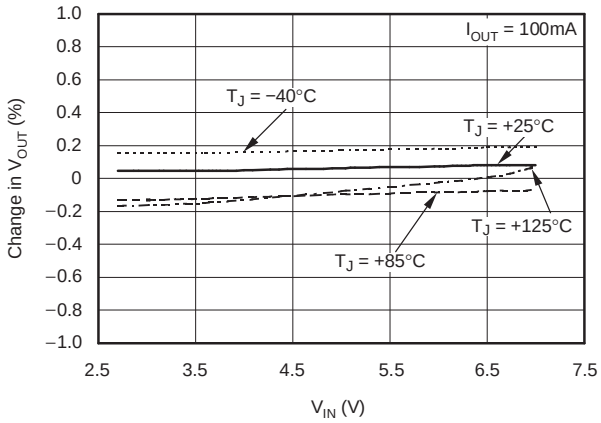


Figure 4.

OUTPUT VOLTAGE vs JUNCTION TEMPERATURE

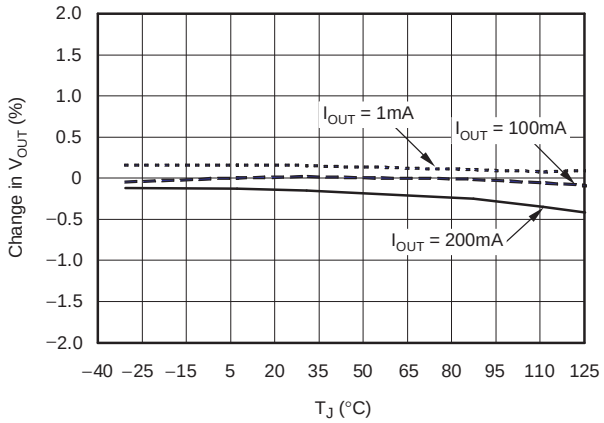


Figure 5.

TPS79901 DROPOUT vs INPUT VOLTAGE

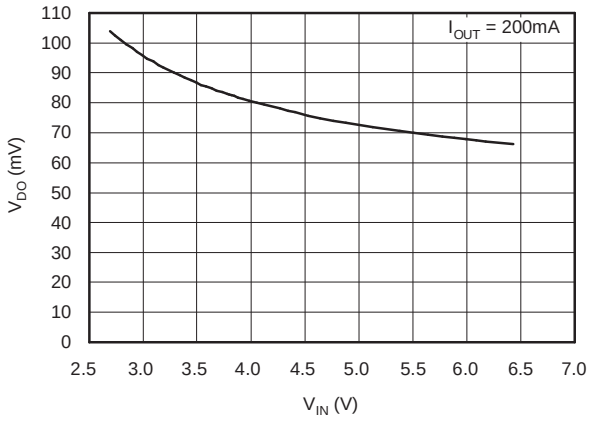


Figure 6.

GROUND PIN CURRENT vs INPUT VOLTAGE

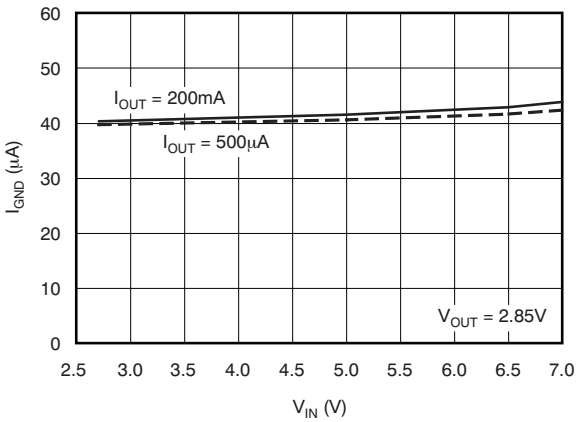


Figure 7.

GROUND PIN CURRENT (DISABLED) vs JUNCTION TEMPERATURE

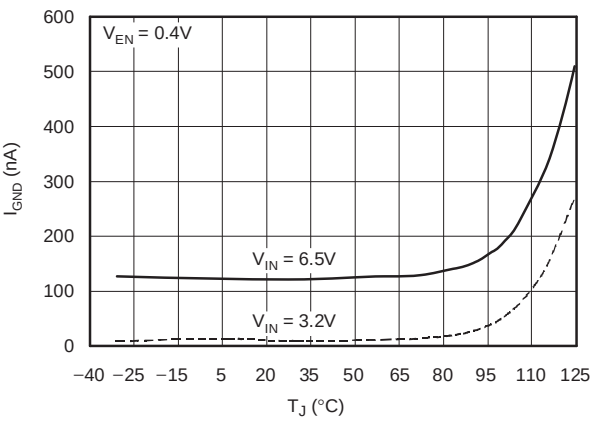


Figure 8.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.3 V or 2.7 V, whichever is greater; I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{OUT} = 2.2 µF, C_{NR} = 0.01 µF (unless otherwise noted). For TPS79901, V_{OUT} = 3 V. Typical values are at T_J = 25°C.

POWER-SUPPLY RIPPLE REJECTION vs V_{IN} – V_{OUT}, I_{OUT} = 1 mA

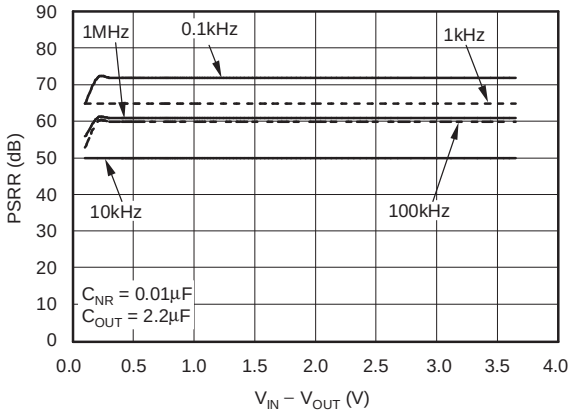


Figure 9.

POWER-SUPPLY RIPPLE REJECTION vs V_{IN} – V_{OUT}, I_{OUT} = 100 mA

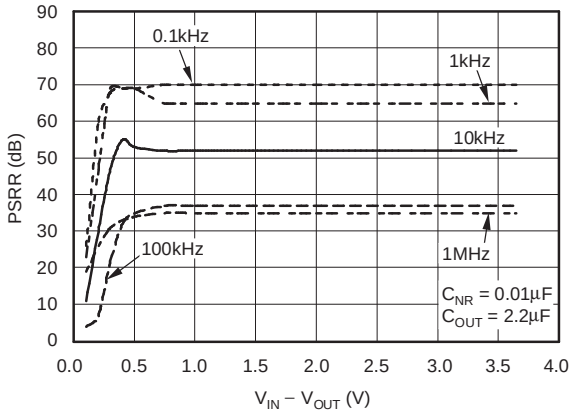


Figure 10.

POWER-SUPPLY RIPPLE REJECTION vs V_{IN} – V_{OUT}, I_{OUT} = 200 mA

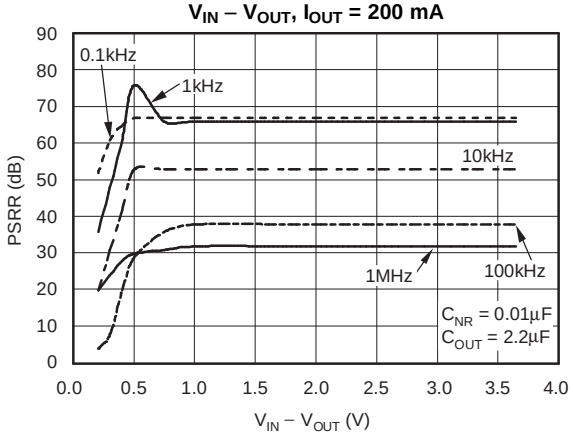


Figure 11.

APPLICATION INFORMATION

The TPS799xx family of LDO regulators combines the high performance required of many RF and precision analog applications with ultra-low current consumption. High PSRR is provided by a high gain, high bandwidth error loop with good supply rejection at very low headroom (V_{IN} – V_{OUT}). Fixed voltage versions provide a noise reduction pin to bypass noise generated by the bandgap reference and to improve PSRR while a quick-start circuit fast-charges this capacitor at startup. The combination of high performance and low ground current also make the TPS799xx an excellent choice for portable applications. All versions have thermal and over-current protection and are fully specified from –40°C to 125°C.

Figure 12 shows the basic circuit connections for fixed-voltage model. Figure 13 gives the connections for the adjustable output version (TPS79901). R_1 and R_2 can be calculated for any output voltage using the formula in Figure 13. Sample resistor values for common output voltages are shown in Figure 13.

Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1-µF to 1-µF low ESR capacitor across the input supply near the regulator. This counteracts reactive input sources and improve transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated or the device is located several inches from the power source. If source impedance is not sufficiently low, a 0.1-µF input capacitor may be necessary to ensure stability.

The TPS799xx is designed to be stable with standard ceramic capacitors of values 2.2 µF or larger. X5R and X7R type capacitors are best as they have minimal variation in value and ESR over temperature. Maximum ESR should be <1.0 Ω.

Feedback Capacitor Requirements (TPS79901 only)

The feedback capacitor, C_{FB}, shown in Figure 13 is required for stability. For a parallel combination of R_1 and R_2 equal to 250 kΩ, any value from 3 pF to 1 nF can be used. Fixed voltage versions have an internal 30-pF feedback capacitor which is quick-charged at start-up. The adjustable version does not have this quick-charge circuit, so values below 5 pF should be used to ensure fast startup; values above 47 pF can be used to implement an output voltage soft-start. Larger value capacitors also improve noise slightly. The TPS79901 is stable in unity-gain configuration (OUT tied to FB) without C_{FB}.

Output Noise

In most LDOs, the bandgap is the dominant noise source. If a noise reduction capacitor (C_{NR}) is used with the TPS799xx, the bandgap does not contribute significantly to noise. Instead, noise is dominated by the output resistor divider and the error amplifier input. To minimize noise in a given application, use a 0.01-µF noise reduction capacitor; for the adjustable version, smaller value resistors in the output resistor divider reduce noise. A parallel combination that gives 2 µA of divider current has the same noise performance as a fixed-voltage version. To further optimize noise, equivalent series resistance of the output capacitor can be set to approximately 0.2 Ω. This configuration maximizes phase margin in the control loop, reducing total output noise by up to 10%.

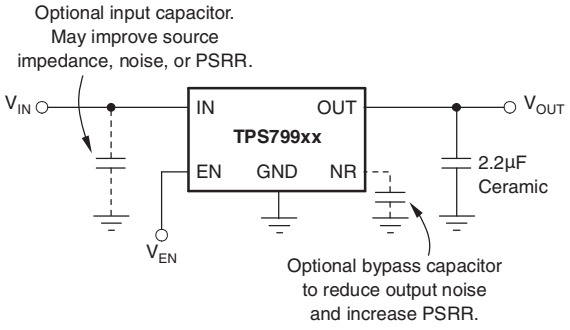


Figure 12. Typical Application Circuit for Fixed Voltage Version

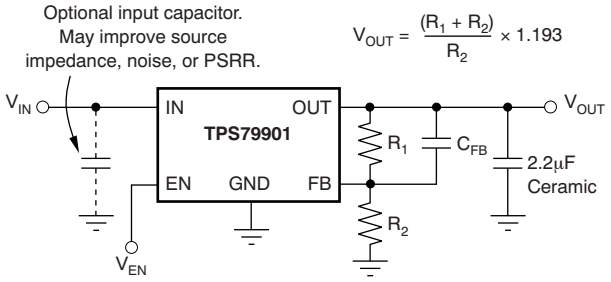


Figure 13. Typical Application Circuit for Adjustable Voltage Version

Noise can be referred to the feedback point (FB pin) such that with C_{NR} = 0.01 µF, total noise is approximately given by Equation 1:

$$V_N = \frac{10.5\mu V_{RMS}}{V} \times V_{OUT} \quad (1)$$

The TPS79901 adjustable version does not have the noise-reduction pin available, so ultra-low noise operation is not possible. Noise can be minimized according to the previous recommendations.

Board Layout Recommendations to Improve PSRR and Noise Performance

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

Internal Current Limit

The TPS799xx internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. For reliable operation, the device should not be operated in current limit for extended periods of time.

The PMOS pass element in the TPS799xx has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting may be appropriate.

Shutdown

The enable pin (EN) is active high and is compatible with standard and low voltage TTL-CMOS levels. When shutdown capability is not required, EN can be connected to IN.

Dropout Voltage

The TPS799xx uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in its linear region of operation and the input-to-output resistance is the $R_{DS,\ ON}$ of the PMOS pass element. Because the PMOS device behaves like a resistor in dropout, V_{DO} scales approximately with output current.

As with any linear regulator, PSRR and transient response are degraded as (V_{IN} – V_{OUT}) approaches dropout. This effect is shown in Figure 9 through Figure 11 in the *Typical Characteristics* section.

Startup

Fixed voltage versions of the TPS799xx use a quick-start circuit to fast-charge the noise reduction capacitor, C_{NR}, if present (see *Functional Block Diagrams*, Figure 1). This allows the combination of very low output noise and fast start-up times. The NR pin is high impedance so a low leakage C_{NR} capacitor must be used; most ceramic capacitors are appropriate in this configuration.

Note that for fastest startup, V_{IN} should be applied first, then the enable pin (EN) driven high. If EN is tied to IN, startup is somewhat slower. The quick-start switch is closed for approximately 135 µs. To ensure that C_{NR} is fully charged during the quick-start time, a 0.01 µF or smaller capacitor should be used.

Transient Response

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude but increase duration of the transient response. In the adjustable version, adding C_{FB} between OUT and FB improves stability and transient response. The transient response of the TPS799xx is enhanced by an active pulldown that engages when the output overshoots by approximately 5% or more when the device is enabled. When enabled, the pulldown device behaves like a 350-Ω resistor to ground.

Undervoltage Lockout (UVLO)

The TPS799xx utilizes a UVLO circuit to keep the output shut off until internal circuitry is operating properly. The UVLO circuit has a deglitch feature so that it typically ignores undershoot transients on the input if they are less than 50-µs duration.

Minimum Load

The TPS799xx is stable and well behaved with no output load. To meet the specified accuracy, a minimum load of 500 µA is required. Below 500 µA at junction temperatures near 125°C, the output can drift up enough to cause the output pulldown to turn on. The output pulldown limits voltage drift to 5% typically, but ground current could increase by approximately 50 µA. In typical applications, the junction cannot reach high temperatures at light loads since there is no appreciable dissipated power. The specified ground current would then be valid at no load in most applications.

THERMAL INFORMATION

Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 165°C, allowing the device to cool. When the junction temperature cools to approximately 145°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage due to overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS799xx has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS799xx into thermal shutdown degrades device reliability.

Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the head from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the *Thermal Information* table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through holes to heat-dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation is equal to the product of the output current times the voltage drop across the output pass element, as shown in Equation 2:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

Package Mounting

Solder pad footprint recommendations for the TPS799xx are available from the Texas Instruments' web site at www.ti.com.

REVISION HISTORY

Changes from Revision D (June 2011) to Revision E **Page**

- Changed CDM ESD rating from 500 V to 1000 V 2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS79901QDRVRQ1	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS79912QDRVRQ1	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS79915QDDCRQ1	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS79915QDRVRQ1	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS79918QDDCRQ1	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS79925QDDCRQ1	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS79927QDDCRQ1	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS79927QDRVRQ1	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS79933QDDCRQ1	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

OTHER QUALIFIED VERSIONS OF TPS79901-Q1, TPS79912-Q1, TPS79915-Q1, TPS79918-Q1, TPS79925-Q1, TPS79927-Q1, TPS79933-Q1 :

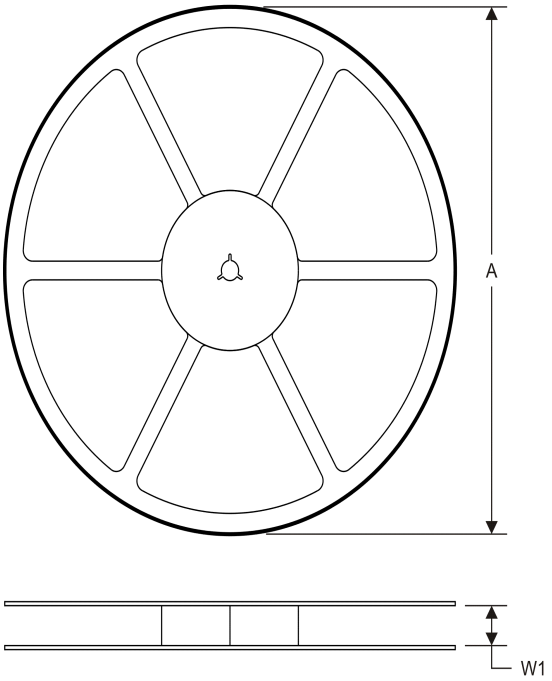
- Catalog: TPS79901, TPS79912, TPS79915, TPS79918, TPS79925, TPS79927, TPS79933

NOTE: Qualified Version Definitions:

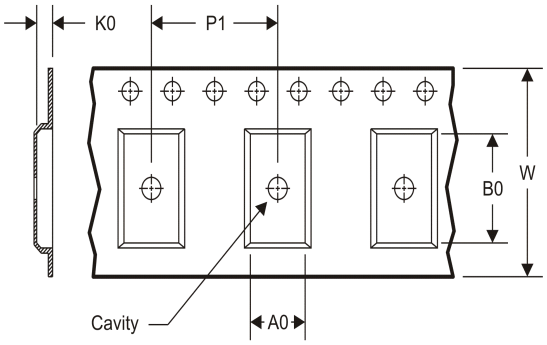
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



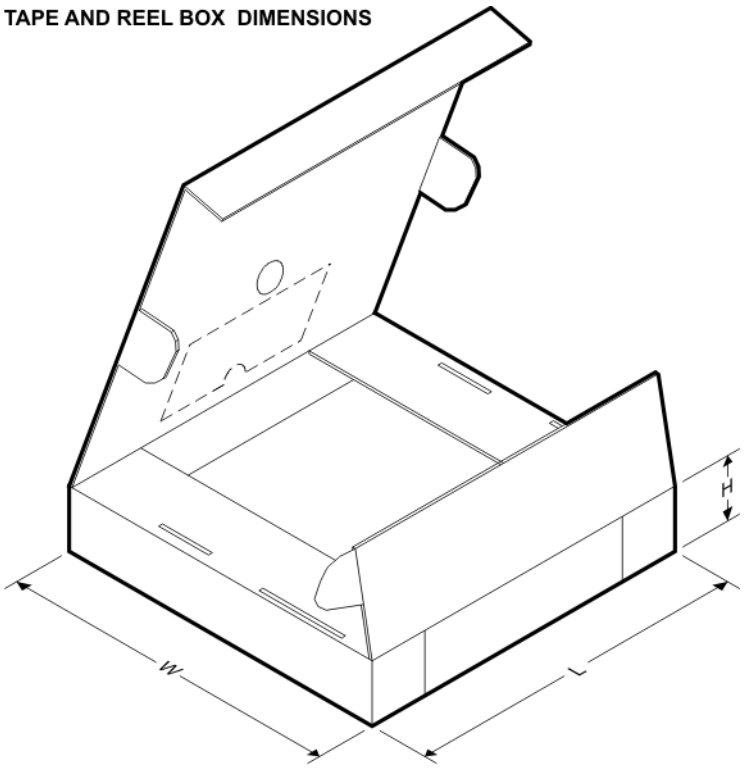
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS79912QDRVRQ1	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS79915QDDCRQ1	SOT	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79915QDRVRQ1	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS79925QDDCRQ1	SOT	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79927QDDCRQ1	SOT	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79927QDRVRQ1	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS79933QDDCRQ1	SOT	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

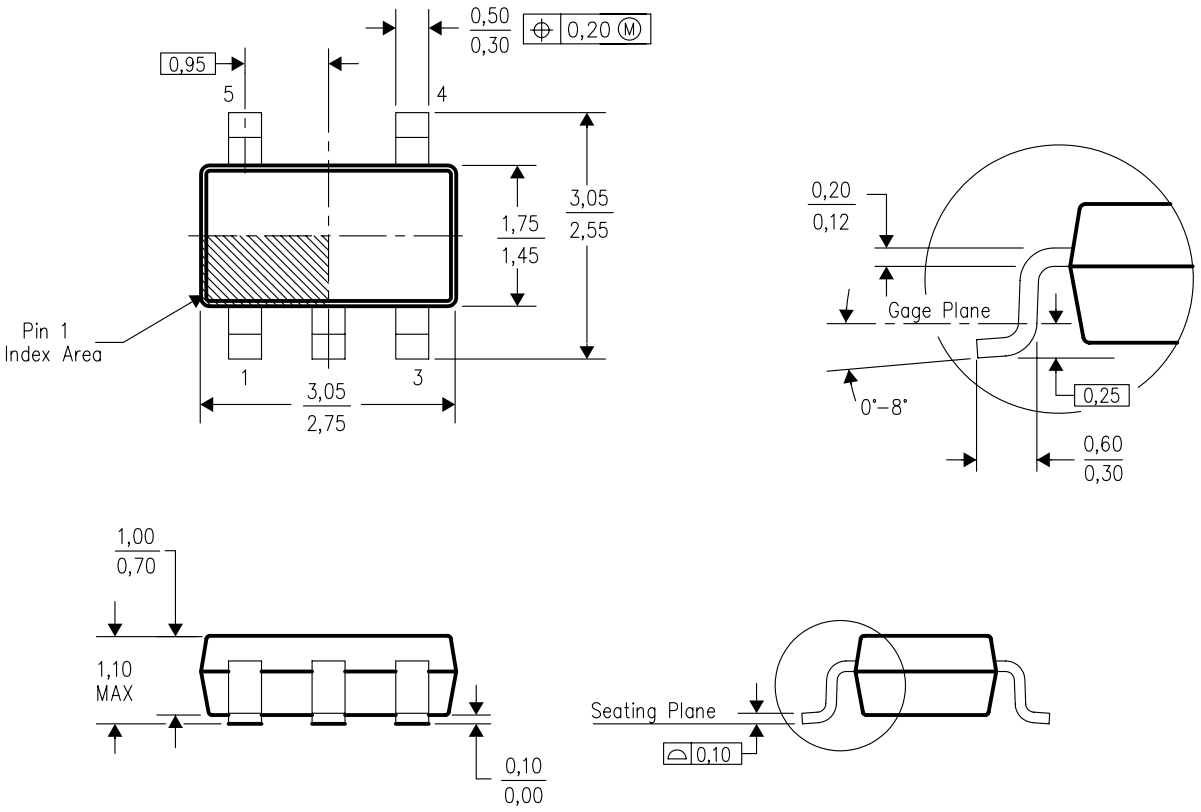
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS79912QDRVRQ1	SON	DRV	6	3000	195.0	200.0	45.0
TPS79915QDDCRQ1	SOT	DDC	5	3000	203.0	203.0	35.0
TPS79915QDRVRQ1	SON	DRV	6	3000	195.0	200.0	45.0
TPS79925QDDCRQ1	SOT	DDC	5	3000	203.0	203.0	35.0
TPS79927QDDCRQ1	SOT	DDC	5	3000	203.0	203.0	35.0
TPS79927QDRVRQ1	SON	DRV	6	3000	195.0	200.0	45.0
TPS79933QDDCRQ1	SOT	DDC	5	3000	203.0	203.0	35.0

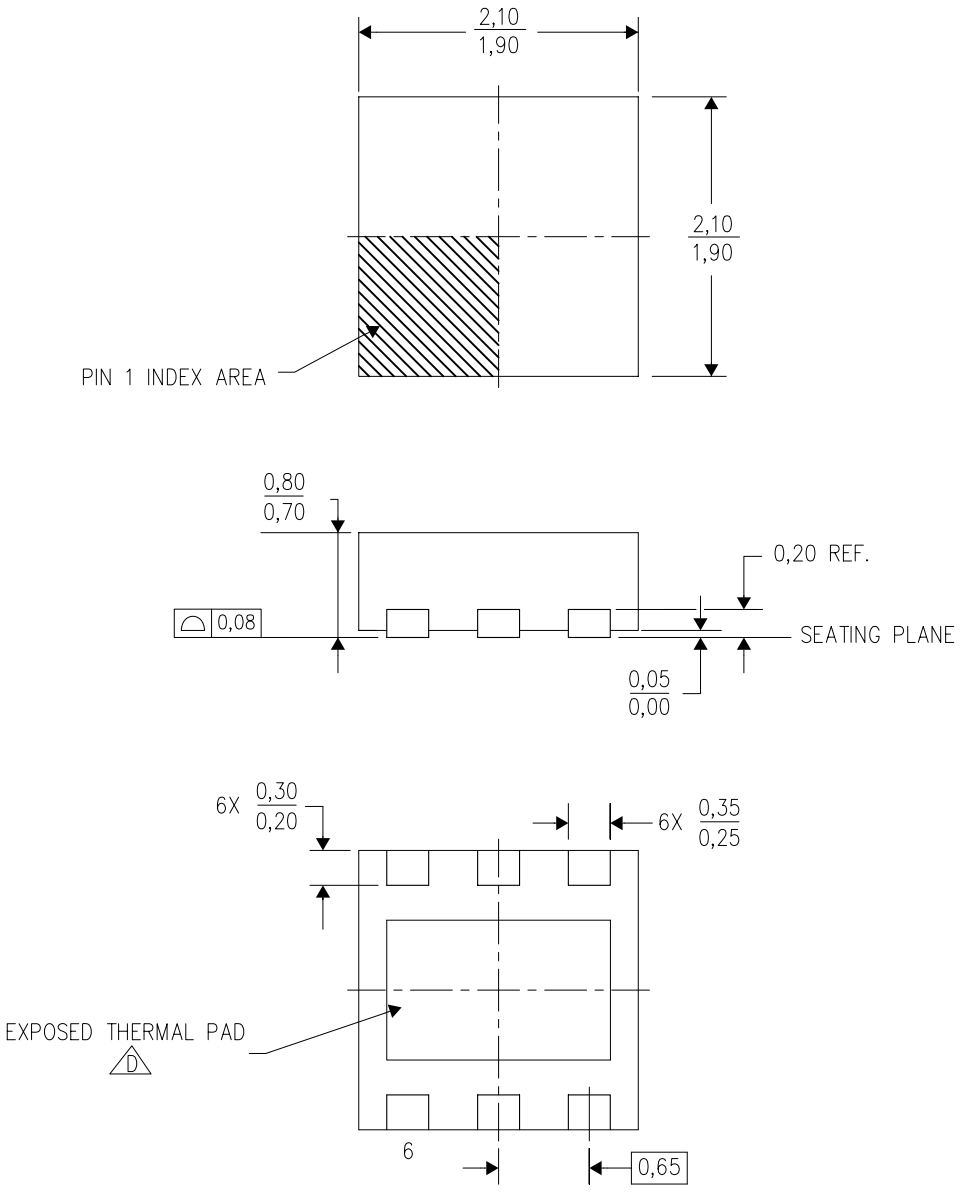
DDC (R–PDSO–G5) PLASTIC SMALL–OUTLINE



4204403–2/E 06/05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–193 variation AB (5 pin).

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



4206925/E 10/10

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

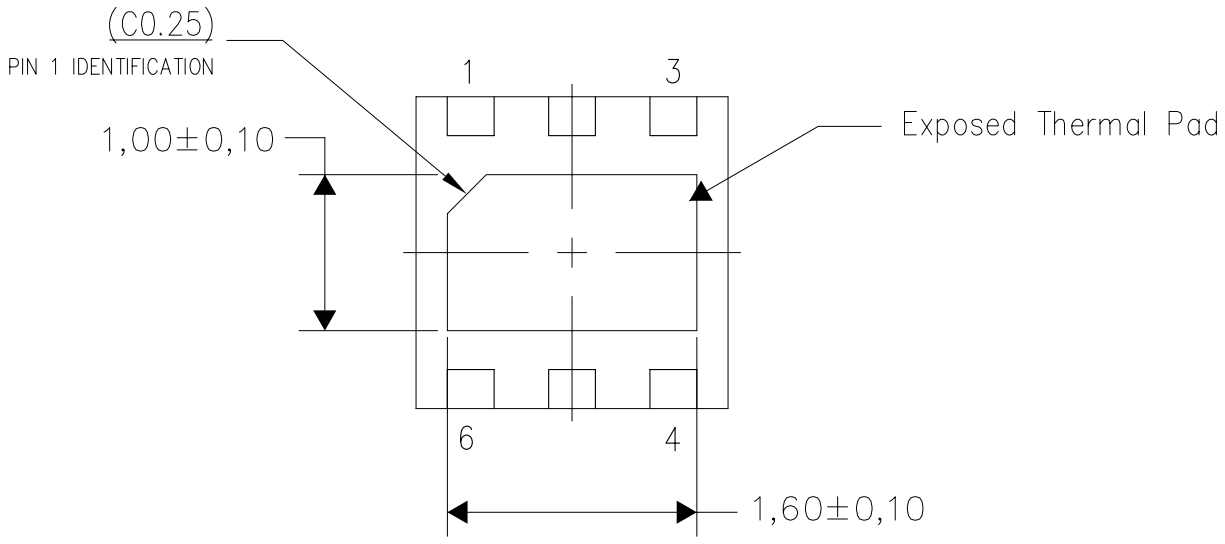
DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



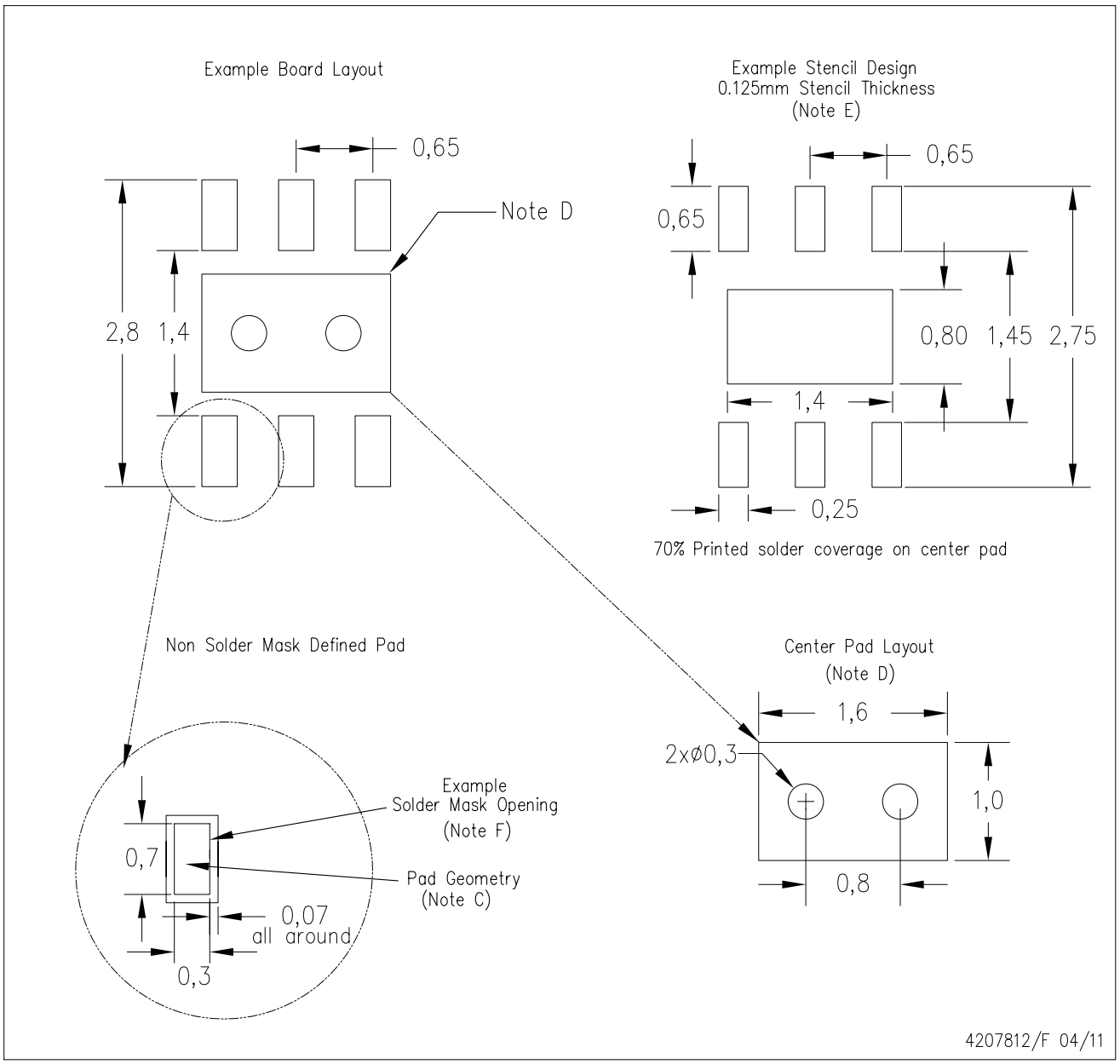
Bottom View

Exposed Thermal Pad Dimensions

4206926–3/L 11/11

NOTE: A. All linear dimensions are in millimeters

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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