TEXAS INSTRUMENTS

TPS92311

Off-Line Primary Side Sensing Converter with PFC

General Description

The TPS92311 is an off-line converter specifically designed to drive high power LEDs for lighting applications. Features include an integrated 3.75Ω 600V power MOSFET, adaptive constant on-time control, quasi-resonant switching, and capable of operating in various topologies via mode selection pins. The TPS92311 is ideally suited for driving 8W LED loads and below. Power Factor Correction is inherent if the TPS92311 is operated in the constant on-time mode with an adaptive algorithm. Resonant switching allows for a reduced EMI signature and increased system efficiency. Low external parts count is realized with its simplified and high level of integration. The control algorithm of TPS92311 adjusts the on time with reference to the primary side inductor peak current and secondary side inductor discharge time dynamically, the response time of which is set by an external capacitor. Other supervisory features of the TPS92311 include cycle-by-cycle primary side inductor current limit, VCC under-voltage lockout, output over-voltage protection and thermal shutdown. The TPS92311 is available in 16–pin narrow SOIC package.

Features

- Integrated 600V power MOSFET
- Regulates LED current without secondary side sensing
- Adaptive ON-time control with inherent PFC
- Critical-Conduction-Mode (CRM) with Zero-Current Detection (ZCD) for valley switching
- Programmable switch turn ON delay
- Programmable Constant ON-Time (COT) and Peak Current Control
- Over-temperature protection

Applications

- LED Lamps: A19 (E26/27, E14), PAR30/38, GU10
- Solid State Lighting

Typical Application

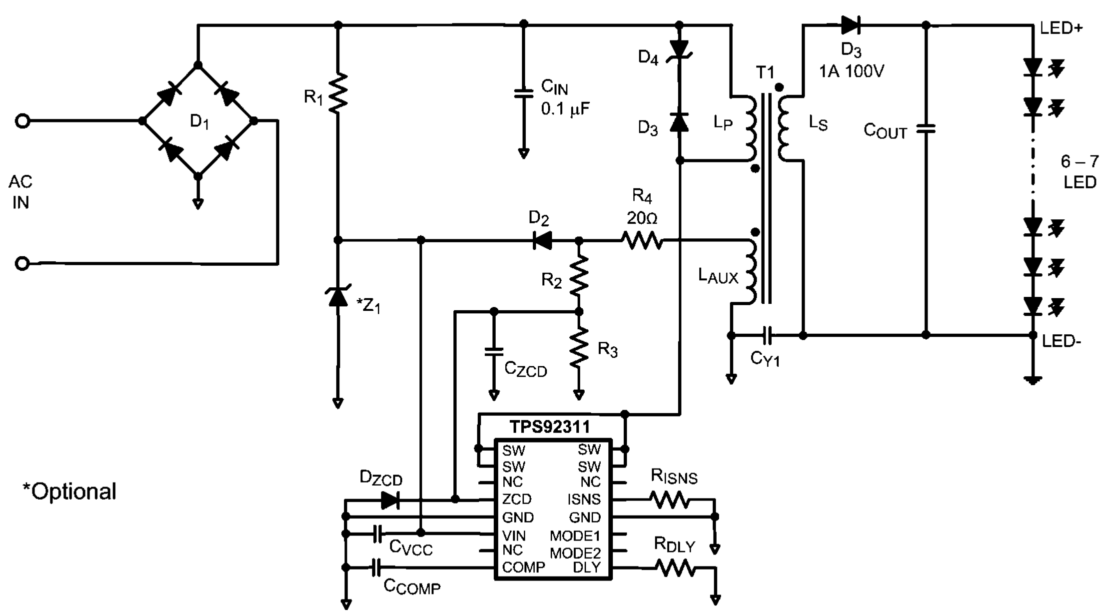
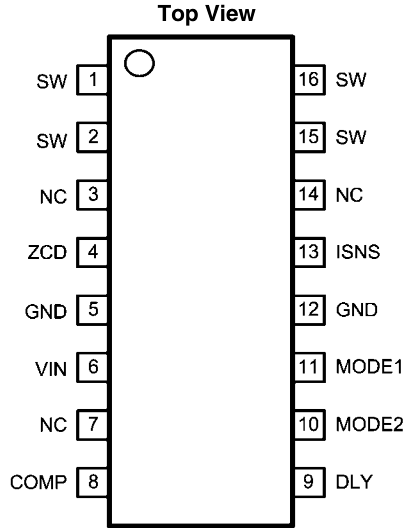


FIGURE 1.

Connection Diagram



16–Lead Narrow SOIC package

Ordering Information

Order Number	Package Type	Package QTY	Supplied As
TPS92311D	Narrow SOIC-16	48	Rails
TPS92311DR	Narrow SOIC-16	2500	Tape and Reel

Pin Descriptions

Pin	Name	Description	Application Information
1, 2, 15, 16	SW	Drain	Internal power MOSFET drain pin
3, 7, 14	NC	No Connection	No connection pin
4	ZCD	Zero crossing detection input	The pin senses the voltage of the auxiliary winding for zero current detection.
5, 12	GND	Ground	Circuit ground.
6	VIN	Power supply Input	This pin provides power to the internal control
8	COMP	Compensation network	Output of the error amplifier. Connect a capacitor from this pin to ground to set the frequency response of the LED current regulation loop.
9	DLY	Delay control input	Connect a resistor from this pin to ground to set the delay between switching ON and OFF periods.
10	MODE2	Mode selection input 2	Select operating mode for isolated or non-isolated mode.
11	MODE1	Mode selection input 1	Select operating mode for peak current mode or constant ON time.
13	ISNS	Current sense voltage feedback	Switch current sensing input.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

SW to GND	-0.3V to 600V
VCC to GND	-0.3V to 40V
DLY, COMP, ZCD to GND	-0.3V to 7V
ISNS to GND	-0.3V to 7V
MODE1 to GND	-0.3V to 7V
MODE2 to GND	-0.3V to 7V
SW FET Drain Current:	
Peak	1.2A
Continuous	Limited by T_{J-MAX}
Continuous Power Dissipation	Internally Limited
ESD Susceptibility:	
HBM (Note 3)	±2 kV
Storage Temperature Range	-65°C to +150°C
Junction Temperature (T_{J-MAX})	+125°C
Maximum Lead Temperature (Solder and Reflow)	260°C

Operating Conditions

Supply Voltage range VCC	13V to 36V
Junction Temperature (T_J)	-40°C to +125°C
Thermal Resistance (θ_{JA}) (Note 6)	95°C/W

Electrical Characteristics

V_{CC} = 18V unless otherwise indicated. Typicals and limits appearing in plain type apply for $T_A = T_J$ = +25°C. Limits appearing in **boldface** type apply over the full Operating Temperature Range. Data sheet minimum and maximum specification limits are guaranteed by design, test or statistical analysis.

Symbol	Parameter	Conditions	Min	Typ (Note 5)	Max	Units
SUPPLY VOLTAGE INPUT (VCC)						
$V_{CC-UVLO}$	VCC Turn on threshold		23.4 / **23**	25.6	27.8 / **29**	V
	VCC Turn off threshold		11.1 / **10.4**	13	14.7 **/ 15.7**	V
	Hysteresis			12.6		
$I_{STARTUP}$	Startup Current	$V_{CC} = V_{CC-UVLO}$–3.0V	**10**	12.5	**14.75**	µA
I_{VCC}	Operating supply current	Not switching	**0.9**	1.2	**1.5**	mA
		65kHz switching		2		mA
ZERO CROSS DETECT (ZCD)						
I_{ZCD}	ZCD bais current	V_{ZCD}= 5V		0.1	1	uA
$V_{ZCD-OVP}$	ZCD over-voltage threshold		**4.1**	4.3	**4.5**	V
T_{OVP}	Over voltage de-bounce time			3		cycle
$V_{ZCD-ARM}$	ZCD Arming threshold	V_{ZCD} = Increasing	**1.16**	1.24	**1.3**	V
$V_{ZCD-TRIG}$	ZCD Trigger threshold	V_{ZCD} = Decreasing	**0.48**	0.6	**0.77**	V
$V_{ZCD-HYS}$	ZCD Hysteresis	$V_{ZCD-ARM}$-$V_{ZCD-TRIG}$		0.64		V
COMPENSATION (COMP)						
$I_{COMP-SOURCE}$	Internal reference current for primary side current regulation	V_{COMP} = 2.0V, V_{ISNS} = 0V, Measure at COMP pin		27		µA
gm_{ISNS}	ISNS error amp trans-conductance	ΔV_{ISNS} to ΔI_{COMP} @ V_{COMP} = 2.0V		100		µmho
V_{COMP}	COMP operating range		2.0		3.5	V
DELAY CONTROL (DLY)						
V_{DLY}	DLY pin internal reference voltage		**1.21**	1.23	**1.26**	V
$I_{DLY-MAX}$	DLY source current	V_{DLY} = 0V	**250**			µA

Symbol	Parameter	Conditions	Min	Typ (Note 5)	Max	Units
CURRENT SENSE (ISNS)						
$V_{ISNS-OCP}$	Over Current Detection Threshold	Non isolation mode	0.56	0.61	0.68	V
$V_{ISNS-OCP}$	Over Current Detection Threshold	Isolation mode	3.2	3.4	3.6	V
I_{ISNS}	Current Sense Bias Current	V_{ISNS} = 5V	-1		1	µA
T_{OCP}	Over current Detection Propagation Delay	R_{SNS} = 1K, Measure ISNS pin pulse width with V_{SW} = 6V		210		ns
OUTPUT MOSFET (SW FET)						
V_{BVDS}	SW to ISNS breakdown voltage		600	660		V
I_{DS}	SW to ISNS leakage current (Note 4)	V_{SW}-V_{ISNS} = 600V			1.35	µA
R_{DS}	SW to ISNS switch on resistance			3.75		Ω
T_{ON-MIN}	Minimum ON time		**330**	540	**900**	ns
T_{ON-MAX}	Maximum ON time		**28**	44	**58**	µs
$T_{OFF-MIN}$	Minimum OFF time		**1.04**	1.5	**1.93**	µs
$T_{OFF-MAX}$	Maximum OFF time	R_{SNS} = 1K, Measure ISNS pull-down period with V_{SW} = 6V and V_{ZCD} = 0V	**50**	70	**94**	µs
THERMAL SHUTDOWN						
TSD	Thermal shutdown temperature	(Note 2)		165		°C
	Thermal Shutdown hysteresis			20		°C

Note 1: Absolute maximum ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is intended to be functional, but device parameter specifications may not be guaranteed. For guaranteed specifications and test conditions, see the Electrical Characteristics. All voltages are with respect to the potential at the GND pin, unless otherwise specified.

Note 2: Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 165°C (typ.) and disengages at T_J = 145°C (typ).

Note 3: Human Body Model, applicable std. JESD22-A114-C.

Note 4: High voltage devices such as the TPS92311 are susceptible to increased leakage currents when exposed to high humidity and high pressure operating environments. Users of this device are cautioned to satisfy themselves as to the suitability of this product in the intended end application and take any necessary precautions (e.g. system level HAST/HALT testing, conformal coating, potting, etc.) to ensure proper device operation.

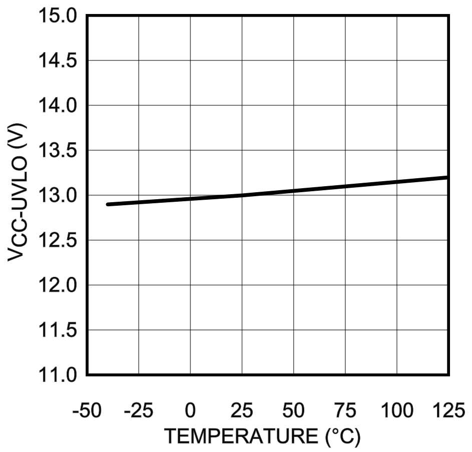
Note 5: Typical numbers are at 25°C and represent the most likely norm.

Note 6: This $R_{θJA}$ typical value determined using JEDEC specifications JESD51-1 to JESD51-11. However junction-to-ambient thermal resistance is highly boardlayout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues during board design. In high-power dissipation applications, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application ($R_{θJA}$), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (R_{θJA} \times P_{D-MAX})$.

Typical Performance Characteristics

All curves taken at V_{CC}=18V with configuration in typical application for driving seven power LEDs with I_{LED}=350mA shown in this datasheet. T_A=25°C, unless otherwise specified.

$V_{CC\text{-}UVLO}$ vs Temperature



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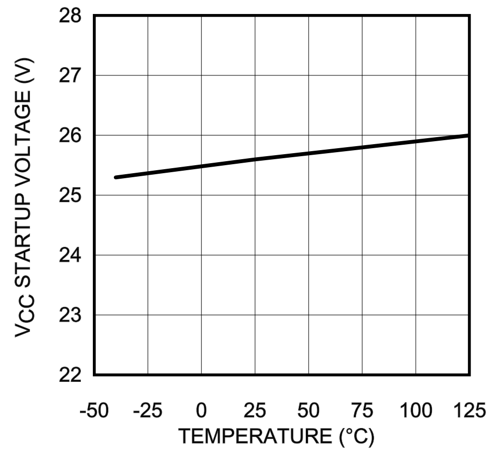
V_{CC} Startup Voltage vs Temperature



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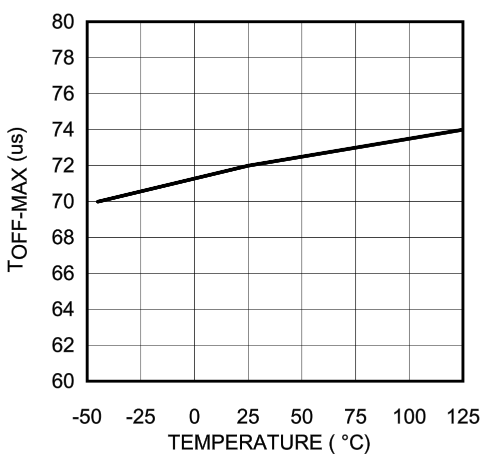
$T_{OFF\text{-}MAX}$ vs Temperature



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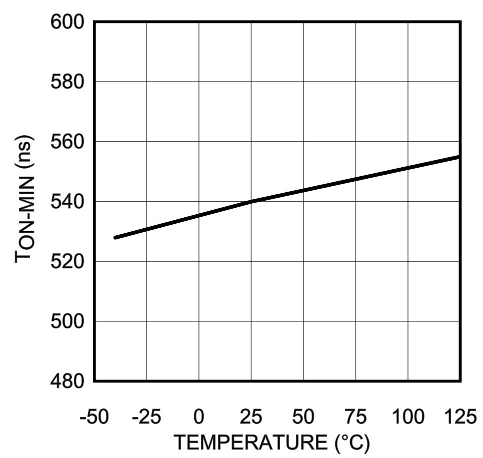
$T_{ON\text{-}MIN}$ vs Temperature



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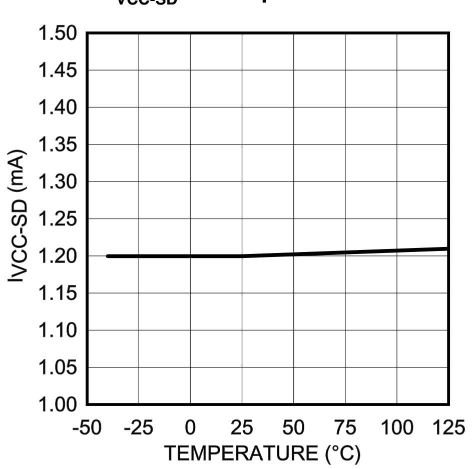
$I_{VCC\text{-}SD}$ vs Temperature



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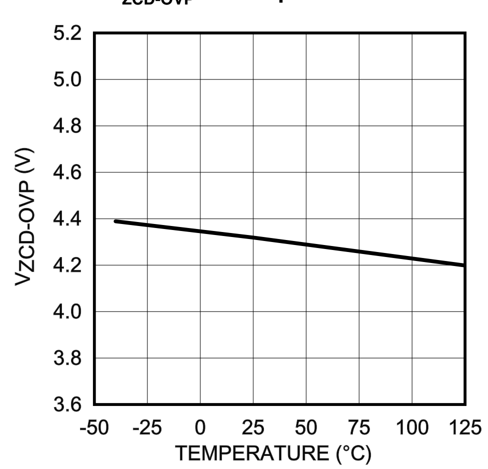
$V_{ZCD\text{-}OVP}$ vs Temperature



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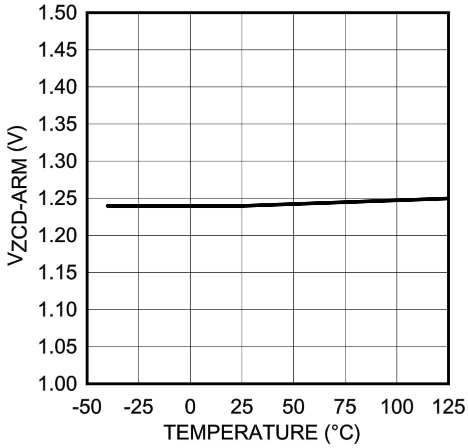
$V_{ZCD-ARM}$ vs Temperature



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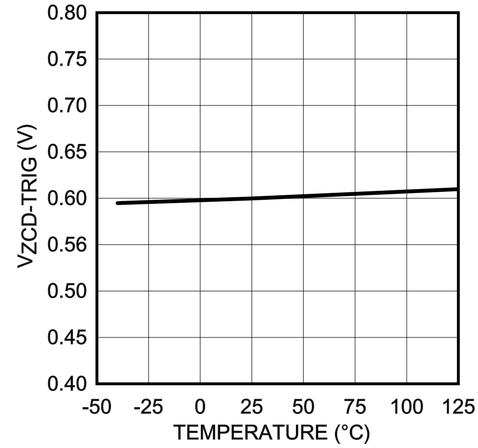
$V_{ZCD-TRIG}$ vs Temperature



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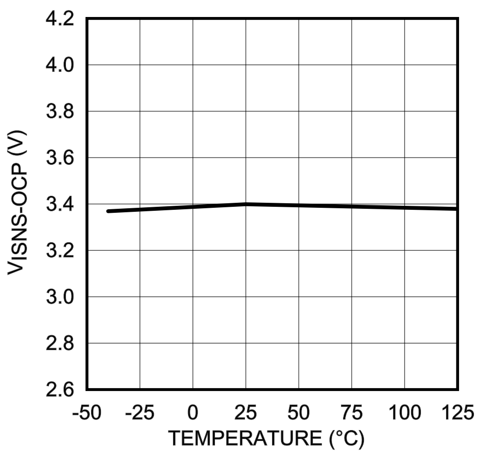
$V_{ISNS-OCP}$ (Isolated Mode) vs Temperature



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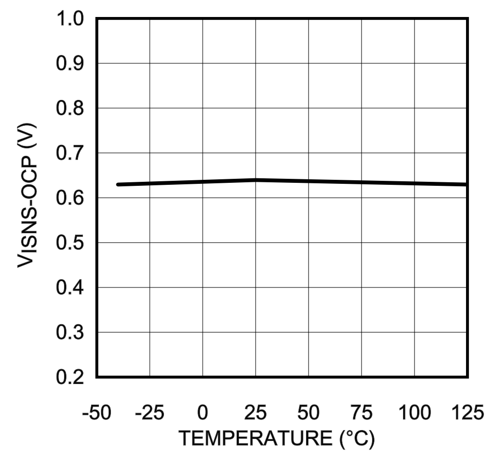
$V_{ISNS-OCP}$ (Non-Isolated Mode) vs Temperature



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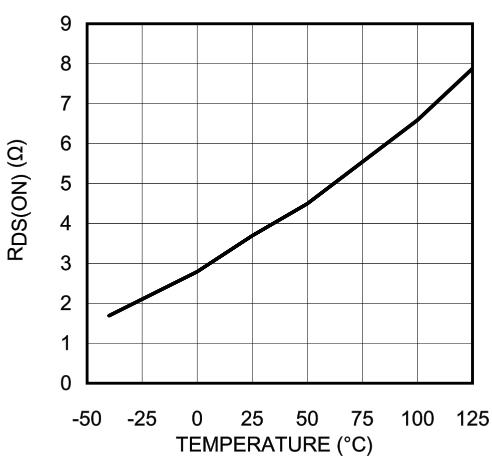
R_{DS} vs Temperature



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Simplified Internal Block Diagram

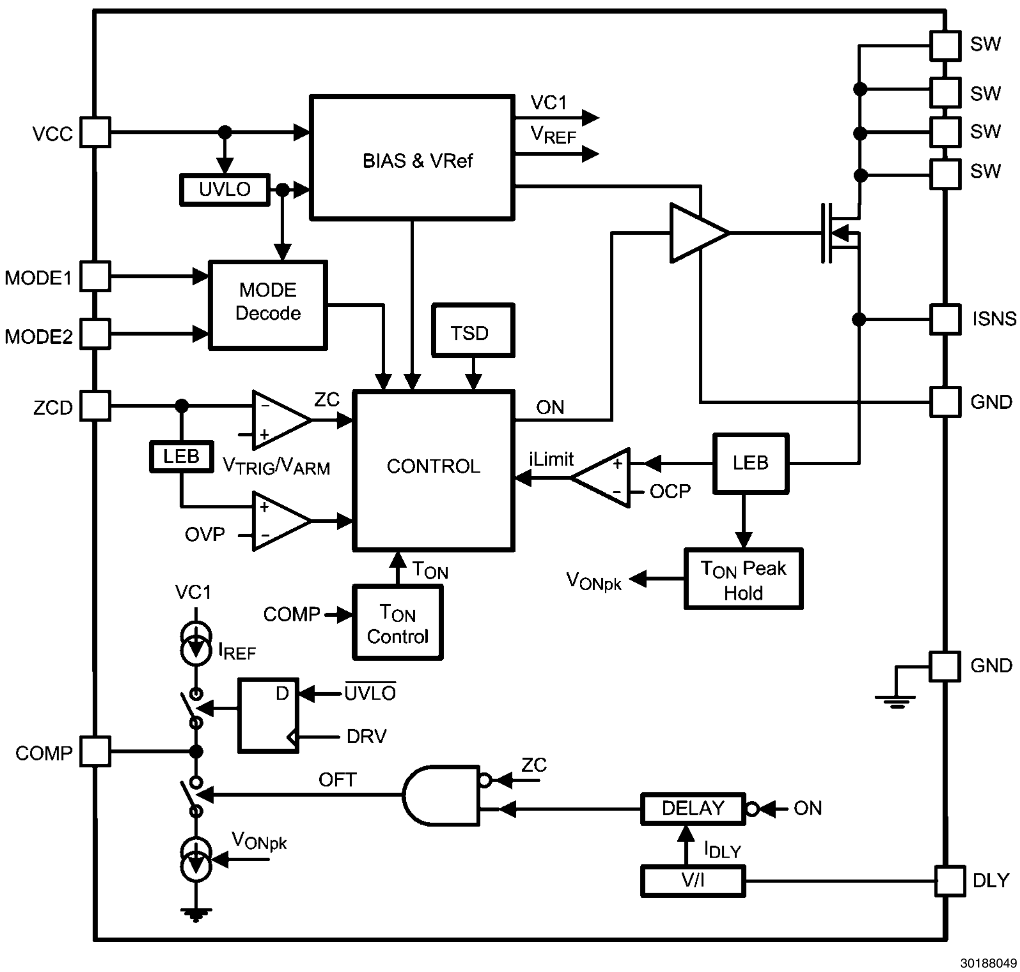


FIGURE 2. Simplified Block Diagram

Application Information

The TPS92311 is an off-line convertor specifically designed to drive LEDs. This device operates in Critical Conduction Mode (CRM) with adaptive Constant ON-Time control, so that high power factor can be achieved naturally. The TPS92311- can be configured as an isolated or non-isolated off-line converter. Please refer to TPS92311 typical schematic Figure 1, on the front page, in the following discussion. The TPS9231 flyback converter consists of a transformer which includes three windings L_P, L_S and L_{AUX}, an internal MOSFET Q_1 and inductor current sensing resistor R_{ISNS}. Secondary side components are secondary side transformer winding L_S, output diode D_3, and output capacitor C_{OUT}. An auxiliary winding is required, and serves two functions. Auxiliary power is developed from the winding to power the TPS92311 after start-up, and detect the zero crossing point due to the end of a complete switching cycle. During the on-period, Q_1 is turned on, and current flows through L_P, Q_1 and R_{ISNS} to ground, input energy is stored in the primary inductor L_P. Simultaneously, the I_{SNS} pin of the device monitors the voltage of the current sensing resistor R_{ISNS} to perform the cycle-by-cycle inductor current limit function. During the time MOSFET Q_1 is off, current flow in L_P ceases and the energy stored during the on cycle is released to output and auxiliary circuits. During Q_1 off-time current in the secondary winding $L_S$charges the output capacitor C_{OUT} through D_3 and supplies the LED load. During Q_1 on-time, C_{OUT} is responsible to supply load current to LED load during subsequent on-period. Also during Q_1 off-time current is delivered to the auxiliary winding through D_2 and powers the TPS92311. The voltage across L_{AUX}, V_{LAUX} is fed back to the ZCD pin through a resistor divider network formed by R_2 and R_3 to perform zero crossing detection of V_{LAUX}, which determines the end of the off-period of a switching cycle. The next on period of a new cycle will be initiated after an inserted delay of 2 x t_{DLY}. The t_{DLY} is programmable by a single resistor connecting the DLY pin and ground. The setting of the delay time, t_{DLY} will be described in a separate paragraph. During steady state operation, the duration of the on-period t_{ON} can be determined with two different modes: the Constant On-Time (COT) mode and the Peak Current Mode (PCM), which are configured by setting the MODE1 and MODE2 pins. For the COT mode, t_{ON} is generated by comparing an internal generated saw-tooth waveform with the voltage on the COMP pin (V_{COMP}). Since V_{COMP} is slow varying, t_{ON} is nearly constant within an AC line cycle. For the PCM, the on-period is terminated when the voltage of the ISNS pin (V_{ISNS}) reaches a threshold determined by V_{COMP}. Since the instantaneous input voltage (AC voltage) varies, t_{ON} varies accordingly within an AC line cycle. The duration of the off-period (t_{OFF}) is determined by the rate of discharging of the secondary current through the transformer. Also,

$$I_{LS\text{-}PEAK} = n \times I_{LP\text{-}PEAK}$$

where n is the turn ratio of L_P and L_S. Figure 3 shows the typical waveforms in normal operation.

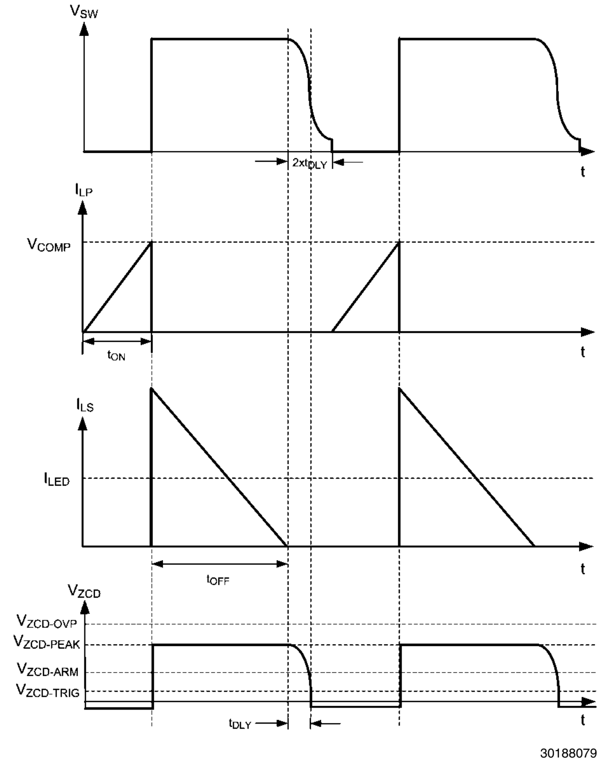


FIGURE 3. Primary and Secondary Side Current Waveforms

Startup Bias and UVLO

During startup, the TPS92311 is powered from the AC line through R_1 and D_1 (Figure 1). In the startup state, most of the internal circuits of the TPS92311 are shut down in order to minimize internal quiescent current. When V_{CC} reaches the rising threshold of the $V_{CC\text{-}UVLO}$ (typically 25.6V), the TPS92311 is operating in a low switching frequency mode, where t_{ON} and t_{OFF} are fixed to 1.5μs and 72μs. When $V_{ZCD\text{-}PEAK}$ is higher than $V_{ZCD\text{-}ARM}$, the TPS92311 enters normal operation.

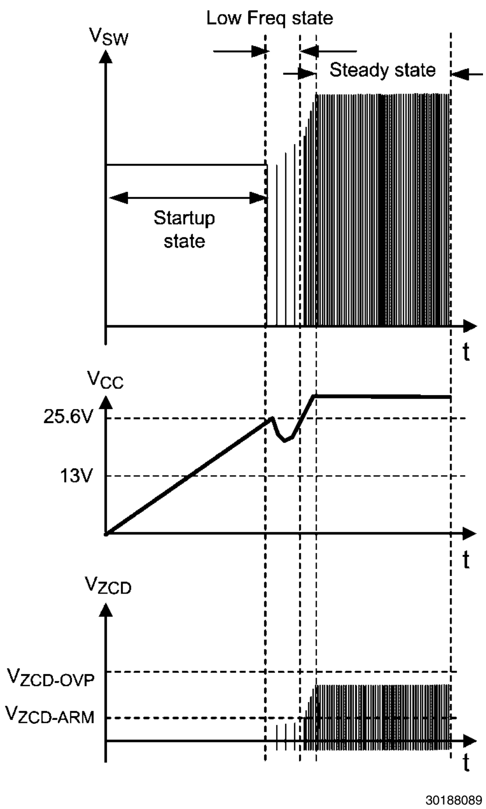


FIGURE 4. Start up Bias Waveforms

Mode Decoder

The TPS92311 is capable of operating in two control modes as an isolated topology, Peak Current Mode (PCM) or Constant On-Time (COT). The TPS92311 can also be configured in a non-isolated topology using COT operation. Depending on system requirements, the designer will chose between the two modes of operation. COT mode gives a high power factor, PCM can achieve a lower output current ripple. COT mode using a non-isolated topology can achieve a higher efficiency and good load regulation. The above modes can be selected by setting the MODE1 and MODE2 pins according to Table 1.

TABLE 1. MODE Configuration

MODE1	MODE2	Mode of operation
OPEN	OPEN	COT mode using isolated topology
GND	OPEN	PCM using isolated topology
OPEN	GND	COT mode using non-isolated topology
GND	GND	Reserved

Zero Crossing Detection

To minimized the switching loss of the internal power MOSFET, a zero crossing detection circuit is embedded in the TPS92311. V_{LAUX} is AC voltage coupled from V_{SW} by means of the transformer, with the lower part of the waveform clipped by D_{ZCD}. V_{LAUX} is fed back to the ZCD pin to detect a zero crossing point through a resistor divider network which consists of R_2 and R_3. The next turn on time of Q_1 is selected V_{SW} is the minimum, an instant corresponding to a small delay after the zero crossing occurs. (Figure 5) The actual delay time depends on the drain capacitance of the Q_1 and the primary inductance of the transformer (L_P). Such delay time is set by a single external resistor as described in Delay Setting section.

During the off-period at steady state, V_{ZCD} reaches its maximum $V_{ZCD-PEAK}$ (Figure 3), which is scalable by the turn ratio of the transformer and the resistor divider network R_2 and R_3. It is recommended that $V_{ZCD-PEAK}$ is set to 3V during normal operation.

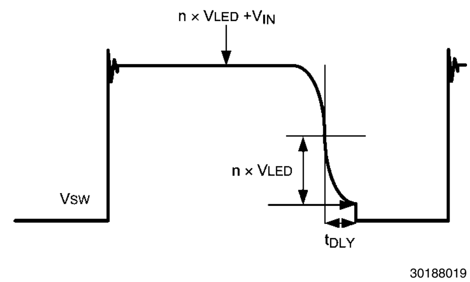


FIGURE 5. Switching Node Waveforms

Delay Time Setting

In order to reduce EMI and switching loss, the TPS92311 inserts a delay between the off-period and the on-period. The delay time is set by a single resistor which connects across the DLY pin and ground, and their relationship is shown in Figure 6. The optimal delay time depends on the resonance frequency between L_P and the drain to source capacitance of Q_1 (C_{DS}). Circuit designers should optimize the delay time according to the following equation.

$$f_{SW} = \frac{1}{2\pi\sqrt{L_P C_{DS}}}$$

$$t_{DLY} = \frac{\pi\sqrt{L_P C_{DS}}}{2}$$

After determining the delay time, t_{DLY} can be implemented by setting R_{DLY} according to the following equation:

$$R_{DLY} = K_{DLY}(t_{DLY} - 105\text{ns})$$

where K_{DLY} = 32MΩ/ns is a constant.

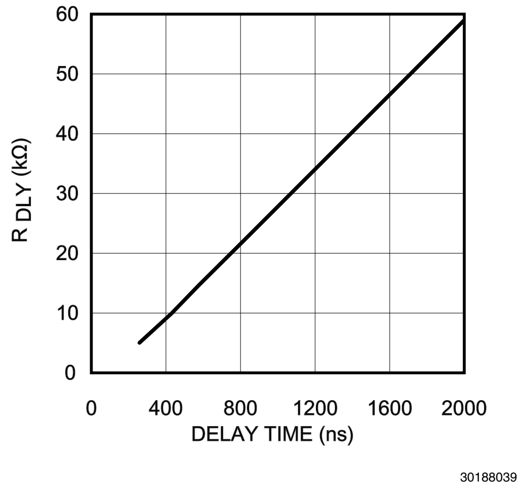


FIGURE 6. Delay Time Setting

Protection Features

OUTPUT OPEN CIRCUIT PROTECTION

If the LED string is disconnected from the output of the TPS92311, The output voltage (V_{LED}) increases and thus $V_{ZCD\text{-}PEAK}$ increases. When $V_{ZCD\text{-}PEAK}$ is greater than $V_{ZCD\text{-}OVP}$ for 3 continues switching cycles, the Over Voltage Protection (OVP) feature is triggered. Switching of Q_1 is stopped, and V_{CC} decreases until it drops below the falling threshold of $V_{CC\text{-}UVLO}$, the TPS92311 restarts, and re-enter into startup state (Figure 8).

OUTPUT SHORT CIRCUIT PROTECTION

If the LED string is shorted, $V_{ZCD\text{-}PEAK}$ drops, and as $V_{ZCD\text{-}PEAK}$ drops below $V_{ZCD\text{-}TRIG}$, the TPS92311 will enter low switching frequency operation. During low switching frequency operation, power supplied from L_{AUX} to V_{CC} is not enough to maintain V_{CC}. If the short remains V_{CC} will drop below the falling threshold of $V_{CC\text{-}UVLO}$, the TPS92311 will attempt to restart at this time (Figure 7). When the short is removed the TPS92311 will restore to steady state operation.

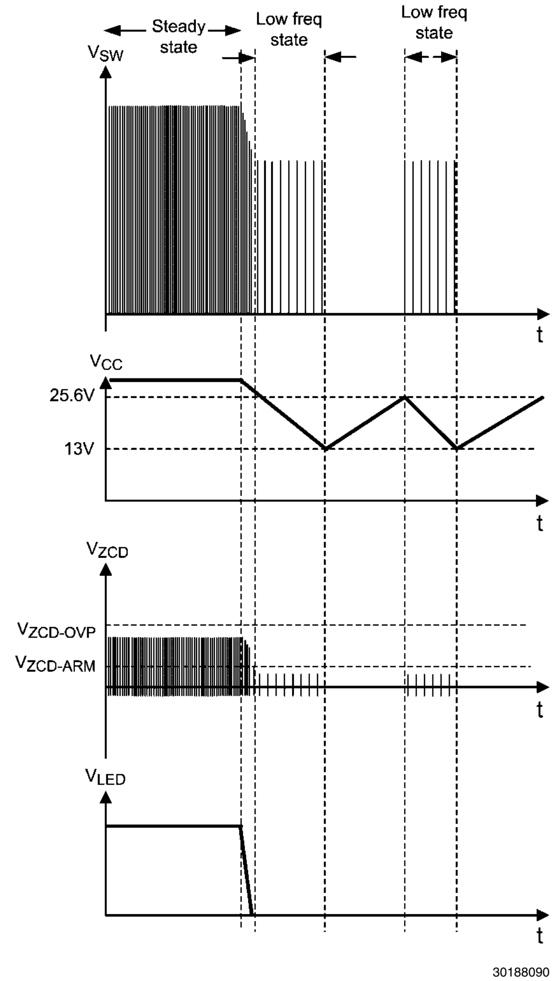


FIGURE 7. Output Short Circuit waveforms

OVER CURRENT PROTECTION

Over Current Protection (OCP) limits the drain current of internal MOSFET and prevents inductor / transformer saturation. When V_{ISNS} reaches a threshold, the OCP is triggered and the internal MOSFET will turn off immediately. The threshold is typically 3.4V and 0.64V when the TPS92311 is using an isolated topology and a non-isolated topology respectively.

THERMAL PROTECTION

Thermal protection is implemented by an internal thermal shutdown circuit, which activates at 160°C (typically). In this case, the internal switching power MOSFET will turn off. Capacitor C_{VCC} will discharge until UVLO. When the junction temperature of the TPS92311 falls back below 130°C, the TPS92311 resumes normal operation.

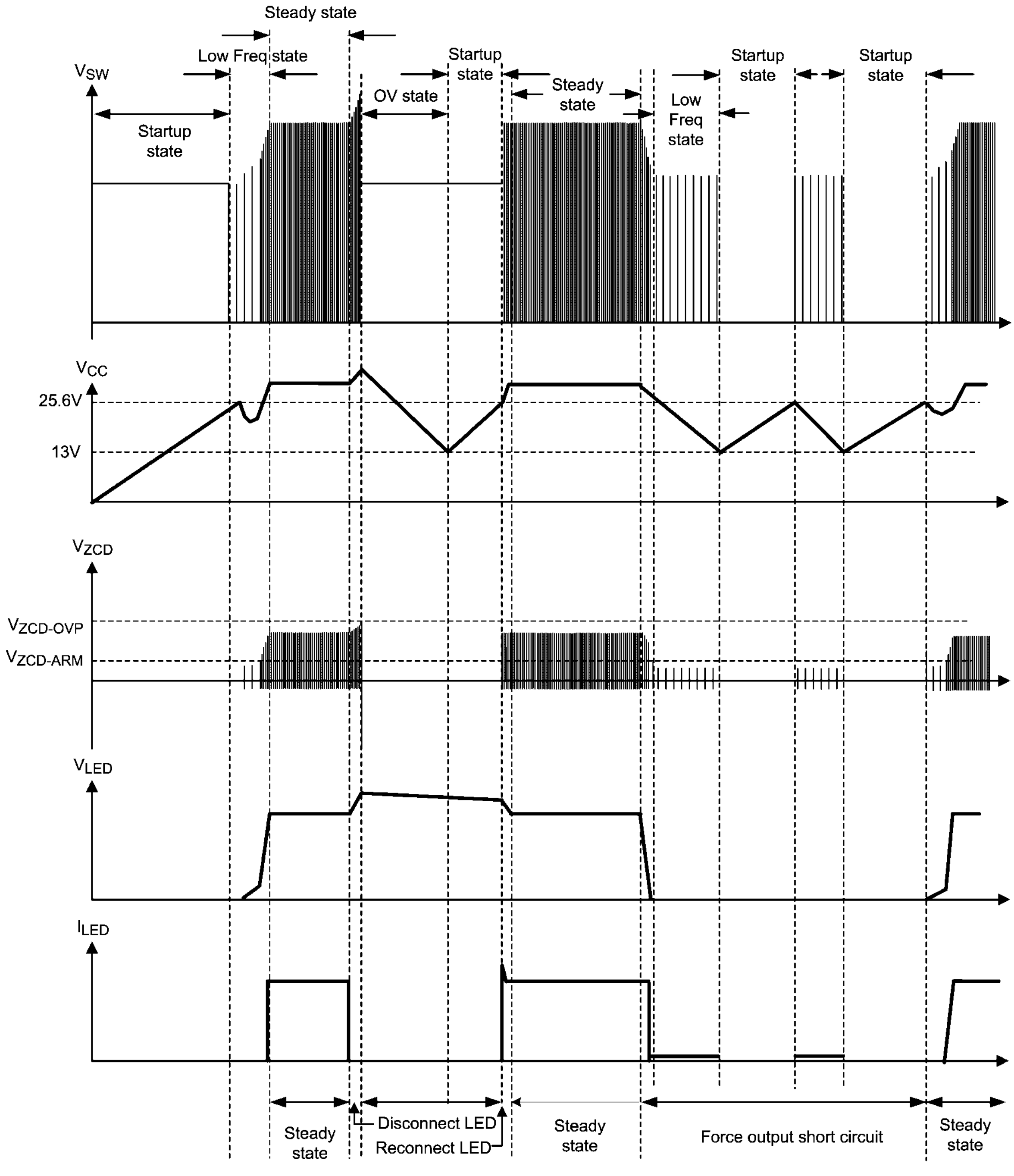


FIGURE 8. Auto Restart Operation

Design Example

The following design example illustrates the procedures to calculate the external component values for the TPS92311 isolated single stage fly-back LED driver with PFC.

Design Specifications:

Input voltage range, V_{AC_RMS} = 85VAC – 132VAC

Nominal input voltage, $V_{AC\_RMS(NOM)}$ = 110VAC

Number of LED in serial =7

LED current, I_{LED} = 350mA

Forward voltage drop of single LED = 3.0V

Forward voltage of LED stack, V_{LED} = 21V

Key operating Parameters:

Converter minimum switching frequency, f_{SW} = 75kHz

Output rectifier maximum reverse voltage, $V_{D3(MAX)}$ = 100V

Power MOSFET rating, $V_{Q1(MAX)}$ = 600V (3.75Ω)

Power MOSFET Output Capacitance, C_{DS} = 37pF (estimated)

Nominal output power, P_{OUT} = 8W

START UP BIAS RESISTOR

During start up, the V_{CC} will be powered by the rectified line voltage through external resistor, R_1. The V_{CC} start up current, $I_{VCC(SU)}$ must set in the range $I_{VCC(MIN)} > I_{VCC(SU)} > I_{STARTUP(MAX)}$ to ensure proper restart operation during OVP fault. In this example, a value of 0.55mA is suggested. The resistance of R_1 can be calculated by dividing the nominal input voltage in RMS by the start up current suggested.

So, R_1 = 110V/0.55mA = 200KΩ is recommended.

TRANSFORMER TURN RATIO

The transformer winding turn ratio, n is governed by the internal MOSFET Q1 maximum rated voltage, ($V_{Q3(MAX)}$), highest line input peak voltage ($V_{AC\text{-}PEAK}$) and output diode maximum reverse voltage rating ($V_{D3(MAX)}$). The output diode rating limits the lower bound of the turn ratio and the internal power MOSFET rating provide the upper bound of the turn ratio. The transformer turn ratio must be selected in between the bounds. If the maximum reverse voltage of D3 ($V_{D3(MAX)}$) is 100V. the minimum transformer turn ratio can be calculated with the equation in below.

$$n > \frac{V_{AC\text{-}PEAK}}{\left(V_{D3(MAX)} - V_{LED}\right)}$$

$$n > \frac{132 x \sqrt{2}}{100-30} = 2.33$$

In operation, the voltage at the switching node, V_{SW} must be small than the internal MOSFET maximum rated voltage $V_{Q1(MAX)}$, For reason of safety, 10% safety margin is recommended. Hence, 90% of $V_{Q1(MAX)}$ is used in the following equation.

$$n < \frac{V_{Q1(MAX)} x 0.9 - V_{AC\text{-}PEAK} - V_{os}}{V_{LED(MAX)}}$$

$$n < \frac{600 x 0.9 - 132\sqrt{2} - 50}{30} = 12.1$$

where V_{OS} is the maximum switching node overshoot voltage allowed, in this example, 50V is assumed. As a rule of thumb, lower turn ratio of transformer can provide a better line regulation and lower secondly side peak current. In here, turn ratio n = 3.8 is recommended.

SWITCHING FREQUENCY SELECTION

TPS92311 can operate at high switching frequency in the range of 60kHz to 150kHz. In most off-line applications, with considering of efficiency degradation and EMC requirements, the recommended switching frequency range will be 60kHz to 80kHz. In this design example, switching frequency at 75kHz is selected.

SWITCHING ON TIME

The maximum power switch on-time, t_{ON} depends on the low line condition of $85V_{AC}$. At $85V_{AC}$ the switching frequency was chosen at 75kHz. This transformer design will follow the formulae as shown below.

$$t_{ON} = \frac{1}{f_{sw}\left(\frac{V_{AC\_MIN\_PEAK}}{n x V_{LED}} + 1\right)}$$

$$t_{ON} = \frac{1}{75000\left(\frac{85\sqrt{2}}{3.8 \text{ x } 21} + 1\right)} = 5.3\,\mu s$$

TRANSFORMER PRIMARY INDUCTANCE

The primary inductance, L_P of the transformer is related to the minimum operating switching frequency f_{SW}, converter output power P_{OUT}, system efficiency η and minimum input line voltage $V_{AC\_RMS(MIN)}$. For CRM operation, the output power, P_{OUT} can be described by the equation in below.

$$P_{OUT} = \eta x \frac{1}{2} L_P x I_{LP\text{-}PEAK}{}^2 x f_{SW}$$

By re-arranging terms, the transformer primary inductance required in this design example can be calculated with the equation follows:

$$L_P = \frac{\eta x V_{AC\_RMS(MIN)}{}^2 t_{ON}{}^2}{2 x P_{OUT} x \frac{1}{f_{sw}}}$$

The converter minimum switching frequency is 75kHz, t_{ON} is 5.3µs, $V_{AC\_RMS(MIN)}$ = 85V and P_{OUT} = 8W, assume the system efficiency, η = 85%. Then,

$$L_P = \frac{0.85 x (85)^2 x (5.3\mu)^2}{2x8x13.3\mu} = 0.81mH$$

From the calculation in above, the inductance of the primary winding required is 0.81mH.

Calculate The Current Sensing Resistor

After the primary inductance and transformer turn ratio is determined, the current sensing resistor, R_{ISNS} can be calculated.

The resistance for R_{ISNS} is governed by the output current and transformer turn ratio, the equation in below can be used.

$$R_{ISNS} = n \times \left(\frac{V_{REF}}{I_{LED}}\right)$$

where V_{REF} is fixed to 0.14V internally.

Transformer turn ratio, $N_P : N_S$ is 3.8 : 1 and I_{LED} = 0.35A

$$R_{ISNS} = 3.8 \times \frac{0.14}{0.35} = 1.52\,\Omega$$

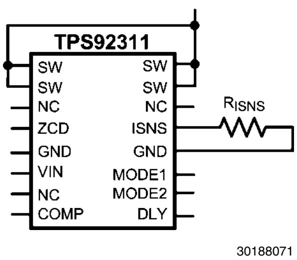


FIGURE 9. R_{ISNS} Resistor Interface

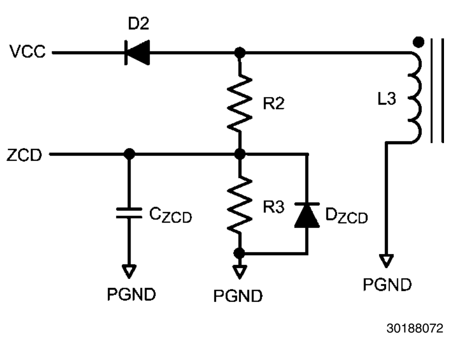


FIGURE 10. Auxiliary Winding Interface to ZCD

Auxiliary Winding Interface To ZCD

In Figure 10, R2 and R3 forms a resistor divider which sets the thresholds for over voltage protection of $V_{LED,}$ $V_{ZCD\text{-}OVP}$, and $V_{ZCD\text{-}PEAK}$. Before the calculation, we need to set the voltage of the auxiliary winding, V_{LAUX} at open circuit.

For example :

Assume the nominal forward voltage of LED stack (V_{LED}) is 21V.

To avoid false triggering ZCD_{OVP} voltage threshold at normal operation, select ZCD_{OVP} voltage at 1.3 times of the V_{LED} is typical in most applications. In case the transformer leakage is higher, the ZCD_{OVP} threshold can be set to 1.5 times of the V_{LED}.

In this design example, open circuit AUX winding OVP voltage threshold is set to 30V. Assume the current through the AUX winding is 0.4mA typical.

As a result, R2 is 66kΩ and R3 is 11kΩ. Also, for suppressing high frequency noise at the ZCD pin, a 15pF capacitor connects the ZCD pin to ground is recommended.

Auxiliary Winding V_{cc} Diode Selection

The VCC diode D2 provides the supply current to the converter, low temperature coefficient , low reverse leakage and ultra fast diode is recommended.

Compensation Capacitor And Delay Timer Resistor Selection

To achieve PFC function with a constant on time flyback converter, a low frequency response loop is required. In most applications, a 3.3µF C_{COMP} capacitor is suitable for compensation.

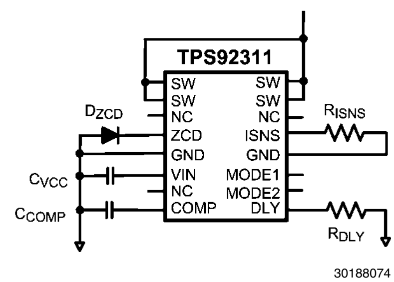


FIGURE 11. Compensation and DLY Timer connection

The resistor R_{DLY} connecting the DLY pin to ground is used to set the delay time between the ZCD trigger to power MOSFET turn on. The delay time required can be calculated with the parasitic capacitance at the drain of MOSFET to ground and primary inductance of the transformer. Equation in below can be used to find the delay time and Figure 6 in previous page can help to find the resistance once the delay time is calculated

$$t_{DLY} = \frac{\pi\sqrt{L_P C_{DS}}}{2}$$

For example, using a transformer with primary inductance L_P = 1mH, and power MOSFET drain to ground capacitor C_{DS}=37pF, the t_{DLY} can be calculated by the upper equation. As a result, t_{DLY}=302ns and R_{DLY} is 6.31kΩ. The delay time may need to change according to the primary inductance of the transformer. The typical level of output current will shift if inappropriate delay time is chosen.

Output Flywheel Diode Selection

To increase the overall efficiency of the system, a low forward voltage schottky diode with appropriate rating should be used.

Primary Side Snubber Design

The leakage inductance can induce a high voltage spike when power MOSFET is turned off. Figure 12 illustrate the operation waveform. A voltage clamp circuit is required to protect the power MOSFET. The voltage of snubber clamp (V_{SN}) must be higher than the sum of over shoot voltage (V_{OS}), LED open load voltage multiplied by the transformer turn ratio (n). In this examples, the V_{OS} is 50V and LED maximum voltage,

$V_{LED(MAX)}$ is 30V, transformer turn ratio is 3.8. The snubber voltage required can be calculated with following equations.

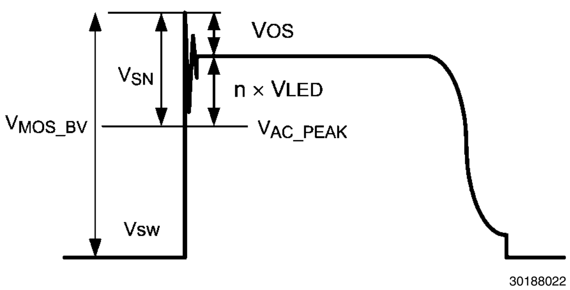


FIGURE 12. Snubber Waveform

$$V_{SN} > V_{OS} + V_{LED(MAX)} \text{ x } n$$

where n is the turn ratio of the transformer.

$$V_{SN} > 50V + 30V \times 3.8 = 164V$$

At the same time, sum of the snubber clamp voltage and V_{AC} peak voltage (V_{AC_PEAK}) must be smaller than the MOSFET breakdown voltage (V_{MOS_BV}). By re-arranging terms, equation in below can be used.

$$V_{SN} < V_{MOS\_BV} - V_{AC}\sqrt{2}$$

$$V_{SN} < 600 - 132 \times \sqrt{2} = 414V$$

In here, snubber clamp voltage, V_{SN} = 250V is recommended.

Output Capacitor

The capacitance of the output capacitor is determined by the equivalent series resistance (ESR) of the LED, R_{LED} and the ripple current allowed for the application. The equation in below can be used to calculate the required capacitance.

$$C_{OUT} = \frac{\sqrt{\left(2\frac{I_{LED}}{\Delta I_{LED}}\right)^2 - 1}}{4 \text{ x } \pi \text{x} f_{AC} R_{LED}}$$

Assume the ESR of the LED stack contains 7 LEDs and is 2.6Ω, AC line frequency f_{AC} is 60Hz.

In this example, LED current I_{LED} is 350mA and output ripple current is 30% of I_{LED}:

$$C_{OUT} = \frac{\sqrt{\left(\frac{2x0.35}{0.3x0.35}\right)^2 - 1}}{4x\pi x60x7x2.6}$$

Then, C_{OUT} = 480µF.

In here, a 470µF output capacitor with 10µF ceramic capacitor in parallel is suggested.

PCB Layout Considerations

The performance of any switching power supplies depend as much upon the layout of the PCB as the component selection. Good layout practices are important when constructing the PCB. The layout must be as neat and compact as possible, and all external components must be as close as possible to their associated pins. High current return paths and signal return paths must be separated and connect together at single ground point. All high current connections must be as short and direct as possible with thick traces. The SW pin of the internal MOSFET should be connected close to the transformer pin with short and thick trace to reduce potential electro-magnetic interference. For off-line applications, one more consideration is the safety requirements. The clearance and creepage to high voltage traces must be complied to all applicable safety regulations.

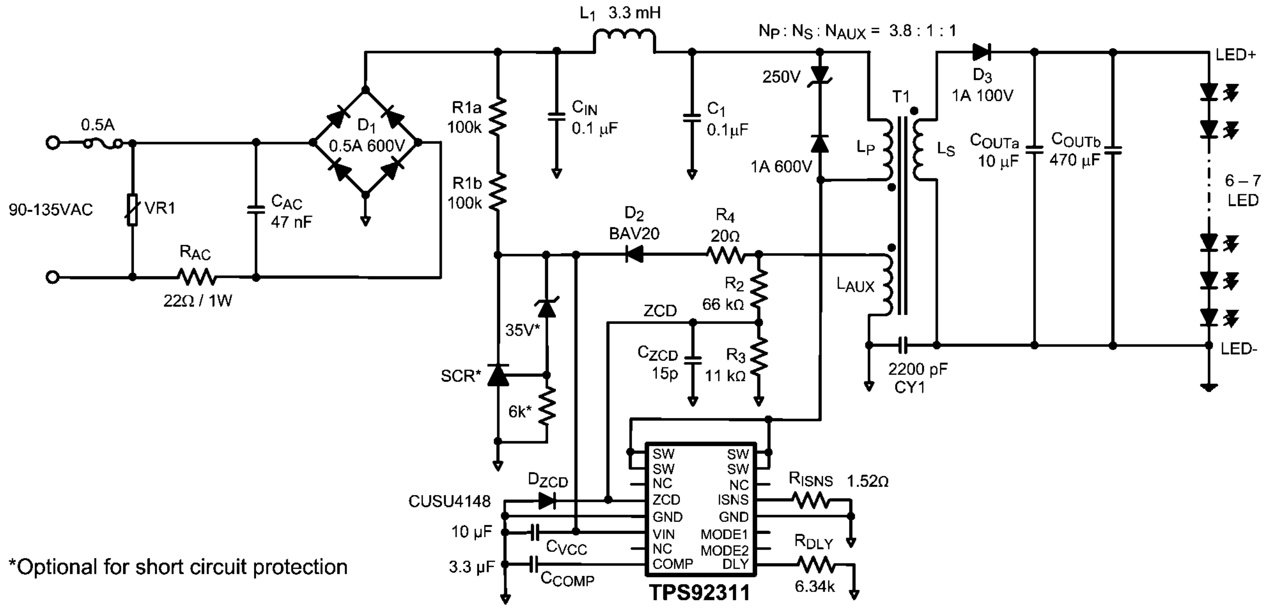


FIGURE 13. Isolated topology schematic

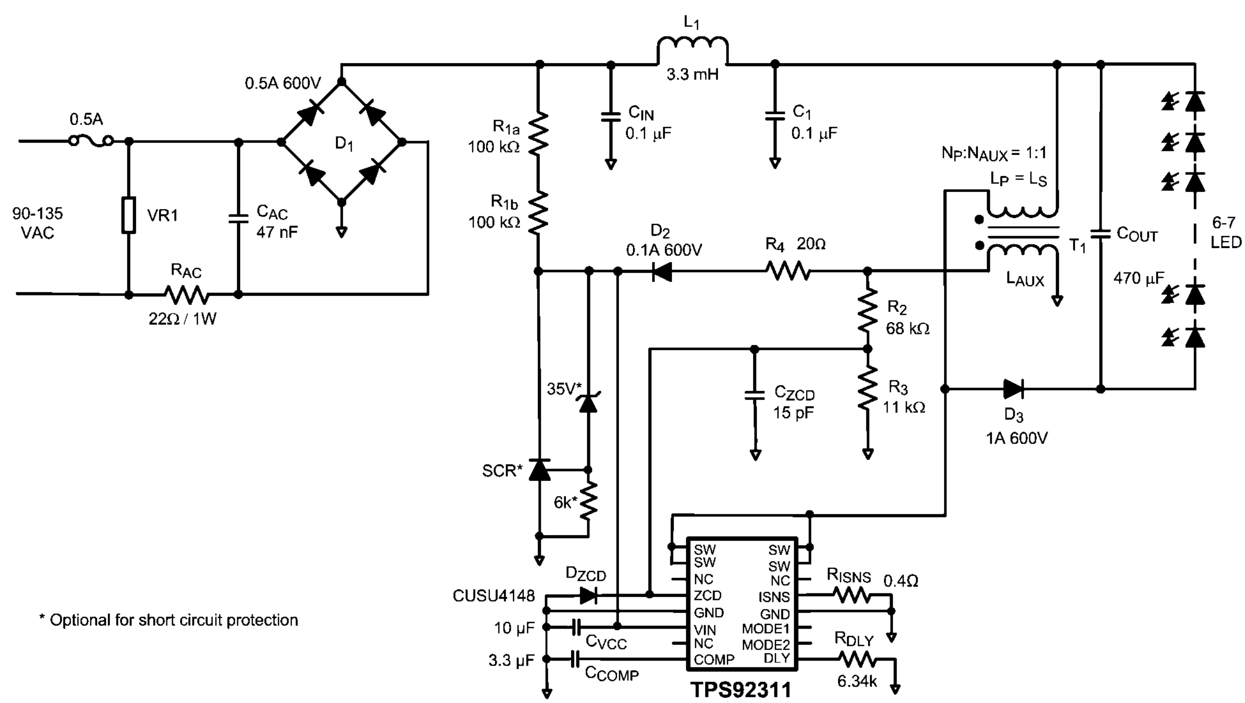
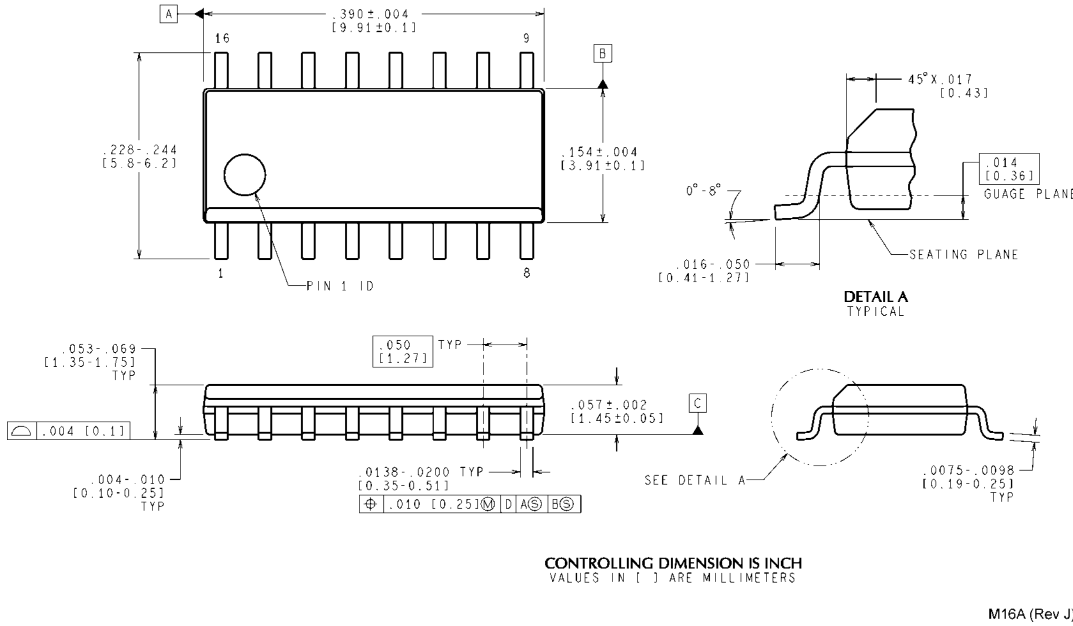


FIGURE 14. Non-isolated topology schematic

Physical Dimensions inches (millimeters) unless otherwise noted



MSOP-16 Pin Package (mm)
For Ordering, Refer to Ordering Information Table
NS Package Number M16A

Notes

Notes

IMPORTANT NOTICE