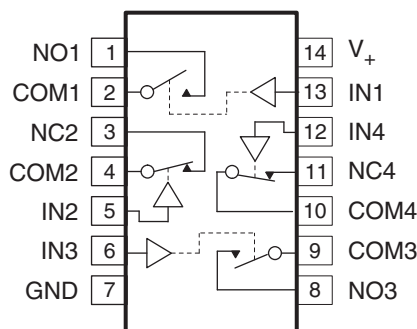


## LOW ON-STATE RESISTANCE QUAD SPST CMOS ANALOG SWITCHES

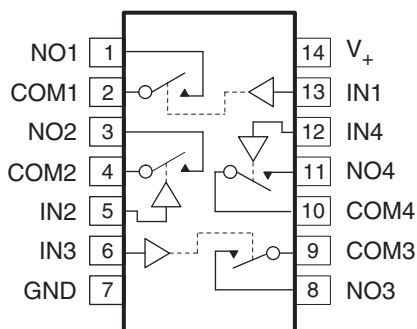
### FEATURES

- 2-V to 12-V Single-Supply Operation
- Specified ON-State Resistance:
  - 15  $\Omega$  Max With 12-V Supply
  - 20  $\Omega$  Max With 5-V Supply
  - 50  $\Omega$  Max With 3.3-V Supply
- $R_{DS(ON)}$  Matching
  - 2.5  $\Omega$  (Max) at 12 V
  - 3  $\Omega$  (Max) at 5 V
  - 3.5  $\Omega$  (Max) at 3.3 V
- Specified Low OFF-Leakage Currents:
  - 1 nA at 25°C
  - 10 nA at 85°C
- Specified Low ON-Leakage Currents:
  - 1 nA at 25°C
  - 10 nA at 85°C
- Low Charge Injection: 11.5 pC (12-V Supply)
- Fast Switching Speed:
  - $t_{ON} = 80$  ns,  $t_{OFF} = 50$  ns (12-V Supply)
- Break-Before-Make Operation ( $t_{ON} > t_{OFF}$ )
- TTL/CMOS-Logic Compatible With 5-V Supply
- Available in TSSOP-14 Package, SOIC-14

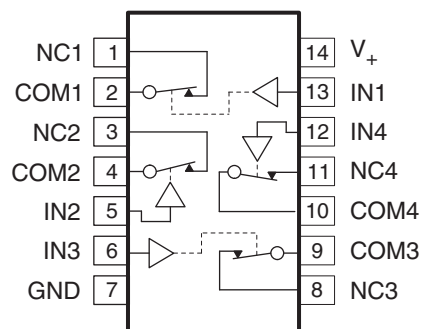
D OR PW PACKAGE...TS12A44513  
(TOP VIEW)



D OR PW PACKAGE...TS12A44514  
(TOP VIEW)



D OR PW PACKAGE...TS12A44515  
(TOP VIEW)



### DESCRIPTION/ORDERING INFORMATION

The TS12A44513/TS12A44514/TS12A44515 are quad single pole/single throw (SPST), low-voltage / wide range, single-supply CMOS analog switches, with very low switch ON-state resistance. The TS12A44513 has two switches normally closed (NC) and two switches normally open (NO), the TS12A44514 switches are normally open (NO), the TS12A44515 switches are normally closed (NC).

These CMOS switches can operate continuously with a single supply between 2 V and 12 V. Each switch can handle rail-to-rail analog signals. The OFF-leakage current maximum is only 1 nA at 25°C or 10 nA at 85°C.

All digital inputs have 0.8-V to 2.4-V logic thresholds, ensuring TTL/CMOS-logic compatibility when using a 5-V supply.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**ORDERING INFORMATION**

| $T_A$         | PACKAGE <sup>(1)(2)</sup> |              | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|---------------------------|--------------|-----------------------|------------------|
| –40°C to 85°C | SOIC – D                  | Reel of 2500 | TS12A44513DR          | TS12A44513       |
|               |                           | Reel of 2500 | TS12A44514DR          | TS12A44514       |
|               |                           | Reel of 2500 | TS12A44515DR          | TS12A44515       |
|               | TSSOP – PW                | Reel of 2000 | TS12A44513PWR         | YD4513           |
|               |                           | Reel of 2000 | TS12A44514PWR         | YD4514           |
|               |                           | Reel of 2000 | TS12A44515PWR         | YD4515           |

(1) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at [www.ti.com](http://www.ti.com).

**ABSOLUTE MINIMUM AND MAXIMUM RATINGS <sup>(1)(2)</sup>**

voltages referenced to GND

|                                                        |                                                          |                                                                                                       | MIN        | MAX                  | UNIT |
|--------------------------------------------------------|----------------------------------------------------------|-------------------------------------------------------------------------------------------------------|------------|----------------------|------|
| V <sub>+</sub>                                         | Supply voltage range                                     |                                                                                                       | −0.3       | 13                   | V    |
| V <sub>NC</sub><br>V <sub>NO</sub><br>V <sub>COM</sub> | Analog voltage range <sup>(3)</sup>                      |                                                                                                       | −0.3       | V <sub>+</sub> + 0.3 | V    |
| I <sub>NC</sub><br>I <sub>NO</sub><br>I <sub>COM</sub> | Analog Current range                                     |                                                                                                       | -20        | 20                   | mA   |
|                                                        | Continuous current into any terminal                     |                                                                                                       |            | ±20                  | mA   |
|                                                        | Peak current, NO or COM (pulsed at 1 ms, 10% duty cycle) |                                                                                                       |            | ±30                  | mA   |
|                                                        | ESD per method 3015.7                                    |                                                                                                       |            | 2000                 | V    |
| T <sub>A</sub>                                         | Operating temperature range                              |                                                                                                       | −40        | 85                   | °C   |
| P <sub>D</sub>                                         | Power dissipation                                        | Mounted on JEDEC 4-layer board (JESD 51-7), No airflow, T <sub>A</sub> = 25°C, T <sub>J</sub> = 125°C | D package  | 1.15                 | W    |
|                                                        |                                                          |                                                                                                       | PW package | 0.88                 |      |
| T <sub>stg</sub>                                       | Storage temperature range                                |                                                                                                       | −65        | 150                  | °C   |
|                                                        | Lead temperature (soldering, 10 s)                       |                                                                                                       |            | 300                  | °C   |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(3) Voltages exceeding  $V_+$  or GND on any signal terminal are clamped by internal diodes. Limit forward-diode current to maximum current rating.

**THERMAL IMPEDANCE**

|               |                                            |                                                           |            | UNIT |      |
|---------------|--------------------------------------------|-----------------------------------------------------------|------------|------|------|
| $\theta_{JA}$ | Thermal impedance,<br>junction to free air | Mounted on JEDEC 1-layer board (JESD 51-3),<br>No airflow | D package  | 133  | °C/W |
|               |                                            |                                                           | PW package | 167  |      |
|               |                                            | Mounted on JEDEC 4-layer board (JESD 51-7),<br>No airflow | D package  | 86   |      |
|               |                                            |                                                           | PW package | 112  |      |

**ELECTRICAL CHARACTERISTICS FOR 5-V SUPPLY<sup>(1)</sup>**
 $V_+ = 4.5 \text{ V to } 5.5 \text{ V}$ ,  $V_{\text{INH}} = 2.4 \text{ V}$ ,  $V_{\text{INL}} = 0.8 \text{ V}$ ,  $T_A = -40^\circ\text{C to } 85^\circ\text{C}$  (unless otherwise noted)

| PARAMETER                                                    | SYMBOL                                               | TEST CONDITIONS                                                                                   | T <sub>A</sub>                       | MIN  | TYP <sup>(2)</sup> | MAX            | UNIT |
|--------------------------------------------------------------|------------------------------------------------------|---------------------------------------------------------------------------------------------------|--------------------------------------|------|--------------------|----------------|------|
| Analog Switch                                                |                                                      |                                                                                                   |                                      |      |                    |                |      |
| Analog signal range                                          | V <sub>COM</sub> , V <sub>NO</sub> , V <sub>NC</sub> |                                                                                                   |                                      | 0    |                    | V <sub>+</sub> | V    |
| ON-state resistance                                          | r <sub>on</sub>                                      | V <sub>+</sub> = 4.5 V, V <sub>COM</sub> = 3.5 V, I <sub>COM</sub> = 1 mA                         | 25°C                                 | 12   | 20                 | Ω              |      |
|                                                              |                                                      |                                                                                                   | Full                                 |      | 30                 |                |      |
| ON-state resistance flatness                                 | r <sub>on(flat)</sub>                                | V <sub>COM</sub> = 1 V, 2 V, 3 V, I <sub>COM</sub> = 1 mA                                         | 25°C                                 | 1    | 3                  | Ω              |      |
|                                                              |                                                      |                                                                                                   | Full                                 |      | 4                  |                |      |
| ON-state resistance matching between channels <sup>(3)</sup> | Δr <sub>on</sub>                                     | V <sub>+</sub> = 4.5 V, I <sub>COM</sub> = 5 mA, V <sub>NO</sub> or V <sub>NC</sub> = 3 V         | 25°C                                 |      | 3                  | Ω              |      |
|                                                              |                                                      |                                                                                                   | T <sub>MIN</sub> to T <sub>MAX</sub> |      | 4                  |                |      |
| NO, NC OFF leakage current <sup>(4)</sup>                    | I <sub>NO(OFF)</sub> , I <sub>NC(OFF)</sub>          | V <sub>+</sub> = 5.5 V, V <sub>COM</sub> = 1 V, V <sub>NO</sub> or V <sub>NC</sub> = 4.5 V        | 25°C                                 |      | 1                  | nA             |      |
|                                                              |                                                      |                                                                                                   | Full                                 |      | 10                 |                |      |
| COM OFF leakage current <sup>(4)</sup>                       | I <sub>COM(OFF)</sub>                                | V <sub>+</sub> = 5.5 V, V <sub>COM</sub> = 1 V, V <sub>NO</sub> or V <sub>NC</sub> = 4.5 V        | 25°C                                 |      | 1                  | nA             |      |
|                                                              |                                                      |                                                                                                   | Full                                 |      | 10                 |                |      |
| COM ON leakage current <sup>(4)</sup>                        | I <sub>COM(ON)</sub>                                 | V <sub>+</sub> = 5.5 V, V <sub>COM</sub> = 4.5 V, V <sub>NO</sub> or V <sub>NC</sub> = 4.5 V      | 25°C                                 |      | 1                  | nA             |      |
|                                                              |                                                      |                                                                                                   | Full                                 |      | 10                 |                |      |
| Digital Control Input (IN)                                   |                                                      |                                                                                                   |                                      |      |                    |                |      |
| Input logic high                                             | V <sub>IH</sub>                                      |                                                                                                   | Full                                 | 2.4  |                    | V <sub>+</sub> | V    |
| Input logic low                                              | V <sub>IL</sub>                                      |                                                                                                   | Full                                 | 0    |                    | 0.8            | V    |
| Input leakage current                                        | I <sub>IH</sub> , I <sub>IL</sub>                    | V <sub>IN</sub> = V <sub>+</sub> , 0 V                                                            | Full                                 |      |                    | 0.01           | μA   |
| Dynamic                                                      |                                                      |                                                                                                   |                                      |      |                    |                |      |
| Turn-on time                                                 | t <sub>ON</sub>                                      | see <a href="#">Figure 6</a>                                                                      | 25°C                                 | 45   | 100                | ns             |      |
|                                                              |                                                      |                                                                                                   | Full                                 |      | 125                |                |      |
| Turn-off time                                                | t <sub>OFF</sub>                                     | see <a href="#">Figure 6</a>                                                                      | 25°C                                 | 35   | 50                 | ns             |      |
|                                                              |                                                      |                                                                                                   | Full                                 |      | 70                 |                |      |
| Charge injection <sup>(5)</sup>                              | Q <sub>C</sub>                                       | C <sub>L</sub> = 1 nF, V <sub>NO</sub> = 0 V, R <sub>S</sub> = 0 Ω, See <a href="#">Figure 5</a>  | 25°C                                 | –1.5 |                    | pC             |      |
| NO, NC OFF capacitance                                       | C <sub>NO(OFF)</sub> , C <sub>NC(OFF)</sub>          | f = 1 MHz, See <a href="#">Figure 8</a>                                                           | 25°C                                 | 8    |                    | pF             |      |
| COM OFF capacitance                                          | C <sub>COM(OFF)</sub>                                | f = 1 MHz, See <a href="#">Figure 8</a>                                                           | 25°C                                 | 8    |                    | pF             |      |
| COM ON capacitance                                           | C <sub>COM(ON)</sub>                                 | f = 1 MHz, See <a href="#">Figure 8</a>                                                           | 25°C                                 | 19   |                    | pF             |      |
| Digital input capacitance                                    | C <sub>I</sub>                                       | V <sub>IN</sub> = V <sub>+</sub> , 0 V                                                            | 25°C                                 | 2    |                    | pF             |      |
| Bandwidth                                                    | BW                                                   | R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 15 pF, V <sub>NO</sub> = 1 V <sub>RMS</sub> , f = 100 kHz | 25°C                                 | 530  |                    | MHz            |      |
| OFF isolation                                                | O <sub>ISO</sub>                                     | R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 15 pF, V <sub>NO</sub> = 1 V <sub>RMS</sub> , f = 100 kHz | 25°C                                 | –94  |                    | dB             |      |
| Total harmonic distortion                                    | THD                                                  | R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 15 pF, V <sub>NO</sub> = 1 V <sub>RMS</sub> , f = 100 kHz | 25°C                                 | 0.09 |                    | %              |      |
| Supply                                                       |                                                      |                                                                                                   |                                      |      |                    |                |      |
| V <sub>+</sub> supply current                                | I <sub>+</sub>                                       | V <sub>IN</sub> = 0 V or V <sub>+</sub>                                                           | 25°C                                 |      | 0.05               | μA             |      |
|                                                              |                                                      |                                                                                                   | Full                                 |      | 0.1                |                |      |

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

(2) Typical values are at  $T_A = 25^\circ\text{C}$ .

(3)  $\Delta r_{\text{ON}} = r_{\text{ON(MAX)}} - r_{\text{ON(MIN)}}$ 

(4) Leakage parameters are 100% tested at maximum-rated hot operating temperature, and are ensured by correlation at 25°C.

(5) Specified by design, not production tested

**ELECTRICAL CHARACTERISTICS FOR 12-V SUPPLY<sup>(1)</sup>**
 $V_+ = 11.4\text{ V to }12.6\text{ V}$ ,  $V_{INH} = 5\text{ V}$ ,  $V_{INL} = 0.8\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

| PARAMETER                                                    | SYMBOL                                               | TEST CONDITIONS                                                                                   | T <sub>A</sub>                       | MIN | TYP <sup>(2)</sup> | MAX            | UNIT |
|--------------------------------------------------------------|------------------------------------------------------|---------------------------------------------------------------------------------------------------|--------------------------------------|-----|--------------------|----------------|------|
| Analog Switch                                                |                                                      |                                                                                                   |                                      |     |                    |                |      |
| Analog signal range                                          | V <sub>COM</sub> , V <sub>NO</sub> , V <sub>NC</sub> |                                                                                                   |                                      | 0   |                    | V <sub>+</sub> | V    |
| ON-state resistance                                          | r <sub>on</sub>                                      | V <sub>+</sub> = 11.4 V, V <sub>COM</sub> = 10 V, I <sub>COM</sub> = 1 mA                         | 25°C                                 | 6.5 | 10                 |                | Ω    |
|                                                              |                                                      |                                                                                                   | Full                                 |     | 15                 |                |      |
| ON-state resistance flatness                                 | r <sub>on(flat)</sub>                                | V <sub>+</sub> = 11.4 V, V <sub>COM</sub> = 2 V, 5 V, 10 V, I <sub>COM</sub> = 1 mA               | 25°C                                 | 1.5 | 3                  |                | Ω    |
|                                                              |                                                      |                                                                                                   | Full                                 |     | 4                  |                |      |
| ON-state resistance matching between channels <sup>(3)</sup> | Δr <sub>on</sub>                                     | V <sub>+</sub> = 11.4 V, I <sub>COM</sub> = 5 mA, V <sub>NO</sub> or V <sub>NC</sub> = 10 V       | 25°C                                 |     | 2.5                |                | Ω    |
|                                                              |                                                      |                                                                                                   | T <sub>MIN</sub> to T <sub>MAX</sub> |     | 3                  |                |      |
| NO, NC OFF leakage current <sup>(4)</sup>                    | I <sub>NO(OFF)</sub> , I <sub>NC(OFF)</sub>          | V <sub>+</sub> = 12.6 V, V <sub>COM</sub> = 1 V, V <sub>NO</sub> or V <sub>NC</sub> = 10 V        | 25°C                                 |     | 1                  |                | nA   |
|                                                              |                                                      |                                                                                                   | Full                                 |     | 10                 |                |      |
| COM OFF leakage current <sup>(4)</sup>                       | I <sub>COM(OFF)</sub>                                | V <sub>+</sub> = 12.6 V, V <sub>COM</sub> = 1 V, V <sub>NO</sub> or V <sub>NC</sub> = 10 V        | 25°C                                 |     | 1                  |                | nA   |
|                                                              |                                                      |                                                                                                   | Full                                 |     | 10                 |                |      |
| COM ON leakage current <sup>(4)</sup>                        | I <sub>COM(ON)</sub>                                 | V <sub>+</sub> = 12.6 V, V <sub>COM</sub> = 10 V, V <sub>NO</sub> or V <sub>NC</sub> = 10 V       | 25°C                                 |     | 1                  |                | nA   |
|                                                              |                                                      |                                                                                                   | Full                                 |     | 10                 |                |      |
| Digital Control Input (IN)                                   |                                                      |                                                                                                   |                                      |     |                    |                |      |
| Input logic high                                             | V <sub>IH</sub>                                      |                                                                                                   | Full                                 | 5   |                    | V <sub>+</sub> | V    |
| Input logic low                                              | V <sub>IL</sub>                                      |                                                                                                   | Full                                 | 0   |                    | 0.8            | V    |
| Input leakage current                                        | I <sub>IH</sub> , I <sub>IL</sub>                    | V <sub>IN</sub> = V <sub>+</sub> , 0 V                                                            | Full                                 |     |                    | 0.001          | μA   |
| Dynamic                                                      |                                                      |                                                                                                   |                                      |     |                    |                |      |
| Turn-on time                                                 | t <sub>ON</sub>                                      | See <a href="#">Figure 6</a>                                                                      | 25°C                                 | 25  | 75                 |                | ns   |
|                                                              |                                                      |                                                                                                   | Full                                 |     | 80                 |                |      |
| Turn-off time                                                | t <sub>OFF</sub>                                     | See <a href="#">Figure 6</a>                                                                      | 25°C                                 | 20  | 45                 |                | ns   |
|                                                              |                                                      |                                                                                                   | Full                                 |     | 50                 |                |      |
| Charge injection <sup>(5)</sup>                              | Q <sub>C</sub>                                       | C <sub>L</sub> = 1 nF, V <sub>NO</sub> = 0 V, R <sub>S</sub> = 0 Ω, See <a href="#">Figure 5</a>  | 25°C                                 |     | −10.5              |                | pC   |
| NO, NC OFF capacitance                                       | C <sub>NO(OFF)</sub> , C <sub>NC(OFF)</sub>          | f = 1 MHz, See <a href="#">Figure 8</a>                                                           | 25°C                                 |     | 8                  |                | pF   |
| COM OFF capacitance                                          | C <sub>COM(OFF)</sub>                                | f = 1 MHz, See <a href="#">Figure 8</a>                                                           | 25°C                                 |     | 8                  |                | pF   |
| COM ON capacitance                                           | C <sub>COM(ON)</sub>                                 | f = 1 MHz, See <a href="#">Figure 8</a>                                                           | 25°C                                 |     | 21.5               |                | pF   |
| Digital input capacitance                                    | C <sub>I</sub>                                       | V <sub>IN</sub> = V <sub>+</sub> , 0 V                                                            | 25°C                                 |     | 2                  |                | pF   |
| Bandwidth                                                    | BW                                                   | R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 15 pF, V <sub>NO</sub> = 1 V <sub>RMS</sub> , f = 100 kHz | 25°C                                 |     | 530                |                | MHz  |
| OFF isolation                                                | O <sub>ISO</sub>                                     | R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 15 pF, V <sub>NO</sub> = 1 V <sub>RMS</sub> , f = 100 kHz | 25°C                                 |     | −95                |                | dB   |
| Total harmonic distortion                                    | THD                                                  | R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 15 pF, V <sub>NO</sub> = 1 V <sub>RMS</sub> , f = 100 kHz | 25°C                                 |     | 0.07               |                | %    |
| Supply                                                       |                                                      |                                                                                                   |                                      |     |                    |                |      |
| V <sub>+</sub> supply current                                | I <sub>+</sub>                                       | V <sub>IN</sub> = 0 V or V <sub>+</sub>                                                           | 25°C                                 |     | 0.05               |                | μA   |
|                                                              |                                                      |                                                                                                   | Full                                 |     | 0.2                |                |      |

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

(2) Typical values are at  $T_A = 25^\circ\text{C}$ .(3)  $\Delta r_{ON} = r_{ON(MAX)} - r_{ON(MIN)}$ (4) Leakage parameters are 100% tested at maximum-rated hot operating temperature, and are ensured by correlation at  $25^\circ\text{C}$ .

(5) Specified by design, not production tested

**ELECTRICAL CHARACTERISTICS FOR 3-V SUPPLY<sup>(1)</sup>**
 $V_+ = 3\text{ V to }3.6\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

| PARAMETER                                                    | SYMBOL                                               | TEST CONDITIONS                                                                                      | T <sub>A</sub>                       | MIN | TYP <sup>(2)</sup> | MAX            | UNIT |
|--------------------------------------------------------------|------------------------------------------------------|------------------------------------------------------------------------------------------------------|--------------------------------------|-----|--------------------|----------------|------|
| Analog Switch                                                |                                                      |                                                                                                      |                                      |     |                    |                |      |
| Analog signal range                                          | V <sub>COM</sub> , V <sub>NO</sub> , V <sub>NC</sub> |                                                                                                      |                                      | 0   |                    | V <sub>+</sub> | V    |
| ON-state resistance                                          | r <sub>on</sub>                                      | V <sub>+</sub> = 3 V, V <sub>COM</sub> = 1.5 V,<br>I <sub>NO</sub> = 1 mA,                           | 25°C                                 |     | 20                 | 40             | Ω    |
|                                                              |                                                      |                                                                                                      | Full                                 |     |                    | 50             |      |
| ON-state resistance flatness                                 | r <sub>on(flat)</sub>                                | V <sub>+</sub> = 3 V,<br>V <sub>COM</sub> = 1 V, 1.5 V, 2 V,<br>I <sub>COM</sub> = 1 mA              | 25°C                                 |     | 1                  | 3              | Ω    |
|                                                              |                                                      |                                                                                                      | Full                                 |     |                    | 4              |      |
| ON-state resistance matching between channels <sup>(3)</sup> | Δr <sub>on</sub>                                     | V <sub>+</sub> = 2.7 V, I <sub>COM</sub> = 5 mA,<br>V <sub>NO</sub> or V <sub>NC</sub> = 1.5 V       | 25°C                                 |     |                    | 3.5            | Ω    |
|                                                              |                                                      |                                                                                                      | T <sub>MIN</sub> to T <sub>MAX</sub> |     |                    | 4.5            |      |
| NO, NC OFF leakage current <sup>(4)</sup>                    | I <sub>NO(OFF)</sub> ,<br>I <sub>NC(OFF)</sub>       | V <sub>+</sub> = 3.6 V, V <sub>COM</sub> = 1 V,<br>V <sub>NO</sub> or V <sub>NC</sub> = 3 V          | 25°C                                 |     |                    | 1              | nA   |
|                                                              |                                                      |                                                                                                      | Full                                 |     |                    | 10             |      |
| COM OFF leakage current <sup>(4)</sup>                       | I <sub>COM(OFF)</sub>                                | V <sub>+</sub> = 3.6 V, V <sub>COM</sub> = 1 V,<br>V <sub>NO</sub> or V <sub>NC</sub> = 3 V          | 25°C                                 |     |                    | 1              | nA   |
|                                                              |                                                      |                                                                                                      | Full                                 |     |                    | 10             |      |
| COM ON leakage current <sup>(4)</sup>                        | I <sub>COM(ON)</sub>                                 | V <sub>+</sub> = 3.6 V, V <sub>COM</sub> = 3 V,<br>V <sub>NO</sub> or V <sub>NC</sub> = 3 V          | 25°C                                 |     |                    | 1              | nA   |
|                                                              |                                                      |                                                                                                      | Full                                 |     |                    | 10             |      |
| Digital Control Input (IN)                                   |                                                      |                                                                                                      |                                      |     |                    |                |      |
| Input logic high                                             | V <sub>IH</sub>                                      |                                                                                                      | Full                                 |     | 2.4                | V <sub>+</sub> | V    |
| Input logic low                                              | V <sub>IL</sub>                                      |                                                                                                      | Full                                 |     | 0                  | 0.8            | V    |
| Input leakage current                                        | I <sub>IH</sub> , I <sub>IL</sub>                    | V <sub>IN</sub> = V <sub>+</sub> , 0 V                                                               | Full                                 |     |                    | 0.01           | μA   |
| Dynamic                                                      |                                                      |                                                                                                      |                                      |     |                    |                |      |
| Turn-on time <sup>(5)</sup>                                  | t <sub>ON</sub>                                      | See <a href="#">Figure 6</a>                                                                         | 25°C                                 |     | 70                 | 120            | ns   |
|                                                              |                                                      |                                                                                                      | Full                                 |     |                    | 175            |      |
| Turn-off time <sup>(5)</sup>                                 | t <sub>OFF</sub>                                     | See <a href="#">Figure 6</a>                                                                         | 25°C                                 |     | 50                 | 80             | ns   |
|                                                              |                                                      |                                                                                                      | Full                                 |     |                    | 120            |      |
| Charge injection <sup>(5)</sup>                              | Q <sub>C</sub>                                       | C <sub>L</sub> = 1 nF, See <a href="#">Figure 5</a>                                                  | 25°C                                 |     | −0.5               |                | pC   |
| NO, NC OFF capacitance                                       | C <sub>NO(OFF)</sub> ,<br>C <sub>NC(OFF)</sub>       | f = 1 MHz, See <a href="#">Figure 8</a>                                                              | 25°C                                 |     | 8                  |                | pF   |
| COM OFF capacitance                                          | C <sub>COM(OFF)</sub>                                | f = 1 MHz, See <a href="#">Figure 8</a>                                                              | 25°C                                 |     | 8                  |                | pF   |
| COM ON capacitance                                           | C <sub>COM(ON)</sub>                                 | f = 1 MHz, See <a href="#">Figure 8</a>                                                              | 25°C                                 |     | 17                 |                | pF   |
| Digital input capacitance                                    | C <sub>I</sub>                                       | V <sub>IN</sub> = V <sub>+</sub> , 0 V                                                               | 25°C                                 |     | 2                  |                | pF   |
| Bandwidth                                                    | BW                                                   | R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 15 pF,<br>V <sub>NO</sub> = 1 V <sub>RMS</sub> , f = 100 kHz | 25°C                                 |     | 510                |                | MHz  |
| OFF isolation                                                | O <sub>ISO</sub>                                     | R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 15 pF,<br>V <sub>NO</sub> = 1 V <sub>RMS</sub> , f = 100 kHz | 25°C                                 |     | −94                |                | dB   |
| Total harmonic distortion                                    | THD                                                  | R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 15 pF,<br>V <sub>NO</sub> = 1 V <sub>RMS</sub> , f = 100 kHz | 25°C                                 |     | 0.27               |                | %    |
| Supply                                                       |                                                      |                                                                                                      |                                      |     |                    |                |      |
| V <sub>+</sub> supply current                                | I <sub>+</sub>                                       | V <sub>IN</sub> = 0 V or V <sub>+</sub>                                                              | 25°C                                 |     |                    | 0.03           | μA   |
|                                                              |                                                      |                                                                                                      | Full                                 |     |                    | 0.05           |      |

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

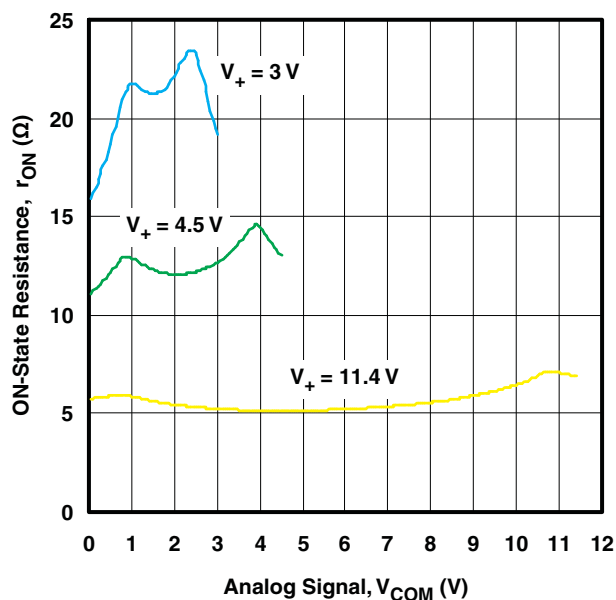
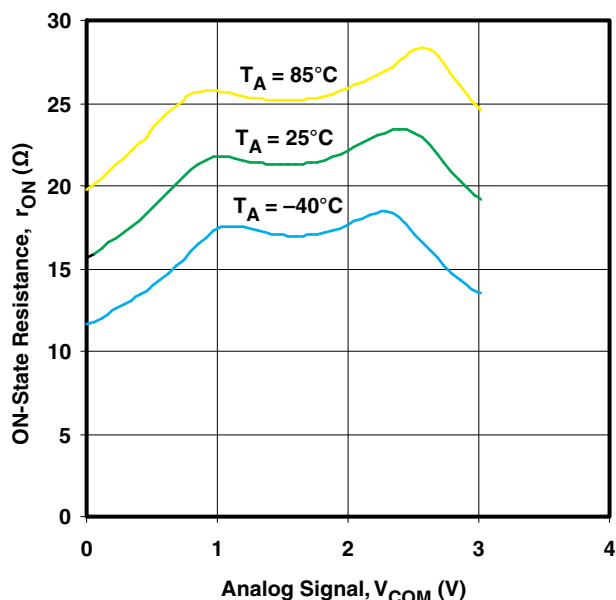
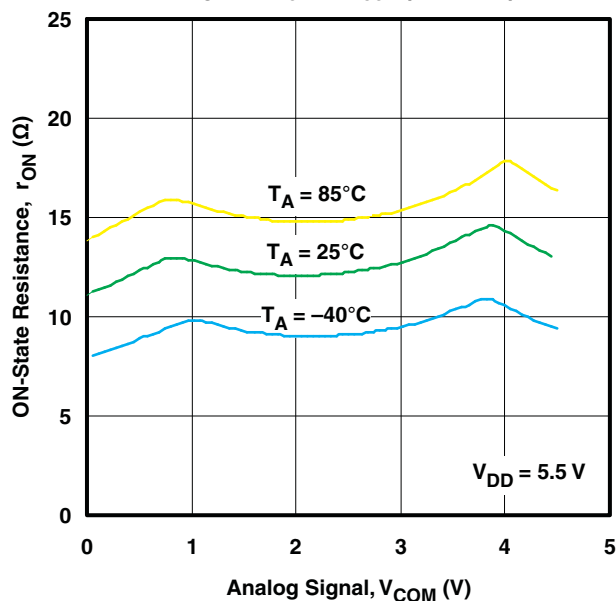
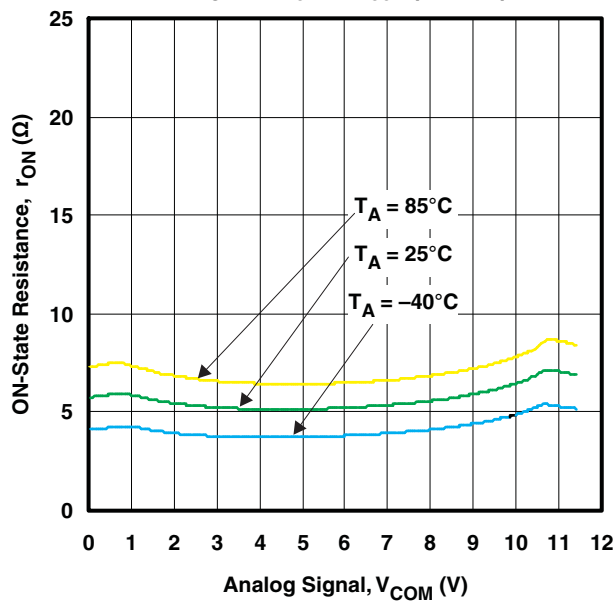
(2) Typical values are at  $T_A = 25^\circ\text{C}$ .

(3)  $\Delta r_{\text{ON}} = r_{\text{ON(MAX)}} - r_{\text{ON(MIN)}}$ 

(4) Leakage parameters are 100% tested at maximum-rated hot operating temperature, and are ensured by correlation at 25°C.

(5) Specified by design, not production tested

## TYPICAL PERFORMANCE

Figure 1.  $r_{ON}$  vs  $V_{COM}$  ( $T_A = 25^\circ\text{C}$ )Figure 2.  $r_{ON}$  vs  $V_{COM}$  ( $V_+ = 3\text{ V}$ )Figure 3.  $r_{ON}$  vs  $V_{COM}$  ( $V_+ = 4.5\text{ V}$ )Figure 4.  $r_{ON}$  vs  $V_{COM}$  ( $V_+ = 11.4\text{ V}$ )

**PIN DESCRIPTION<sup>(1)</sup>**

| PIN NO.         |              |              | NAME           | DESCRIPTION                                |
|-----------------|--------------|--------------|----------------|--------------------------------------------|
| TS12A44513      | TS12A44514   | TS12A44515   |                |                                            |
| <b>TSSOP-14</b> |              |              |                |                                            |
| 2, 4, 9, 10     | 2, 4, 9, 10  | 2, 4, 9, 10  | COM            | Common                                     |
| 14              | 14           | 14           | V <sub>+</sub> | Power supply                               |
| 5, 6, 12, 13    | 5, 6, 12, 13 | 5, 6, 12, 13 | IN             | Digital control to connect COM to NO or NC |
| 7               | 7            | 7            | GND            | Digital ground                             |
| 1, 8            | 1, 3, 8, 11  | –            | NO             | Normally open                              |
| 3, 11           | –            | 1, 3, 8, 11  | NC             | Normally closed                            |

(1) NO, NC, and COM pins are identical and interchangeable. Any may be considered as an input or an output; signals pass in both directions.

## APPLICATION INFORMATION

### Power-Supply Considerations

The TS12A44513/TS12A44514/TS12A44515 construction is typical of most CMOS analog switches, except that they have only two supply pins:  $V_+$  and GND.  $V_+$  and GND drive the internal CMOS switches and set their analog voltage limits. Reverse ESD-protection diodes connected in series are internally connected between each analog-signal pin and both  $V_+$  and GND. If an analog signal exceeds  $V_+$  or GND, one of the diodes will be forward biased, but the other will be reverse biased preventing current flow.

Virtually all the analog leakage current comes from the ESD diodes to  $V_+$  or GND. Although the ESD diodes on a given signal pin are identical and, therefore, fairly well balanced, they are reverse biased differently. Each is biased by either  $V_+$  or GND and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the  $V_+$  and GND pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity.

There is no connection between the analog-signal paths and  $V_+$  or GND.

$V_+$  and GND also power the internal logic and logic-level translators. The logic-level translators convert the logic levels to switched  $V_+$  and GND signals to drive the analog signal gates.

### Logic-Level Thresholds

The logic-level thresholds are CMOS/TTL compatible when  $V_+$  is 5 V. As  $V_+$  is raised, the level threshold increases slightly. When  $V_+$  reaches 12 V, the level threshold is about 3 V – above the TTL-specified high-level minimum of 2.8 V, but still compatible with CMOS outputs.

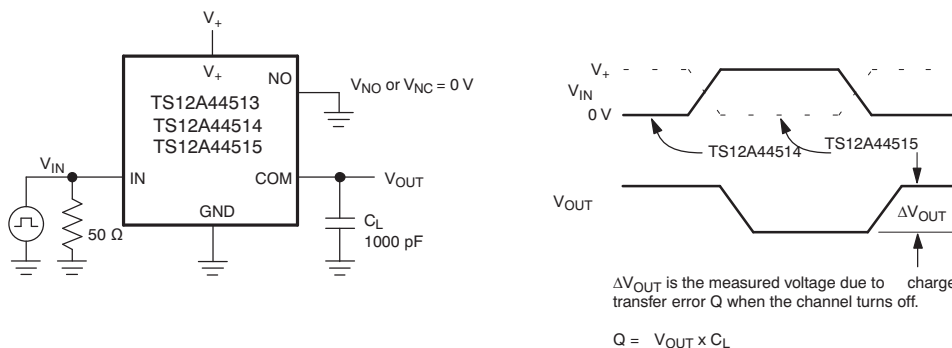
#### CAUTION:

**Do not connect the TS12A44513/TS12A44514/MAS4515  $V_+$  to 3 V and then connect the logic-level pins to logic-level signals that operate from 5-V supply. Output levels can exceed 3 V and violate the absolute maximum ratings, damaging the part and/or external circuits.**

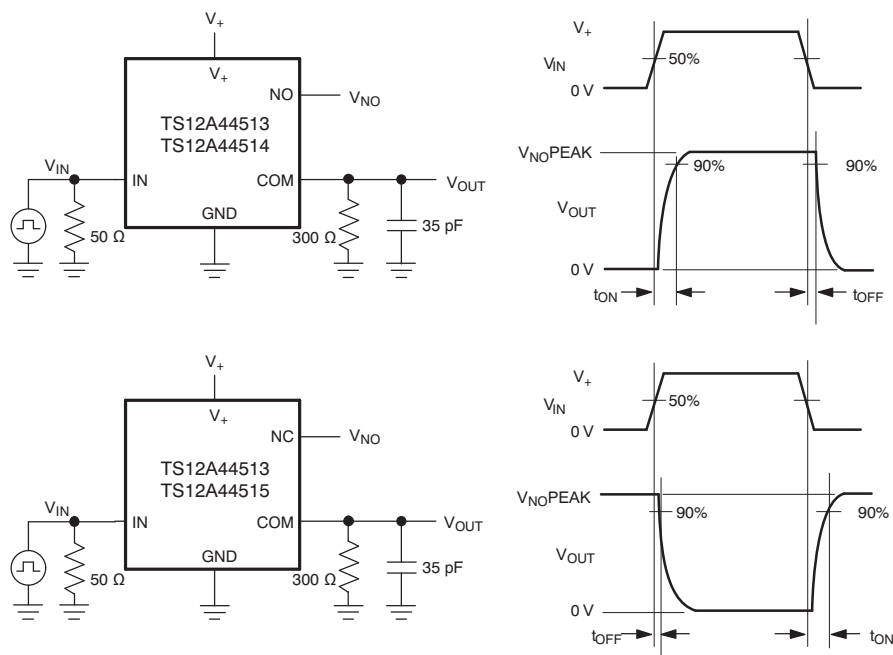
### High-Frequency Performance

In 50- $\Omega$  systems, signal response is reasonably flat up to 250 MHz (see *Typical Operating Characteristics*). Above 20 MHz, the on response has several minor peaks that are highly layout dependent. The problem is not in turning the switch on; it is turning it off. The OFF-state switch acts like a capacitor and passes higher frequencies with less attenuation. At 10 MHz, OFF isolation is about –45 dB in 50- $\Omega$  systems, decreasing (approximately 20 dB per decade) as frequency increases. Higher circuit impedances also make OFF isolation decrease. OFF isolation is about 3 dB above that of a bare IC socket, and is due entirely to capacitive coupling.

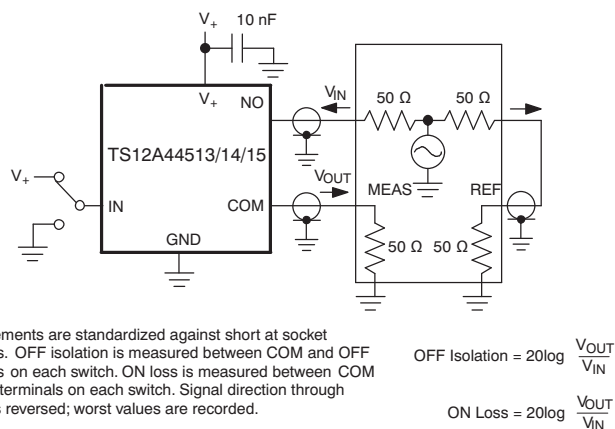
### Test Circuits/Timing Diagrams



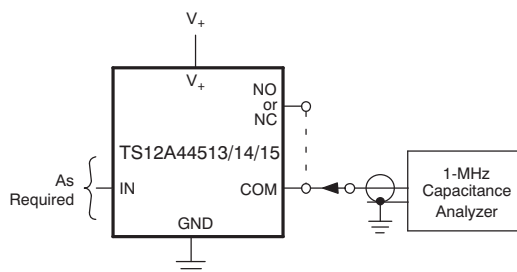
**Figure 5. Charge Injection**



**Figure 6. Switching Times**



**Figure 7. OFF Isolation and ON Loss**



**Figure 8. NO, NC, and COM Capacitance**

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| TS12A44513DR     | ACTIVE                | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| TS12A44513DRG4   | ACTIVE                | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| TS12A44513PWR    | ACTIVE                | TSSOP        | PW              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| TS12A44513PWRG4  | ACTIVE                | TSSOP        | PW              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| TS12A44514DR     | ACTIVE                | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| TS12A44514DRG4   | ACTIVE                | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| TS12A44514PWR    | ACTIVE                | TSSOP        | PW              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| TS12A44514PWRG4  | ACTIVE                | TSSOP        | PW              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| TS12A44515DR     | ACTIVE                | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| TS12A44515DRG4   | ACTIVE                | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| TS12A44515PWR    | ACTIVE                | TSSOP        | PW              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| TS12A44515PWRG4  | ACTIVE                | TSSOP        | PW              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TS12A44513DR  | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| TS12A44513PWR | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| TS12A44514DR  | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| TS12A44514PWR | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| TS12A44515DR  | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| TS12A44515PWR | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TS12A44513DR  | SOIC         | D               | 14   | 2500 | 346.0       | 346.0      | 33.0        |
| TS12A44513PWR | TSSOP        | PW              | 14   | 2000 | 346.0       | 346.0      | 29.0        |
| TS12A44514DR  | SOIC         | D               | 14   | 2500 | 346.0       | 346.0      | 33.0        |
| TS12A44514PWR | TSSOP        | PW              | 14   | 2000 | 346.0       | 346.0      | 29.0        |
| TS12A44515DR  | SOIC         | D               | 14   | 2500 | 346.0       | 346.0      | 33.0        |
| TS12A44515PWR | TSSOP        | PW              | 14   | 2000 | 346.0       | 346.0      | 29.0        |

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



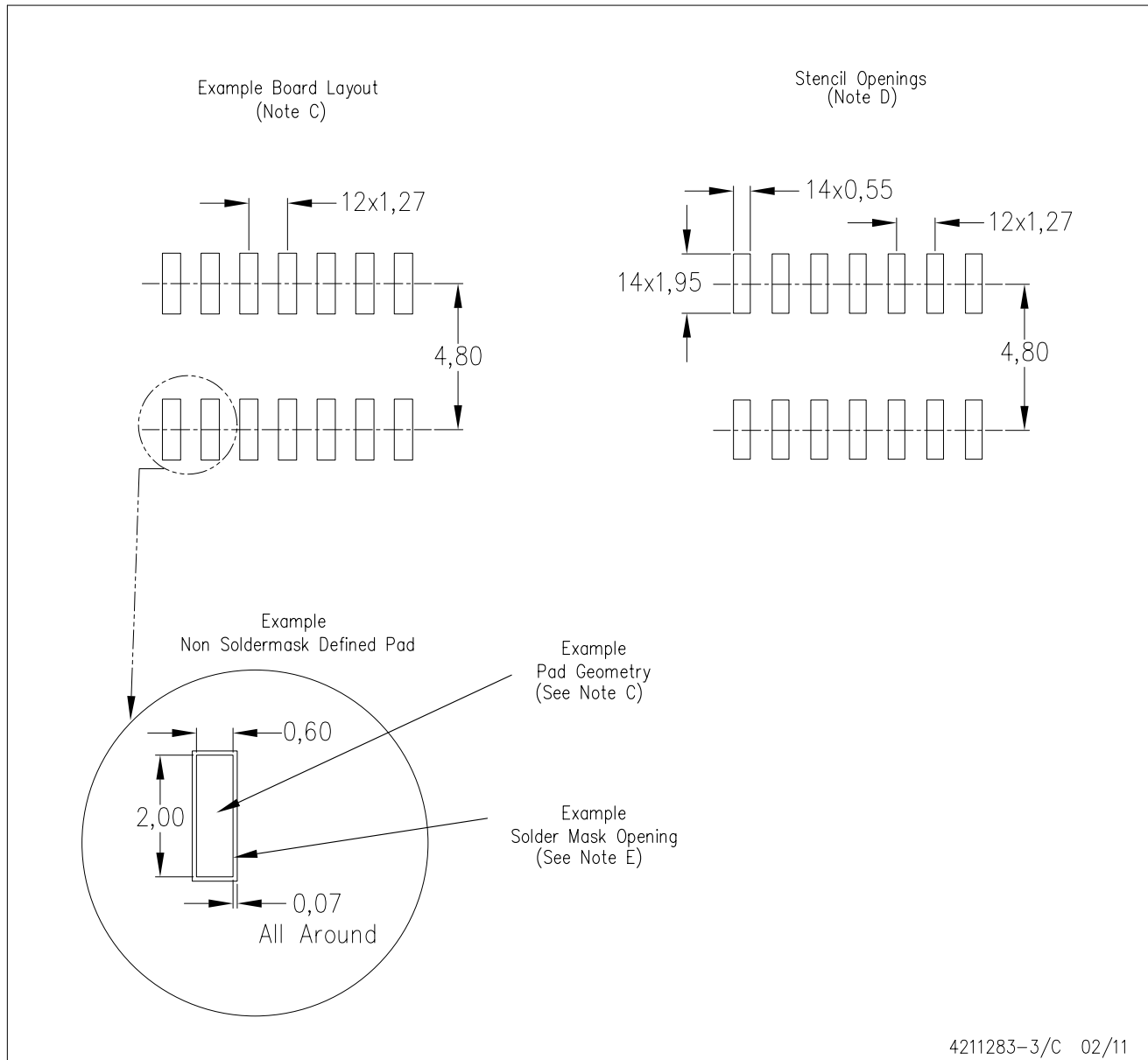
4040047-5/M 06/11

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

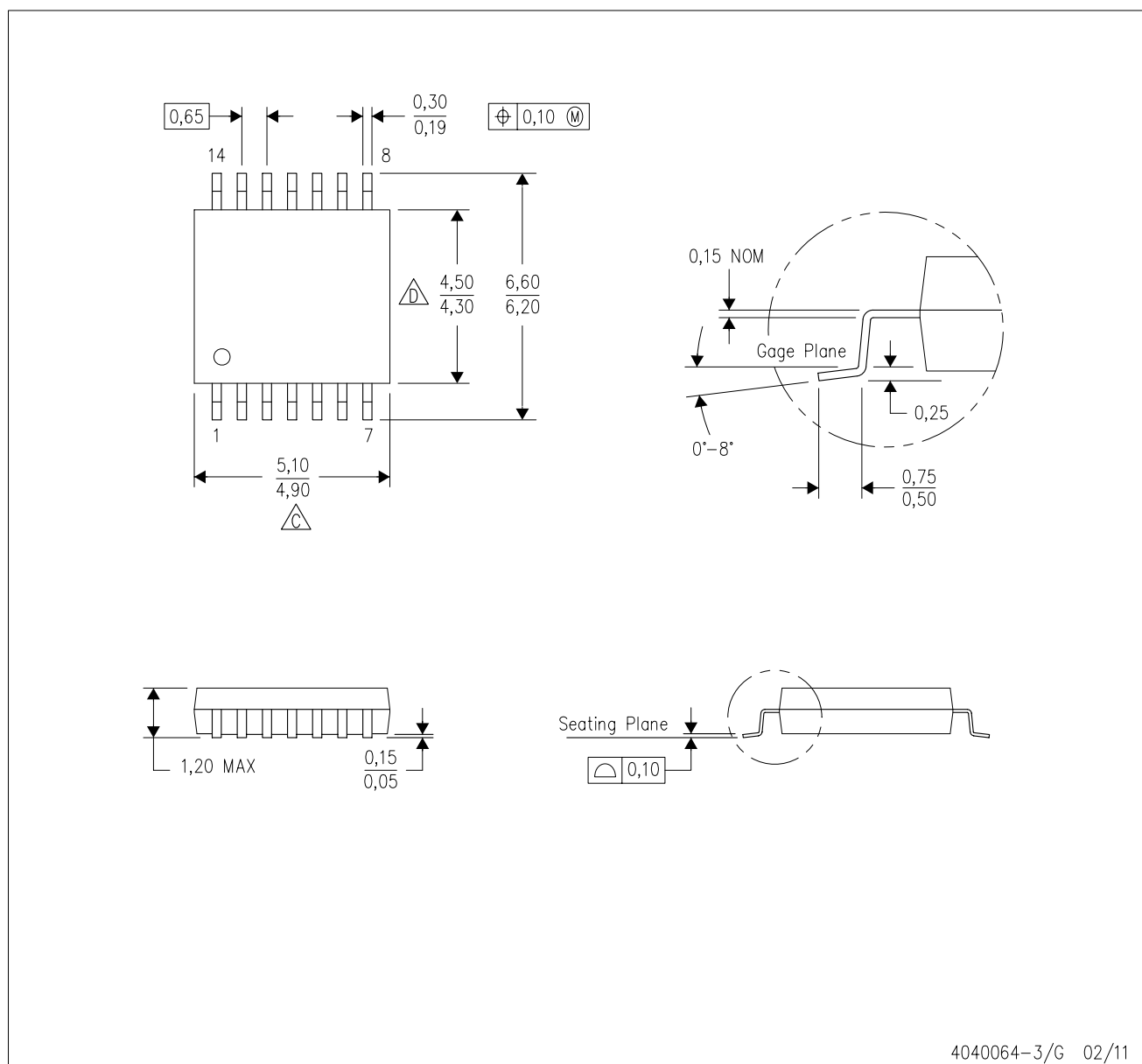
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

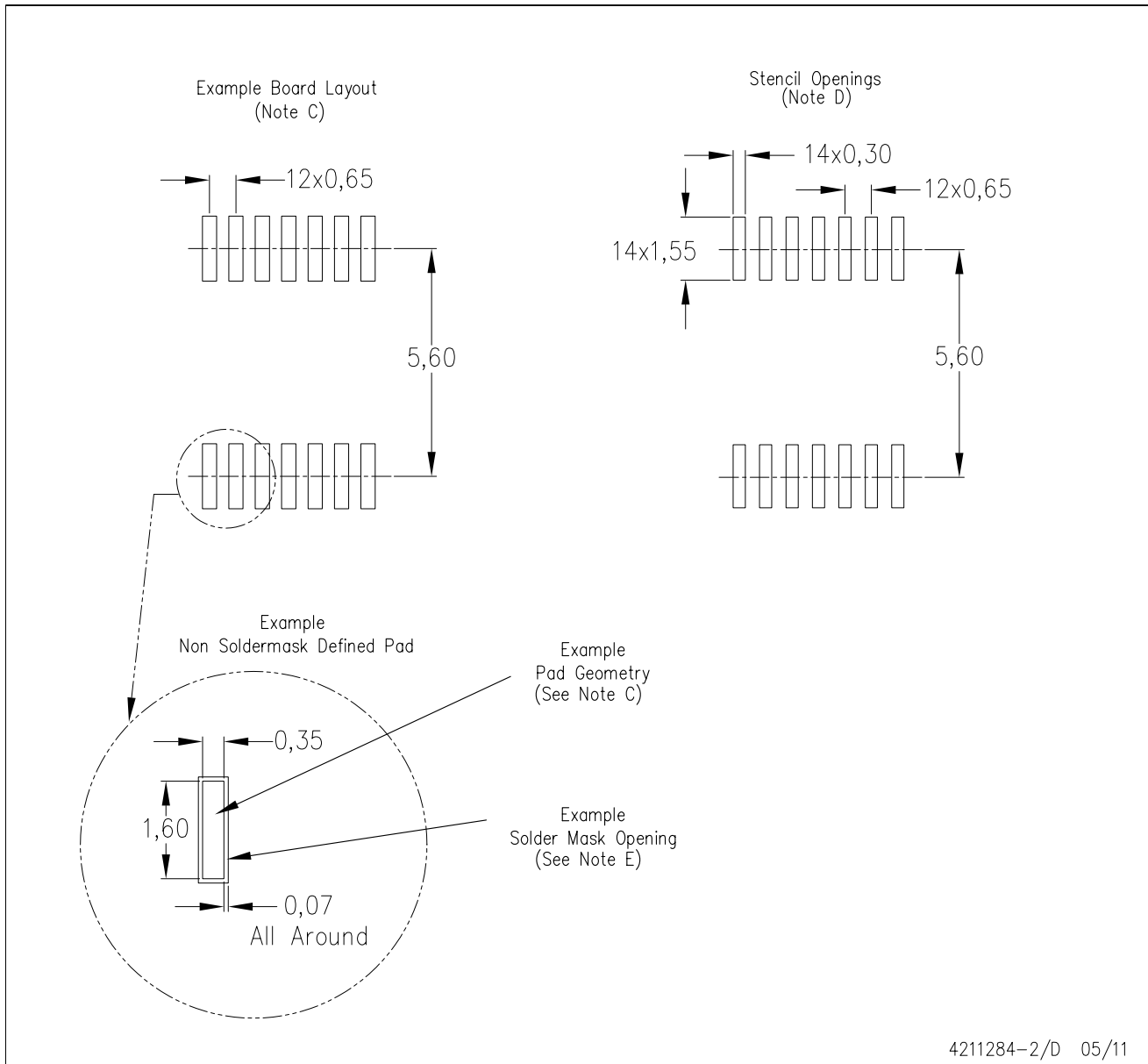
PLASTIC SMALL OUTLINE



4040064-3/G 02/11

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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