UNITRODE

UC1543 UC1544
UC2543 UC2544
UC3543 UC3544

Power Supply Supervisory Circuit

FEATURES

- Includes Over-voltage, Under-voltage, And Current Sensing Circuits
- Internal 1% Accurate Reference
- Programmable Time Delays
- SCR "Crowbar" Drive Of 300mA
- Remote Activation Capability
- Optional Over-voltage Latch
- Uncommitted Comparator Inputs For Low Voltage Sensing (UC1544 Series Only)

DESCRIPTION

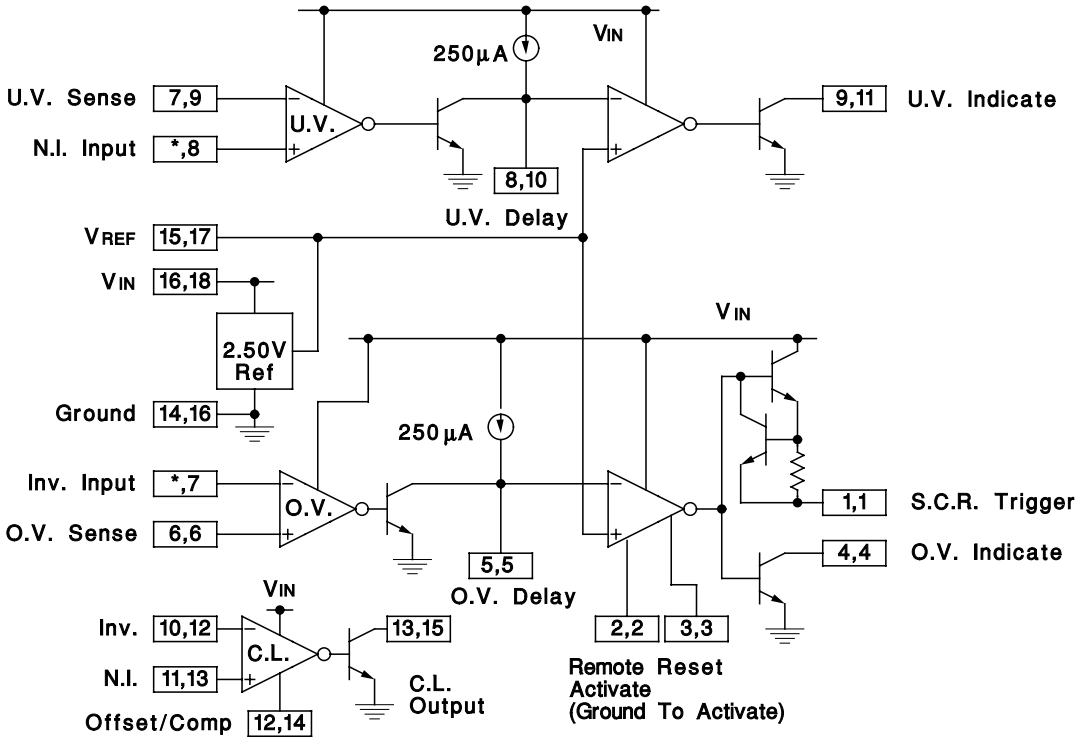
The monolithic integrated circuits contain all the functions necessary to monitor and control the output of a sophisticated power supply system. Over-voltage (O.V.) sensing with provision to trigger an external SCR "crowbar" shutdown; an under-voltage (U.V.) circuit which can be used to monitor either the output or to sample the input line voltage; and a third op amp/comparator usable for current sensing (C.L.) are all included in this IC, together with an independent, accurate reference generator.

Both over- and under-voltage sensing circuits can be externally programmed for minimum time duration of fault before triggering. All functions contain open collector outputs which can be used independently or wire-or'ed together, and although the SCR trigger is directly connected only to the over-voltage sensing circuit, it may be optionally activated by any of the other outputs, or from an external signal. The O.V. circuit also includes an optional latch and external reset capability.

The UC1544/2544/3544 devices have the added versatility of completely uncommitted inputs to the voltage sensing comparators so that levels less than 2.5V may be monitored by dividing down the internal reference voltage. The current sense circuit may be used with external compensation as a linear amplifier or as a high-gain comparator. Although nominally set for zero input offset, a fixed threshold may be added with an external resistor. Instead of current limiting, this circuit may also be used as an additional voltage monitor.

The reference generator circuit is internally trimmed to eliminate the need for external potentiometers and the entire circuit may be powered directly from either the output being monitored or from a separate bias voltage.

BLOCK DIAGRAM



Note: For each terminal, first number refers to 1543 series, second to 1544 series.
** On 1543 series, this function is internally connected to VREF.*

ABSOLUTE MAXIMUM RATINGS

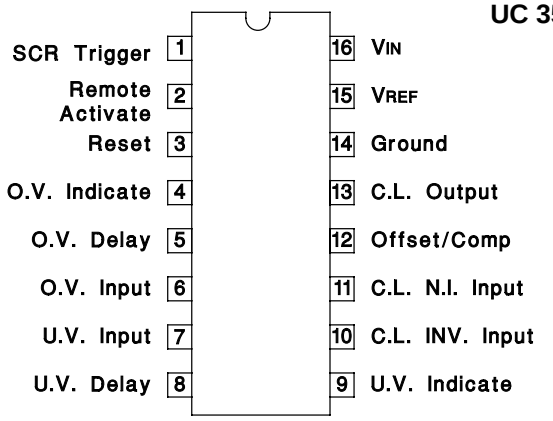
Input Supply Voltage, V_{IN} 40V
Sense Inputs, Voltage Range . . . . . 0 to V_{IN}
SCR Trigger Current (Note 1) . . . . . -600mA
Indicator Output Voltage 40V
Indicator Output Sink Current 50mA
Power Dissipation (Package Limitation) 1000mW
Operating Temperature Range
UC1543, UC1544 . . . . . -55°C to +125°C
UC2543, UC2544 . . . . . -25°C to +85°C
UC3543, UC3544 . . . . . 0°C to +70°C
Storage Temperature Range . . . . . -65°C to +150°C

Note 1: At higher input voltages, a dissipation limiting resistor, RG, is required.
Note 2: Currents are positive-into, negative-out of the specified terminal. Consult Packaging section of Databook for thermal limitations and considerations of package.

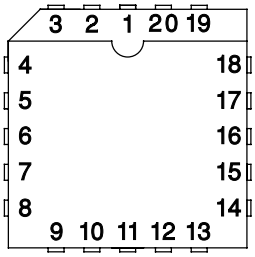
CONNECTION DIAGRAMS

DIL-16, SOIC-16 (TOP VIEW)
J or N, DW Package

UC 1543
UC 2543
UC 3543



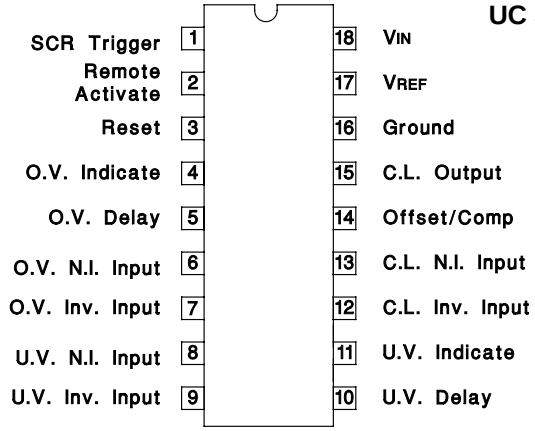
PLCC-20, LCC-20
(TOP VIEW)
Q or L Package



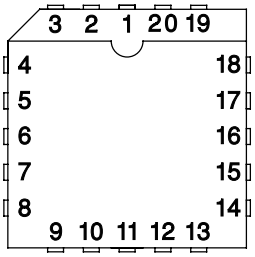
PACKAGE PIN FUNCTION	
FUNCTION	**PIN**
N/C	1
SCR Trigger	2
Remote Activate	3
Reset	4
O.V. Indicate	5
N/C	6
O.V. Delay	7
O.V. Input	8
N/C	9
N/C	10
U.V. Input	11
U.V. Delay	12
U.V. Indicate	13
C.L. INV. Input	14
C.L. N.I. Input	15
Offset/Comp	16
C.L. Output	17
Ground	18
V_{REF}	19
V_{IN}	20

DIL-18, SOIC-18 (TOP VIEW)
J or N, DW Package

UC 1544
UC 2544
UC 3544



PLCC-20, LCC-20
(TOP VIEW)
Q or L Package

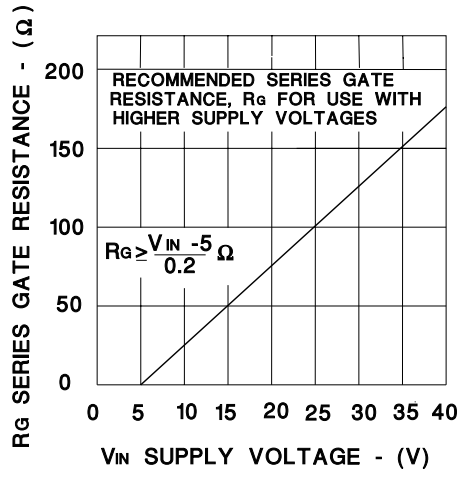


PACKAGE PIN FUNCTION	
FUNCTION	**PIN**
N/C	1
SCR Trigger	2
Remote Activate	3
Reset	4
O.V. Indicate	5
N/C	6
O.V. Delay	7
O.V. N.I. Input	8
O.V. INV. Input	9
U.V. N.I. Input	10
U.V. INV. Input	11
U.V. Delay	12
U.V. Indicate	13
C.L. INV. Input	14
C.L. N.I. Input	15
Offset/Comp	16
C.L. Output	17
Ground	18
V_{REF}	19
V_{IN}	20

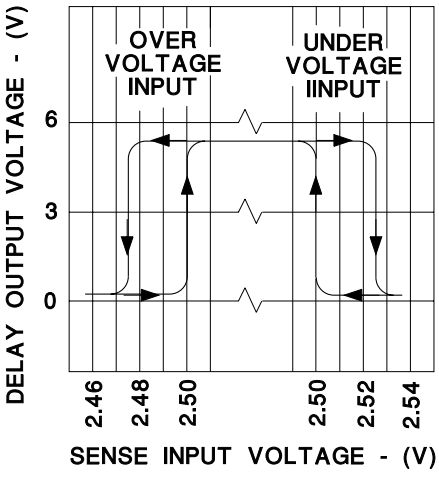
ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1543 and UC1544; -25°C to +85°C for the UC2543 and UC2544; and 0°C to +70°C for the UC3543 and UC3544. Electrical tests are performed with V_{IN} = 10V and 2kΩ pull-up resistors on all indicator outputs. All electrical specifications for the UC1544, UC2544, and UC3544 devices are tested with the inverting over-voltage input and the non-inverting under-voltage input externally connected to the 2.5V reference. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	UC1543/UC1544 UC2543/UC2544			UC3543/UC3544			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Voltage Range	T_J = 25°C to T_{MAX}	4.5		40	4.5		40	V
	T_{MIN} to T_{MAX}	4.7		40	4.7		40	V
Supply Current	V_{IN} = 40V, Output Open, T_J = 25°C		7	10		7	10	mA
	$T_{MIN} \le T_J \le T_{MAX}$			15			15	mA
Reference Section								
Output Voltage	T_J = 25°C	2.48	2.50	2.52	2.45	2.50	2.55	V
Output Voltage	Over Temperature Range	2.45		2.55	2.40		2.60	V
Line Regulation	V_{IN} = 5 to 30V		1	5		1	5	mV
Load Regulation	I_{REF} = 0 to 10mA		1	10		1	10	mV
Short Circuit Current	V_{REF} = 0	-10	-20	-40	-12	-20	-40	mA
Temperature Stability			50			50		ppm/°C
SCR Trigger Section								
Peak Output Current	V_{IN} = 5V, R_G = 0, V_O = 0	-100	-300	-600	-100	-300	-600	mA
Peak Output Voltage	V_{IN} = 15V, I_O = -100mA	12	13		12	13		V
Output Off Voltage	V_{IN} = 40V		0	0.1		0	0.1	V
Remote Activate Current	R/A Pin = Gnd		-0.4	-0.8		-0.4	-0.8	mA
Remote Activate Voltage	R/A Pin Open		2	6		2	6	V
Reset Current	Reset = Gnd, R/A = Gnd		-0.4	-0.8		-0.4	-0.8	mA
Reset Voltage	Reset open, R/A = Gnd		2	6		2	6	V
Output Current Rise Time	R_L = 50Ω, T_J = 25°C, C_D = 0		400			400		mA/µs
Prop. Delay from R/A	R_L = 50Ω, T_J = 25°C, C_D = 0		300			300		ns
Prop. Delay from O/V input	R_L = 50Ω, T_J = 25°C, C_D = 0		500			500		ns
Comparator Section								
Input Threshold (Input voltage rising on O.V. and falling on U.V.)	T_J = 25°C	2.45	2.50	2.55	2.40	2.50	2.60	V
	Over Temperature Range	2.40		2.60	2.35		2.65	V
Input Hysteresis			25			25		mV
Input Bias Current	Sense Input = 0V		-0.3	-1.0		-0.3	-1.0	µA
Delay Saturation			0.2	0.5		0.2	0.5	V
Delay High Level			6	7		6	7	V
Delay Charging Current	V_O = 0	-200	-250	-300	-200	-250	-300	µA
Indicate Saturation	I_L = 10mA		0.2	0.5		0.2	0.5	V
Indicate Leakage	V_{IND} = 40V		.01	1.0		.01	1.0	µA
Propagation Delay	Input Over Drive = 200mV, T_J = 25°C, C_D = 0		400			400		ns
	Input Over Drive = 200mV, T_J = 25°C, C_D = 1µF		10			10		ms
Current Limit Section								
Input Voltage Range		0		V_{IN}-3V	0		V_{IN}-3V	V
Input Bias Current	Offset Pin Open, V_{CM} = 0		-0.3	-1.0		-0.3	-1.0	µA
Input Offset Voltage	Offset Pin Open, V_{CM} = 0		0	10		0	10	mV
	10kΩ from Offset Pin to Gnd	80	100	120	80	100	120	mV
CMRR	0 ≤ V_{CM} ≤ 12V, V_{IN} = 15V	60	70		60	70		dB
AVOL	Offset Pin Open, V_{CM} = 0V, R_L = 10k to 15kΩ, ΔV_{OUT} = 1 to 6V	72	80		72	80		dB
Output Saturation	I_L = 10mA		0.2	0.5		0.2	0.5	V
Output Leakage	V_{IND} = 40V		.01	1.0		.01	1.0	µA
Small Signal Bandwidth	A_V = 0dB, T_J = 25°C		5			5		MHz
Propagation Delay	$V_{OVERDRIVE}$ = 100mV, T_J = 25°C		200			200		ns

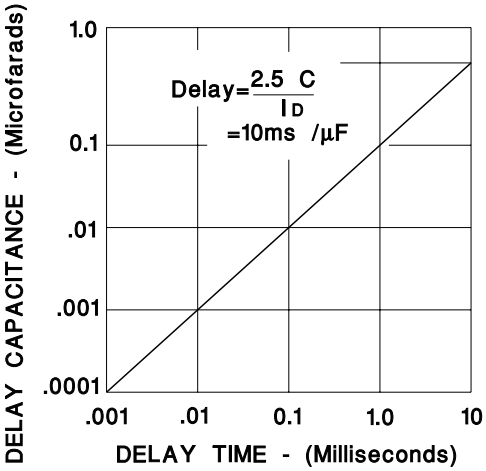
SCR Trigger Power Limiting



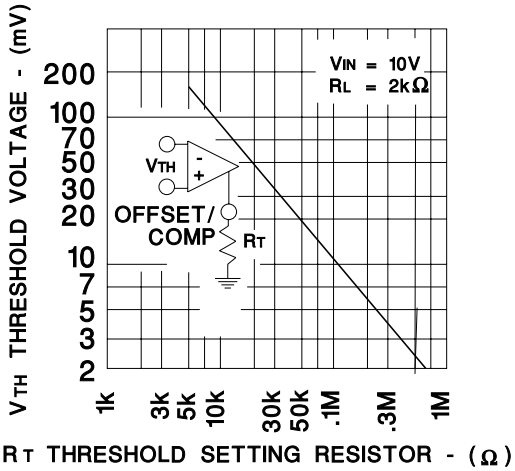
Comparator Input Hysteresis



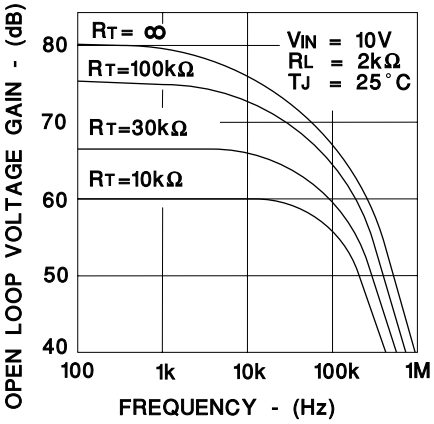
Activation Delay vs Capacitor Value



Current Limit Input Threshold

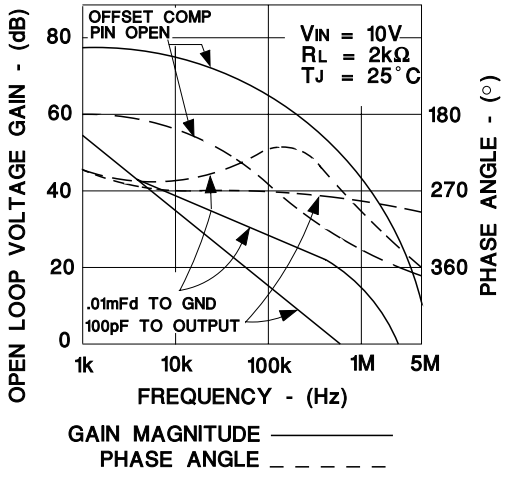


Current Limit Amplifier Gain



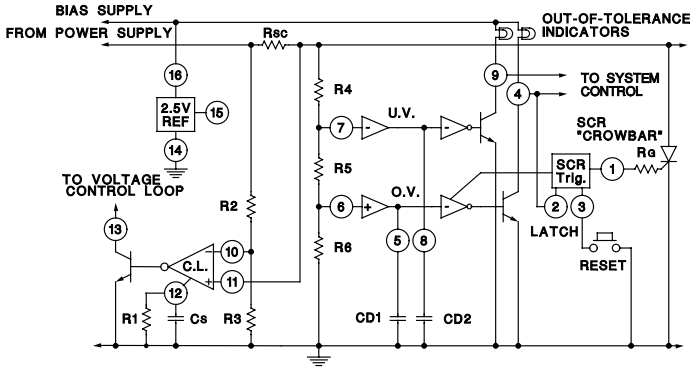
Note: R_T is connected from Offset Pin to Gnd. Values of R_T below 5.0k may cause Amplifier Cutoff at -55°C.

Current Limit Amplifier Frequency Response



APPLICATIONS (Pin numbers given for UC1543 series devices)

Typical Application



The values for the external components are determined as follows:

Current limit input threshold, $V_{TH} = \frac{1000}{R_1}$

CS is determined by the current loop dynamics

Peak current to load, $I_P \cong \frac{V_{TH}}{R_{SC}} + \frac{V_O}{R_{SC}}\left(\frac{R_2}{R_2 + R_3}\right)$

Short Circuit Current, $I_{SC} = \frac{V_{TH}}{R_{SC}}$

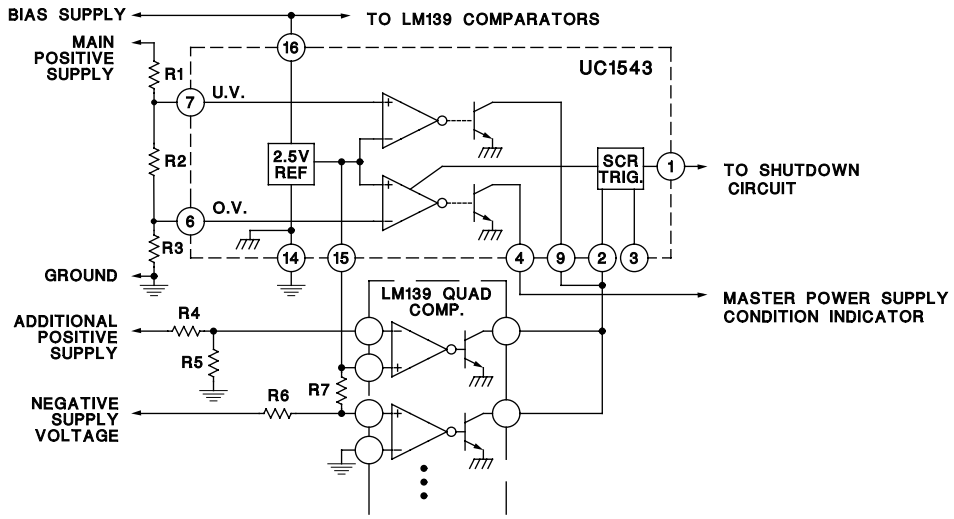
Low output voltage limit, $V_O\ (Low) = \frac{2.5\ (R_4 + R_5 + R_6)}{R_5 + R_6}$

High output voltage limit, $V_O\ (High) = \frac{2.5\ (R_4 + R_5 + R_6)}{R_6}$

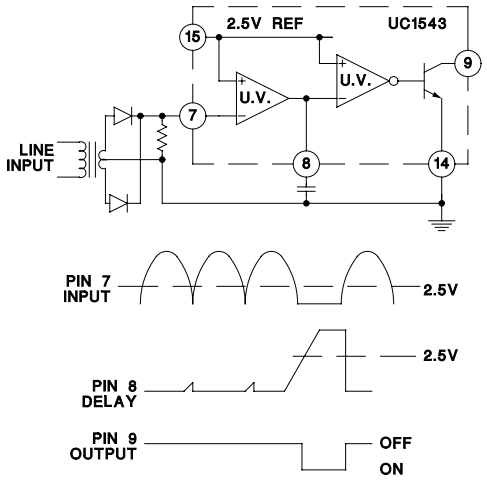
Voltage sensing delay, $t_D = 10{,}000Cd$

SCR trigger power limiting resistor, $R_G > \frac{V_{IN} - 5}{0.2}$

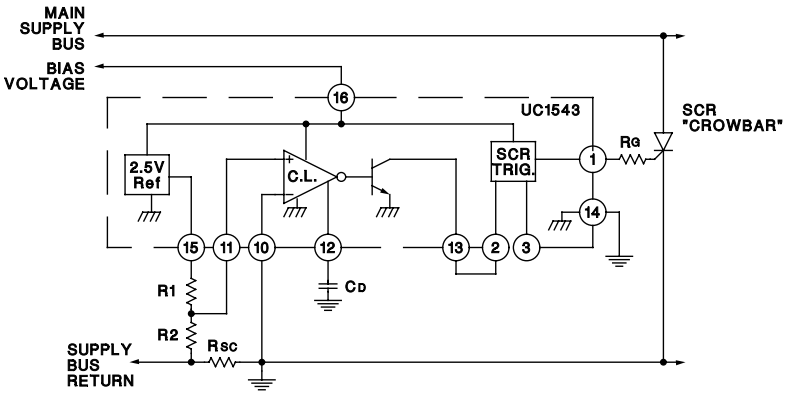
Sensing Multiple Supply Voltages



Input Line Monitor



Overcurrent Shutdown



UNITRODE CORPORATION
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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
5962-8774001EA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	Level-NC-NC-NC
5962-8774002VA	OBSOLETE	CDIP	J	18		TBD	Call TI	Call TI
UC1543J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	Level-NC-NC-NC
UC1543J/80265	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	Level-NC-NC-NC
UC1543J883B	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	Level-NC-NC-NC
UC1543L	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
UC1543L883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
UC1544J	OBSOLETE	CDIP	J	18		TBD	Call TI	Call TI
UC1544J883B	OBSOLETE	CDIP	J	18		TBD	Call TI	Call TI
UC1544L	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
UC1544L883B	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
UC2543DW	NRND	SOIC	DW	16	40	TBD	CU NIPDAU	Level-2-220C-1 YEAR
UC2543DWTR	NRND	SOIC	DW	16	2000	TBD	CU NIPDAU	Level-2-220C-1 YEAR
UC2543J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	Level-NC-NC-NC
UC2543N	NRND	PDIP	N	16	25	TBD	CU NIPDAU	Level-NA-NA-NA
UC2544DW	NRND	SOIC	DW	18	40	TBD	CU NIPDAU	Level-2-220C-1 YEAR
UC2544DWTR	NRND	SOIC	DW	18	2000	TBD	CU NIPDAU	Level-2-220C-1 YEAR
UC2544J	OBSOLETE	CDIP	J	18		TBD	Call TI	Call TI
UC2544N	NRND	PDIP	N	18	20	TBD	CU NIPDAU	Level-NA-NA-NA
UC3543DW	NRND	SOIC	DW	16	40	TBD	CU NIPDAU	Level-2-220C-1 YEAR
UC3543DWTR	NRND	SOIC	DW	16	2000	TBD	CU NIPDAU	Level-2-220C-1 YEAR
UC3543J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	Level-NC-NC-NC
UC3543N	NRND	PDIP	N	16	25	TBD	CU NIPDAU	Level-NA-NA-NA
UC3544DW	NRND	SOIC	DW	18	40	TBD	CU NIPDAU	Level-2-220C-1 YEAR
UC3544DWTR	NRND	SOIC	DW	18	2000	TBD	CU NIPDAU	Level-2-220C-1 YEAR
UC3544J	OBSOLETE	CDIP	J	18		TBD	Call TI	Call TI
UC3544N	NRND	PDIP	N	18	20	TBD	CU NIPDAU	Level-NA-NA-NA

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.