

UC1573 UC2573 UC3573

Buck Pulse Width Modulator Stepdown Voltage Regulator

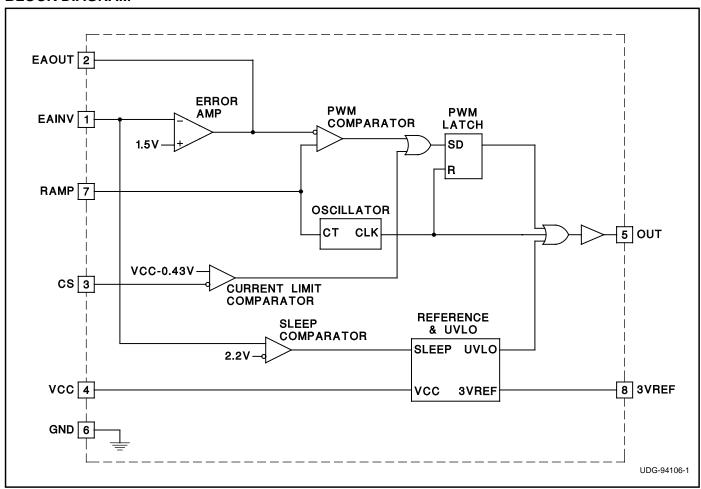
FEATURES

- Simple Single Inductor Buck PWM Stepdown Voltage Regulation
- Drives External PMOS Switch
- Contains UVLO Circuit
- Includes Pulse-by-Pulse Current Limit
- Low 50μA Sleep Mode Current

DESCRIPTION

The UC3573 is a Buck pulse width modulator which steps down and regulates a positive input voltage. The chip is optimized for use in a single inductor buck switching converter employing an external PMOS switch. The block diagram consists of a precision reference, an error amplifier configured for voltage mode operation, an oscillator, a PWM comparator with latching logic, and a 0.5A peak gate driver. The UC3573 includes an undervoltage lockout circuit to insure sufficient input supply voltage is present before any switching activity can occur, and a pulse-by-pulse current limit. Input current can be sensed and limited to a user determined maximum value. In addition, a sleep comparator interfaces to the UVLO circuit which turns the chip off when the input voltage is below the UVLO threshold. This reduces the supply current to only $50\mu A$, making the UC3573 ideal for battery powered applications.

BLOCK DIAGRAM

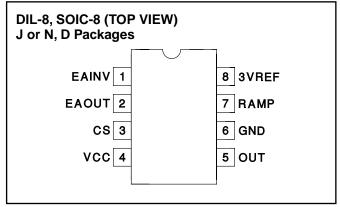


ABSOLUTE MAXIMUM RATINGS

VCC35V
EAINV0.6V to VCC
I _{EAOUT}
RAMP
CS
I _{OUT} 0.7A to 0.7A
$I_{3VREF} \dots -15 mA$
Storage Temperature65°C to +150°C
Junction Temperature65°C to +150°C
Lead Temperature (Soldering, 10 sec.) +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, these parameters apply for $T_A = -55^{\circ}C$ to +125°C for the UC1573, -40°C to +85°C for the UC2573, and 0°C to +70°C for the UC3573, VCC = 5V, CT = 680pF, $T_A = T_J$.

	•		TYP		UNITS
Reference Section		<u> </u>			•
3VREF		2.94	3	3.06	V
Line Regulation	VCC = 4.75 to 30V		1	10	mV
Load Regulation	I _{3VREF} = 0 to -5mA		1	10	mV
Oscillator Section		•			•
Frequency	V _{CC} = 5V, 30V	85	100	115	kHz
Error Amp Section					•
EAINV	EAOUT = 2V	1.45	1.5	1.55	V
I _{EAINV}	EAOUT = 2V		-0.2	-1	μΑ
AVOL	EAOUT = 0.5V to 3V	65	90		dB
EAOUT High	EAINV = 1.4V	3.6	4	4.4	V
EAOUT Low	EAINV = 1.6V		0.1	0.2	V
I _{EAOUT}	EAINV = 1.4V, EAOUT = 2V	-350	-500		μΑ
	EAINV = 1.6V, EAOUT = 2V	7	20		mA
Unity Gain Bandwidth	T _J = 25°C, F = 10kHz	0.6	1		MHz
Current Sense Comparator Section					
Threshold (referred to VCC)		-0.39	-0.43	-0.47	V
Input Bias Current	CS = VCC		150	800	nA
CS Propagation Delay			400		ns
Gate Drive Output Section					
OUT High Saturation	$I_{OUT} = 0$		0	0.3	V
	$I_{OUT} = -10$ mA		0.7	1.5	V
	$I_{OUT} = -100$ mA		1.5	2.5	V
OUT Low Saturation	I _{OUT} = 10mA		0.1	0.4	V
	I _{OUT} = 100mA		1.5	2.2	V
Rise Time	$T_J = 25$ °C, $C_{LOAD} = 1$ nF + 3.3 Ohms		30	80	ns
Fall Time	$T_J = 25$ °C, $C_{LOAD} = 1$ nF + 3.3 Ohms		30	80	ns
Pulse Width Modulator Section					
Maximum Duty Cycle	EAINV = 1.4V		92	96	%
Minimum Duty Cycle	EAINV = 1.6V			0	%
Modulator Gain	EAOUT = 1.5V to 2.5V	25	35	45	%/V
Undervoltage Lockout Section					
Start Threshold		3.5	4.2	4.5	V
Hysteresis		100	200	300	mV

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PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Sleep Mode Section					
Threshold		1.8	2.2	2.6	V
Supply Current Section					
I _{VCC}	VCC = 30V		9	12	mA
Ivcc	VCC = 30V, EAINV = 3V		50	150	А

PIN DESCRIPTIONS

3VREF: Precision 3V reference. Bypass with 100nF capacitor.

CS: Peak current limit sense pin. Senses the current across a current sense resistor placed between VCC and source of the PMOS Buck switch. OUT will be held high (PMOS buck switch off) if VCC – CS exceeds 0.4V.

EAINV: Inverting input to error amplifier. VOUT sense feedback connected to this pin. The non-inverting input of the error amplifier is internally connected to:

$$\frac{3VREF}{2}$$
 Volts.

Connecting the EAINV pin to an external voltage greater than 2.6V commands the chip to go into a low current sleep mode.

EAOUT: Output of error amplifier. Use EAOUT and EAINV for loop compensation components.

GND: Circuit Ground.

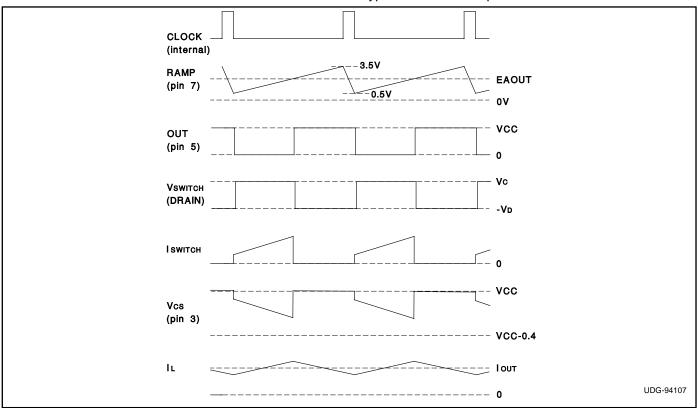
OUT: Gate drive for external PMOS switch connected between VCC and the flyback inductor. OUT drives the gate of the PMOS switch between VCC and GND.

RAMP: Oscillator and ramp for pulse width modulator. Frequency is set by a capacitor to GND by the equation

$$F = \frac{1}{15k C_{RAMP}}$$

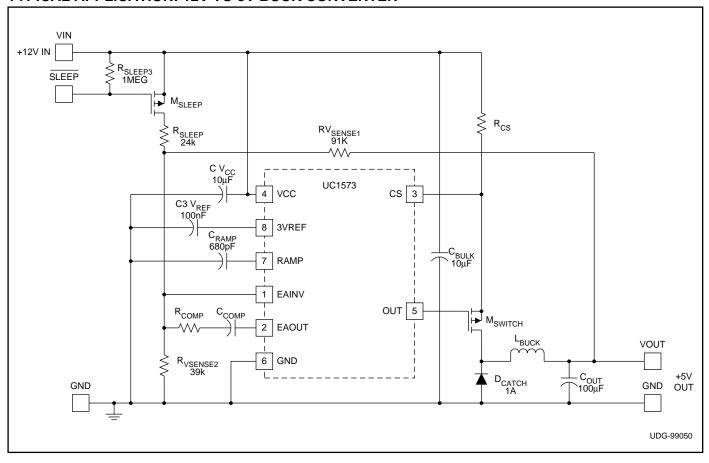
Recommended operating frequency range is 10kHz to 200kHz.

VCC: Input voltage supply to chip. Range is 4.75V to 30V. Bypass with a 1 F capacitor.



Typical Waveforms.

TYPICAL APPLICATION: 12V TO 5V BUCK CONVERTER







i.com 5-Feb-2007

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Packag Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
UC1573J	OBSOLETE	CDIP	J	8		TBD	Call TI	Call TI
UC2573D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2573DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2573DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2573DTRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2573N	ACTIVE	PDIP	Р	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC2573NG4	ACTIVE	PDIP	Р	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3573D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3573DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3573DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3573DTRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3573N	ACTIVE	PDIP	Р	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3573NG4	ACTIVE	PDIP	Р	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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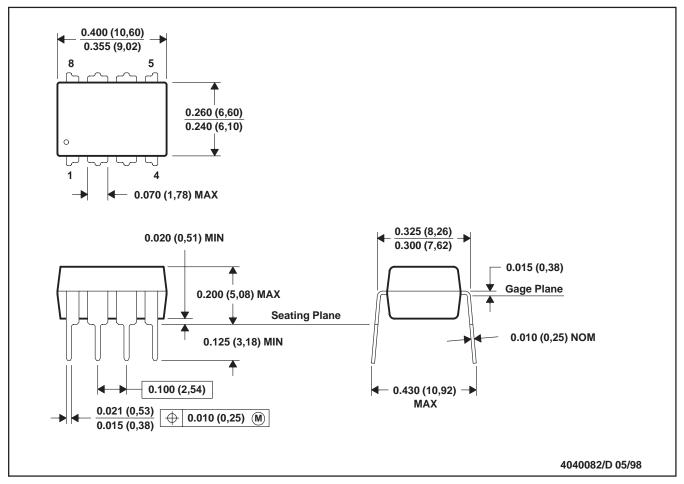
PACKAGE OPTION ADDENDUM

5-Feb-2007

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE



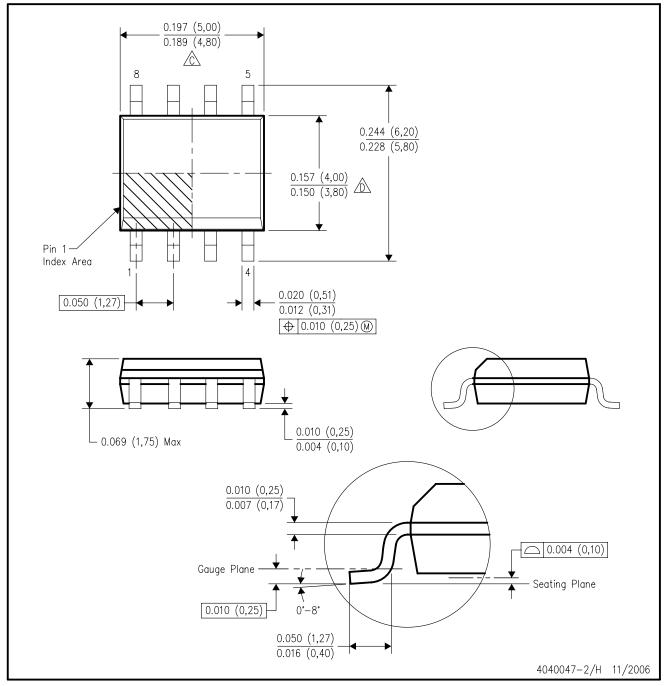
NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001

For the latest package information, go to $http://www.ti.com/sc/docs/package/pkg_info.htm$

D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AA.



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Mailing Address: Texas Instruments

Post Office Box 655303 Dallas, Texas 75265