

TC74VHC165F, TC74VHC165FN, TC74VHC165FT, TC74VHC165FK

8-Bit Shift Register (P-IN, S-OUT)

The TC74VHC165 is an advanced high speed CMOS 8-BIT PARALLEL/SERIAL-IN, SERIAL-OUT SHIFT REGISTER fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

It consists of parallel-in or serial-in, serial-out 8-bit shift register with a gated clock input. When the SHIFT/LOAD input is held high, the serial data input is enabled and the eight flip-flops perform serial shifting with each clock pulse.

When the SHIFT/LOAD input is held low, the parallel data is loaded synchronously into the register at positive going transition of the clock pulse.

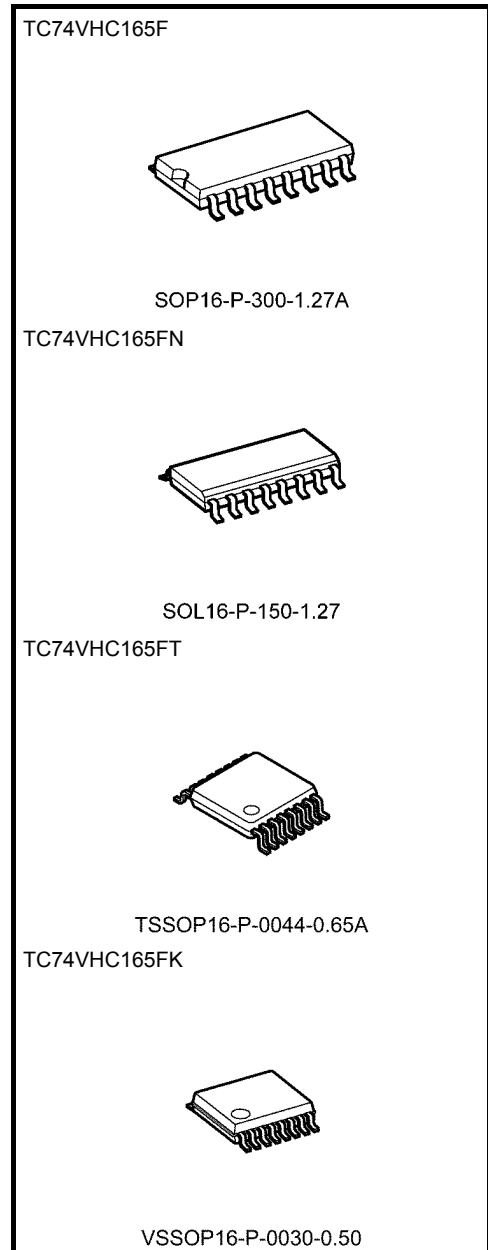
The CK-INH input should be shifted high only when the CK input is held high.

An Input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and on two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

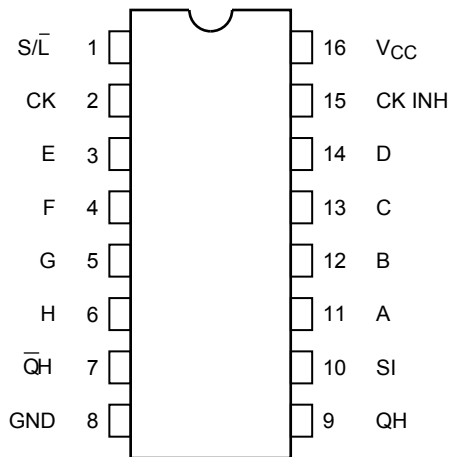
- High speed: $f_{max} = 150$ MHz (typ.) at $V_{CC} = 5$ V
- Low power dissipation: $I_{CC} = 4$ μ A (max) at $T_a = 25^\circ$ C
- High noise immunity: $V_{NIH} = V_{NIL} = 28\%$ V_{CC} (min)
- Power down protection is provided on all inputs.
- Balanced propagation delays: $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range: $V_{CC} (opr) = 2$ V to 5.5 V
- Pin and function compatible with 74ALS165

Note: xxxFN (JEDEC SOP) is not available in Japan.

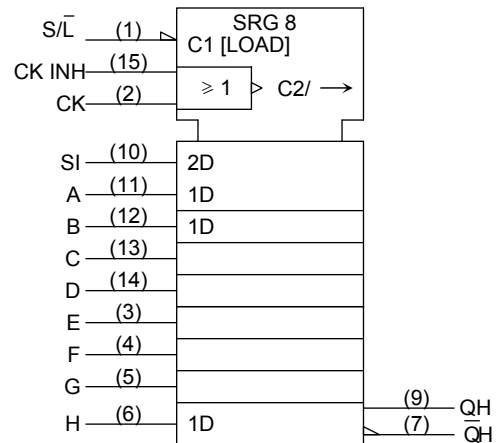


Weight
 SOP16-P-300-1.27A: 0.18 g (typ.)
 SOL16-P-150-1.27: 0.13 g (typ.)
 TSSOP16-P-0044-0.65A: 0.06 g (typ.)
 VSSOP16-P-0030-0.50: 0.02 g (typ.)

Pin Assignment



IEC Logic Symbol



Truth Table

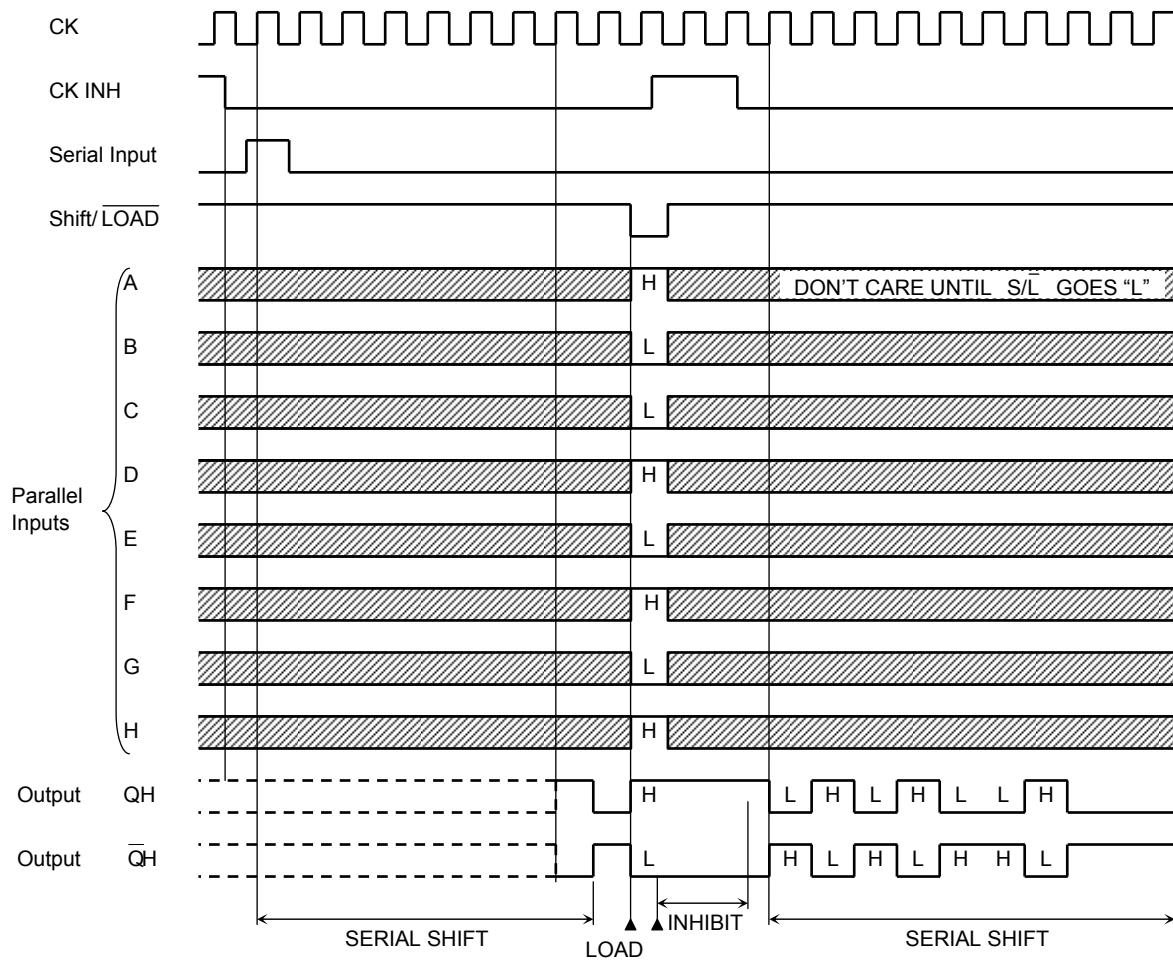
| Inputs | | | | | Internal Outputs | | Outputs | |
|----------------|------------|------------|--------------|---------------------|------------------|-----------------|-----------------|-------------------|
| SHIFT/ LOAD | CK INH | CK | SERIAL IN | PARALLEL A.....H | QA | QB | QH | \overline{QH} |
| L | X | X | X | a.....h | a | b | h | \overline{h} |
| H | L | \uparrow | H | X | H | QA _n | QG _n | \overline{QG}_n |
| H | L | \uparrow | L | X | L | QA _n | QG _n | \overline{QG}_n |
| H | \uparrow | L | H | X | H | QA _n | QG _n | \overline{QG}_n |
| H | \uparrow | L | L | X | L | QA _n | QG _n | \overline{QG}_n |
| H | X | H | X | X | No Change | | | |
| H | H | X | X | X | No Change | | | |

X: Don't care

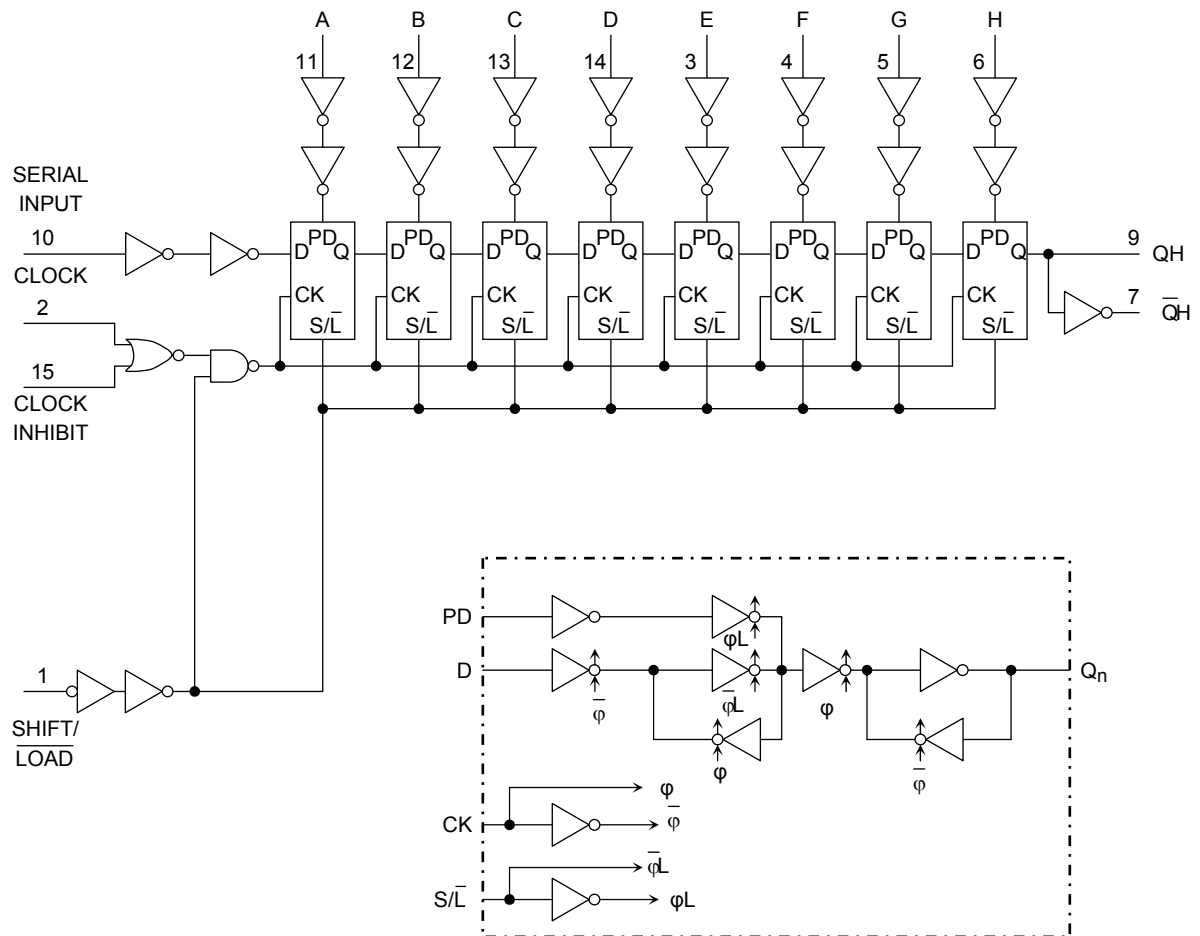
a.....h: The level of steady state input voltage at inputs A through H respectively

QA_n to QG_n: The level of QA to QG, respectively, before the most recent positive transition of the CK.

Timing Chart



System Diagram



Absolute Maximum Ratings (Note)

| Characteristics | Symbol | Rating | Unit |
|-----------------------------|-----------|------------------------|-------------|
| Supply voltage range | V_{CC} | -0.5 to 7.0 | V |
| DC input voltage | V_{IN} | -0.5 to 7.0 | V |
| DC output voltage | V_{OUT} | -0.5 to $V_{CC} + 0.5$ | V |
| Input diode current | I_{IK} | -20 | mA |
| Output diode current | I_{OK} | ± 20 | mA |
| DC output current | I_{OUT} | ± 25 | mA |
| DC V_{CC} /ground current | I_{CC} | ± 50 | mA |
| Power dissipation | P_D | 180 | mW |
| Storage temperature | T_{stg} | -65 to 150 | $^{\circ}C$ |

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note)

| Characteristics | Symbol | Rating | Unit |
|--------------------------|-----------|---|------|
| Supply voltage | V_{CC} | 2.0 to 5.5 | V |
| Input voltage | V_{IN} | 0 to 5.5 | V |
| Output voltage | V_{OUT} | 0 to V_{CC} | V |
| Operating temperature | T_{opr} | -40 to 85 | °C |
| Input rise and fall time | dt/dv | 0 to 100 ($V_{CC} = 3.3 \pm 0.3$ V) 0 to 20 ($V_{CC} = 5 \pm 0.5$ V) | ns/V |

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

| Characteristics | Symbol | Test Condition | V_{CC} (V) | $T_a = 25^\circ\text{C}$ | | | $T_a = -40$ to 85°C | | Unit | |
|---------------------------|----------|-------------------------------|----------------------------|-----------------------------|--------|-----------------------------|-----------------------------------|-----------------------------|---------------|---|
| | | | | Min | Typ. | Max | Min | Max | | |
| High-level input voltage | V_{IH} | — | 2.0 3.0 to 5.5 | 1.50 $V_{CC} \times 0.7$ | — — | — — | 1.50 $V_{CC} \times 0.7$ | — — | V | |
| Low-level input voltage | V_{IL} | — | 2.0 3.0 to 5.5 | — — | — — | 0.50 $V_{CC} \times 0.3$ | — — | 0.50 $V_{CC} \times 0.3$ | V | |
| High-level output voltage | V_{OH} | $V_{IN} = V_{IH}$ or V_{IL} | $I_{OH} = -50 \mu\text{A}$ | 2.0 | 1.9 | 2.0 | — | 1.9 | — | V |
| | | | | 3.0 | 2.9 | 3.0 | — | 2.9 | — | |
| | | | $I_{OH} = -4$ mA | 3.0 | 2.58 | — | — | 2.48 | — | |
| | | | | 4.5 | 3.94 | — | — | 3.80 | — | |
| Low-level output voltage | V_{OL} | $V_{IN} = V_{IH}$ or V_{IL} | $I_{OL} = 50 \mu\text{A}$ | 2.0 | — | 0.0 | 0.1 | — | 0.1 | V |
| | | | | 3.0 | — | 0.0 | 0.1 | — | 0.1 | |
| | | | $I_{OL} = 4$ mA | 3.0 | — | — | 0.36 | — | 0.44 | |
| | | | | 4.5 | — | — | 0.36 | — | 0.44 | |
| Input leakage current | I_{IN} | $V_{IN} = 5.5$ V or GND | 0 to 5.5 | — | — | ± 0.1 | — | ± 1.0 | μA | |
| Quiescent supply current | I_{CC} | $V_{IN} = V_{CC}$ or GND | 5.5 | — | — | 4.0 | — | 40.0 | μA | |

Timing Requirements (input: $t_r = t_f = 3 \text{ ns}$)

| Characteristics | Symbol | Test Condition | Ta = 25°C | | Ta = -40 to 85°C | | Unit |
|---|-----------|----------------|---------------|-------|------------------|-------|------|
| | | | VCC (V) | Limit | Limit | Limit | |
| Minimum pulse width (CK, CK INH) | $t_w (L)$ | — | 3.3 ± 0.3 | 6.0 | 7.0 | ns | |
| | $t_w (H)$ | | 5.0 ± 0.5 | 4.0 | 4.0 | | |
| Minimum pulse width (S/\bar{L}) | $t_w (L)$ | — | 3.3 ± 0.3 | 7.5 | 9.0 | ns | |
| | | | 5.0 ± 0.5 | 5.0 | 6.0 | | |
| Minimum set-up time (PI- S/\bar{L}) | t_s | — | 3.3 ± 0.3 | 7.5 | 8.5 | ns | |
| | | | 5.0 ± 0.5 | 5.0 | 5.0 | | |
| Minimum set-up time (SI-CK, CK INH) | t_s | — | 3.3 ± 0.3 | 5.0 | 6.0 | ns | |
| | | | 5.0 ± 0.5 | 4.0 | 4.0 | | |
| Minimum set-up time (S/\bar{L} -CK, CK INH) | t_s | — | 3.3 ± 0.3 | 5.0 | 6.0 | ns | |
| | | | 5.0 ± 0.5 | 4.0 | 4.0 | | |
| Minimum hold time (PI- S/\bar{L}) | t_h | — | 3.3 ± 0.3 | 0.5 | 0.5 | ns | |
| | | | 5.0 ± 0.5 | 1.0 | 1.0 | | |
| Minimum hold time (SI-CK, CK INH) | t_h | — | 3.3 ± 0.3 | 0.0 | 0.0 | ns | |
| | | | 5.0 ± 0.5 | 0.5 | 0.5 | | |
| Minimum hold time (S/\bar{L} -CK, CK INH) | t_h | — | 3.3 ± 0.3 | 0.0 | 0.0 | ns | |
| | | | 5.0 ± 0.5 | 0.5 | 0.5 | | |
| Minimum removal time (CK INH-CK) | t_{rem} | — | 3.3 ± 0.3 | 5.0 | 5.0 | ns | |
| (CK-CK INH) | | | 5.0 ± 0.5 | 3.5 | 3.5 | | |

AC Characteristics (input: $t_r = t_f = 3 \text{ ns}$)

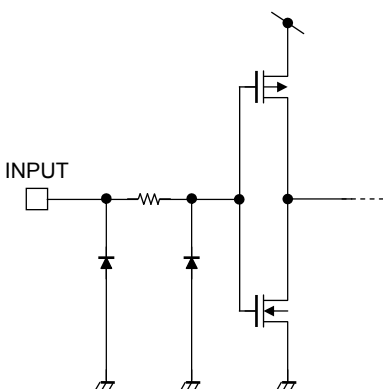
| Characteristics | Symbol | Test Condition | Ta = 25°C | | | Ta = -40 to 85°C | | Unit | | |
|--|-----------------|----------------|---------------------|---------------------|-----|------------------|------|------|------|-----|
| | | | V _{CC} (V) | C _L (pF) | Min | Typ. | Max | | Min | Max |
| Propagation delay time (CK, CK INH-QH, $\bar{Q}H$) | t_{pLH} | — | 3.3 ± 0.3 | 15 | — | 9.9 | 15.4 | 1.0 | 18.0 | ns |
| | | | | 50 | — | 12.4 | 18.9 | 1.0 | 21.5 | |
| | t_{pHL} | | 5.0 ± 0.5 | 15 | — | 6.6 | 9.9 | 1.0 | 11.5 | |
| | | | | 50 | — | 8.1 | 11.9 | 1.0 | 13.5 | |
| Propagation delay time (S/L-QH, $\bar{Q}H$) | t_{pLH} | — | 3.3 ± 0.3 | 15 | — | 9.9 | 15.8 | 1.0 | 18.5 | ns |
| | | | | 50 | — | 12.4 | 19.3 | 1.0 | 22.0 | |
| | t_{pHL} | | 5.0 ± 0.5 | 15 | — | 6.7 | 9.9 | 1.0 | 11.5 | |
| | | | | 50 | — | 8.2 | 11.9 | 1.0 | 13.5 | |
| Propagation delay time (H-QH, $\bar{Q}H$) | t_{pLH} | — | 3.3 ± 0.3 | 15 | — | 9.2 | 14.1 | 1.0 | 16.5 | ns |
| | | | | 50 | — | 11.7 | 17.6 | 1.0 | 20.0 | |
| | t_{pHL} | | 5.0 ± 0.5 | 15 | — | 5.9 | 9.0 | 1.0 | 10.5 | |
| | | | | 50 | — | 7.4 | 11.0 | 1.0 | 12.5 | |
| Maximum clock frequency | f_{max} | — | 3.3 ± 0.3 | 15 | 65 | 85 | — | 55 | — | MHz |
| | | | | 50 | 60 | 105 | — | 50 | — | |
| | | | 5.0 ± 0.5 | 15 | 110 | 150 | — | 90 | — | |
| | | | | 50 | 95 | 130 | — | 85 | — | |
| Input capacitance | C _{IN} | — | — | — | 4 | 10 | — | 10 | pF | |
| Power dissipation capacitance | C _{PD} | (Note) | — | — | 50 | — | — | — | pF | |

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

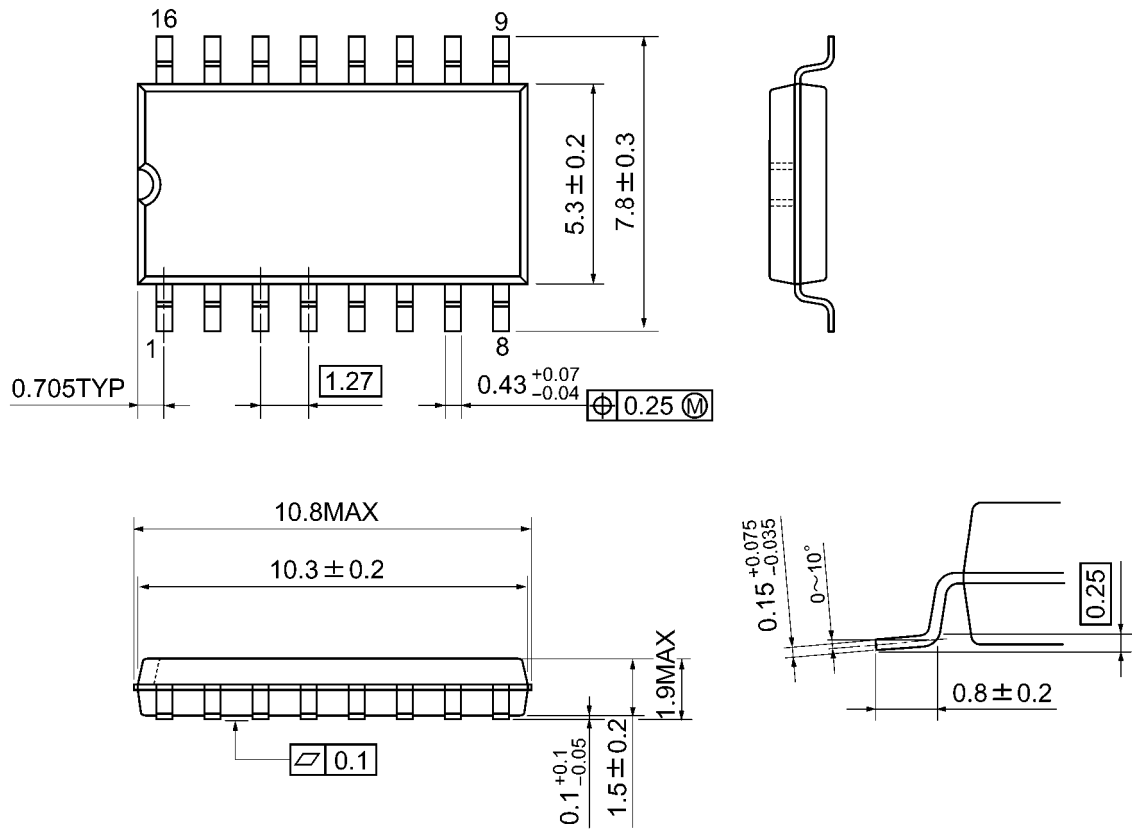
Input Equivalent Circuit



Package Dimensions

SOP16-P-300-1.27A

Unit: mm

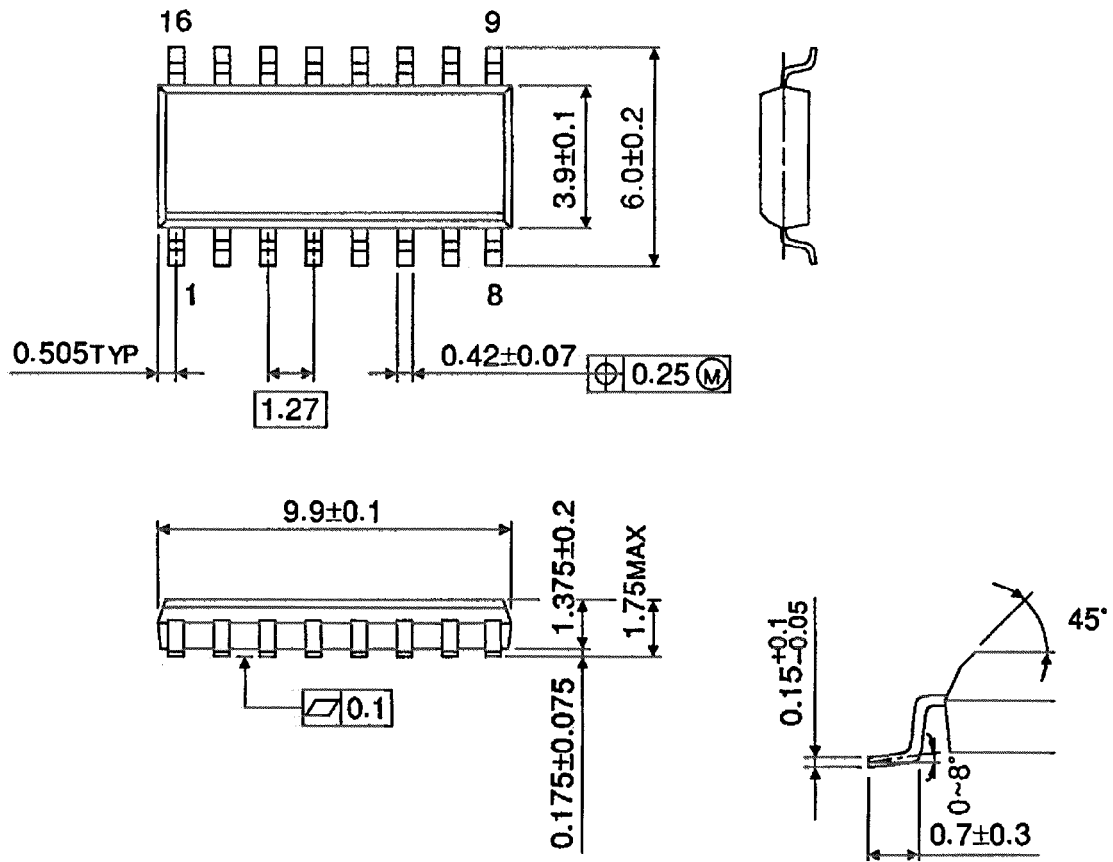


Weight: 0.18 g (typ.)

Package Dimensions (Note)

SOL16-P-150-1.27

Unit : mm



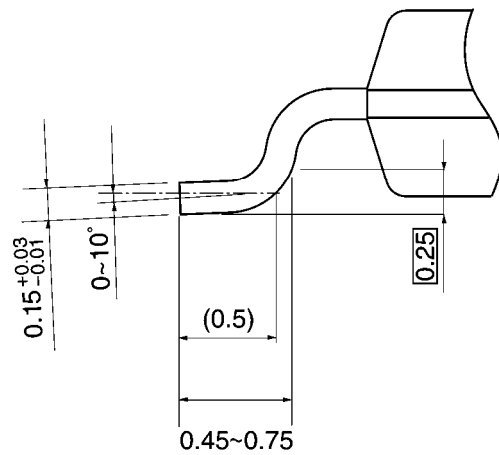
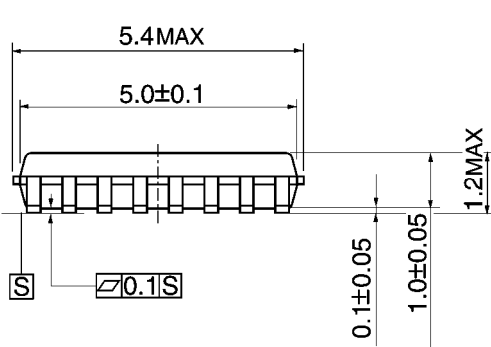
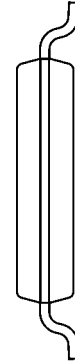
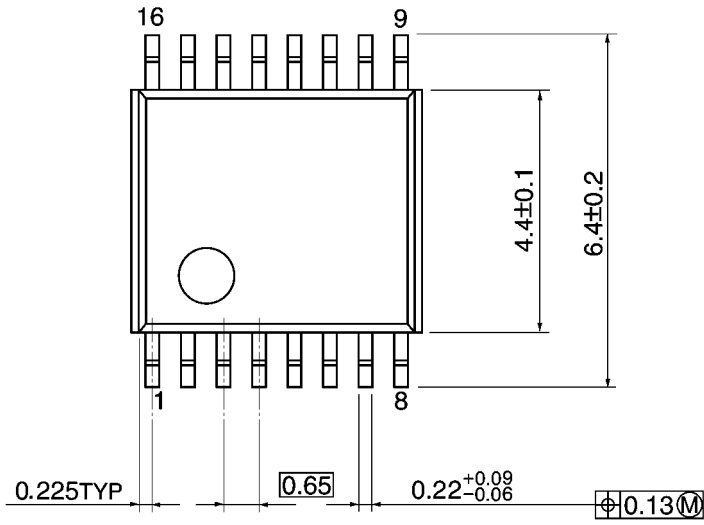
Note: This package is not available in Japan.

Weight: 0.13 g (typ.)

Package Dimensions

TSSOP16-P-0044-0.65A

Unit: mm

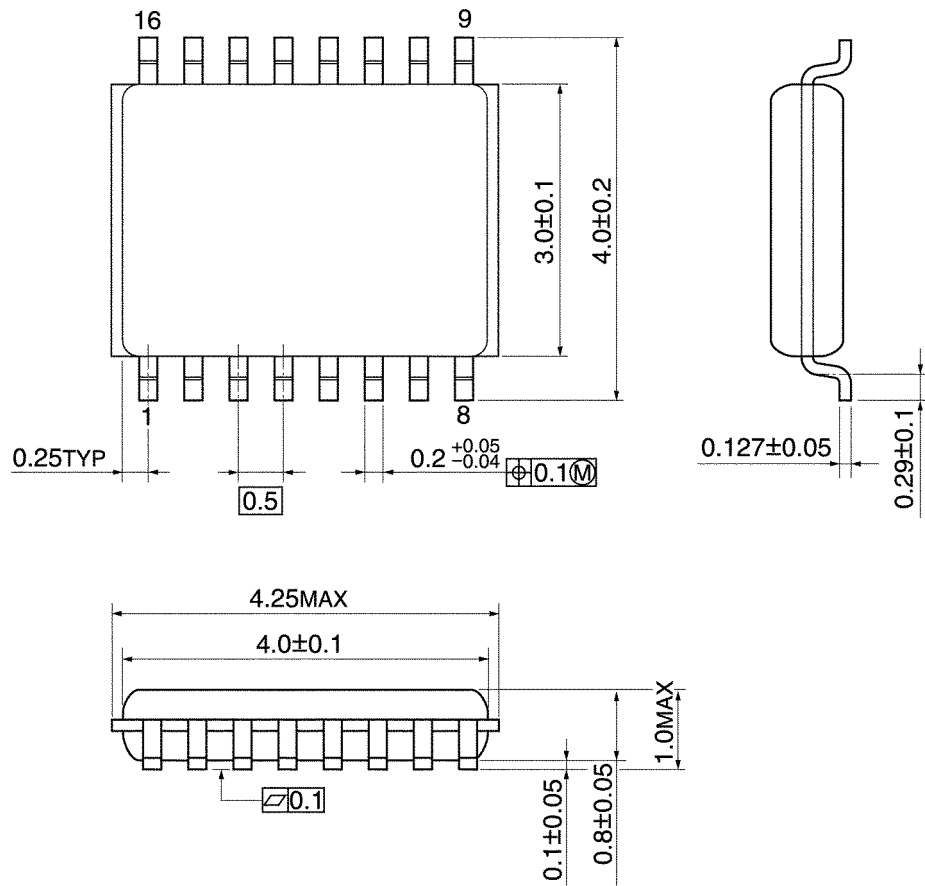


Weight: 0.06 g (typ.)

Package Dimensions

VSSOP16-P-0030-0.50

Unit: mm



Weight: 0.02 g (typ.)

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