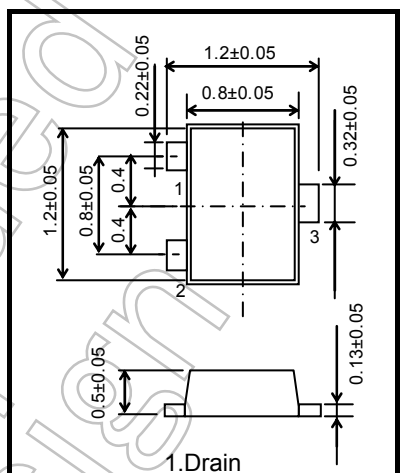
TOSHIBA Field Effect Transistor Silicon N Channel Junction Type

TTK101MFV

For ECM

Application for compact ECM
Thin package: 0.5mm
Low capacitance: Ciss = 1.8 pF (typ.) @V_{DS} = 2 V, V_{GS} = 0, f = 1MHz
Low noise: V_N = 15 mV (typ.)
@V_{DD}=2 V, RK=1kΩ, C_g=10pF, G_V=80dB, A-Cuve Filter

Unit: mm



VESM	1.Drain 2.Source 3.Gate
JEDEC	-
JEITA	-
TOSHIBA	2-1L1C

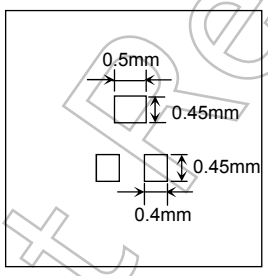
Weight: 1.5mg (typ.)

Absolute Maximum Ratings (Ta=25°C)

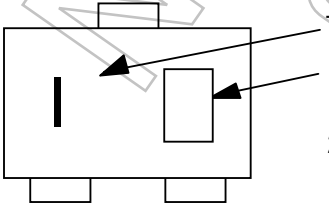
Characteristic	Symbol	Rating	Unit
Gate-drain voltage	V_{GDO}	-20	V
Gate current	I_G	10	mA
Drain power dissipation	P_D (Note 1)	150	mW
Junction temperature	T_j	125	°C
Storage temperature range	T_{stg}	−55 to 125	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Mounted on FR4 board (25.4 mm × 25.4 mm × 1.6 t)



Marking

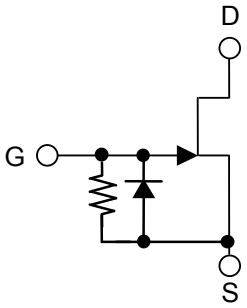


Type Name

I_{DSS} Classification Symbol
1: A-Rank
2: B-Rank

I_{DSS} Classification
A-Rank 140 to 240 μA
B-Rank 210 to 340 μA

Equivalent Circuit



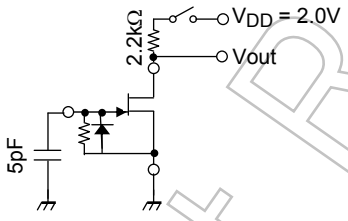
Start of commercial production
2009-03

Electrical Characteristics (Ta=25°C)

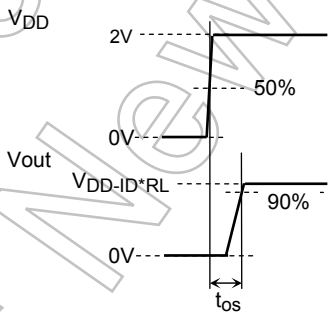
Characteristic	Symbol	Test Condition		Min	Typ.	Max	Unit
Drain current	I_{DSS}	V_{DS} = 2 V, V_{GS} = 0	A	140	—	240	μA
			B	210	—	350	
Drain current	I_D	V_{DD} = 2 V, RL= 2.2kΩ,Cg = 5pF	A	125	—	260	μA
			B	190	—	370	
Gate-source cut-off voltage	$V_{GS(OFF)}$	V_{DS} = 2 V, I_D = 1μA		-0.1	—	-1.0	V
Forward transfer admittance	$\|Y_{fs}\|$	V_{DS} = 2 V, V_{GS} = 0V		0.65	0.9	—	mS
Gate-drain breakdown voltage	$V_{(BR)GDO}$	IG = -100 μA		-20	—	—	V
Input capacitance	C_{iss}	V_{DS} = 2 V, V_{GS} = 0, f = 1 MHz		—	1.8	—	pF
Voltage gain	Gv	V_{DD} = 2V, RL= 2.2kΩ,Cg = 5pF, f = 1kHz,vin=100mV	A	-2.7	-1.3	—	dB
			B	-1.8	-0.6	—	
Delta voltage gain	DGv(f)	V_{DD} = 2V, RL= 2.2kΩ,Cg = 5pF,f = 1kHz to 100Hz,vin=100mV		—	0	-1.0	dB
Delta voltage gain	DGv(V)	V_{DD} = 2 V to 1.5 V, RL = 2.2 kΩ, Cg = 5pF,f = 1kHz, vin=100mV	A	—	-0.7	-1.4	dB
			B	—	-1.4	-3.0	
Noise voltage	VN	V_{DD} = 2 V, RL = 1 kΩ, Cg = 10 pF, Gv = 80 dB, A-Curve Filter		—	15	30	mV
Total harmonic distortion	THD	V_{DD} = 2 V, RL = 2.2kΩ, Cg = 5 pF, f = 1kHz, vin = 50mV	A	—	1.1	—	%
			B	—	0.6	—	
Time output stability	tos	V_{DD} = 2 V, RL = 2.2 kΩ, Cg = 5 pF		—	20	50	ms

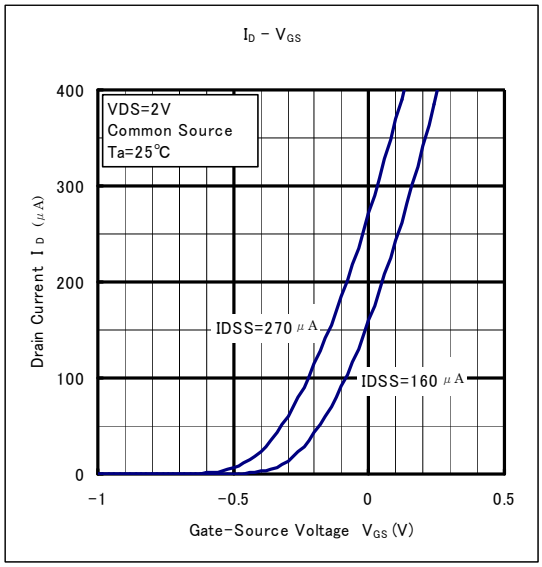
Time Output Stability Test Method

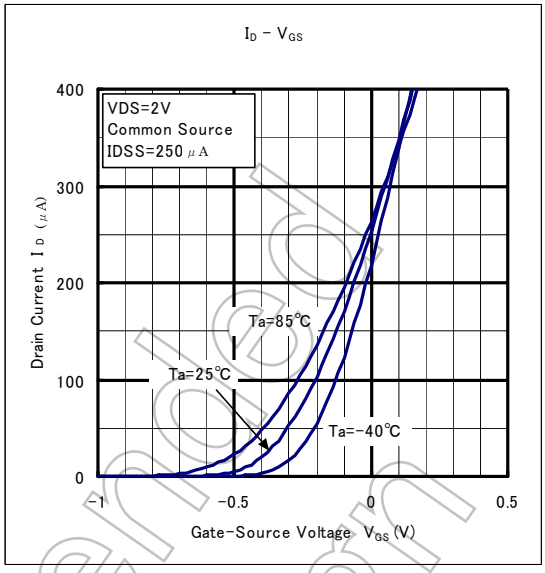
a) TEST CIRCUIT

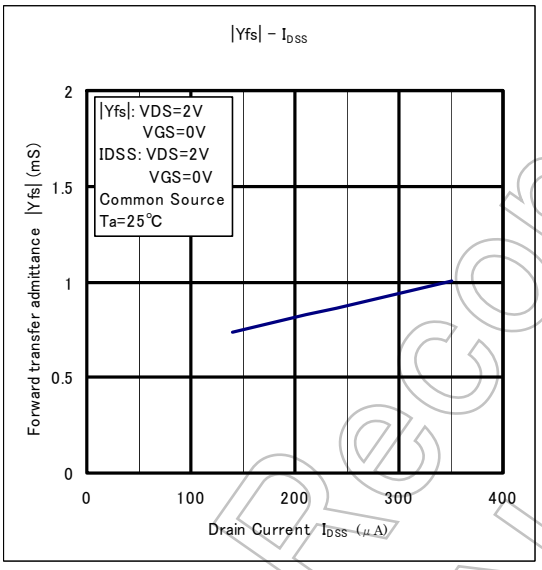


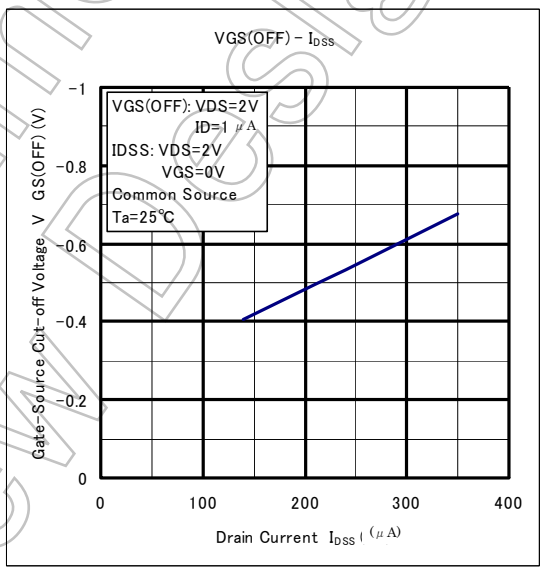
b) TEST SIGNAL

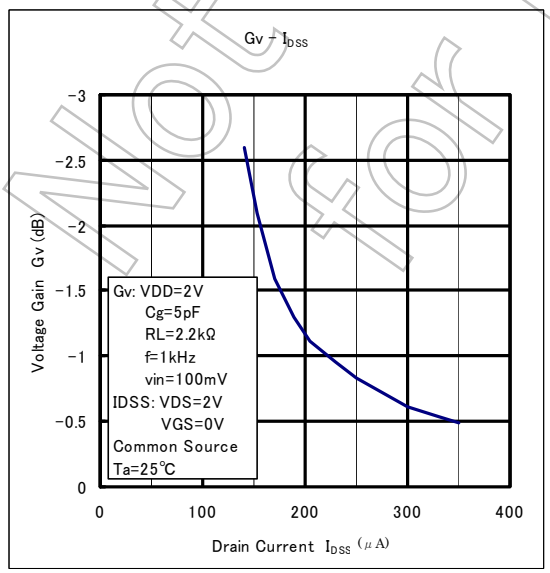


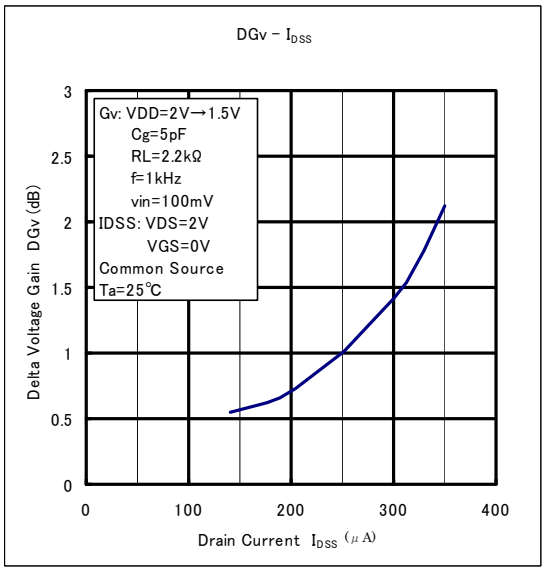


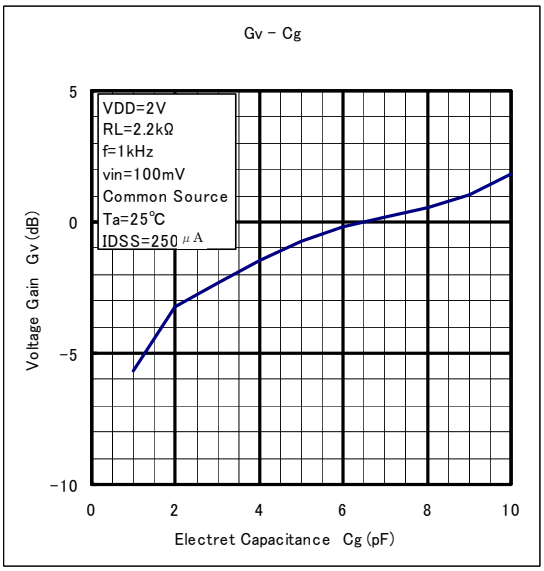


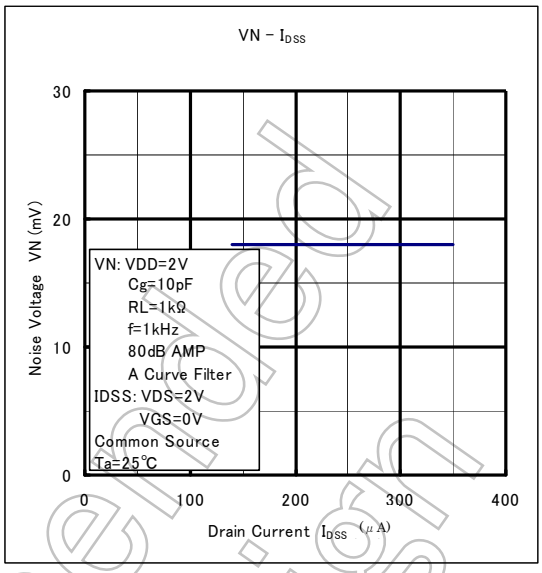


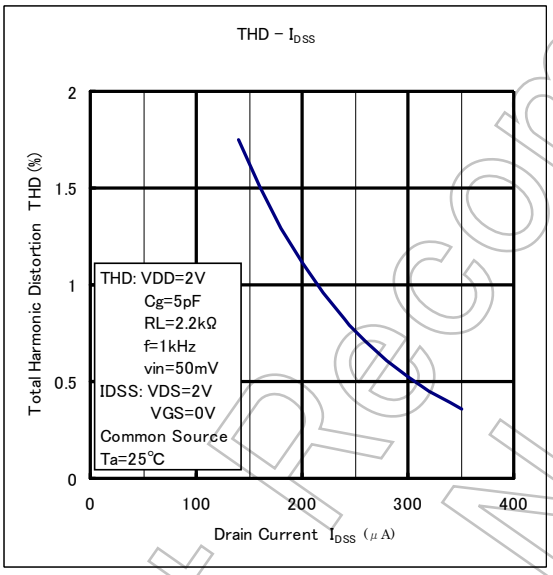


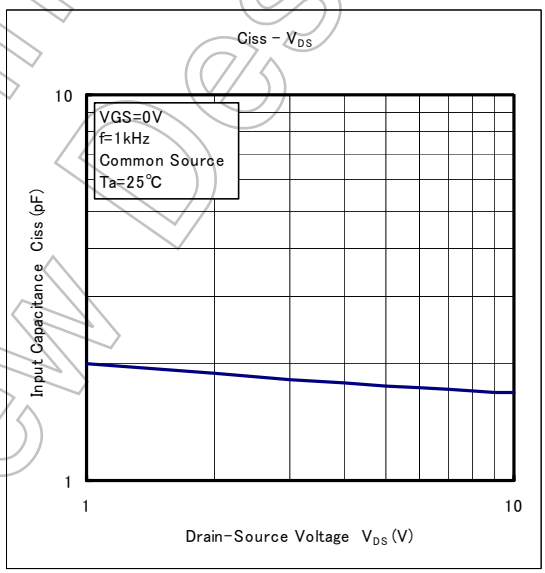












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