SARA-N2/N3 series

Multi-band NB-IoT (LTE Cat NB1 / NB2) modules

System integration manual

Abstract

This document describes the features and the system integration of the SARA-N2 series and the SARA-N3 series NB-IoT modules. These modules are a complete and cost efficient solution offering from single-band up to multi-band data transmission for the Internet of Things technology in the compact SARA form factor.

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Product status	Corresponding content status	
Functional sample	Draft	For functional testing. Revised and supplementary data will be published later.
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Engineering sample	Advance information	Data based on early testing. Revised and supplementary data will be published later.
Initial production	Early production information	Data from product verification. Revised and supplementary data may be published later.
Mass production / End of life	Production information	Document contains the final product specification.

This document applies to the following products:

Product name	Type number	Modem version	Application version	PCN reference	Product status
SARA-N200	SARA-N200-02B-00	06.57	A07.03	UBX-18005015	End of life
	SARA-N200-02B-01	06.57	A09.06	UBX-18048558	End of life
	SARA-N200-02B-02	06.57	A10.08	UBX-19030865	End of life
SARA-N201	SARA-N201-02B-00	06.57	A07.03	UBX-18005015	End of life
	SARA-N201-02B-01	06.57	A08.05	UBX-19030865	End of life
SARA-N210	SARA-N210-02B-00	06.57	A07.03	UBX-18005015	End of life
	SARA-N210-02B-01	06.57	A09.06	UBX-18048558	End of life
	SARA-N210-02B-02	06.57	A10.08	UBX-19030865	End of life
SARA-N211	SARA-N211-02X-00	06.57	A07.03	UBX-18005015	End of life
	SARA-N211-02X-01	06.57	A09.06	UBX-18048558	End of life
	SARA-N211-02X-02	06.57	A10.08	UBX-19030865	End of life
SARA-N280	SARA-N280-02B-00	06.57	A07.03	UBX-18005015	End of life
	SARA-N280-02B-01	06.57	A09.06	UBX-19030865	End of life
SARA-N300	SARA-N300-00B-00	18.03	A05.05	UBX-19042932	Engineering sample
SARA-N310	SARA-N310-00X-00	18.03	A05.05	UBX-19042932	Engineering sample

Contents

1 System description

1.1 Overview

SARA-N2/N3 series modules are Narrow Band Internet of Things (NB-IoT) solutions in the miniature SARA LGA form factor (26.0 x 16.0 mm, 96-pin), offering LTE Cat NB1 / NB2 data communication over an extended operating temperature range of –40 to +85 °C, with extremely low power consumption.

SARA-N2 series include four variants supporting single-band LTE Cat NB1 data communication for Europe, China, APAC and South America, plus a dual-band variant mainly designed for Europe.

SARA-N3 series offer multi-band LTE Cat NB2 data communication enabling multi-regional coverage, supporting several new functionalities for NB-IoT products, including features like TCP, MQTT, DTLS, SSL/TLS, LwM2M, HTTP(S) and many others.

SARA-N2/N3 series modules are ideally suited to battery-powered IoT applications characterized by occasional communications of small amounts of data.

The modules are the optimal choice for IoT devices designed to operate in locations with very limited coverage and requiring low energy consumption to permit a very long operating life with the primary batteries. Examples of applications include and are not limited to: smart grids, smart metering, telematics, street lighting, environmental monitoring and control, security and asset tracking.

Table 1 describes a summary of interfaces and features provided by SARA-N2/N3 series modules.

Module	Region	Cellular RAT			Interfaces						Features															Grade		
		3GPP release baseline	3GPP LTE Category	LTE FDD bands	UARTs	USB	DDC (I2C)	USIM	ADCs	GPIOs	Antenna supervisor	Power Save Mode	eDRX	Bluetooth 4.2 (BR/EDR and BLE)	UDP/IP, CoAP	TCP/IP, MQTT	Embedded HTTP, FTP, PPP, DNS	Embedded HTTPS, FTPS, TLS, SSL	IPv4	IPv4 / IPv6	LwM2M Device Management	Last gasp	FW update over AT (FOAT)	FW update over the air (FOTA)	Standard	Professional	Automotive
SARA-N200	Europe APAC	13	NB1	8	●			●		●		●	●		●				●				●	●		●	
SARA-N201	APAC	13	NB1	5	●			●		●		●	●		●				●				●	●		●	
SARA-N210	Europe	13	NB1	20	●			●		●		●	●		●				●				●	●		●	
SARA-N211	Europe	13	NB1	8,20	●			●		●		●	●		●				●				●	●		●	
SARA-N280	S.America APAC	13	NB1	28	●			●		●		●	●		●				●				●	●		●	
SARA-N300	China	14	NB2	3,5,8	●		○	●	●	●	●	●	●	○	●	●[1]	●	●	●	●		●	●	●		●	
SARA-N310	Global	14	NB2	3,5,8 20,28,★	●		○	●	●	●	●	●	●	○	●	●	●	●	●	●	●	●	●	●		●	

● = Supported ○ = Available in future FW ★ = Additional bands (1, 2, 4, 12, 13, 18, 19, 26, 66, 71, 85) available in future FW

Table 1: SARA-N2/N3 series characteristics summary

[1] Only TCP/IP and MQTT-SN are supported

Table 2 summarizes cellular radio access technology characteristics of SARA-N2/N3 series modules.

Item	SARA-N2 series	SARA-N3 series
Protocol stack	3GPP release 13	3GPP release 14[2]
Radio Access Technology	LTE Category NB1 Half-Duplex Single-tone Single HARQ process eDRX Power Saving Mode Coverage enhancement A and B	LTE Category NB2 Half-Duplex Multi-tone Two HARQ process eDRX Power Saving Mode Coverage enhancement A and B
Operating band	SARA-N200: • Band 8 (900 MHz) SARA-N201: • Band 5 (850 MHz) SARA-N210: • Band 20 (800 MHz) SARA-N211: • Band 8 (900 MHz) • Band 20 (800 MHz) SARA-N280: • Band 28 (700 MHz)	SARA-N300: • Band 5 (850 MHz) • Band 8 (900 MHz) • Band 20 (800 MHz) SARA-N310[3]: • Band 3 (1800 MHz) • Band 5 (850 MHz) • Band 8 (900 MHz) • Band 20 (800 MHz) • Band 28 (700 MHz)
Power Class	Class 3 (23 dBm)[4]	Class 3 (23 dBm)[4]
Deployment mode	In-Band Guard-Band Standalone	In-Band Guard-Band Standalone
Data rate	Up to 31.25 kb/s UL Up to 27.2 kb/s DL	Up to 140 kb/s UL Up to 125 kb/s DL
Protocols and other	UDP IP CoAP	TCP IP / UDP IP CoAP / DTLS MQTT[5] MQTT-SN LwM2M Device Management Objects[5] HTTP/HTTPS FTP/FTPS PPP/DNS SSL, TLS Radio Policy Manager[5] SIM provisioning[5]

Table 2: SARA-N2/N3 series NB-IoT characteristics summary

[2] Key subset of features
[3] Additional bands (1, 2, 4, 12, 13, 18, 19, 26, 66, 71, 85) available in future FW versions
[4] Configurable to other Power Class by AT command
[5] Not supported by SARA-N300-00B

1.2 Architecture

Figure 1 and Figure 2 summarize the architecture of SARA-N2 series and SARA-N3 series modules respectively, describing the internal blocks of the modules, consisting of the RF, Baseband and Power Management main sections, and the available interfaces.

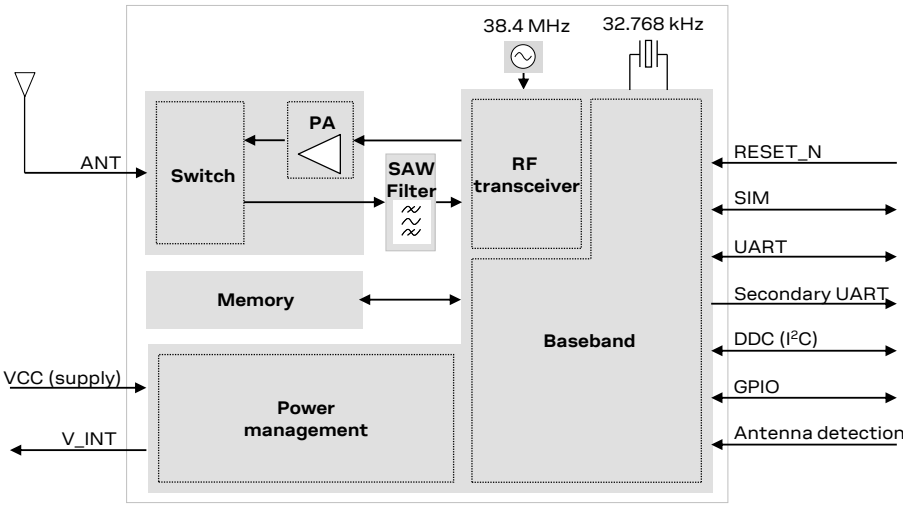

Figure 1: SARA-N2 series modules block diagram

The “02" product version of SARA-N2 series modules do not support the following interfaces, which should not be driven by external devices:

- Antenna detection
- DDC (I2C) interface

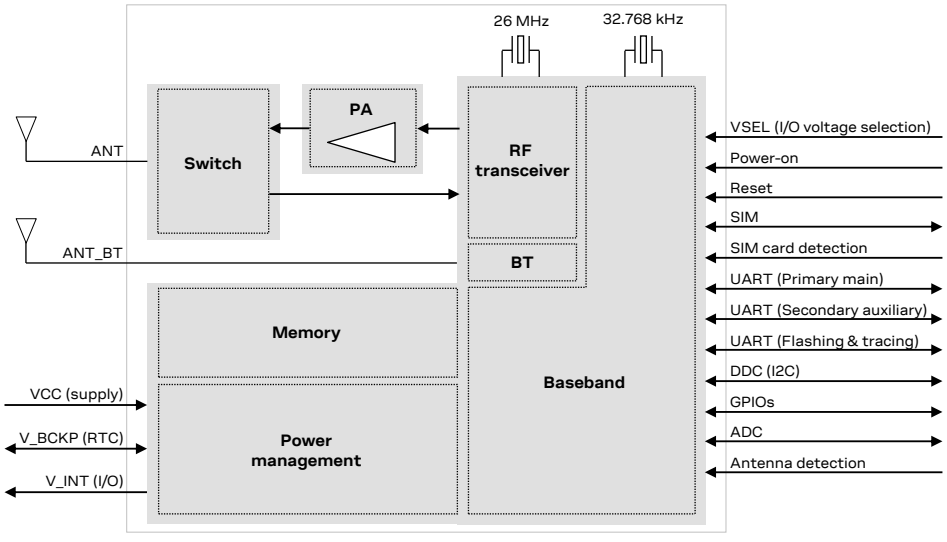

Figure 2: SARA-N3 series block diagram

The “00" product version of SARA-N3 series modules do not support the following interfaces, which should not be driven by external devices:

- Bluetooth interface (ANT_BT)
- Secondary auxiliary UART interface (UART AUX)
- DDC (I2C) interface

The RF section is composed of the following main elements:

- LTE power amplifier, which amplifies the signals modulated by the RF transceiver
- RF switches, which connect the antenna input/output pin (**ANT**) of the module to the suitable RX/TX path
- RX low-loss filters
- 38.4 MHz (SARA-N2 series) / 26.0 MHz (SARA-N3 series) crystal oscillator for the clock reference in active-mode and connected-mode

The Baseband and Power Management section is composed of the following main elements:

- Baseband processor
- Flash memory
- Voltage regulators to derive all the system supply voltages from the module supply **VCC**
- Circuit for the RTC clock reference in low power deep-sleep

1.3 Pin-out

Table 3 lists the pin-out of the SARA-N2/N3 series modules, with pins grouped by function

Function	Pin name	Modules	Pin No	I/O	Description	Remarks
Power	**VCC**	All	51,52,53	I	Module supply input	All **VCC** pins must be connected to external supply. **VCC** supply circuit affects the RF performance and compliance of the device integrating the module with applicable required certification schemes. See section 1.5.1 for description and requirements. See section 2.2.1 for external circuit design-in.
	GND	All	1,3,5,14, 20,22,30, 32,43,50, 54,55,57, 58,60,61, 63-96	N/A	Ground	All **GND** pins have to be connected to external ground. External ground connection affects the RF and thermal performance of the device. See section 2.2.1.8 for external circuit design-in.
	GND	SARA-N2	21,59	N/A	Ground	All **GND** pins have to be connected to external ground. External ground connection affects the RF and thermal performance of the device. See section 2.2.1.8 for external circuit design-in.
	V_BCKP	SARA-N3	2	I/O	RTC supply input/output	See section 1.5.2 for functional description. See section 2.2.2 for external circuit design-in.
	V_INT	All	4	O	Generic Digital Interfaces supply output	SARA-N2 modules: • Supply output generated by internal linear LDO regulator when the radio is on • Voltage domain of I2C and GPIOs • **V_INT** = 1.8 V (typical) SARA-N3 modules: • Supply output generated by internal linear LDO regulator when the module is on • Voltage domain of UARTs, I2C and GPIOs • **V_INT** = 1.8 V (typ.), if **VSEL** is connected to GND • **V_INT** = 2.8 V (typ.), if **VSEL** is unconnected Provide a test point on this pin for diagnostic purpose. See section 1.5.3 for functional description. See section 2.2.3 for external circuit design-in.

Function	Pin name	Modules	Pin No	I/O	Description	Remarks
System	**PWR_ON**	SARA-N3	15	I	Power-on input	Internal pull-up. Provide a test point on this pin for diagnostic purpose. See section 1.6.1, 1.6.2 for functional description. See section 2.3.1 for external circuit design-in.
	RESET_N	All	18	I	HW reset input	Internal pull-up. Provide a test point on this pin for diagnostic purpose. See section 1.6.3 for functional description. See section 2.3.2 for external circuit design-in.
	VSEL	SARA-N3	21	I	Voltage selection	Input to select the operating voltage of the **V_INT** supply output, voltage domain of UARTs, I2C, GPIOs. **V_INT** = 1.8 V (typical), if **VSEL** pin is connected to GND **V_INT** = 2.8 V (typical), if **VSEL** pin is unconnected See section 1.6.4 for functional description. See section 2.3.3 for external circuit design-in.
Antenna	**ANT**	All	56	I/O	Cellular RF input/output	50 Ω nominal characteristic impedance. Antenna circuit affects the RF performance and compliance of the device integrating the module with applicable required certification schemes. See section 1.7.1 for description and requirements. See section 2.4.1 for external circuit design-in.
	ANT_BT	SARA-N3	59	I/O	Bluetooth RF input/output	50 Ω nominal characteristic impedance. See section 1.7.2 for description and requirements. See section 2.4.2 for external circuit design-in.
	ANT_DET	All	62	I	Input for antenna detection	ANT_DET not supported by SARA-N2 modules. ADC input usable for antenna detection function. See section 1.7.3 for functional description. See section 2.4.3 for external circuit design-in.
SIM	**VSIM**	All	41	O	SIM supply output	Supply output for external SIM / UICC See section 1.8 for functional description. See section 2.5 for external circuit design-in.
	SIM_IO	All	39	I/O	SIM data	Data line for communication with external SIM, operating at **VSIM** voltage level. Internal 4.7 kΩ pull-up to **VSIM**. See section 1.8 for functional description. See section 2.5 for external circuit design-in.
	SIM_CLK	All	38	O	SIM clock	Clock for external SIM, operating at **VSIM** voltage level. See section 1.8 for functional description. See section 2.5 for external circuit design-in.
	SIM_RST	All	40	O	SIM reset	Reset for external SIM, operating at **VSIM** voltage level See section 1.8 for functional description. See section 2.5 for external circuit design-in.
UART (main)	**RXD**	All	13	O	Data output	Circuit 104 (RXD) in ITU-T V.24 SARA-N2 modules: • Supporting AT communication, FOAT and FW upgrade via dedicated tool • **VCC** voltage level SARA-N3 modules: • Supporting AT communication and FOAT • **V_INT** voltage level Provide a test point on this pin for diagnostic purpose. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.

Function	Pin name	Modules	Pin No	I/O	Description	Remarks
	TXD	All	12	I	Data input	Circuit 103 (TXD) in ITU-T V.24 SARA-N2 modules: • Supporting AT communication, FOAT and FW upgrade via dedicated tool • **VCC** voltage level, without internal pull-up/down SARA-N3 modules: • Supporting AT communication and FOAT • **V_INT** voltage level, with internal pull-up Provide a test point on this pin for diagnostic purpose. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	CTS	All	11	O	Clear To Send output	Circuit 106 (CTS) in ITU-T V.24 SARA-N2 modules: • HW flow control not supported by “02” versions • Configurable as RI and other • **VCC** voltage level SARA-N3 modules: • HW flow control output • Configurable as RI and other • **V_INT** voltage level See section 1.9.1 and 1.11 for functional description. See section 2.6.1 for external circuit design-in.
	RTS	All	10	I	Request To Send input	Circuit 105 (RTS) in ITU-T V.24 SARA-N2 modules: • HW flow control not supported by “02” versions • **VCC** voltage level, with internal pull-up SARA-N3 modules: • HW flow control input • **V_INT** voltage level, with internal pull-up by default See section 1.9.1 and 1.11 for functional description. See section 2.6.1 for external circuit design-in.
	RI	SARA-N3	7	O	Ring Indicator	Circuit 125 (RI) in ITU-T V.24, at **V_INT** voltage level See section 1.9.1 and 1.11 for functional description. See section 2.6.1 for external circuit design-in.
	DSR	SARA-N3	6	O	Data Set Ready	Circuit 107 (DSR) in ITU-T V.24, at **V_INT** voltage level DSR not supported by ‘00’ product versions. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	DCD	SARA-N3	8	O	Data Carrier Detect	Circuit 109 (DCD) in ITU-T V.24, at **V_INT** voltage level DCD not supported by ‘00’ product versions. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	DTR	SARA-N3	9	I	Data Terminal Ready	Circuit 108/2 (DTR) in ITU-T V.24, at **V_INT** voltage level DTR not supported by ‘00’ product versions. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
UART (auxiliary)	**RXD_AUX**	SARA-N3	19	O	Data output	Circuit 104 (RXD) in ITU-T V.24, at **V_INT** voltage level UART AUX not supported by ‘00’ product versions. See section 1.9.2 for functional description. See section 2.6.2 for external circuit design-in.
	TXD_AUX	SARA-N3	17	I	Data input	Circuit 103 (TXD) in ITU-T V.24, at **V_INT** voltage level UART AUX not supported by ‘00’ product versions. See section 1.9.2 for functional description. See section 2.6.2 for external circuit design-in.

Function	Pin name	Modules	Pin No	I/O	Description	Remarks
UART (additional)	**RXD_FT**	SARA-N3	28	O	Data output	Circuit 104 (RXD) in ITU-T V.24, at **V_INT** voltage level. Supporting FW update via dedicated tool and Trace log. Provide a test point for FW upgrade and diagnostic. See section 1.9.3 for functional description. See section 2.6.3 for external circuit design-in.
	TXD_FT	SARA-N3	29	I	Data input	Circuit 103 (TXD) in ITU-T V.24, at **V_INT** voltage level. Supporting FW update via dedicated tool and Trace log. Provide a test point for FW upgrade and diagnostic. See section 1.9.3 for functional description. See section 2.6.3 for external circuit design-in.
	GPIO1	SARA-N2	16	O	Data output	Circuit 104 (RXD) in ITU-T V.24, at **V_INT** voltage level. Supporting Trace diagnostic logging. Provide a test point on this pin for diagnostic. See sections 1.9.3 and 1.11 for functional description. See sections 2.6.3 and 2.8 for external circuit design-in.
DDC	**SCL**	All	27	O	I2C bus clock line	Open drain, at **V_INT** voltage level. I2C not supported by SARA-N2 modules "02" versions. I2C not supported by SARA-N3 modules "00" versions. See section 1.9.4 for functional description. See section 2.6.4 for external circuit design-in.
	SDA	All	26	I/O	I2C bus data line	Open drain, at **V_INT** voltage level. I2C not supported by SARA-N2 modules "02" versions. I2C not supported by SARA-N3 modules "00" versions. See section 1.9.4 for functional description. See section 2.6.4 for external circuit design-in.
GPIO	**GPIO1**	SARA-N3	16	I/O	GPIO	GPIO, at **V_INT** voltage level. See section 1.11 for functional description. See section 2.8 for external circuit design-in.
	GPIO2	SARA-N2	24	I/O	GPIO	GPIO2 not supported by "02" product versions.
		SARA-N3	23	I/O	GPIO	GPIO, at **V_INT** voltage level. See section 1.11 for functional description. See section 2.8 for external circuit design-in.
	GPIO3	SARA-N3	24	I/O	GPIO	GPIO, at **V_INT** voltage level. See section 1.11 for functional description. See section 2.8 for external circuit design-in.
	GPIO4	SARA-N3	25	I/O	GPIO	GPIO, at **V_INT** voltage level. See section 1.11 for functional description. See section 2.8 for external circuit design-in.
	GPIO5	SARA-N3	42	I/O	GPIO	GPIO, at **V_INT** voltage level. See section 1.11 for functional description. See section 2.8 for external circuit design-in.
ADC	**ADC1**	SARA-N3	33	I	ADC input	See section 1.10 for functional description. See section 2.7 for external circuit design-in.
Reserved	**RSVD**	SARA-N2	33	N/A	RESERVED pin	This pin can be connected to GND. See sections 1.12 and 2.9.
	RSVD	SARA-N2	2, 6-9, 15,17,19, 23, 25, 28,29,42	N/A	RESERVED pin	Leave unconnected. See sections 1.12 and 2.9.
	RSVD	All	31,34-37, 44-49	N/A	RESERVED pin	Leave unconnected. See sections 1.12 and 2.9.

Table 3: SARA-N2/N3 series modules pin definition, grouped by function

1.4 Operating modes

SARA-N2/N3 series modules have several operating modes as defined in Table 4.

General Status	Operating Mode	Definition
Power-down	**Not-Powered mode**	**VCC** supply not present or below the operating range. The module is switched off.
	Power-Off mode [6]	**VCC** supply within the operating range, with the module switched off.
Normal operation	**Deep-sleep mode**	Module processor runs with internal 32 kHz reference. Lowest possible power mode, with current consumption in the ~µA range.
	Sleep mode [6]	Module processor runs with internal 32 kHz reference. PSRAM does not power down, with current consumption in the ~100 µA range.
	Idle mode [6]	Module processor runs with internal 32 kHz reference. Low power mode, with current consumption in the ~mA range.
	Active mode	Module processor runs with internal 38.4 MHz / 26 MHz reference. Data transmission or reception not in progress.
	Connected mode	Module processor runs with internal 38.4 MHz / 26 MHz reference. Data transmission or reception in progress.

Table 4: SARA-N2/N3 series modules' operating modes definition

Figure 3 and Figure 4 illustrate the transition between the different operating modes.

The initial operating mode of SARA-N2/N3 series modules is the one with **VCC** supply not present or below the operating range: the modules are switched off in non-powered mode**.**

Once a valid **VCC** supply is applied to the SARA-N2 modules, this event triggers the switch on routine of the modules that subsequently enter the active mode.

On the other hand, once a valid **VCC** supply is applied to the SARA-N3 modules, they remain switched off in power-off mode. Then the proper toggling of the **PWR_ON** or **RESET_N** input line is necessary to trigger the switch on routine of the modules that subsequently enter the active mode.

SARA-N2/N3 series modules are fully ready to operate when in active mode.

Then, the SARA-N2 modules switch from active mode to deep sleep mode whenever possible, entering the lowest possible power mode, with current consumption in the ~µA range. The UART interface is still completely functional and the module can accept and respond to any AT command, entering back into the active mode as in case of network paging reception and as in case of expiration of the "Periodic Update Timer" according to the Power Saving Mode defined in 3GPP release 13.

Instead, the SARA-N3 modules switch from active mode to the idle mode whenever possible, entering the low power mode, if enabled by a dedicated AT command, with current consumption in the ~mA range. The UART interface is still completely functional and the module can accept and respond to any AT command, entering back into the active mode as in case of network paging reception.

According to AT+NVSETPM setting, the SARA-N3 modules can switch between modes. It can switch from active mode to sleep mode if the eDRX feature is enabled and set to let the module go to sleep for time periods of less than 300 s. It can switch from active mode to deep sleep mode if the Power Saving Mode is enabled or if the eDRX feature is enabled and set to let the module go to sleep for time periods of more than 300 s, thus entering the lowest possible power mode, with current consumption in the ~µA range (Power Saving Mode and eDRX are defined in 3GPP release 13). In both sleep mode and deep sleep mode, the UART interface is not functional: a wake up event, consisting for example in proper toggling of the **PWR_ON** line or in expiration of the "Periodic Update Timer", is necessary to trigger the wake up routine of the modules that subsequently enter back into the active mode.

☞ See the SARA-N2 / SARA-N3 series AT commands manual [4] for the +NVSETPM AT command and for configuration of PSM and eDRX features.

[6] Not available in SARA-N2 series modules

SARA-N2/N3 series modules switch from active mode to connected mode upon RF transmission or reception operations turning back to active mode once RF operations are terminated or suspended.

The switch off routine of the SARA-N3 modules can be properly triggered by the dedicated AT command or by proper toggling of the **PWR_ON** line. The modules subsequently enter the power-off mode and then they enter the non-powered mode by removing the **VCC** supply.

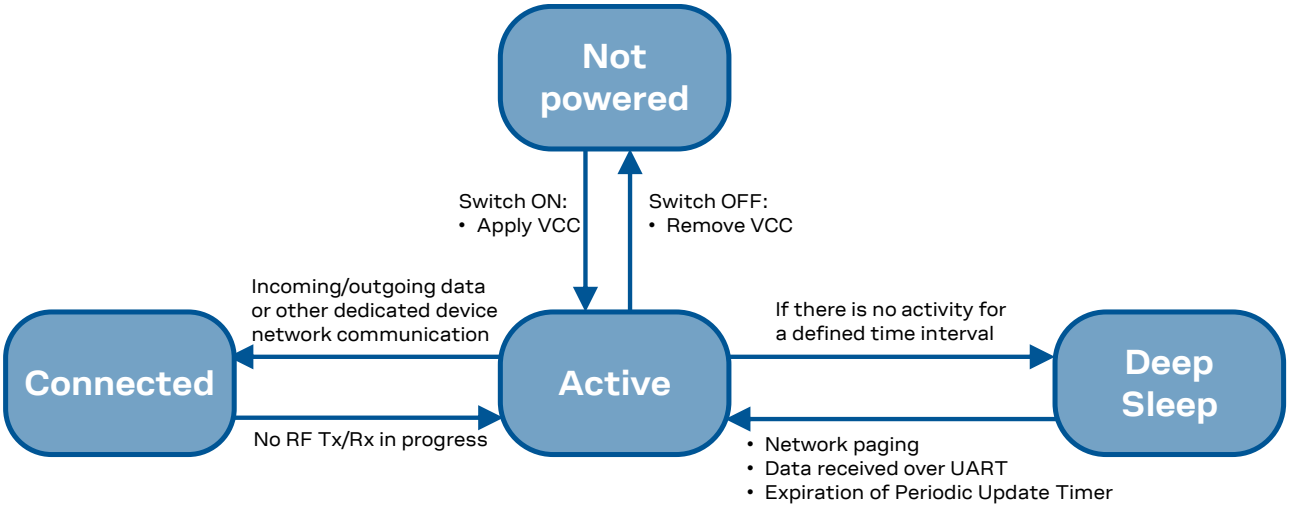

Figure 3: SARA-N2 series modules' operating modes transitions

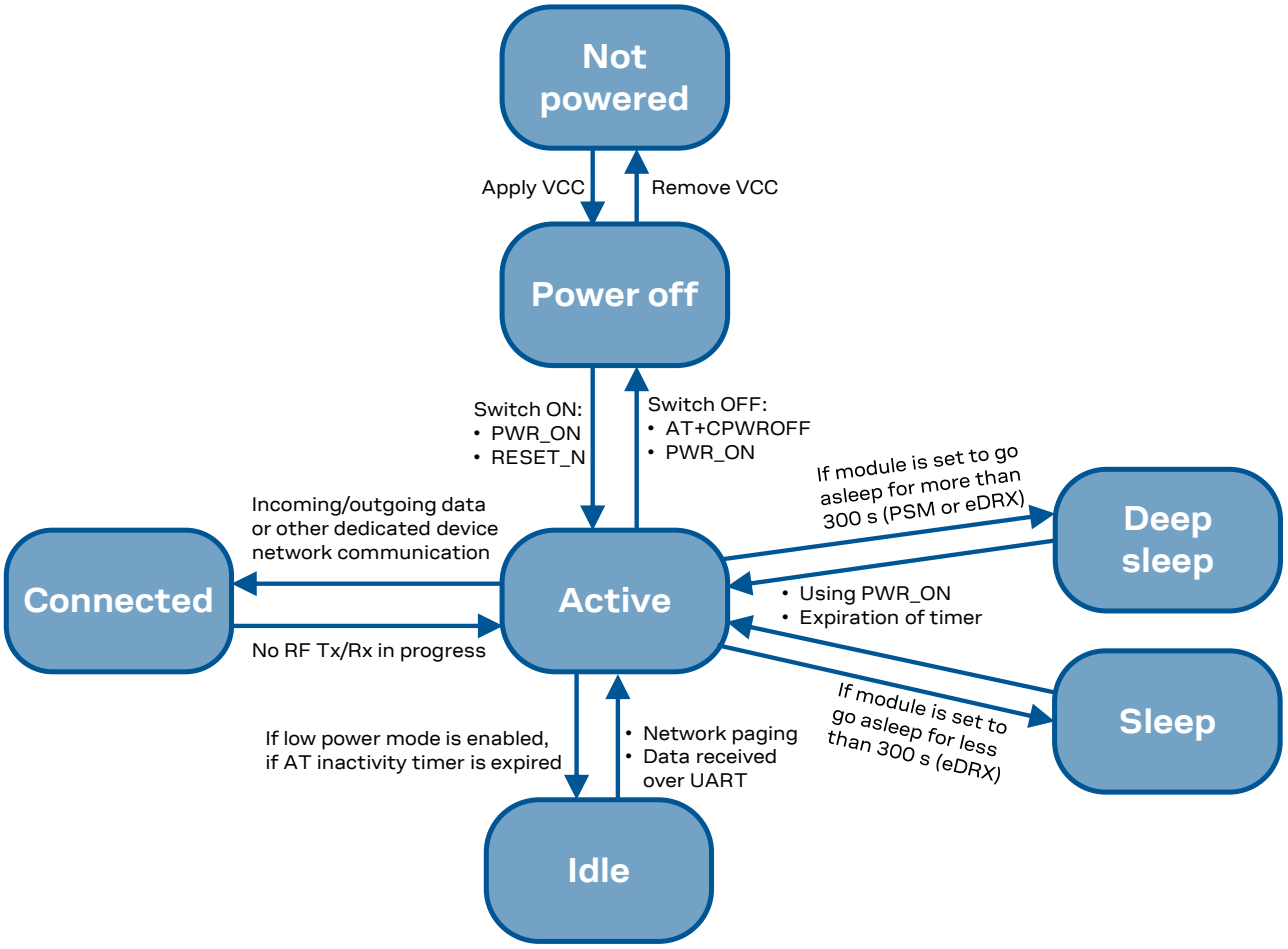

Figure 4: SARA-N3 series modules' operating modes transitions

1.5 Supply interfaces

1.5.1 Module supply input (VCC)

The modules must be supplied via all the three **VCC** pins that represent the module power supply input.

The **VCC** pins are internally connected to the RF power amplifier and to the integrated Power Management Unit: all supply voltages needed by the module are generated from the **VCC** supply by integrated voltage regulators, including **V_INT** (digital interfaces supply) and **VSIM** (SIM card supply).

During operation, the current drawn by the SARA-N2/N3 series modules through the **VCC** pins can vary by several orders of magnitude. This ranges from the high peak of current consumption during data transmission at maximum power level in connected mode, to the low current consumption during deep-sleep mode (as described in section 1.5.1.2).

1.5.1.1 VCC supply requirements

Table 5 summarizes the requirements for the **VCC** module supply. See section 2.2.1 for all the suggestions to properly design a **VCC** supply circuit compliant to the requirements listed in Table 5.

⚠ VCC supply circuit design may affect the RF compliance of the device integrating SARA-N2/N3 series modules with applicable required certification schemes. Compliance is not guaranteed if the VCC requirements summarized in the Table 5 are not fulfilled.

Item	Requirement	Remark
VCC nominal voltage	Within **VCC** normal operating range: • SARA-N2: 3.1 V min. / 4.0 V max • SARA-N3: 3.2 V min. / 4.2 V max	The module cannot be switched on if **VCC** voltage value is below the normal operating range minimum limit. Ensure that the input voltage at **VCC** pins is above the minimum limit of the normal operating range for at least more than 3 s after the module switch-on.
VCC voltage during normal operation	Within **VCC** extended operating range: • SARA-N2: 2.75 V min. / 4.2 V max • SARA-N3: 2.6 V min. / 4.2 V max	The module may switch off when **VCC** voltage drops below the extended operating range minimum limit. Operation above extended operating range limit is not recommended and may affect device reliability. When operating below the normal operating range minimum limit, the internal PA may not be able to transmit at the network-required power level.
VCC average current	Support with margin the highest averaged **VCC** current consumption value in connected mode specified in the SARA-N2 data sheet [1] or in the SARA-N3 data sheet [2].	The maximum average current consumption can be greater than the specified value according to the actual antenna mismatching, temperature and supply voltage.
VCC voltage ripple	Noise in the supply has to be minimized	High supply voltage ripple values during RF transmissions in connected-mode directly affect the RF compliance with applicable certification schemes.

Table 5: Summary of VCC supply requirements

☞ For the additional specific requirements applicable to the integration of the SARA-N211 and the SARA-N310 modules in devices intended for use in potentially explosive atmospheres, see the guidelines reported in section 2.12.

1.5.1.2 VCC current consumption profile

Figure 5 shows an example of the module **VCC** current consumption profile starting from the switch-on event, followed by different phases and operating modes:

- Network registration and context activation procedure
- Transmission of an up-link datagram
- RRC connection release and related signaling operations
- Cyclic paging reception
- Deep sleep mode

Timings in the figure are purely indicative since these may significantly change depending on the network signaling activity. The current consumption peaks occur when the module is in the connected (transmitting) mode and the value of these peaks is strictly dependent on the transmitted power, which is regulated by the network. See the electrical specification section in the SARA-N2 series data sheet [1] or SARA-N3 series data sheet [2] for more details about the current consumption values in the different modes and the influence of the transmitting power level.

A proper power supply circuit for SARA-N2/N3 series modules must be able to withstand the current values present during the data transmission at maximum power, even though NB-IoT systems should be designed to keep the module in deep-sleep mode for most of the time, with an extremely low current consumption in the range of few microamps.

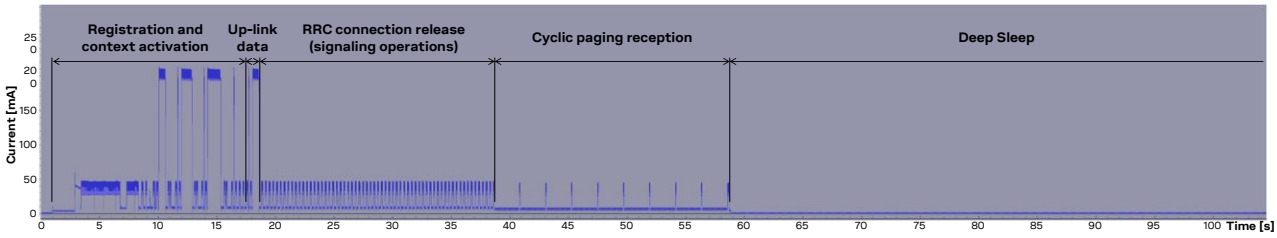

Figure 5: Example of module current consumption from the switch-on event up to deep-sleep mode

1.5.2 RTC supply (V_BCKP)

☞ The RTC supply (**V_BCKP** pin) is not available on SARA-N2 series modules.

V_BCKP is the Real Time Clock (RTC) supply of SARA-N3 series modules. When **VCC** voltage is within the valid operating range, the internal Power Management Unit (PMU) supplies the RTC and the same supply voltage is available on the **V_BCKP** pin. If the **VCC** voltage is under the minimum operating limit (e.g. during non powered mode), the RTC can be externally supplied through the **V_BCKP** pin.

1.5.3 Interfaces supply output (V_INT)

The same voltage domain internally used as supply for the generic digital interfaces of SARA-N2/N3 series modules is also available on the **V_INT** output pin, as illustrated in Figure 6.

In detail, the **V_INT** supply rail is used internally to supply the:

- I2C interface, and the GPIO pins of SARA-N2 series modules
- UART interfaces, the I2C interface, and the GPIO pins of SARA-N3 series modules

The internal regulator that generates the **V_INT** supply output is a low drop out (LDO) converter, which is directly supplied from the **VCC** main supply input of the module.

The **V_INT** supply output provides internal short circuit protection to limit start-up current and protect the load to short circuits.

The **V_INT** voltage regulator output of SARA-N2 series modules is disabled (i.e. 0 V) when the module is switched off, and it can be used to monitor the operating mode when the module is switched on:

- When the radio is off, the voltage level is low (i.e. 0 V)
- When the radio is on, the voltage level is high (i.e. 1.8 V)

The **V_INT** voltage regulator output of SARA-N3 series modules is disabled (i.e. 0 V) when the module is switched off, and it can be used to monitor the operating mode of the module as follows:

- When the module is off, or in deep sleep mode, the voltage level is low (i.e. 0 V)
- When the module is on, outside deep sleep mode, the voltage level is high (i.e. 1.8 V or 2.8 V)

The **V_INT** operating voltage of SARA-N3 series modules can be selected using the **VSEL** input pin:

- If **VSEL** input pin is connected to **GND**, the digital I/O interfaces operate at 1.8 V
- If **VSEL** input pin is left unconnected, the digital I/O interfaces operate at 2.8 V

☞ Provide a test point connected to the **V_INT** pin for diagnostic purpose.

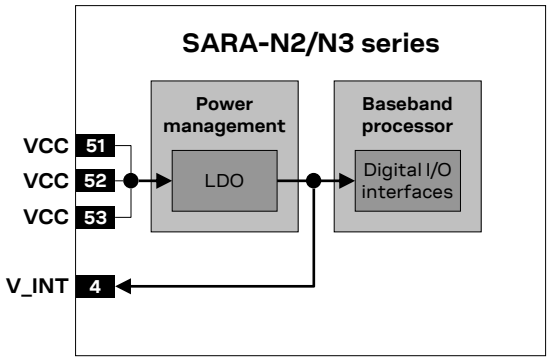

Figure 6: SARA-N2/N3 series interfaces supply output (V_INT) simplified block diagram

1.6 System function interfaces

1.6.1 Module power-on

1.6.1.1 Switch-on events

When the SARA-N2 series modules are in the non-powered mode (i.e. switched off, with the **VCC** module supply not applied), the switch on routine of the module can be triggered by:

- Rising edge on the **VCC** supply input to a valid voltage value for module supply, starting from a voltage value lower than 1.8 V, so that the module switches on applying a proper **VCC** supply within the normal operating range (see SARA-N2 series data sheet [1]).
- Alternately, the **RESET_N** pin can be held low during the **VCC** rising edge, so that the module switches on by releasing the **RESET_N** pin when the **VCC** voltage stabilizes at its nominal value within the normal range.

When the SARA-N3 series modules are in the non-powered mode (i.e. switched off, with the **VCC** module supply not applied), the switch on routine of the module can be triggered by:

- Applying a **VCC** supply within the normal operating range of the module, and then forcing a low level on the **PWR_ON** input pin (normally high due to internal pull-up) for a valid time period (see SARA-N3 series data sheet [2]).
- Applying a **VCC** supply within the normal operating range of the module, and then forcing a low level on the **RESET_N** input pin (normally high due to internal pull-up) for a valid time period (see SARA-N3 series data sheet [2]).
- Alternately, the **RESET_N** pin can be held low during the **VCC** rising edge, so that the module switches on by releasing the **RESET_N** pin when the **VCC** voltage stabilizes at its nominal value within the normal range.

When the SARA-N3 series modules are in power off mode (i.e. switched off, with valid **VCC** supply applied), the switch on routine of the module can be triggered by:

- Forcing a low level on the **PWR_ON** input pin (normally high due to internal pull-up) for a valid time period (see SARA-N3 series data sheet [2]).
- Forcing a low level on the **RESET_N** input pin (normally high due to internal pull-up) for a valid time period (see SARA-N3 series data sheet [2]).

When the SARA-N3 series modules are in deep sleep mode (i.e. in the Power Saving Mode defined by 3GPP Rel. 13, with valid **VCC** supply applied), the wake-up routine of the module can be triggered by:

- Forcing a low level on the **PWR_ON** input pin (normally high due to internal pull-up) for a valid time period (see SARA-N3 series data sheet [2]).

As illustrated in Figure 7, the **PWR_ON** line of SARA-N3 modules is equipped with an internal pull-up.

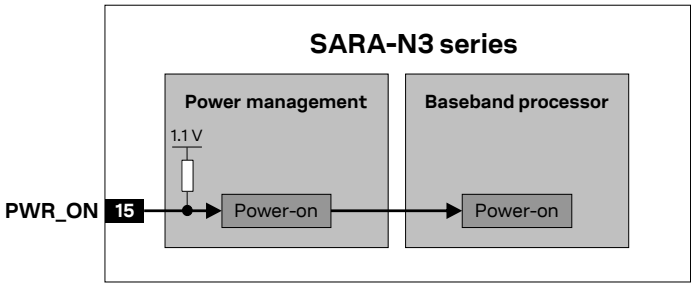

Figure 7: SARA-N3 series PWR_ON input equivalent circuit description

The **PWR_ON** input pin is not available on SARA-N2 series modules.

1.6.1.2 Switch-on sequence from not-powered mode

Figure 8 shows the switch-on sequence of SARA-N2 modules starting from the non-powered mode:

- The external supply is being applied to the **VCC** inputs, representing the start-up event.
- The **RESET_N** line rises suddenly to high logic level due to internal pull-up to **VCC**.
- Then, the **V_INT** generic digital interfaces supply output is enabled by the integrated PMU.
- The **RXD** UART data output pin also rises to the high logic level, at **VCC** voltage value
- A greeting message is sent on the **RXD** pin (for more details see AT commands manual [4])
- From now on the module is fully operational and the UART interface is functional

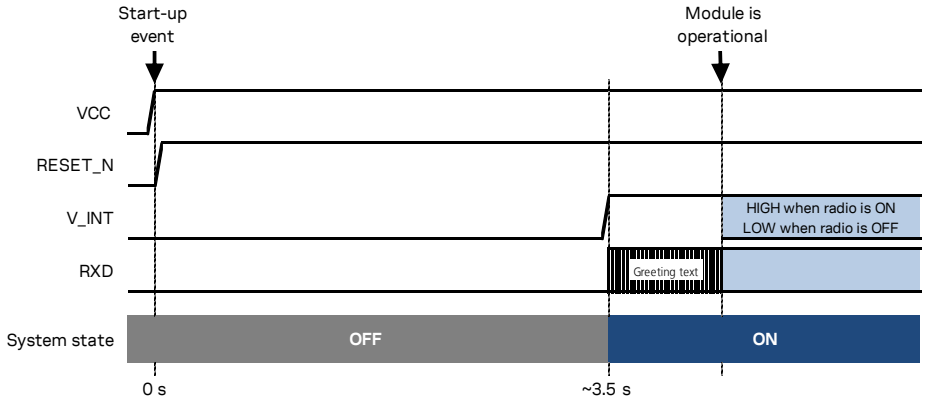

Figure 8: SARA-N2 series power-on sequence from not-powered mode

Figure 9 shows the switch on sequence of SARA-N3 modules starting from the non-powered mode:

- The external supply is being applied to the **VCC** inputs.
- The **PWR_ON** and **RESET_N** lines rise suddenly to high logic level due to internal pull-up.
- Then, the **PWR_ON** line is set low for a proper time period, representing the start-up event.
- Then, the **V_INT** generic digital interfaces supply output is enabled by the integrated PMU.
- The **RXD** UART data output pin also rises to the high logic level, at **V_INT** voltage value.
- A greeting message is sent on the **RXD** pin (for more details, see AT commands manual [4])
- From now on the module is fully operational and the UART interface is functional

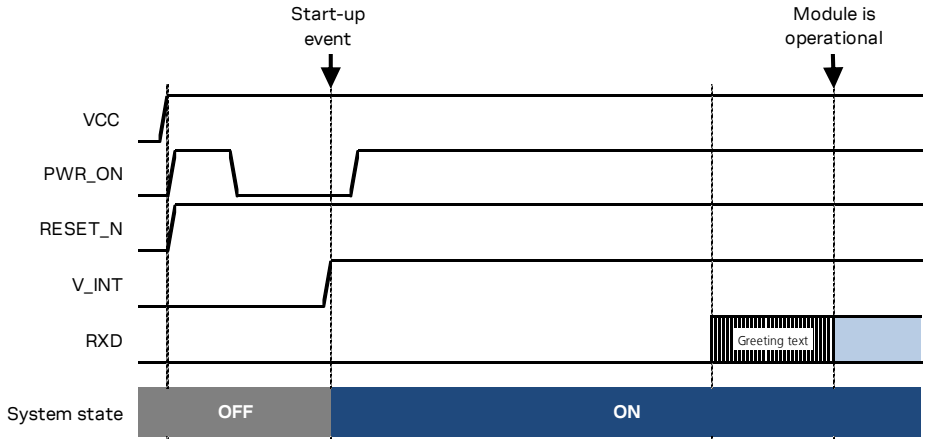

Figure 9: SARA-N3 series power-on sequence from not-powered mode

No voltage driven by an external application should be applied to the UART interface of the module before applying the **VCC** supply, to avoid latch-up of circuits and allow a proper boot of the module.

No voltage driven by an external application should be applied to any generic digital interface of the module (GPIOs, I2C interface) before the switch-on of the generic digital interface supply source of the module (**V_INT**), to avoid latch-up of circuits and allow a proper boot of the module.

1.6.2 Module power-off

The SARA-N2 series modules enter the non-powered mode by removing the **VCC** supply.

The switch-off routine of the SARA-N3 modules can be properly triggered, with storage of current parameter settings in the module's non-volatile memory and clean network detach, by:

- AT+CPWROFF command (see the SARA-N2 / SARA-N3 series AT commands manual [4]).
- Low level on the **PWR_ON** input pin, i.e. forcing the pin (normally high due to internal pull-up) to a low level for a valid time period (see SARA-N3 series data sheet [2]).

An abrupt under-voltage shutdown occurs on the SARA-N3 modules when the **VCC** supply drops below the extended operating range minimum limit (see the SARA-N3 series data sheet [2]), but in this case it is not possible to perform the storing of the current parameter settings in the module's non-volatile memory as well as a clean network detach.

An over-temperature shutdown occurs on the SARA-N3 modules when the temperature measured within the module reaches a critical range. For more details, see the AT commands manual [4].

Figure 10 shows the switch-off sequence of the SARA-N3 series modules started by means of the AT+CPWROFF command, allowing storage of current parameter settings in the module's non-volatile memory and a clean network detach, with the following phases:

- When the +CPWROFF AT command is sent, the module starts the switch-off routine.
- Then, the module replies OK on the AT interface: the switch-off routine is in progress.
- At the end of the switch-off routine, the internal voltage regulator generating the V_INT supply rail is turned off.
  Then, the module remains in switch-off mode as long as a switch on event does not occur (e.g. applying a low level to **PWR_ON**), and enters not-powered mode if the **VCC** supply is removed.

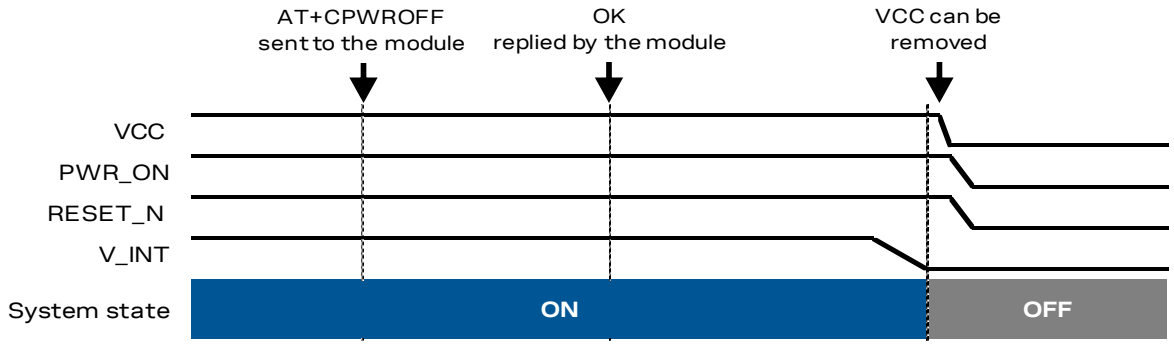

Figure 10: SARA-N3 series modules switch-off sequence by means of AT+CPWROFF command

☞ It is highly recommended to monitor the **V_INT** pin to sense the end of the switch-off sequence.

☞ It is highly recommended to avoid an abrupt removal of the **VCC** supply during module normal operations: the **VCC** supply can be removed only when the **V_INT** rail is switched off by the module.

☞ The duration of each phase in the SARA-N3 series modules' switch-off routines can largely vary depending on the application / network settings and the concurrent module activities.

1.6.3 Module reset

SARA-N2/N3 series modules can be properly reset (rebooted) by:

- AT command (see the SARA-N2 / SARA-N3 AT commands manual [4] for more details).

This command causes an “internal” or “software” reset of the module, which is an asynchronous reset of the module baseband processor. The current parameter settings are saved in the non-volatile memory of the module and a proper network detach is performed.

An abrupt hardware reset occurs on SARA-N2/N3 series modules when a low level is applied on the **RESET_N** input pin for a specific time period. In this case, storage of the current parameter settings in the module’s non-volatile memory and a proper network detach cannot be performed.

As described in Figure 11, the **RESET_N** input pin is equipped with an internal pull-up on SARA-N2/N3 series modules, with sligthly different internal circuits.

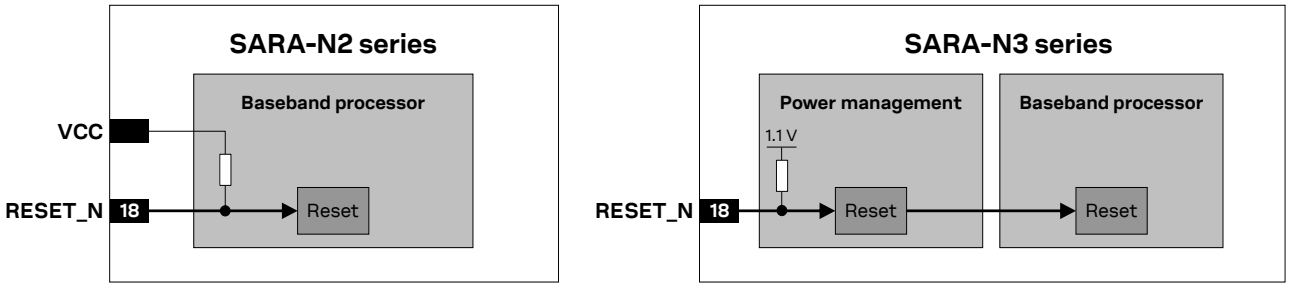

Figure 11: SARA-N2/N3 series RESET_N input equivalent circuit description

☞ It is highly recommended to avoid an abrupt hardware reset of the module by forcing a low level on the **RESET_N** input pin during module normal operation: the **RESET_N** line should be set low only if reset via AT command fails or if the module does not provide a reply to a specific AT command after a time period longer than the one defined in the SARA-N2/N3 series AT commands manual [4].

☞ Provide a test point connected to the **RESET_N** pin for diagnostic purpose.

1.6.4 Voltage selection of interfaces (VSEL)

☞ The digital interfaces’ voltage selection functionality is not available in SARA-N2 series modules.

The digital I/O interfaces of the SARA-N3 series modules (the UARTs, I2C, and GPIOs pins) operate at the **V_INT** voltage, which can be set to 1.8 V or 2.8 V using the **VSEL** input:

- If **VSEL** input pin is externally connected to GND, the digital I/O interfaces operate at 1.8 V
- If **VSEL** input pin is left unconnected, the digital I/O interfaces operate at 2.8 V

The operating voltage cannot be changed dynamically: the **VSEL** input pin configuration has to be set before the boot of the SARA-N3 series modules and then it cannot be changed after switched on.

1.7 Antenna interface

1.7.1 Cellular antenna RF interface (ANT)

The **ANT** pin of SARA-N2/N3 series modules represents the RF input/output for the cellular RF signals reception and transmission. The **ANT** pin has a nominal characteristic impedance of 50 Ω and must be connected to the external cellular antenna through a 50 Ω transmission line for proper reception and transmission of cellular RF signals.

1.7.1.1 Cellular antenna RF interface requirements

Table 6 summarizes the requirements for the cellular antenna RF interface (**ANT**). See section 2.4.1 for suggestions to properly design an antenna circuit compliant to these requirements.

⚠ The cellular antenna circuit affects the RF compliance of the device integrating SARA-N2/N3 series module with applicable required certification schemes.

Item	Requirements	Remarks
Impedance	50 Ω nominal characteristic impedance	The nominal characteristic impedance of the antenna RF connection must match the **ANT** pin 50 Ω impedance.
Frequency range	See the SARA-N2 series data sheet [1] and SARA-N3 series data sheet [2]	The required frequency range of the antenna depends on the operating bands supported by the cellular module.
Return loss	S_{11} < -10 dB (VSWR < 2:1) recommended S_{11} < -6 dB (VSWR < 3:1) acceptable	The return loss or the S_{11}, as the VSWR, refers to the amount of reflected power, measuring how well the RF antenna connection matches the 50 Ω impedance. The impedance of the antenna RF termination must match as much as possible the 50 Ω impedance of the **ANT** pin over the operating frequency range, reducing as much as possible the amount of reflected power.
Efficiency	> -1.5 dB (> 70%) recommended > -3.0 dB (> 50%) acceptable	The radiation efficiency is the ratio of the radiated power to the power delivered to antenna input: the efficiency is a measure of how well an antenna receives or transmits. The efficiency needs to be enough high over the operating frequency range to comply with the Over-The-Air radiated performance requirements, as Total Radiated Power and Total Isotropic Sensitivity, specified by certification schemes
Maximum gain	See section 4.2 for maximum gain limits	The power gain of an antenna is the radiation efficiency multiplied by the directivity: the maximum gain describes how much power is transmitted in the direction of peak radiation to that of an isotropic source. The maximum gain of the antenna connected to ANT pin must not exceed the values stated in section 4.2 to comply with regulatory agencies radiation exposure limits.
Input power	> 0.5 W peak	The antenna connected to ANT pin must support the maximum power transmitted by the modules.

Table 6: Summary of antenna RF interface (ANT) requirements

☞ For the additional specific requirements applicable to the integration of the SARA-N211 and the SARA-N310 modules in devices intended for use in potentially explosive atmospheres, see the guidelines reported in section 2.12.

1.7.2 Bluetooth antenna RF interface (ANT_BT)

☞ The Bluetooth functionality is not available in SARA-N2 series modules.

☞ The Bluetooth functionality is not supported by "00" product version of SARA-N3 series modules. The **ANT_BT** pin can be left unconnected or it can also be connected to GND.

The **ANT_BT** pin has an impedance of 50 Ω and provides the Bluetooth RF antenna interface of the SARA-N3 series modules.

1.7.3 Antenna detection interface (ANT_DET)

☞ Antenna detection interface is not supported in the "02" version of SARA-N2 series modules.

The **ANT_DET** pin is an Analog to Digital Converter (ADC) input used to sense the antenna presence evaluating the resistance from the **ANT** pin to GND by means of an external antenna detection circuit implemented on the application board. This optional functionality can be managed by dedicated AT command (for more details see the SARA-N2/N3 series AT commands manual [4]).

1.8 SIM interface

SARA-N2/N3 series modules provide a high-speed SIM/ME interface on the **VSIM**, **SIM_IO**, **SIM_CLK** and **SIM_RST** pins, which is available to connect an external SIM / UICC.

The SIM interface of the SARA-N2 modules can operate at 1.8 V (**VSIM** domain), with activation and deactivation of the SIM interface implemented according to the ISO-IEC 7816-3 specifications.

The SIM interface of the SARA-N3 modules can operate at 1.8 V and/or 3.0 V voltage (**VSIM** domain), with activation and deactivation of the SIM interface, and automatic 1.8 V / 3.0 V voltage switch according to the voltage class of the external SIM connected to the module implemented according to the ISO-IEC 7816-3 specifications.

The **VSIM** supply output of SARA-N2/N3 series modules provides internal short circuit protection to limit start-up current and protect the external SIM / UICC to short circuits.

1.9 Serial interfaces

SARA-N2/N3 series modules provide the following serial communication interfaces:

- Main primary UART interface (see 1.9.1):
  - In the **VCC** voltage domain (~3.6 V) on the SARA-N2 modules, supporting:
    - AT communication
    - FW upgrades by means of the FOAT feature
    - FW upgrades by means of the dedicated tool
  - In the **V_INT** voltage domain (1.8 V or 2.8 V) on the SARA-N3 modules, supporting:
    - AT communication
    - FW upgrades by means of the FOAT feature
- Auxiliary secondary UART interface (see 1.9.2):
  - Not available on the SARA-N2 modules
  - In the **V_INT** voltage domain (1.8 V or 2.8 V) on the SARA-N3 modules:
    - Not supported by the “00” product versions
- Additional UART interface (see 1.9.3):
  - In the **V_INT** voltage domain (1.8 V) on the SARA-N2 modules, supporting:
    - Diagnostic trace log
  - In the **V_INT** voltage domain (1.8 V or 2.8 V) on the SARA-N3 modules, supporting:
    - FW upgrades by means of the dedicated tool
    - Diagnostic trace log
- DDC I2C-bus compatible interface (see 1.9.4):
  - In the **V_INT** voltage domain (1.8 V) on the SARA-N2 modules:
    - Not supported by the “02” product versions
  - In the **V_INT** voltage domain (1.8 V or 2.8 V) on the SARA-N3 modules:
    - Not supported by the “00” product versions

1.9.1 Main primary UART interface

1.9.1.1 UART features

SARA-N2 modules include the **RXD**, **TXD**, **CTS**, **RTS** pins as main primary UART interface, supporting:

- AT communication
- FW upgrades by means of the FOAT feature
- FW upgrades by means of the dedicated tool

The main characteristics of the SARA-N2 modules primary UART interface are the following:

- Serial port with RS-232 functionality conforming to ITU-T V.24 recommendation [6]
- It operates at **VCC** voltage level
  - 0 V for low data bit or ON state
  - **VCC**, i.e. ~3.6 V, for high data bit or OFF state
- Data lines (**RXD** as module data output, **TXD** as module data input) are provided
- The **CTS** hardware flow control output is not supported by "02" product version: the **CTS** output line can be configured as RING indicator, to signal an incoming message received by the module or an URC event, or as Network status indicator (for more details see section 1.11 and the SARA-N2 / SARA-N3 series AT commands manual [4], +URING, +UGPIOC AT commands),
- The **RTS** hardware flow control input is not supported by "02" product version
- Default baud rate: 9'600 b/s (4'800, 57'600 and 115'200 b/s baud rates are also supported)
- Default frame format: 8N1 (8 data bits, No parity, 1 stop bit)

SARA-N3 modules include the **RXD**, **TXD**, **CTS**, **RTS**, **DTR**, **DSR**, **DCD**, **RI** pins as main primary UART interface, supporting:

- AT communication
- FW upgrades by means of the FOAT feature

The main characteristics of the SARA-N3 modules main primary UART interface are the following:

- Serial port with RS-232 functionality conforming to ITU-T V.24 recommendation [6]
- It operates at **V_INT** level, with voltage value set as per external **VSEL** pin configuration
  - 0 V for low data bit or ON state
  - **V_INT**, i.e. 1.8 V or 2.8 V, for high data bit or OFF state
- Data lines (**RXD** as module data output, **TXD** as module data input) are provided
- Hardware flow control lines (**CTS** as output, **RTS** as input) and **RI** output line are provided, and they can be alternatively configured as described in section 1.11 (for more details see also the SARA-N2 / SARA-N3 series AT commands manual [4])
- The modem status and control lines (**DTR** as input, **DSR** as output, **DCD** as output) are not supported by "00" product versions
- Hardware flow control disabled by default
- One-shot automatic baud rate detection enabled by default
- UART works in low power idle mode and 4’800, 9’600, 19’200, 38’400, 57’600 b/s baud-rates are supported
- 8N1 default frame format

The UART interface provides RS-232 functionality conforming to the ITU-T V.24 Recommendation (more details available in ITU recommendation [6]): SARA-N2/N3 series modules are designed to operate as a cellular modem, which represents the Data Circuit-terminating Equipment (DCE) according to ITU-T V.24 recommendation [6]. The application processor connected to the module through the UART interface represents the Data Terminal Equipment (DTE).

The UART interface settings can be suitably configured by AT commands (for more details, see the SARA-N2 / SARA-N3 series AT commands manual [4]).

☞ The signal names of the SARA-N2/N3 series modules’ UART interface conform to the ITU-T V.24 recommendation [6]: e.g. the **TXD** line represents the data transmitted by the DTE (application processor data line output) and received by the DCE (module data line input).

Figure 12 describes the 8N1 frame format.

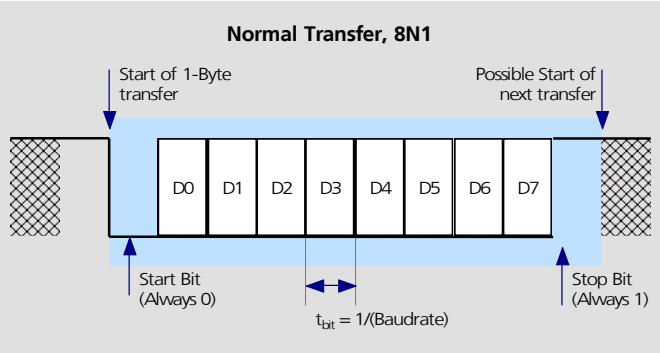

Figure 12: Description of UART default frame format (8N1) with fixed baud rate

1.9.1.2 UART signal behavior

At the module switch-on, before the UART interface initialization (as described in the power-on sequence reported in Figure 8 and Figure 9), each pin is first tri-stated and then is set to its related internal reset state. At the end of the boot sequence, the UART interface is initialized and the UART interface is enabled as AT commands interface.

The configuration and the behavior of the UART signals after the boot sequence are described below. See section 1.4 for definition and description of module operating modes referred to in this section.

RXD signal behavior

The module data output line (**RXD**) is set by default to the OFF state (high level) at UART initialization. The greeting message is sent on the **RXD** line after the completion of the boot sequence to indicate the completion of the UART interface initialization. For more details regarding how to set greeting text, see the SARA-N2 / SARA-N3 series AT commands manual [4].

The module holds **RXD** in the OFF state until the module does not transmit some data.

TXD signal behavior

The module data input line (**TXD**) is assumed to be controlled by the external host once UART is initialized.

There is no internal pull-up / pull-down inside the SARA-N2 modules on the **TXD** input. Instead, the SARA-N3 modules have an internal pull-up on the **TXD** input.

1.9.1.3 UART and deep sleep mode

To limit the current consumption, SARA-N2 modules automatically enter deep-sleep mode whenever possible, that is if there is no data to transmit or receive. When in deep-sleep mode the UART interface is still completely functional and the SARA-N2 module can accept and respond to any AT command. All the other interfaces are disabled.

The application processor should go in standby (or lowest power consumption mode) as soon as the SARA-N2 module enters the deep-sleep mode and there is no more data to be transmitted.

At any time the DTE can request the SARA-N2 module to send data using the related commands (for more details, see the SARA-N2 / SARA-N3 AT commands manual [4] and the NB-IoT application development guide [5]); these commands automatically force the SARA-N2 module to exit the deep-sleep mode.

To limit the current consumption, SARA-N3 modules automatically enter the low power idle mode whenever possible, that is, if there is no data to transmit or receive. In low power idle mode, the UART interface is still completely functional and the SARA-N3 module can accept and respond to any AT command.

SARA-N3 modules automatically enter the deep-sleep mode if the Power Saving Mode defined in 3GPP release 13 is enabled by A dedicated AT command (for more details, see the SARA-N2 / SARA-N3 series AT commands manual [4]), entering the lowest possible power mode. The UART interface is not functional: a wake-up event, consisting in proper toggling of the **PWR_ON** line or the **RESET_N** line, is necessary to trigger the wake up routine of the SARA-N3 modules that subsequently enter back into the active mode as in case of expiration of the “Periodic Update Timer” as per the Power Saving Mode defined in 3GPP release 13.

1.9.2 Secondary auxiliary UART interface

☞ The secondary auxiliary UART interface is not available on SARA-N2 modules.

☞ The secondary auxiliary UART interface is not supported by SARA-N3 "00" product version.

SARA-N3 modules include the **RXD_AUX** and **TXD_AUX** pins as secondary auxiliary UART interface.

The characteristics of the SARA-N3 modules' secondary auxiliary UART interface are:

- Serial port with RS-232 functionality conforming to ITU-T V.24 recommendation [6]
- It operates at **V_INT** level, with voltage value set as per external **VSEL** pin configuration
  - 0 V for low data bit or ON state
  - **V_INT**, i.e. 1.8 V or 2.8 V, for high data bit or OFF state
- Data lines (**RXD_AUX** as module data output, **TXD_AUX** as module data input) are provided

1.9.3 Additional UART interface

SARA-N2 modules include the **GPIO1** pin as additional UART interface, supporting:

- Diagnostic trace log

The characteristics of the SARA-N2 modules' additional UART interface are:

- Serial port with RS-232 functionality conforming to ITU-T V.24 recommendation [6]
- It operates at **V_INT** level, with voltage value set as per external **VSEL** pin configuration
  - 0 V for low data bit or ON state
  - **V_INT**, i.e. 1.8 V, for high data bit or OFF state
- Data line (**GPIO1** as module data output) is provided
- Fixed baud rate: 921'600 b/s
- Fixed frame format: 8N1 (8 data bits, no parity, 1 stop bit)

☞ Provide a test point connected to the **GPIO1** pin for diagnostic purpose.

☞ The trace diagnostic log is temporarily stopped when the SARA-N2 module is in deep-sleep mode.

SARA-N3 modules include the **RXD_FT** and **TXD_FT** pins as additional UART interface, supporting:

- Diagnostic trace log
- FW upgrades by means of the dedicated tool

The characteristics of the SARA-N3 modules' additional UART interface are:

- Serial port with RS-232 functionality conforming to ITU-T V.24 recommendation [6]
- It operates at **V_INT** level, with voltage value set as per external **VSEL** pin configuration
  - 0 V for low data bit or ON state
  - **V_INT**, i.e. 1.8 V or 2.8 V, for high data bit or OFF state
- Data lines (**RXD_FT** as module data output, **TXD_FT** as module data input) are provided

☞ Provide test points to the **RXD_FT** and **TXD_FT** pins for diagnostic and FW update purposes.

☞ The trace diagnostic log is temporarily stopped when the SARA-N3 module is in deep-sleep mode.

1.9.4 DDC (I2C) interface

DDC (I2C) interface is not supported by SARA-N2 "02" product version.

DDC (I2C) interface is not supported by SARA-N3 "00" product version.

SARA-N2/N3 series modules include **SDA** and **SCL** pins as I2C bus compatible Display Data Channel (DDC) interface, operating at the **V_INT** voltage level.

1.10 ADC

ADC interface is not available in the SARA-N2 modules.

The SARA-N3 modules include two Analog-to-Digital Converter input pins, **ANT_DET** and **ADC1**, configurable via dedicated AT command (for further details, see the SARA-N2 / SARA-N3 series AT commands manual [4]).

1.11 General Purpose Input/Output (GPIO)

SARA-N2 modules provide the following pins:

- **GPIO1** pin, working at the **V_INT** (1.8 V) voltage domain, supporting the Secondary UART data output functionality (see section 1.9.3 and Table 7)
- **GPIO2** pin, working at the **V_INT** (1.8 V) voltage domain, not supported by "02" product versions
- **CTS** pin, working at the **VCC** (3.6 V typical) voltage domain, supporting the Network status indication and the RING indicator functionality (see section 1.9.1 and Table 7)

For more details about how the pins can be configured, see the SARA-N2 / SARA-N3 series AT commands manual [4], +UGPIOC, +URING AT commands.

Provide a test point connected to the **GPIO1** pin for diagnostic purpose.

Function	Description	Default GPIO	Configurable GPIOs
Network status indication	Network status: registered home network, registered roaming, data transmission, no service	--	CTS
Ring indication	Indicates an incoming message received by the module or an URC event	--	CTS
Secondary UART	Secondary UART data output for diagnostic purpose, to capture diagnostic logs delivered by the module	GPIO1	GPIO1
Pin disabled	Tri-state with an internal active pull-down enabled	CTS	CTS

Table 7: GPIO custom functions configuration of SARA-N2 series modules

SARA-N3 modules include General Purpose Input/Output pins that can be configured via u-blox AT commands (for further details, see the AT commands manual [4], +UGPIOC, +URING AT commands).

The internal power domain for the GPIO pins is **V_INT**, with 1.8 V or 2.8 V voltage value set according to external **VSEL** pin configuration.

Table 8 summarizes the custom functions available on the GPIO pins of SARA-N3 modules.

Function	Description	Default GPIO	Configurable GPIOs
Network status indication	Output to indicate the network status: registered home network, registered roaming, data transmission, no service	--	GPIO1, GPIO2, CTS
Last gasp	Input to trigger last gasp execution	--	GPIO3
SIM card detection	Input to sense external SIM card physical presence	GPIO5	GPIO5
HW flow control (RTS)	UART request to send input	RTS	RTS
HW flow control (CTS)	UART clear to send output	CTS	CTS
Ring indication	UART ring indicator output	RI	RI
General purpose input	Input to sense high or low digital level	--	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, RI, RTS, CTS
General purpose output	Output to set high or low digital level	--	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, RI, RTS, CTS
Pin disabled	Output tri-stated, with an internal active pull-down enabled	GPIO1, GPIO2, GPIO3, GPIO4	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5 RI, RTS, CTS

Table 8: GPIO custom functions configuration of SARA-N3 series modules

1.12 Reserved pins (RSVD)

SARA-N2/N3 series modules have pins reserved for future use, marked as **RSVD**.

All the **RSVD** pins are to be left unconnected on the application board, except for the **RSVD** pin number **33** that can be externally connected to ground.

2 Design-in

2.1 Overview

For an optimal integration of SARA-N2/N3 series modules in the final application board, follow the design guidelines stated in this section.

Every application circuit must be properly designed to guarantee the correct functionality of the related interface, however a number of points require higher attention during the design of the application device.

The following list provides a ranking of importance in the application design, starting from the highest relevance:

1. Module antenna connection: **ANT** pin. Antenna circuit directly affects the RF compliance of the device integrating a SARA-N2/N3 series module with the applicable certification schemes. Very carefully follow the suggestions provided in section 2.4 for schematic and layout design.
2. Module supply: **VCC** and **GND** pins. The supply circuit affects the RF compliance of the device integrating a SARA-N2/N3 series module with applicable certification schemes as well as antenna circuit design. Very carefully follow the suggestions provided in section 2.2 for schematic and layout design.
3. SIM interface: **VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST** pins. Accurate design is required to guarantee SIM card functionality and compliance with applicable conformance standards, reducing also the risk of RF coupling. Carefully follow the suggestions provided in section 2.5 for schematic and layout design.
4. System function: **PWR_ON**, **RESET_N**, **VSEL** pins. Accurate design is required to guarantee that the voltage level is well defined during operation. Carefully follow the suggestions provided in section 2.3 for schematic and layout design.
5. Other interfaces: UART interfaces, I2C-compatible interface, ADC and GPIOs. Accurate design is required to guarantee proper functionality and reduce the risk of digital data frequency harmonics coupling. Follow the suggestions provided in sections 2.6, 2.7 and 2.8 for schematic and layout design.

2.2 Supply interfaces

2.2.1 Module supply input (VCC)

2.2.1.1 General guidelines for VCC supply circuit selection and design

All the available **VCC** pins must be connected to the external supply minimizing the power loss due to series resistance.

GND pins are internally connected but connect all the available pins to a solid ground on the application board, since a good (low impedance) connection to external ground can minimize power loss and improve RF and thermal performance.

SARA-N2/N3 series modules must be supplied through the **VCC** pins by a proper DC power supply that should comply with the module **VCC** requirements summarized in Table 5.

The proper DC power supply can be selected according to the application requirements (see Figure 13) between the different possible supply sources types, which most common ones are the following:

- Primary (disposable) battery
- Rechargeable Lithium-ion (Li-Ion) or Lithium-ion polymer (Li-Pol) battery
- Switching regulator
- Low Drop-Out (LDO) linear regulator

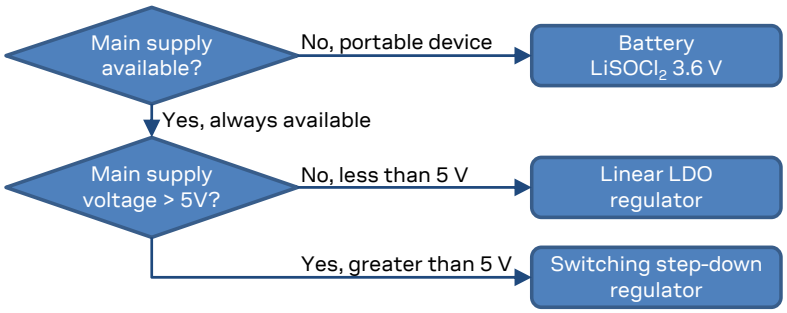

Figure 13: VCC supply concept selection

The NB-IoT technology is primarily intended for battery powered applications. A Lithium Thionyl Chloride ($LiSOCl_2$) battery directly connected to **VCC** pins is the usual choice for battery-powered devices. See sections 2.2.1.2, 2.2.1.3 and 2.2.1.6, 2.2.1.7, 2.2.1.8 for specific design-in.

The DC/DC switching step-down regulator is the typical choice when the available primary supply source has a nominal voltage much higher (e.g. greater than 5 V) than the modules **VCC** operating supply voltage. The use of switching step-down provides the best power efficiency for the overall application and minimizes current drawn from the main supply source. See sections 2.2.1.2, 2.2.1.4 and 2.2.1.6, 2.2.1.7, 2.2.1.8 for specific design-in.

The use of an LDO linear regulator becomes convenient for a primary supply with a relatively low voltage (e.g. less than 5 V). In this case the typical 90% efficiency of the switching regulator diminishes the benefit of voltage step-down and no true advantage is gained in input current savings. On the opposite side, linear regulators are not recommended for high voltage step-down as they dissipate a considerable amount of energy in thermal power. See sections 2.2.1.2, 2.2.1.5 and 2.2.1.6, 2.2.1.7, 2.2.1.8 for specific design-in.

The use of rechargeable batteries is not the typical solution for NB-IoT applications, but it is feasible to implement a suitable external charger circuit. The charger circuit has to be designed to prevent over-voltage on **VCC** pins of the module, and it should be selected according to the application

requirements: a DC/DC switching charger is the typical choice when the charging source has an high nominal voltage (e.g. ~12 V), whereas a linear charger is the typical choice when the charging source has a relatively low nominal voltage (~5 V). If both a permanent primary supply / charging source (e.g. ~12 V) and a rechargeable back-up battery (e.g. 3.7 V Li-Pol) are simultaneously available in the application as possible supply sources, then a proper charger / regulator with integrated power path management function can be selected to supply the module while simultaneously and independently charging the battery.

The usage of more than one DC supply at the same time should be carefully evaluated: depending on the supply source characteristics, different DC supply systems can be mutually exclusive.

The usage of supercapacitors on the **VCC** supply line is generally not recommended since these components are highly temperature sensitive and may increase current leakages draining the battery faster.

The following sections highlight some design aspects for power-supply scenarios, providing application circuit design-in compliant with the module **VCC** requirements summarized in Table 5.

☞ For the additional specific requirements applicable during the integration of SARA-N211 and SARA-N310 modules in devices intended for use in potentially explosive atmospheres, see section 2.12.

2.2.1.2 Guidelines to optimize power consumption

The NB-IoT technology is primarily intended for applications that require small amount of data exchange per day (i.e. few bytes in uplink and downlink per day) and these are typically battery powered. Depending on the application type, an operating life of 5 to 15 years is usually required. For these reasons, the whole application board should be optimized in terms of current consumption and should carefully take into account the following aspects:

- Minimize current leakages on the power supply line
- Optimize the antenna matching since an un-matched antenna leads to higher current consumptions
- Use an application processor with UART interface working at the same level of the UART interface of the module (**VCC**, i.e. ~3.3 ÷ 3.6 V, for SARA-N2 modules; **V_INT**, i.e. 1.8 V or 2.8 V, for SARA-N3 modules), in order to avoid voltage translators on the UART interface
- The application processor should go in standby (or lowest power consumption mode) as soon as the SARA-N2/N3 series module enters the deep-sleep mode and there's no more data to be transmitted: the module will automatically enter the deep-sleep mode whenever possible to limit current consumption and avoid further network registration procedures each time there is an up-link message to be transmitted.
- The application processor can monitor the **V_INT** level to sense when SARA-N2 modules' radio is on or off, or to sense when a SARA-N3 module is on or off
- The application processor can detect the presence of down-link messages monitoring the line providing the Ring Indicator functionality (**CTS** pin on SARA-N2 modules, **RI** pin on SARA-N3 modules), notifying incoming data received by the module or an URC event.
- Possibility to request new network timers and select the optimum set of values depending on the intended application use case

2.2.1.3 Guidelines for VCC supply circuit design using a primary battery

The characteristics of a battery connected to **VCC** pins should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 5:

- **Maximum pulse and DC discharge current**: the non-rechargeable battery with its output circuit must be capable of delivering to **VCC** pins the specified average current during a transmission at maximum power (see the SARA-N2 series data sheet [1] and SARA-N3 series data sheet [2] for more details). The antenna matching influences the current consumption; for this reason, the current consumption at maximum Tx power with the intended antenna (i.e. on the final application board) should be used to characterize the battery maximum pulse requirements.
  The maximum DC discharge current is not always reported in battery data sheets, but it is typically almost equal to the battery capacity in Amp-hours divided by 1 hour.
- **DC series resistance**: the non-rechargeable battery with its output circuit must be capable to limit as much as possible the DC resistance provided on the **VCC** supply line.

The LiSOCl2 (Lithium Thionyl Chloride Batteries) is currently the best technology available for NB-IoT applications since it provides:

- Very low self-discharge behavior and resulting ability to last longer
- Highest specific energy per unit weight and energy density per unit volume
- Wide operating temperature range

For the selection of the proper battery type, the following parameters should be taken into account:

- Capacity: > 3 Ah
- Continuous current capability: ~400 mA (the consumption of whole application with the actual antenna should be considered)
- Temperature range: -20 °C to +85 °C
- Capacity vs temperature behavior: battery capacity is highly influenced by the temperature. This must be considered to properly estimate the battery life time
- Capacity vs discharge current performance
- Voltage vs temperature behavior: the battery voltage typically decreases at low temperatures values (for example, in the -10 °C / -20 °C range). In all the temperature conditions the battery voltage must always be above the SARA-N2 minimum extended operating voltage level
- Voltage vs pulse duration behavior: this information is typically not provided by battery manufacturers, and many batteries reach too low voltage values during a long pulse. It is recommended to execute stress tests on battery samples to verify the voltage behavior as a function of the pulse duration and to guarantee that the battery voltage is always above the minimum extended operating voltage level of SARA-N2 series.
- Construction technology: spiral wound batteries are generically preferred over the bobbin construction
  - This technology typically supports high current pulses without the need for supercaps
  - A bobbin type battery usually does not support the current pulse

Figure 14 shows an example of connection of SARA-N2 module with a primary battery. Table 9 lists different batty pack part numbers that can be used.

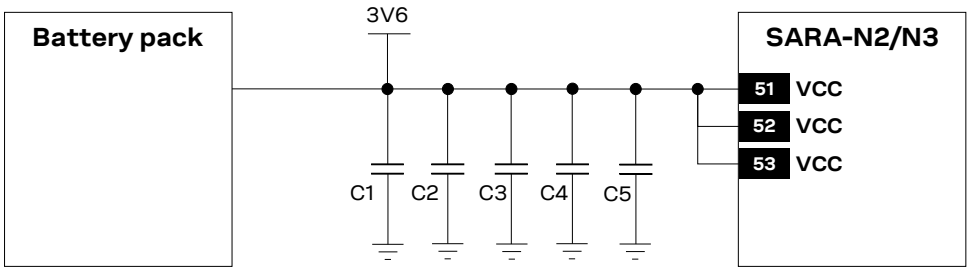

Figure 14: Suggested schematic design for the VCC voltage supply application circuit using a $LiSOCl_2$ primary battery

Reference	Description	Part Number - Manufacturer
C1	100 µF Capacitor Tantalum 6.3V 15mΩ	T520B107M006ATE015 - Kemet
C2	100 nF Capacitor Ceramic X7R 0402	GRM155R71C104KA01 - Murata
C3	10 nF Capacitor Ceramic X7R 0402	GRM155R71C103KA01 - Murata
C4	56 pF Capacitor Ceramic C0G 0402	GRM1555C1E560JA01 - Murata
C5	15 pF Capacitor Ceramic C0G 0402	GRM1555C1E150JA01 - Murata
Battery pack	Size FAT A LiSOCl battery, spiral wound, 3.2Ah	ER18505M - Titus Battery
	Size C LiSOCl battery, spiral wound, 6.5Ah	ER26500M - Titus Battery
	Size D LiSOCl battery, spiral wound, 13Ah	ER34615M - Titus Battery
	Size C LiSOCl battery, spiral wound, 5.8Ah	LSH14 – Saft
	Size D LiSOCl battery, spiral wound, 13Ah	LSH20 - Saft

Table 9: Suggested components for the VCC voltage supply application circuit using a $LiSOCl_2$ primary battery

An alternative battery design solution can be realized combining:

- Generic primary battery pack: not necessarily an optimized $LiSOCl_2$ spiral wound
- DC/DC buck-boost converter
- Load switch

There are switching regulators that integrate the load switch and the DC/DC converter logic with a so called bypass mode. See Figure 15 and Table 10 for an example of such an application circuit. In this case **V_INT** can be used to select between bypass and buck-boost modes:

- V_INT = LOW → SARA-N2 Radio = OFF / SARA-N3 = OFF → Bypass mode
- V_INT = HIGH → SARA-N2 Radio = ON / SARA-N3 = ON → Buck-boost mode

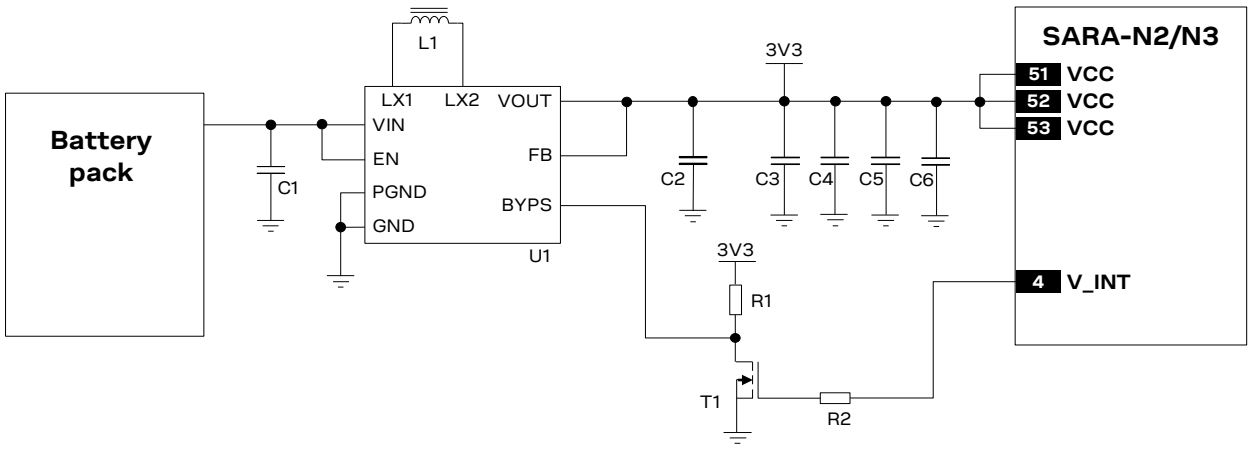

Figure 15: Alternative schematic design for the VCC voltage supply application circuit using a generic primary battery

Reference	Description	Part Number - Manufacturer
C1	10 µF Capacitor Ceramic X5R 0603 6.3 V	GRM188R60J106ME47 - Murata
C2	100 µF Capacitor Tantalum 6.3V 15mΩ	T520B107M006ATE015 - Kemet
L1	1 µH Inductor 20% 3.1 A 60 mΩ	TFM201610GHM-1R0MTAA - TDK
C3	100 nF Capacitor Ceramic X7R 0402	GRM155R71C104KA01 - Murata
C4	10 nF Capacitor Ceramic X7R 0402	GRM155R71C103KA01 - Murata
C5	56 pF Capacitor Ceramic C0G 0402	GRM1555C1E560JA01 - Murata
C6	15 pF Capacitor Ceramic C0G 0402	GRM1555C1E150JA01 - Murata
R1	100 kΩ Resistor	RC0402JR-07100KL - Yageo Phycomp
R2	1 kΩ Resistor	RC0402JR-071KL - Yageo Phycomp
T1	N-channel MOSFET	DMG1012T - Diodes Incorporated
U1	High Efficiency Low Power Buck-Boost Regulator with Bypass mode	ISL9120IRTNZ - Intersil

Table 10: Suggested components for an alternative VCC voltage supply application circuit using a generic primary battery

2.2.1.4 Guidelines for VCC supply circuit design using a switching regulator

The use of a switching regulator is suggested when the difference from the available supply rail to the **VCC** value is high: switching regulators provide good efficiency transforming a 12 V or greater voltage supply to the typical 3.6 V value of the **VCC** supply.

The characteristics of the switching regulator connected to **VCC** pins should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 5:

- **Power capability**: the switching regulator with its output circuit must be capable of providing a voltage value to the **VCC** pins within the specified operating range and must be capable of delivering to **VCC** pins the specified average current during a transmission at maximum power (see SARA-N2 series data sheet [1] and SARA-N3 series data sheet [2]).
- **Low output ripple**: the switching regulator together with its output circuit must be capable of providing a clean (low noise) **VCC** voltage profile.
- **PWM mode operation**: it is preferable to select regulators with Pulse Width Modulation (PWM) mode. While in connected-mode Pulse Frequency Modulation (PFM) mode and PFM/PWM mode, transitions must be avoided to reduce the noise on the **VCC** voltage profile. Switching regulators that are able to switch between low ripple PWM mode and high efficiency burst or PFM mode can be used, provided the mode transition occurs when the module changes status from active-mode to connected-mode: it is suggest to use a regulator that switches from the PWM mode to the burst or PFM mode at an appropriate current threshold (e.g. 10 mA).

Figure 16 and the components listed in Table 11 show an example of a power supply circuit, where the module **VCC** is supplied by a step-down switching regulator capable of delivering the specified maximum current to the **VCC** pins, with low output ripple and with fixed switching frequency in PWM.

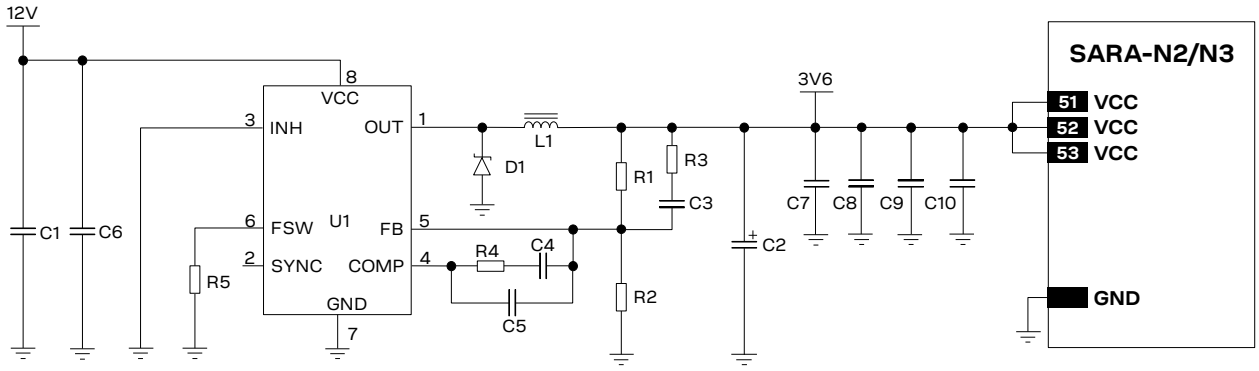

Figure 16: Suggested schematic design for the VCC voltage supply application circuit using a step-down regulator

Reference	Description	Part Number - Manufacturer
C1	22 µF Capacitor Ceramic X5R 25 V	GRM32ER61E226KE15 - Murata
C2	100 µF Capacitor Tantalum 6.3V 15mΩ	T520B107M006ATE015 - Kemet
C3	5.6 nF Capacitor Ceramic X7R 0402	GRM155R71H562KA88 - Murata
C4	6.8 nF Capacitor Ceramic X7R 0402	GRM155R71H682KA88 - Murata
C5	56 pF Capacitor Ceramic C0G 0402	GRM1555C1H560JA01 - Murata
C6	220 nF Capacitor Ceramic X7R 25 V	GRM188R71E224KA88 - Murata
C7	100 nF Capacitor Ceramic X7R 0402	GRM155R71C104KA01 - Murata
C8	10 nF Capacitor Ceramic X7R 0402	GRM155R71C103KA01 - Murata
C9	56 pF Capacitor Ceramic C0G 0402	GRM1555C1E560JA01 - Murata
C10	15 pF Capacitor Ceramic C0G 0402	GRM1555C1E150JA01 - Murata
D1	Schottky Diode 25V 2 A	STPS2L25 - STMicroelectronics
L1	5.2 µH Inductor 30% 5.28A 22 mΩ	MSS1038-522NL - Coilcraft
R1	4.7 kΩ Resistor 1%	RC0402FR-074K7L - Yageo
R2	1 kΩ Resistor 1%	RC0402FR-071KL - Yageo
R3	82 Ω Resistor	RC0402JR-0782RL - Yageo
R4	8.2 kΩ Resistor	RC0402JR-078K2L - Yageo
R5	39 kΩ Resistor	RC0402JR-0739KL - Yageo
U1	Step-Down Regulator 8-VFQFPN 0.7 A 1 MHz	L5980TR - ST Microelectronics

Table 11: Suggested components for the VCC voltage supply application circuit using a step-down regulator

2.2.1.5 Guidelines for VCC supply circuit design using an LDO linear regulator

The use of a linear regulator is suggested when the difference from the available supply rail and the **VCC** value is low: linear regulators provide high efficiency when transforming a 5 V supply to a voltage value within the module **VCC** normal operating range.

The characteristics of the LDO linear regulator connected to the **VCC** pins should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 5:

- **Power capabilities**: the LDO linear regulator with its output circuit must be capable of providing a proper voltage value to the **VCC** pins and of delivering to **VCC** pins the specified maximum average current during a transmission at maximum power (see the SARA-N2 series data sheet [1] and SARA-N3 series data sheet [2])
- **Power dissipation**: the power handling capability of the LDO linear regulator must be checked to limit its junction temperature to the maximum rated operating range (i.e. check the voltage drop from the maximum input voltage to the minimum output voltage to evaluate the power dissipation of the regulator)

Figure 17 and the components listed in Table 12 show a power supply circuit example, where the **VCC** module supply is provided by an LDO linear regulator capable of delivering the specified current.

It is recommended to configure the LDO linear regulator to generate a voltage supply value slightly below the maximum limit of the module **VCC** normal operating range. This reduces the power on the linear regulator and improves the whole thermal design of the supply circuit.

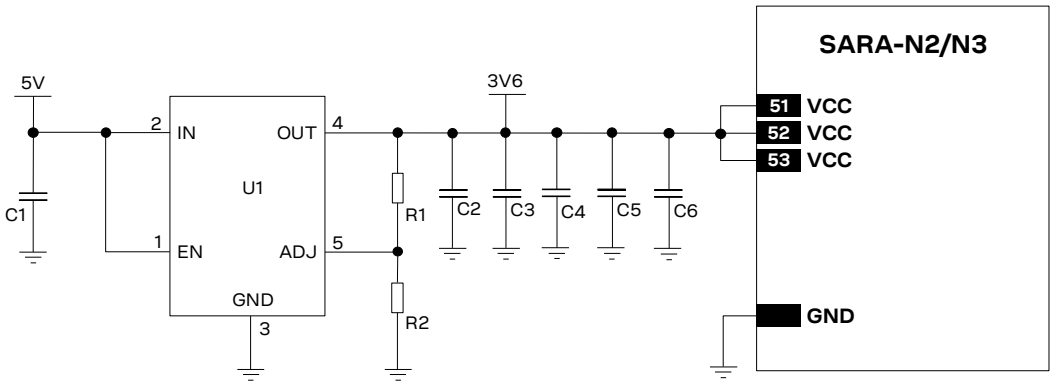

Figure 17: Suggested schematic design for the VCC voltage supply application circuit using an LDO linear regulator

Reference	Description	Part Number - Manufacturer
C1	10 µF Capacitor Ceramic X5R 6.3 V	GRM188R60J106ME47 - Murata
C2	100 µF Capacitor Tantalum 15mΩ	T520B107M006ATE015 - Kemet
R1	29.4 kΩ Resistor	RC0402FR-0729K4L - Yageo Phycomp
R2	4.7 kΩ Resistor	RC0402JR-074K7L - Yageo Phycomp
U1	LDO Linear Regulator ADJ 800 mA	LP38511TJ-ADJ/NOPB - Texas Instrument
C3	100 nF Capacitor Ceramic X7R 0402	GRM155R71C104KA01 - Murata
C4	10 nF Capacitor Ceramic X7R 0402	GRM155R71C103KA01 - Murata
C5	56 pF Capacitor Ceramic C0G 0402	GRM1555C1E560JA01 - Murata
C6	15 pF Capacitor Ceramic C0G 0402	GRM1555C1E150JA01 - Murata

Table 12: Suggested components for VCC voltage supply application circuit using an LDO linear regulator

2.2.1.6 Additional guidelines for VCC supply circuit design

To reduce voltage drops, use a low impedance power source. The resistance of the power supply lines (connected to the **VCC** and **GND** pins of the module) on the application board and battery pack should also be considered and minimized: cabling and routing must be as short as possible to minimize power losses.

Three pins are allocated for **VCC** supply. Another twenty pins are designated for **GND** connection. It is highly recommended to properly connect all the **VCC** pins and all the **GND** pins to supply the module, to minimize series resistance losses.

To reduce voltage noise, especially if the application device integrates an internal antenna, place the following bypass capacitors near the **VCC** pins:

- 56 pF 0402 capacitor with self-resonant frequency in 700/800/900 MHz range (e.g. Murata GRM1555C1E560J) to filter transmission EMI in the NB-IoT bands 28 / 20 / 5 / 8
- 15 pF 0402 capacitor with self-resonant frequency in 1800/1900 MHz range (e.g. Murata GRM1555C1E150J) to filter transmission EMI in the NB-IoT band 3
- 10 nF capacitor (e.g. Murata GRM155R71C103K) to filter noise from clocks and data sources
- 100 nF capacitor (e.g. Murata GRM155R61C104K) to filter noise from clocks and data sources
- 100 µF low ESR capacitor (e.g. Kemet T520B107M006ATE015) to avoid voltage undershoot and overshoot at the start and end of a RF transmit burst, stabilizing the voltage profile at max Tx power, recommended in particular for noise sensitive applications

For devices integrating an internal antenna, it is recommended to provide space to allocate all the components shown in Figure 18 and listed in Table 13.

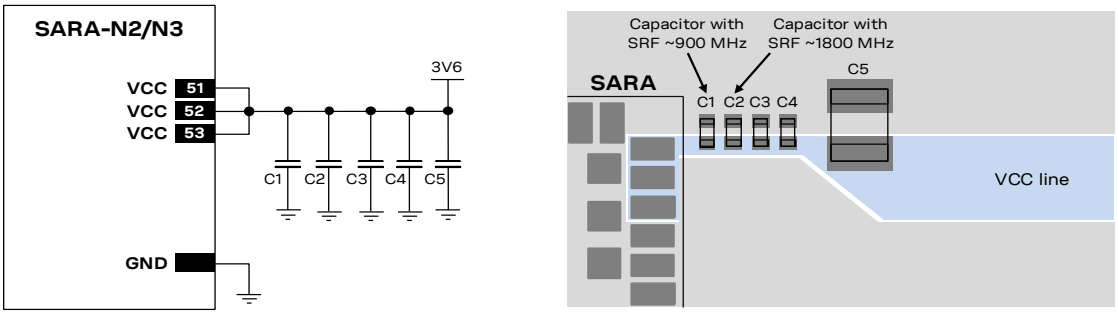

Figure 18: Suggested schematic and layout design for the VCC line, highly recommended when using an integrated antenna

Reference	Description	Part Number - Manufacturer
C1	56 pF Capacitor Ceramic C0G 0402	GRM1555C1E560JA01 - Murata
C2	15 pF Capacitor Ceramic C0G 0402	GRM1555C1E150JA01 - Murata
C3	10 nF Capacitor Ceramic X7R 0402	GRM155R71C103KA01 - Murata
C4	100 nF Capacitor Ceramic X7R 0402	GRM155R71C104KA01 - Murata
C5	100 µF Capacitor Tantalum 15mΩ	T520B107M006ATE015 - Kemet

Table 13: Suggested components to reduce noise on VCC

ESD sensitivity rating of **VCC** pins is 1 kV (HBM according to JESD22-A114). Higher protection level can be required if the line is externally accessible on the application board, e.g. if accessible battery connector is directly connected to **VCC** pins. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible point.

2.2.1.7 Guidelines for VCC supply layout design

Good connection of the module **VCC** pins with DC supply source is required for correct RF performance. Guidelines are summarized in the following list:

- All the available **VCC** pins must be connected to the DC source.
- **VCC** connection must be as wide as possible and as short as possible.
- Any series component with Equivalent Series Resistance (ESR) greater than few milliohms must be avoided.
- **VCC** connection must be routed through a PCB area separated from sensitive analog signals and sensitive functional units: it is good practice to interpose at least one layer of PCB ground between **VCC** track and other signal routing.
- The bypass capacitors in the pF range described in Figure 18 and Table 13 should be placed as close as possible to the **VCC** pins. This is highly recommended if the application device integrates an internal antenna.
- High frequency voltage ripples on the **VCC** line may result in unwanted spurious modulation of transmitter RF signal. This is more likely to happen with switching DC-DC converters, in which case it is better to select the highest operating frequency for the switcher and add a large L-C filter before connecting to the SARA-N2/N3 series modules in the worst case.
- If **VCC** is protected by transient voltage suppressor to ensure that the voltage maximum ratings are not exceeded, place the protecting device along the path from the DC source toward the cellular module, preferably closer to the DC source (otherwise protection functionality may be compromised).

2.2.1.8 Guidelines for grounding layout design

Good connection of the module **GND** pins with application board solid ground layer is required for correct RF performance. It significantly reduces EMC issues and provides a thermal heat sink for the module.

- Connect each **GND** pin with application board solid GND layer. It is strongly recommended that each **GND** pin surrounding **VCC** pins have one or more dedicated via down to the application board solid ground layer.
- The **VCC** supply current flows back to main DC source through GND as ground current: provide adequate return path with suitable uninterrupted ground plane to main DC source.
- It is recommended to implement one layer of the application board as ground plane as wide as possible.
- If the application board is a multilayer PCB, then all the board layers should be filled with GND plane as much as possible and each GND area should be connected together with complete via stack down to the main ground layer of the board.
- If the whole application device is composed by more than one PCB, then it is required to provide a good and solid ground connection between the GND areas of all the different PCBs.
- Good grounding of **GND** pins also ensures thermal heat sink. This is critical during call connection, when the real network commands the module to transmit at maximum power: proper grounding helps prevent module overheating.

2.2.2 RTC supply (V_BCKP)

2.2.2.1 Guidelines for V_BCKP circuit design

☞ The RTC supply (**V_BCKP** pin) is not available on SARA-N2 series modules.

V_BCKP is the Real Time Clock (RTC) supply of SARA-N3 modules. When **VCC** voltage is within the valid operating range, the internal Power Management Unit (PMU) supplies the RTC and the same supply voltage is available on the **V_BCKP** pin.

If the **VCC** voltage is under the minimum operating limit (e.g. during non powered mode), the RTC can be externally supplied through the **V_BCKP** pin, as for example using a suitable external capacitor, a suitable supercapacitor, or a suitable non-rechargeable battery as illustrated in Figure 19.

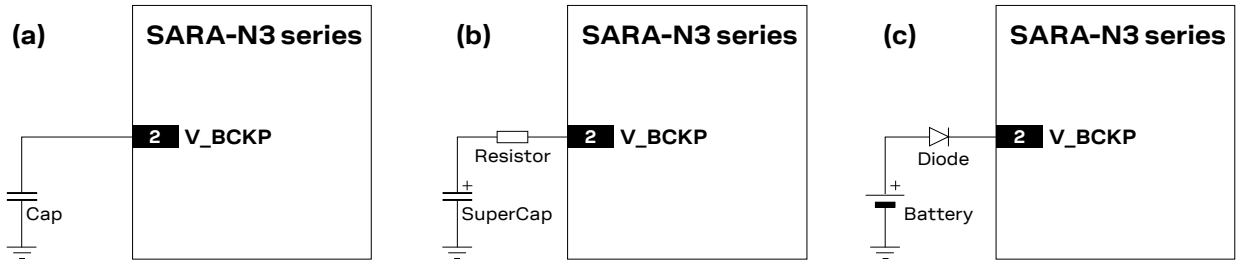

Figure 19: V_BCKP application circuits using: (a) a capacitor, (b) a supercapacitor, (c) a non-rechargeable battery

☞ If the RTC timing is not required when the **VCC** supply is removed, it is not needed to connect the **V_BCKP** pin to an external capacitor or battery. In this case, the date and time are not updated when **VCC** is disconnected. If **VCC** is always supplied, then the internal regulator is supplied from the main supply and there is no need for an external component on **V_BCKP**.

☞ The internal regulator for **V_BCKP** is optimized for low leakage current and very light loads. Do not apply loads that might exceed the limit for maximum available current from **V_BCKP** supply, as this can cause malfunction in the module.

☞ The **V_BCKP** pin provides internal short circuit protection to limit start-up current and protect the device in short circuit situations. No additional external short circuit protection is required.

☞ The ESD sensitivity rating of the **V_BCKP** pin is 1 kV (Human Body Model according to JESD22-A114). Higher protection level could be required if the line is externally accessible on the application board. Higher protection level can be achieved by mounting an external ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible point.

2.2.2.2 Guidelines for V_BCKP layout design

The RTC supply (**V_BCKP**) requires careful layout: avoid injecting noise on this voltage domain as it may affect the stability of the 32 kHz oscillator

2.2.3 Interfaces supply output (V_INT)

2.2.3.1 Guidelines for V_INT circuit design

The **V_INT** digital interfaces supply output can be mainly used to:

- Indicate when the SARA-N2 modules' radio is on (see section 1.6.1 for more details)
- Indicate when the SARA-N3 module is on (see section 1.6.1 for more details)
- Supply external devices, as voltage translators, instead of using an external discrete regulator
- Pull-up SIM detection signal (see section 2.5 for more details)

☞ Do not apply loads that might exceed the limit for maximum available current from **V_INT** supply, as this can cause malfunctions in internal circuitry supplies to the same domain. The SARA-N2 series data sheet [1] and SARA-N3 series data sheet [2] describes the electrical characteristics.

☞ **V_INT** can only be used as an output; do not connect any external regulator on **V_INT**.

☞ **V_INT** supply output pin provides internal short circuit protection to limit start-up current and protect the device in short circuit situations. No additional external short circuit protection is required.

☞ ESD sensitivity rating of the **V_INT** supply pin is 1 kV (HBM according to JESD22-A114). Higher protection level could be required if the line is externally accessible on the application board. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible point.

☞ It is recommended providing direct access to the **V_INT** supply output pin on the application board by means of Test-Point directly accessible for diagnostic purpose

2.2.3.2 Guidelines for V_INT layout design

There are no specific layout design recommendations for **V_INT** output.

2.3 System functions interfaces

2.3.1 Module power-on (PWR_ON)

2.3.1.1 Guidelines for PWR_ON circuit design

☞ The **PWR_ON** input pin is not available in SARA-N2 series modules.

As described in SARA-N3 series data sheet [2], the module has an internal pull-up resistor on the **PWR_ON** input line, so an external pull-up is not required on the application board.

When the **PWR_ON** input is connected to a push button that shorts the **PWR_ON** input pin to ground, the pin will be externally accessible on the application device. According to EMC/ESD requirements of the application, provide an additional ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) on the line connected to this pin, close to an accessible point, as described in Figure 20 and Table 14.

☞ The ESD sensitivity rating of the **PWR_ON** pin is 1 kV (Human Body Model according to JESD22-A114). Higher protection level can be required if the line is externally accessible on the application board, e.g. if an accessible push button is directly connected to **PWR_ON** pin. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to the accessible point.

When the **PWR_ON** input is connected to an external device (e.g. application processor), an open drain output can be directly connected without any external pull-up, as described in Figure 20 and Table 14. The internal pull-up resistor provided by the module pulls the line to the high logic level when the application processor does not force the **PWR_ON** pin low.

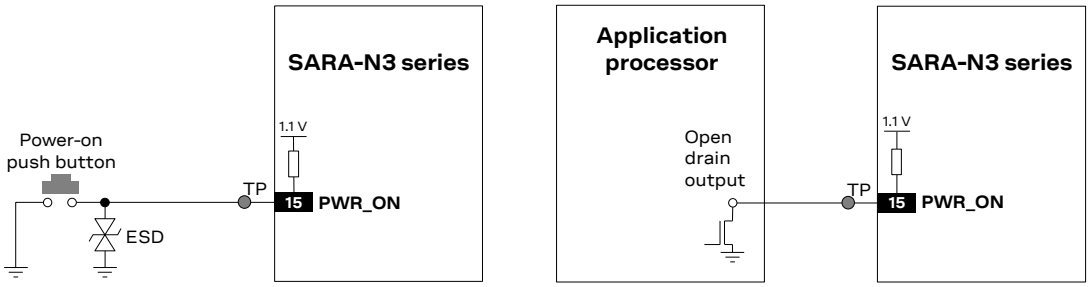

Figure 20: PWR_ON application circuits using a push button and an open drain output of an application processor

Reference	Description	Part Number - Manufacturer
ESD	Varistor for ESD protection	CT0402S14AHSG - EPCOS

Table 14: Example of ESD protection component for the PWR_ON application circuit

☞ It is recommended to provide on the application board a directly accessible Test-Point connected to the **PWR_ON** pin for diagnostic purpose.

2.3.1.2 Guidelines for PWR_ON layout design

The power-on circuit (**PWR_ON**) requires careful layout due to the pin function: ensure that the voltage level is well defined during operation and no transient noise is coupled on this line; otherwise the module might detect a spurious power-on request.

2.3.2 Module reset (RESET_N)

2.3.2.1 Guidelines for RESET_N circuit design

As described in SARA-N2 series data sheet [1] and SARA-N3 series data sheet [2], the modules have an internal pull-up resistor on the **RESET_N** input line, so an external pull-up is not required on the application board.

When the **RESET_N** input is connected to a push button that shorts the **RESET_N** pin to ground, the pin will be externally accessible on the application device. According to EMC/ESD requirements of the application, provide an additional ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) on the line connected to this pin, close to accessible point, as described in Figure 21 and Table 15.

ESD sensitivity rating of the **RESET_N** pin is 1 kV (Human Body Model according to JESD22-A114). Higher protection level can be required if the line is externally accessible on the application board, e.g. if an accessible push button is directly connected to **RESET_N** pin. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible point.

When the **RESET_N** input is connected to an external device (e.g. application processor), an open drain output can be directly connected without any external pull-up, as described in Figure 21 and Table 15. The internal pull-up resistor provided by the module pulls the line to the high logic level when the application processor does not force the **RESET_N** pin low.

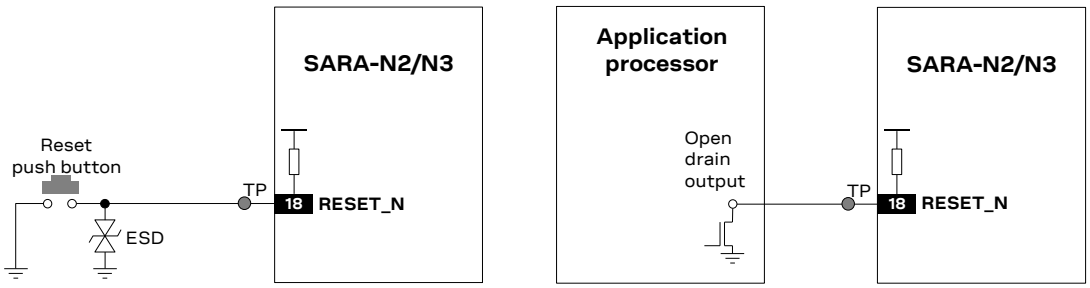

Figure 21: RESET_N application circuits using a push button and an open drain output of an application processor

Reference	Description	Part Number - Manufacturer
ESD	Varistor for ESD protection	CT0402S14AHSG - EPCOS

Table 15: Example of ESD protection component for the RESET_N application circuit

If the external reset function is not required by the customer application, the **RESET_N** input pin can be left unconnected to external components, but it is recommended providing direct access on the application board by means of accessible testpoint for diagnostic purpose.

2.3.2.2 Guidelines for RESET_N layout design

The reset circuit (**RESET_N**) requires careful layout due to the pin function: ensure that the voltage level is well defined during operation and no transient noise is coupled on this line, otherwise the module might detect a spurious reset request. It is recommended to keep the connection line to **RESET_N** as short as possible.

2.3.3 Voltage selection of interfaces (VSEL)

2.3.3.1 Guidelines for VSEL circuit design

The **VSEL** input pin is not available in SARA-N2 series modules.

The state of the **VSEL** input pin is used to configure the **V_INT** supply output and the voltage domain for the generic digital interfaces of the SARA-N3 modules (the UARTs, I2C, and GPIOs pins):

- If the **VSEL** input pin is externally connected to GND, the digital I/O interfaces operate at 1.8 V
- If the **VSEL** input pin is left unconnected, the digital I/O interfaces operate at 2.8 V

The operating voltage cannot be changed dynamically: the **VSEL** input pin configuration has to be set before booting the SARA-N3 modules and then it cannot be changed after switched on.

If digital I/O interfaces are intended to operate at 1.8 V, the **VSEL** pin must be connected to GND, as described in Figure 22.

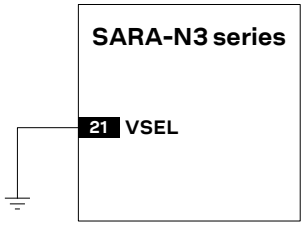

Figure 22: VSEL application circuit, configuring digital interfaces to operate at 1.8 V

If digital I/O interfaces are intended to operate at 2.8 V, the **VSEL** pin must be left unconnected, as described in Figure 23.

Figure 23: VSEL application circuit, configuring digital interfaces to operate at 2.8 V

The ESD sensitivity rating of the **VSEL** pin is 1 kV (Human Body Model according to JESD22-A114). A higher protection level can be required if the line is externally accessible on the application board. A higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible points.

2.3.3.2 Guidelines for VSEL layout design

There are no specific layout design recommendations for the **VSEL** input.

2.4 Antenna interface

The **ANT** pin, provided by all the SARA-N2/N3 series modules, represents the RF input/output used to transmit and receive the RF cellular signals: the antenna must be connected to this pin. The **ANT** pin has a nominal characteristic impedance of 50 Ω and must be connected to the antenna through a 50 Ω transmission line to allow transmission and reception of RF signals in the operating bands.

2.4.1 Cellular antenna RF interface (ANT)

2.4.1.1 General guidelines for antenna selection and design

The cellular antenna is the most critical component to be evaluated: care must be taken about it at the start of the design development, when the physical dimensions of the application board are under analysis/decision, since the RF compliance of the device integrating a SARA-N2/N3 series module with all the applicable required certification schemes depends from antenna radiating performance.

Cellular antennas are typically available as:

- External antenna (e.g. linear monopole):
  - External antenna usage basically does not imply physical restrictions on the design of the PCB where the SARA-N2/N3 series module is mounted.
  - The radiation performance mainly depends on the antenna: select the antenna with optimal radiating performance in the operating bands.
  - If antenna detection functionality is required, select an antenna assembly provided with a proper built-in diagnostic circuit with a resistor connected to ground: see section 2.4.3.
  - Select an RF cable with minimum insertion loss: additional insertion loss due to low quality or long cable reduces radiation performance.
  - Select a suitable 50 Ω connector providing proper PCB-to-RF-cable transition: it is recommended to strictly follow the layout and cable termination guidelines provided by the connector manufacturer.
- Integrated antenna (PCB antennas such as patches or ceramic SMT elements):
  - Internal integrated antenna implies physical restriction to the design of the PCB: the ground plane can be reduced down to a minimum size that must be similar to the quarter of the wavelength of the minimum frequency that has to be radiated. As numerical example:

    Frequency = 750 MHz → Wavelength = 40 cm → Minimum GND plane size = 10 cm

  - The radiation performance depends on the whole PCB and antenna system design, including product mechanical design and usage: select the antenna with optimal radiating performance in the operating bands according to the mechanical specifications of the PCB and the whole product.
  - Select a complete custom antenna designed by an antenna manufacturer if the required ground plane dimensions are very small (e.g. less than 6.5 cm long and 4 cm wide): the antenna design process should begin at the start of the whole product design process.
  - Select an integrated antenna solution provided by an antenna manufacturer if the required ground plane dimensions are large enough according to the related integrated antenna solution specifications: the antenna selection and the definition of its placement in the product layout should begin at the start of the product design process.
  - It is highly recommended to strictly follow the detailed and specific guidelines provided by the antenna manufacturer regarding correct installation and deployment of the antenna system, including PCB layout and matching circuitry.
  - Further to the custom PCB and product restrictions, the antenna may require tuning to obtain the required performance to comply with applicable certification schemes. It is recommended to ask the antenna manufacturer for design-in guidelines related to the custom application.

In both cases, selecting an external or an internal antenna, observe these recommendations:

- Select an antenna providing optimal return loss (or V.S.W.R.) figure over all the operating frequencies.
- Select an antenna providing optimal efficiency figure over all the operating frequencies.
- Select an antenna providing appropriate gain figure (i.e. combined antenna directivity and efficiency figure) so that the electromagnetic field radiation intensity do not exceed the regulatory limits specified in some countries (e.g. by FCC in the United States).

☞ For the additional specific guidelines for the SARA-N211 and SARA-N310 modules integration in applications intended for use in potentially explosive atmospheres, see section 2.12.

2.4.1.2 Guidelines for antenna RF interface design

Guidelines for ANT pin RF connection design

Proper transition between the **ANT** pin and the application board PCB must be provided, implementing the following design-in guidelines for the layout of the application PCB close to the pad designed for the **ANT** pin:

- On a multi layer board, the whole layer stack below the RF connection should be free of digital lines
- Increase GND keep-out (i.e. clearance, a void area) around the **ANT** pad, on the top layer of the application PCB, to at least 250 µm up to adjacent pads metal definition and up to 400 µm on the area below the module, to reduce parasitic capacitance to ground, as described in the left picture in Figure 24
- Add GND keep-out (i.e. clearance, a void area) on the buried metal layer below the **ANT** pad if the top-layer to buried layer dielectric thickness is below 200 µm, to reduce parasitic capacitance to ground, as described in the right picture in Figure 24

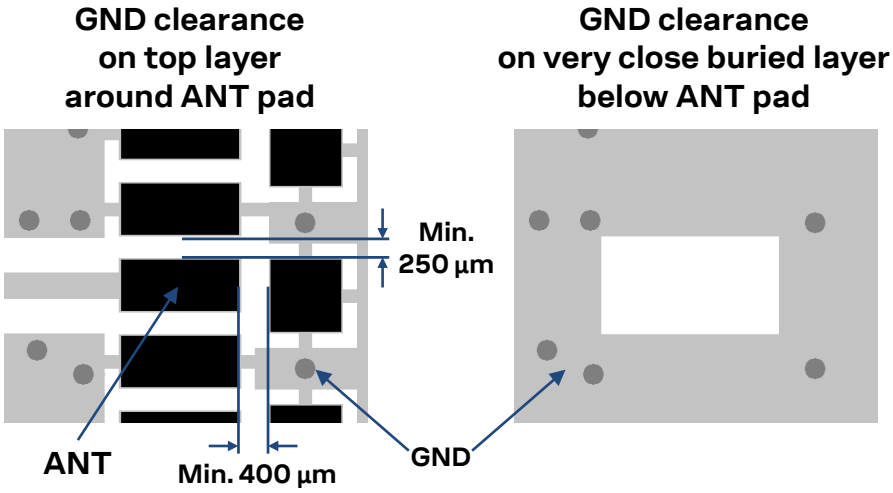

Figure 24: GND keep-out area on the top layer around ANT pad and on the very close buried layer below ANT pad

Guidelines for RF transmission line design

The transmission line from the **ANT** pad up to antenna connector or up to the internal antenna pad must be designed so that the characteristic impedance is as close as possible to 50 Ω.

The transmission line can be designed as a micro strip (consists of a conducting strip separated from a ground plane by a dielectric material) or a strip line (consists of a flat strip of metal which is sandwiched between two parallel ground planes within a dielectric material). The micro strip, implemented as a coplanar waveguide, is the most common configuration for printed circuit board.

Figure 25 and Figure 26 provide two examples of proper 50 Ω coplanar waveguide designs. The first transmission line can be implemented in case of 4-layer PCB stack-up herein described, the second transmission line can be implemented in case of 2-layer PCB stack-up herein described.

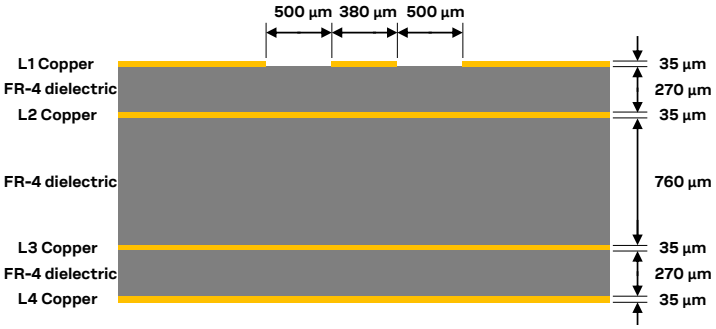

Figure 25: Example of 50 Ω coplanar waveguide transmission line design for the described 4-layer board layup

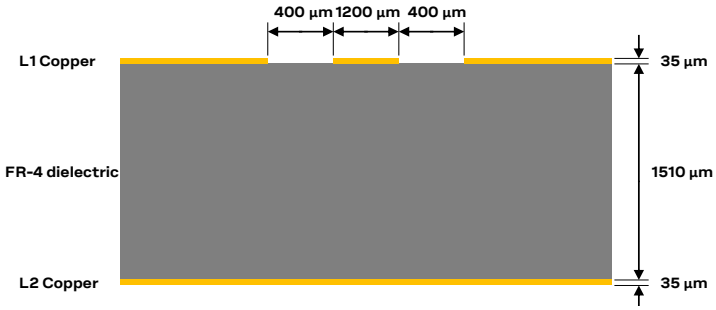

Figure 26: Example of 50 Ω coplanar waveguide transmission line design for the described 2-layer board layup

If the two examples do not match the application PCB layup, the 50 Ω characteristic impedance calculation can be made using the HFSS commercial finite element method solver for electromagnetic structures from Ansys Corporation, or using freeware tools like Avago / Broadcom AppCAD (https://www.broadcom.com/appcad), taking care of the approximation formulas used by the tools for the impedance computation.

To achieve a 50 Ω characteristic impedance, the width of the transmission line must be chosen depending on:

- the thickness of the transmission line itself (e.g. 35 µm in the example of Figure 25 / Figure 26)
- the thickness of the dielectric material between the top layer (where the transmission line is routed) and the inner closer layer implementing the ground plane (e.g. 270 µm in Figure 25, 1510 µm in Figure 26)
- the dielectric constant of the dielectric material (e.g. dielectric constant of the FR-4 dielectric material in Figure 25 and Figure 26)
- the gap from the transmission line to the adjacent ground plane on the same layer of the transmission line (e.g. 500 µm in Figure 25, 400 µm in Figure 26)

If the distance between the transmission line and the adjacent GND area (on the same layer) does not exceed 5 times the track width of the micro strip, use the “Coplanar Waveguide” model for the 50 Ω calculation.

Additionally to the 50 Ω impedance, the following guidelines are recommended for the transmission line design:

- Minimize the transmission line length: the insertion loss should be minimized as much as possible, in the order of a few tenths of a dB.
- Add GND keep-out (i.e. clearance, a void area) on buried metal layers below any pad of component present on the RF transmission line, if top-layer to buried layer dielectric thickness is below 200 µm, to reduce parasitic capacitance to ground.
- The transmission line width and spacing to GND must be uniform and routed as smoothly as possible: avoid abrupt changes of width and spacing to GND.
- Add GND vias around transmission line, as described in Figure 27.
- Ensure solid metal connection of the adjacent metal layer on the PCB stack-up to main ground layer, providing enough on the adjacent metal layer, as described in Figure 27.
- Route RF transmission line far from any noise source (as switching supplies and digital lines) and from any sensitive circuit (as analog audio lines).
- Avoid stubs on the transmission line.
- Avoid signal routing in parallel to transmission line or crossing the transmission line on buried metal layer.
- Do not route microstrip line below discrete component or other mechanics placed on top layer.

Two examples of proper RF circuit design are reported in the Figure 27, where the antenna detection circuit is not implemented (if the antenna detection function is required by the application, follow the guidelines for circuit and layout implementation reported in section 2.4.3):

- In the first example described on the left, the **ANT** pin is directly connected to an SMA connector by means of a proper 50 Ω transmission line, designed with proper layout.
- In the second example described on the right, the **ANT** pin is connected to an SMA connector by means of a proper 50 Ω transmission line, designed with proper layout, with an additional high pass filter (consisting of a proper series capacitor and a proper shunt inductor, as for example the Murata GRM1555C1H150JA01 15 pF capacitor and the Murata LQG15HN39NJ02 39 nH inductor with Self-Resonant Frequency ~1 GHz) to improve the ESD immunity at the antenna port of the modules

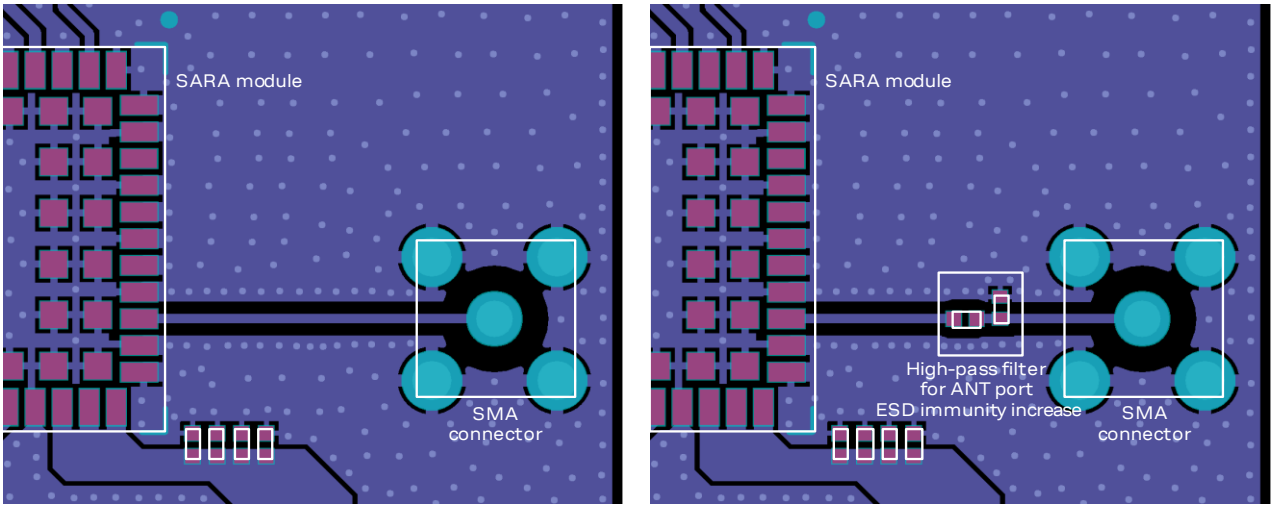

Figure 27: Suggested circuit and layout for antenna RF circuit on application board, if antenna detection is not required

Guidelines for RF termination design

The RF termination must provide a characteristic impedance of 50 Ω as well as the RF transmission line up to the RF termination itself, to match the characteristic impedance of the **ANT** pin of the module.

However, real antennas do not have perfect 50 Ω load on all the supported frequency bands. Therefore, to reduce as much as possible performance degradation due to antenna mismatch, the RF termination must provide optimal return loss (or V.S.W.R.) figure over all the operating frequencies, as summarized in Table 6.

If an external antenna is used, the antenna connector represents the RF termination on the PCB:

- Use a suitable 50 Ω connector providing proper PCB-to-RF-cable transition.
- Strictly follow the connector manufacturer's recommended layout, for example:
  - SMA Pin-Through-Hole connectors require GND keep-out (i.e. clearance, a void area) on all the layers around the central pin up to annular pads of the four GND posts (see Figure 27)
  - U.FL surface mounted connectors require no conductive traces (i.e. clearance, a void area) in the area below the connector between the GND land pads.
- Cut out the GND layer under RF connectors and close to buried vias, to remove stray capacitance and thus keep the RF line 50 Ω: e.g. the active pad of U.FL connectors needs to have a GND keep-out (i.e. clearance, a void area) at least on first inner layer to reduce parasitic capacitance to ground

If an integrated antenna is used, the RF termination is represented by the integrated antenna itself:

- Use an antenna designed by an antenna manufacturer, providing the best possible return loss.
- Provide a ground plane large enough according to the related integrated antenna requirements: the ground plane of the application PCB can be reduced to a minimum size that must be similar to one quarter of wavelength of the minimum frequency that has to be radiated. As numerical example:

  Frequency = 750 MHz → Wavelength = 40 cm → Minimum GND plane size = 10 cm

- It is highly recommended to strictly follow the detailed and specific guidelines provided by the antenna manufacturer regarding correct installation and deployment of the antenna system, including PCB layout and matching circuitry.
- Further to the custom PCB and product restrictions, the antenna may require a tuning to comply with all the applicable required certification schemes. It is recommended to consult the antenna manufacturer for antenna design-in guidelines related to the custom application.

Additionally, these recommendations regarding the antenna system must be followed:

- Do not include antenna within closed metal case.
- Do not place the antenna in close vicinity to end users, since the emitted radiation in human tissue is limited by regulatory requirements.
- Place the antenna far from sensitive analog systems or employ countermeasures to reduce electromagnetic compatibility issues.
- Take care of interaction between co-located RF systems since the cellular transmitted RF power may interact or disturb the performance of companion systems.
- The antenna shall provide optimal efficiency figure over all the operating frequencies.
- The antenna shall provide appropriate gain figure (i.e. combined antenna directivity and efficiency figure) so that the electromagnetic field radiation intensity does not exceed the regulatory limits specified in some countries (e.g. by FCC in the United States).
- Consider including extra footprints for a "pi" network in between the cellular module and the antenna, for further improvement in the antenna matching circuit to reach optimal antenna performance.

Examples of antennas

Table 16 lists some examples of possible internal on-board surface-mount antennas

Manufacturer	Part number	Product name	Description
Taoglas	PA.710.A	Warrior	GSM / WCDMA / LTE SMD Antenna 698..960 MHz, 1710..2170 MHz, 2300..2400 MHz, 2490..2690 MHz 40.0 x 6.0 x 5.0 mm
Taoglas	PCS.06.A	Havok	GSM / WCDMA / LTE SMD Antenna 698..960 MHz, 1710..2170 MHz, 2500..2690 MHz 42.0 x 10.0 x 3.0 mm
Taoglas	MCS6.A		GSM / WCDMA / LTE SMD Antenna 698..960 MHz, 1710..2690 MHz 42.0 x 10.0 x 3.0 mm
Antenova	SR4L002	Lucida	GSM / WCDMA / LTE SMD Antenna 698..960 MHz, 1710..2170 MHz, 2300..2400 MHz, 2490..2690 MHz 35.0 x 8.5 x 3.2 mm
Ethertronics	P822601		GSM / WCDMA / LTE SMD Antenna 698..960 MHz, 1710..2170 MHz, 2490..2700 MHz 50.0 x 8.0 x 3.2 mm
Ethertronics	P822602		GSM / WCDMA / LTE SMD Antenna 698..960 MHz, 1710..2170 MHz, 2490..2700 MHz 50.0 x 8.0 x 3.2 mm
Ethertronics	1002436		GSM / WCDMA / LTE Vertical Mount Antenna 698..960 MHz, 1710..2700 MHz 50.6 x 19.6 x 1.6 mm
Pulse	W3796	Domino	GSM / WCDMA / LTE SMD Antenna 698..960 MHz, 1427..1661 MHz, 1695..2200 MHz, 2300..2700 MHz 42.0 x 10.0 x 3.0 mm
TE Connectivity	2118310-1		GSM / WCDMA / LTE Vertical Mount Antenna 698..960 MHz, 1710..2170 MHz, 2300..2700 MHz 74.0 x 10.6 x 1.6 mm
Molex	1462000001		GSM / WCDMA / LTE SMD Antenna 698..960 MHz, 1700..2700 MHz 40.0 x 5.0 x 5.0 mm
Cirocomm	DPAN0S07		GSM / WCDMA / LTE SMD Antenna 698..960 MHz, 1710..2170 MHz, 2500..2700 MHz 37.0 x 5.0 x 5.0 mm

Table 16: Examples of internal surface-mount antennas

Table 17 lists some examples of possible internal off-board antennas with cable and connector.

Manufacturer	Part number	Product name	Description
Taoglas	FXUB63.07.0150C		GSM / WCDMA / LTE PCB Antenna with cable and U.FL connector 698..960 MHz, 1575.42 MHz, 1710..2170 MHz, 2400..2690 MHz 96.0 x 21.0 mm
Taoglas	FXUB66.07.0150C	Maximus	GSM / WCDMA / LTE Antenna on flexible PCB with cable and U.FL 698..960 MHz, 1390..1435 MHz, 1575.42 MHz, 1710..2170 MHz, 2400..2700 MHz, 3400..3600 MHz, 4800..6000 MHz 120.2 x 50.4 mm
Antenova	SRFL029	Moseni	GSM / WCDMA / LTE Antenna on flexible PCB with cable and U.FL 689..960 MHz, 1710..2170 MHz, 2300..2400 MHz, 2500..2690 MHz 110.0 x 20.0 mm
Antenova	SRFL026	Mitis	GSM / WCDMA / LTE Antenna on flexible PCB with cable and U.FL 689..960 MHz, 1710..2170 MHz, 2300..2400 MHz, 2500..2690 MHz 110.0 x 20.0 mm
Ethertronics	1002289		GSM / WCDMA / LTE Antenna on flexible PCB with cable and U.FL 698..960 MHz, 1710..2700 MHz 140.0 x 75.0 mm
EAD	FSQS35241-UF-10	SQ7	GSM / WCDMA / LTE PCB Antenna with cable and U.FL connector 690..960 MHz, 1710..2170 MHz, 2500..2700 MHz 110.0 x 21.0 mm

Table 17: Examples of internal antennas with cable and connector

Table 18 lists some examples of possible external antennas.

Manufacturer	Part number	Product name	Description
Taoglas	GSA.8827.A.101111	Phoenix	GSM / WCDMA / LTE low-profile adhesive-mount Antenna with cable and SMA(M) connector 698..960 MHz, 1575.42 MHz, 1710..2170 MHz, 2490..2690 MHz 105 x 30 x 7.7 mm
Taoglas	TG.30.8112		GSM / WCDMA / LTE swivel dipole Antenna with SMA(M) connector 698..960 MHz, 1575.42 MHz, 1710..2170 MHz, 2400..2700 MHz 148.6 x 49 x 10 mm
Taoglas	MA241.BI.001	Genesis	GSM / WCDMA / LTE MIMO 2in1 adhesive-mount combination antenna waterproof IP67 rated with cable and SMA(M) 698..960 MHz, 1710..2170 MHz, 2400..2700 MHz 205.8 x 58 x 12.4 mm
Laird Tech.	TRA6927M3PW-001		GSM / WCDMA / LTE screw-mount antenna with N-type(F) 698..960 MHz, 1710..2170 MHz, 2300..2700 MHz 83.8 x Ø 36.5 mm
Laird Tech.	CMS69273		GSM / WCDMA / LTE ceiling-mount Antenna with N-type(F) connector 698..960 MHz, 1575.42 MHz, 1710..2700 MHz 86 x Ø 199 mm
Laird Tech.	OC69271-FNM		GSM / WCDMA / LTE pole-mount Antenna with N-type(M) connector 698..960 MHz, 1710..2690 MHz 248 x Ø 24.5 mm
Pulse Electronics	WA700/2700SMA		GSM / WCDMA / LTE clip-mount MIMO antenna with cables and SMA(M) 698..960 MHz,1710..2700 MHz 149 x 127 x 5.1 mm

Table 18: Examples of external antennas

2.4.2 Bluetooth antenna RF interface (ANT_BT)

☞ The Bluetooth functionality is not available in SARA-N2 series modules.

☞ The Bluetooth functionality is not supported by "00" product version of SARA-N3 series modules. The **ANT_BT** pin can be left unconnected or it can also be connected to GND.

2.4.3 Antenna detection interface (ANT_DET)

☞ The antenna detection interface is not supported by "02" product version of SARA-N2 series modules.

2.4.3.1 Guidelines for ANT_DET circuit design

Figure 28 and Table 19 describe the recommended schematic and components for the antenna detection circuit to be provided on the application board for the diagnostic circuit that must be provided on the antenna assembly to achieve antenna detection functionality.

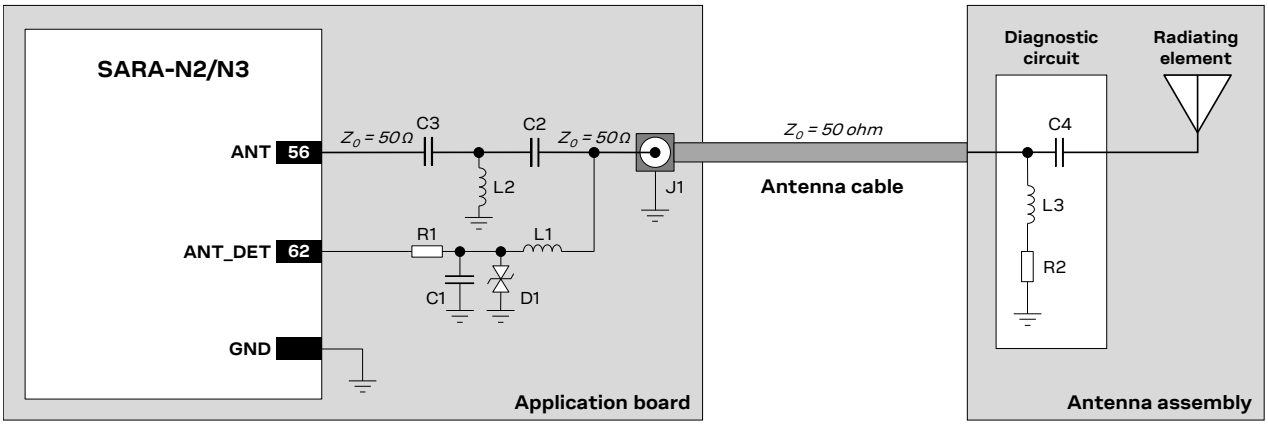

Figure 28: Suggested schematic for antenna detection circuit on application PCB and diagnostic circuit on antenna assembly

Reference	Description	Part Number - Manufacturer
C1	27 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H270J - Murata
C2	33 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H330J - Murata
D1	Very Low Capacitance ESD Protection	PESD0402-140 - Tyco Electronics
L1	68 nH Multilayer Inductor 0402 (SRF ~1 GHz)	LQG15HS68NJ02 - Murata
R1	10 kΩ Resistor 0402 1% 0.063 W	RK73H1ETTP1002F - KOA Speer
J1	SMA Connector 50 Ω Through Hole Jack	SMA6251A1-3GT50G-50 - Amphenol
C3	15 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H150J - Murata
L2	39 nH Multilayer Inductor 0402 (SRF ~1 GHz)	LQG15HN39NJ02 - Murata
C4	22 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1H220J - Murata
L3	68 nH Multilayer Inductor 0402 (SRF ~1 GHz)	LQG15HS68NJ02 - Murata
R2	15 kΩ Resistor for Diagnostic	Various Manufacturers

Table 19: Suggested parts for antenna detection circuit on application board and diagnostic circuit on antenna assembly

The antenna detection circuit and diagnostic circuit shown in Figure 28 / Table 19 are explained below:

- When antenna detection is forced by the dedicated AT command (see SARA-N2/N3 series AT commands manual [4]), the **ANT_DET** pin generates a DC current measuring the resistance (R2) from the antenna connector (J1) provided on the application board to GND.
- DC blocking capacitors are needed at the **ANT** pin (C2) and at the antenna radiating element (C4) to decouple the DC current generated by the **ANT_DET** pin.
- Choke inductors with a Self Resonance Frequency (SRF) in the range of 1 GHz are needed in series at the **ANT_DET** pin (L1) and in series at the diagnostic resistor (L3), to avoid a reduction of the RF performance of the system, improving the RF isolation of the load resistor.
- Additional components (R1, C1 and D1 in Figure 28) are needed at the **ANT_DET** pin as ESD protection.
- Additional high pass filter (C3 and L2 in Figure 28) is provided at the **ANT** pin as ESD immunity improvement
- The **ANT** pin must be connected to the antenna connector by means of a transmission line with nominal characteristics impedance as close as possible to 50 Ω.

The DC impedance at RF port for some antennas may be a DC open (e.g. linear monopole) or a DC short to reference GND (e.g. PIFA antenna). For those antennas, without the diagnostic circuit of Figure 28, the measured DC resistance is always at the limits of the measurement range (respectively open or short), and there is no mean to distinguish between a defect on antenna path with similar characteristics (respectively: removal of linear antenna or RF cable shorted to GND for PIFA antenna).

Furthermore, any other DC signal injected to the RF connection from ANT connector to radiating element will alter the measurement and produce invalid results for antenna detection.

☞ It is recommended to use an antenna with a built-in diagnostic resistor in the range from 5 kΩ to 30 kΩ to assure good antenna detection functionality and avoid a reduction of module RF performance. The choke inductor should exhibit a parallel Self Resonance Frequency (SRF) in the range of 1 GHz to improve the RF isolation of load resistor.

For example:

Consider an antenna with built-in DC load resistor of 15 kΩ. Using the dedicated AT command (see SARA-N2/N3 series AT commands manual [4]), the module reports the resistance value evaluated from the antenna connector provided on the application board to GND:

- Reported values close to the used diagnostic resistor nominal value (i.e. values from 13 kΩ to 17 kΩ if a 15 kΩ diagnostic resistor is used) indicate that the antenna is properly connected.
- Values close to the measurement range maximum limit, or an open-circuit “over range” report, means that that the antenna is not connected or the RF cable is broken.
- Reported values below the measurement range minimum limit (1 kΩ) highlights a short to GND at antenna or along the RF cable.
- Measurement inside the valid measurement range and outside the expected range may indicate an improper connection, damaged antenna or wrong value of antenna load resistor for diagnostic.
- Reported value could differ from the real resistance value of the diagnostic resistor mounted inside the antenna assembly due to antenna cable length, antenna cable capacity and the used measurement method.

☞ If the antenna detection function is not required by the customer application, the **ANT_DET** pin can be left not connected and the **ANT** pin can be directly connected to the antenna connector by means of a 50 Ω transmission line as described in Figure 27.

2.4.3.2 Guidelines for ANT_DET layout design

Figure 29 describes the recommended layout for the antenna detection circuit to be provided on the application board to achieve antenna detection functionality, implementing the recommended schematic described in the previous Figure 28 and Table 19.

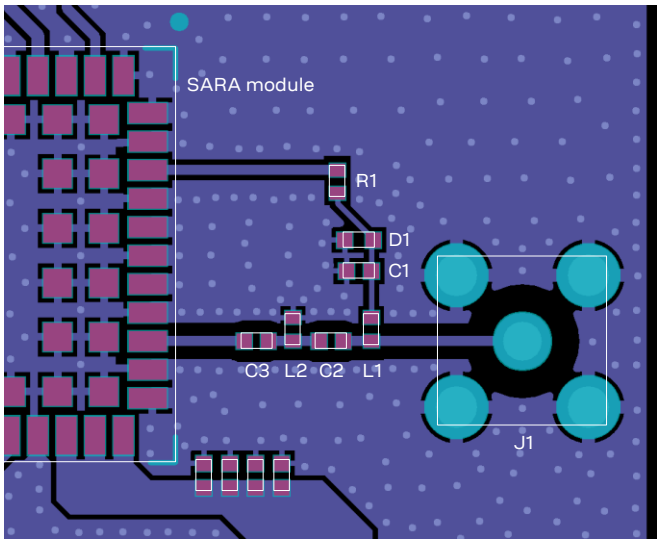

Figure 29: Suggested layout for antenna detection circuit on application board

The antenna detection circuit layout suggested in Figure 29 is here explained:

- The **ANT** pin is connected to the antenna connector by means of a 50 Ω transmission line, implementing the design guidelines described in section 2.4.1 and the recommendations of the SMA connector manufacturer.
- DC blocking capacitor at the **ANT** pin (C2) is placed in series to the 50 Ω transmission line.
- The **ANT_DET** pin is connected to the 50 Ω transmission line by means of a sense line.
- Choke inductor in series at the **ANT_DET** pin (L1) is placed so that one pad is on the 50 Ω transmission line and the other pad represents the start of the sense line to the **ANT_DET** pin.
- The additional components (R1, C1 and D1) on the **ANT_DET** line are placed as ESD protection.
- The additional high pass filter (C3 and L2) on the **ANT** line are placed as ESD immunity improvement.

2.5 SIM interface

2.5.1.1 Guidelines for SIM circuit design

Guidelines for SIM cards, SIM connectors and SIM chips selection

The ISO/IEC 7816, the ETSI TS 102 221 and the ETSI TS 102 671 specifications define the physical, electrical and functional characteristics of Universal Integrated Circuit Cards (UICC) which contains the Subscriber Identification Module (SIM) integrated circuit that securely stores all the information needed to identify and authenticate subscribers over the cellular network.

Removable UICC / SIM card contacts mapping is defined by ISO/IEC 7816 and ETSI TS 102 221 as follows:

- Contact C1 = VCC (Supply) → It must be connected to **VSIM**
- Contact C2 = RST (Reset) → It must be connected to **SIM_RST**
- Contact C3 = CLK (Clock) → It must be connected to **SIM_CLK**
- Contact C4 = AUX1 (Auxiliary contact) → It must be left not connected
- Contact C5 = GND (Ground) → It must be connected to **GND**
- Contact C6 = VPP (other) → It can be left not connected
- Contact C7 = I/O (Data input/output) → It must be connected to **SIM_IO**
- Contact C8 = AUX2 (Auxiliary contact) → It must be left not connected

A removable SIM card can have 6 contacts (C1 = VCC, C2 = RST, C3 = CLK, C5 = GND, C6 = VPP, C7 = I/O) or 8 contacts, providing also the auxiliary contacts C4 = AUX1 and C8 = AUX2 for USB interfaces and other uses. Only 5 contacts are required and must be connected to the module SIM card interface as described above, since the modules do not support the additional auxiliary features (contacts C4 = AUX1 and C8 = AUX2).

Removable SIM card are suitable for applications where the SIM changing is required during the product lifetime.

A SIM card holder can have 6 or 8 positions if a mechanical card presence detector is not provided, or it can have 6+2 or 8+2 positions if two additional pins related to the normally-open mechanical switch integrated in the SIM connector for the mechanical card presence detection are provided.

Solderable UICC / SIM chip contacts mapping (M2M UICC Form Factor) is defined by ETSI TS 102 671 as follows:

- Package pin 8 = UICC contact C1 = VCC (Supply) → It must be connected to **VSIM**
- Package pin 7 = UICC contact C2 = RST (Reset) → It must be connected to **SIM_RST**
- Package pin 6 = UICC contact C3 = CLK (Clock) → It must be connected to **SIM_CLK**
- Package pin 5 = UICC contact C4 = AUX1 (Auxiliary) → It must be left not connected
- Package pin 1 = UICC contact C5 = GND (Ground) → It must be connected to **GND**
- Package pin 2 = UICC contact C6 = VPP (other) → It can be left not connected
- Package pin 3 = UICC contact C7 = I/O (Data I/O) → It must be connected to **SIM_IO**
- Package pin 4 = UICC contact C8 = AUX2 (Auxiliary) → It must be left not connected

A solderable SIM chip has 8 contacts and can provide also the auxiliary contacts C4 = AUX1 and C8 = AUX2 for USB interfaces and other uses, but only 5 contacts are required and must be connected to the module SIM card interface as described above, since the SARA-N2/N3 series modules do not support the additional auxiliary features (contacts C4 = AUX1 and C8 = AUX2).

Solderable SIM chips are suitable for M2M applications where it is not required to change the SIM once installed.

Guidelines for SIM card connection

An application circuit for the connection to a removable SIM card placed in a SIM card holder is described in Figure 30.

Follow these guidelines connecting the module to a SIM connector:

- Connect the UICC / SIM contact C1 (VCC) to the **VSIM** pin of the module.
- Connect the UICC / SIM contact C7 (I/O) to the **SIM_IO** pin of the module.
- Connect the UICC / SIM contact C3 (CLK) to the **SIM_CLK** pin of the module.
- Connect the UICC / SIM contact C2 (RST) to the **SIM_RST** pin of the module.
- Connect the UICC / SIM contact C5 (GND) to ground.
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) at the SIM supply line (**VSIM**), close to the related pad of the SIM connector, to prevent digital noise.
- Provide a bypass capacitor of about 22 pF to 33 pF (e.g. Murata GRM1555C1H330JA01) on each SIM line (**VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST**), very close to each related pad of the SIM connector, to prevent RF coupling especially in case the RF antenna is placed closer than 10 - 30 cm from the SIM card holder.
- Provide a low capacitance (i.e. less than 1 pF) ESD protection (e.g. Tyco Electronics PESD0402-140) on each externally accessible SIM line, close to each related pad of the SIM connector ESD sensitivity rating of the SIM interface pins is 1 kV (Human Body Model according to JESD22-A114), so that, according to the EMC/ESD requirements of the custom application, higher protection level can be required if the lines are externally accessible on the application device.
- Limit capacitance and series resistance on each SIM signal (**SIM_CLK**, **SIM_IO**, **SIM_RST**) to match the requirements for the SIM interface regarding maximum allowed rise time on the lines.

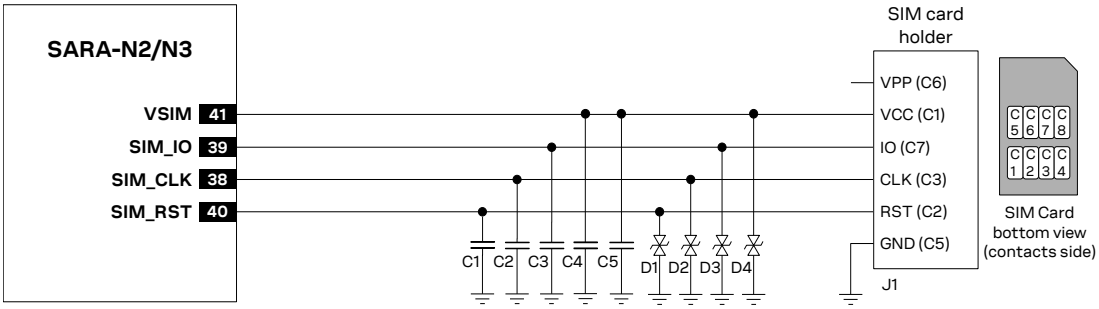

Figure 30: Application circuit for the connection to a single removable SIM card

Reference	Description	Part Number - Manufacturer
C1, C2, C3, C4	33 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H330JA01 - Murata
C5	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
D1, D2, D3, D4	Very Low Capacitance ESD Protection	PESD0402-140 - Tyco Electronics
J1	SIM Card Holder 6 positions, without card presence switch	Various Manufacturers, C707 10M006 136 2 - Amphenol

Table 20: Example of components for the connection to a removable SIM card

Guidelines for single SIM chip connection

Figure 31 describes an application circuit for the connection to a solderable SIM chip (M2M UICC Form Factor).

Follow these guidelines connecting the module to a solderable SIM chip:

- Connect the UICC / SIM contact C1 (VCC) to the **VSIM** pin of the module.
- Connect the UICC / SIM contact C7 (I/O) to the **SIM_IO** pin of the module.
- Connect the UICC / SIM contact C3 (CLK) to the **SIM_CLK** pin of the module.
- Connect the UICC / SIM contact C2 (RST) to the **SIM_RST** pin of the module.
- Connect the UICC / SIM contact C5 (GND) to ground.
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) at the SIM supply line (**VSIM**) close to the related pad of the SIM chip, to prevent digital noise.
- Provide a bypass capacitor of about 22 pF to 33 pF (e.g. Murata GRM1555C1H330JA01) on each SIM line (**VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST**), to prevent RF coupling especially in case the RF antenna is placed closer than 10 - 30 cm from the SIM card holder.
- Limit capacitance and series resistance on each SIM signal (**SIM_CLK**, **SIM_IO**, **SIM_RST**) to match the requirements for the SIM interface regarding maximum allowed rise time on the lines.

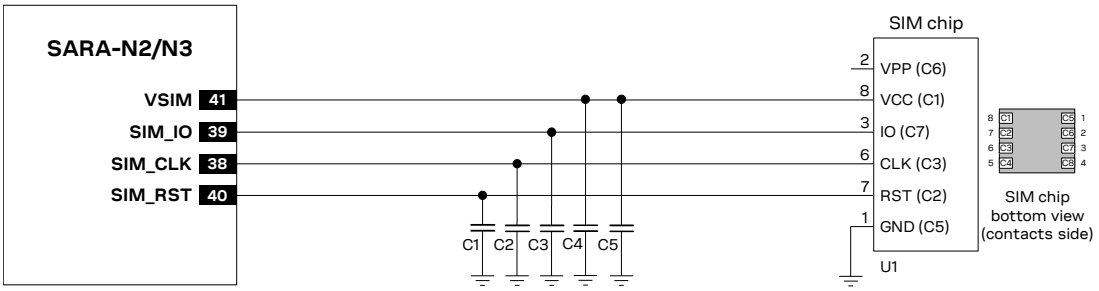

Figure 31: Application circuit for the connection to a single solderable SIM chip

Reference	Description	Part Number - Manufacturer
C1, C2, C3, C4	33 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H330JA01 - Murata
C5	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
U1	SIM chip (M2M UICC Form Factor)	Various Manufacturers

Table 21: Example of components for the connection to a solderable SIM chip

Guidelines for single SIM card connection with detection

☞ The SIM card detection functionality over GPIO is not supported by the SARA-N2 series modules.

An application circuit for connecting to a single removable SIM card placed in a SIM card holder is described in Figure 32, where the optional SIM card detection feature is implemented.

Follow these guidelines while connecting the module to a SIM connector implementing SIM presence detection:

- Connect the UICC / SIM contact C1 (VCC) to the **VSIM** pin of the module.
- Connect the UICC / SIM contact C7 (I/O) to the **SIM_IO** pin of the module.
- Connect the UICC / SIM contact C3 (CLK) to the **SIM_CLK** pin of the module.
- Connect the UICC / SIM contact C2 (RST) to the **SIM_RST** pin of the module.
- Connect the UICC / SIM contact C5 (GND) to ground.
- Connect one pin of the normally-open mechanical switch integrated in the SIM connector (as the SW2 pin in Figure 32) to the **GPIO5** input pin, providing a weak pull-down resistor (e.g. 470 kΩ, as R2 in Figure 32).

- Connect the other pin of the normally-open mechanical switch integrated in the SIM connector (SW1 pin in Figure 32) to **V_INT** 1.8 V supply output by means of a strong pull-up resistor (e.g. 1 kΩ, as R1 in Figure 32)
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) at the SIM supply line (**VSIM**), close to the related pad of the SIM connector, to prevent digital noise.
- Provide a bypass capacitor of about 22 pF to 33 pF (e.g. Murata GRM1555C1H330JA01) on each SIM line (**VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST**), very close to each related pad of the SIM connector, to prevent RF coupling especially in case the RF antenna is placed closer than 10 - 30 cm from the SIM card holder.
- Provide a low capacitance (i.e. less than 1 pF) ESD protection (e.g. Tyco Electronics PESD0402-140) on each externally accessible SIM line, close to each related pad of the SIM connector. The ESD sensitivity rating of SIM interface pins is 1 kV (HBM according to JESD22-A114), so that, according to the EMC/ESD requirements of the custom application, higher protection level can be required if the lines are externally accessible.
- Limit capacitance and series resistance on each SIM signal to match the requirements for the SIM interface (18.7 ns = maximum rise time on **SIM_CLK**, 1.0 µs = maximum rise time on **SIM_IO** and **SIM_RST**).

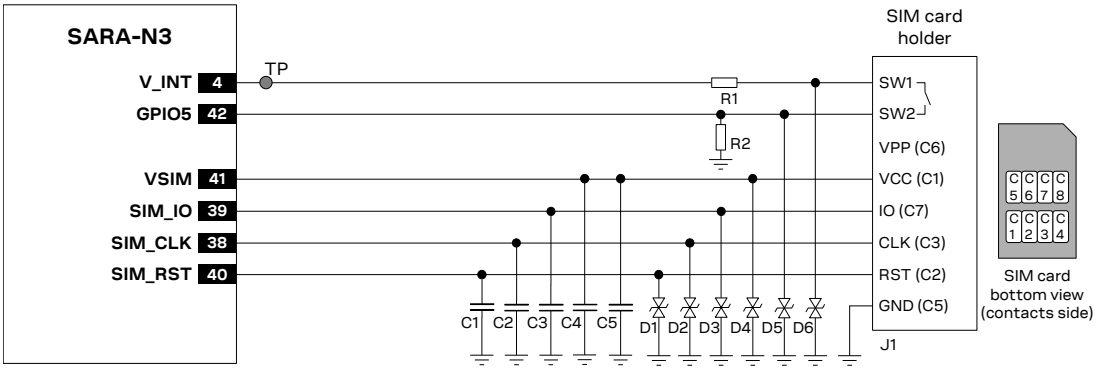

Figure 32: Application circuit for the connection to a single removable SIM card, with SIM detection implemented

Reference	Description	Part Number - Manufacturer
C1, C2, C3, C4	33 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H330JA01 - Murata
C5	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
D1 – D6	Very Low Capacitance ESD Protection	PESD0402-140 - Tyco Electronics
R1	1 kΩ Resistor 0402 5% 0.1 W	RC0402JR-071KL - Yageo Phycomp
R2	470 kΩ Resistor 0402 5% 0.1 W	RC0402JR-07470KL- Yageo Phycomp
J1	SIM Card Holder 6 + 2 positions, with card presence switch	Various Manufacturers, CCM03-3013LFT R102 - C&K Components

Table 22: Example of components for the connection to a single removable SIM card, with SIM detection implemented

2.5.1.2 Guidelines for SIM layout design

The layout of the SIM card interface lines (**VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST**) may be critical if the SIM card is placed far away from the SARA-N2/N3 series modules or in close proximity to the RF antenna: these two cases should be avoided or at least mitigated as described below.

In the first case, the long connection can cause the radiation of some harmonics of the digital data frequency as any other digital interface: keep the traces short and avoid coupling with RF line or sensitive analog inputs.

In the second case, the same harmonics can be picked up and create self-interference that can reduce the sensitivity of the receiver channels whose carrier frequency is coincidental with harmonic frequencies: placing the RF bypass capacitors suggested in 2.5.1.1 near the SIM connector will mitigate the problem.

In addition, since the SIM card is typically accessed by the end user, it can be subjected to ESD discharges: add adequate ESD protection as suggested in 2.5.1.1 to protect module SIM pins near the SIM connector.

Limit capacitance and series resistance on each SIM signal to match the SIM specifications: the connections should always be kept as short as possible.

Avoid coupling with any sensitive analog circuit, since the SIM signals can cause the radiation of some harmonics of the digital data frequency.

2.6 Serial interfaces

2.6.1 Main primary UART interface

The SARA-N2 modules do not support hardware flow control functionality over the **CTS** and **RTS** pins. The SARA-N2 modules do not include the **DTR**, **DSR**, **DCD** and **RI** pins.

The "00" product version of SARA-N3 modules do not support **DTR**, **DSR** and **DCD** functionality: the lines can be left unconnected, and the **DTR** input line can also be connected to GND.

2.6.1.1 Guidelines for main primary UART circuit design

Guidelines for SARA-N3 modules' TXD, RXD, RTS, CTS and RI lines connection

If RS-232 compatible signal levels are needed, two different external voltage translators (e.g. Maxim MAX3237E and Texas Instruments SN74AVC4T774) can be used. The Texas Instruments chips provide the translation from 1.8 V / 2.8 V to 3.3 V, while the Maxim chip provides the translation from 3.3 V to RS-232 compatible signal level.

If a 1.8 V application processor (DTE) is used, and the generic digital interfaces of the module (DCE) are configured to operate at 1.8 V (**V_INT** = 1.8 V, if **VSEL** pin is connected to GND: see 1.5.3), the circuit should be implemented as described in Figure 33.

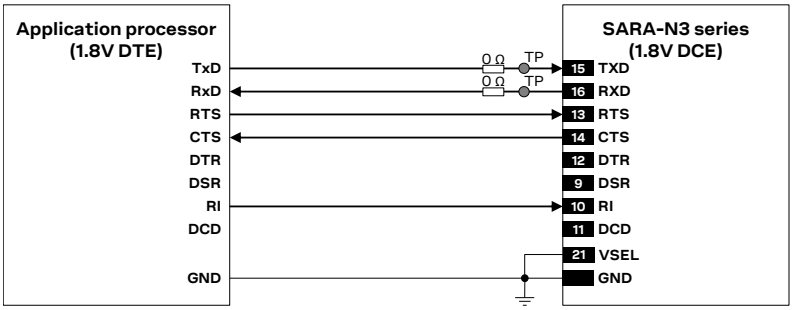

Figure 33: SARA-N3 series' UART application circuit with TXD, RXD, RTS, CTS and RI lines connection (1.8 V DTE / 1.8 V DCE)

If a 2.8 V application processor (DTE) is used, and the generic digital interfaces of the module (DCE) are configured to operate at 2.8 V (**V_INT** = 2.8 V, if **VSEL** pin is left unconnected: see 1.5.3), the circuit should be implemented as described in Figure 34.

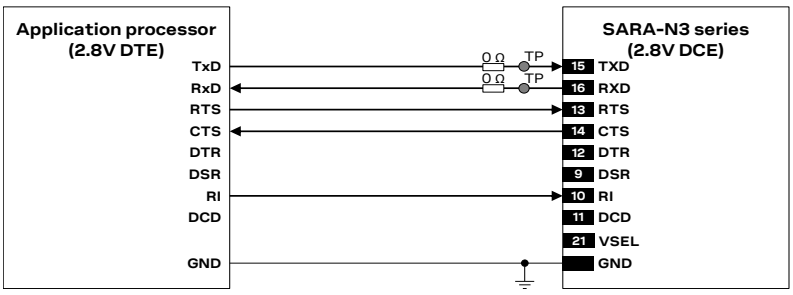

Figure 34: SARA-N3 series' UART application circuit with TXD, RXD, RTS, CTS and RI lines connection (2.8 V DTE / 2.8 V DCE)

If a 3.0 V application processor is used and the generic digital interfaces of the module are configure to operate at 1.8 V (**V_INT** = 1.8 V, if **VSEL** pin is connected to GND: see 1.5.3), then the 1.8 V UART of the module (DCE) can be connected to the 3.0 V UART of the application processor (DTE) by means of an appropriate unidirectional voltage translators providing partial power down feature (thus the DTE 3.0 V supply can be also ramped up before the module **V_INT** 1.8 V supply), using the **V_INT** supply output of the module as the 1.8 V supply for the voltage translators on the module side, and the 3.0 V supply rail application processor on the application processor side.

Guidelines for SARA-N3 modules' TXD, RXD, RTS and CTS lines connection

If RS-232 compatible signal levels are needed, two different external voltage translators (e.g. Maxim MAX3237E and Texas Instruments SN74AVC4T774) can be used. The Texas Instruments' chips provide the translation from 1.8 V / 2.8 V to 3.3 V, while the Maxim chip provides the translation from 3.3 V to RS-232 compatible signal level.

If a 1.8 V application processor (DTE) is used, and the generic digital interfaces of the module (DCE) are configured to operate at 1.8 V (**V_INT** = 1.8 V, if **VSEL** pin is connected to GND; see 1.5.3), the circuit should be implemented as described in Figure 35.

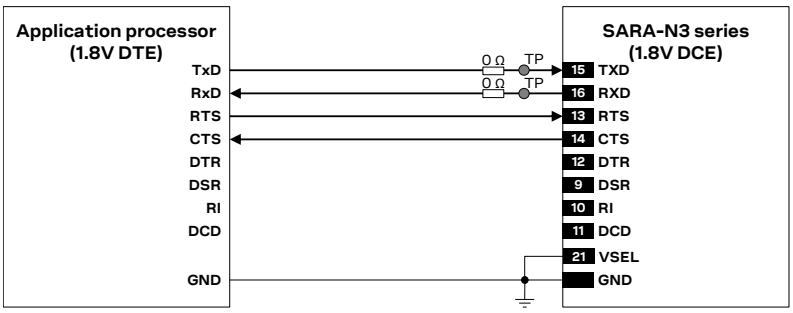

Figure 35: SARA-N3 series' UART application circuit with TXD, RXD, RTS and CTS lines connection (1.8 V DTE / 1.8 V DCE)

If a 2.8 V application processor (DTE) is used, and the generic digital interfaces of the module (DCE) are configured to operate at 2.8 V (**V_INT** = 2.8 V, if **VSEL** pin is left unconnected: see 1.5.3), the circuit should be implemented as described in Figure 36.

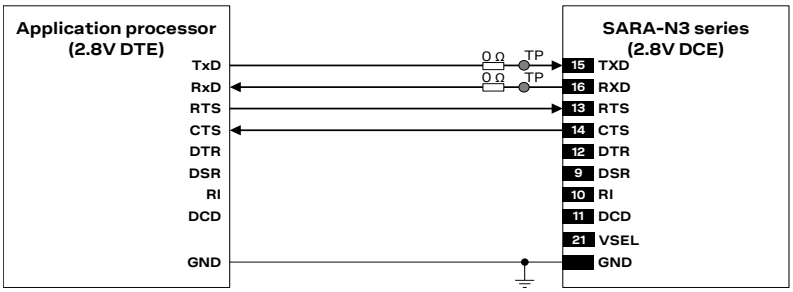

Figure 36: SARA-N3 series' UART application circuit with TXD, RXD, RTS and CTS lines connection (2.8 V DTE / 2.8 V DCE)

If a 3.0 V application processor is used and the generic digital interfaces of the module are configured to operate at 1.8 V (**V_INT** = 1.8 V, if **VSEL** pin is connected to GND: see 1.5.3), then the 1.8 V UART of the module (DCE) can be connected to the 3.0 V UART of the application processor (DTE) by means of an appropriate unidirectional voltage translators providing partial power down feature (thus the DTE 3.0 V supply can be also ramped up before the module **V_INT** 1.8 V supply), using the **V_INT** supply output of the module as the 1.8 V supply for the voltage translators on the module side, and the 3.0 V supply rail application processor on the application processor side.

Guidelines for SARA-N3 modules' TXD and RXD lines connection

If RS-232 compatible signal levels are needed, two different external voltage translators (e.g. Maxim MAX3237E and Texas Instruments SN74AVC4T774) can be used. The Texas Instruments' chips provide the translation from 1.8 V / 2.8 V to 3.3 V, while the Maxim chip provides the translation from 3.3 V to RS-232 compatible signal level.

If a 1.8 V application processor (DTE) is used, and the generic digital interfaces of the module (DCE) are configured to operate at 1.8 V (**V_INT** = 1.8 V, if **VSEL** pin is connected to GND; see 1.5.3), the circuit should be implemented as described in Figure 37.

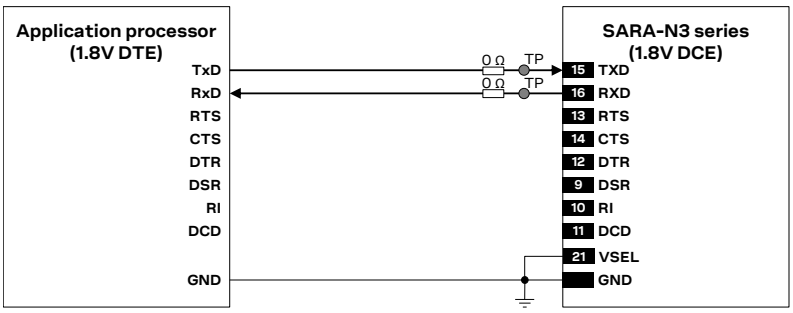

Figure 37: SARA-N3 series' UART application circuit with TXD and RXD lines connection (1.8 V DTE / 1.8 V DCE)

If a 2.8 V application processor (DTE) is used, and the generic digital interfaces of the module (DCE) are configured to operate at 2.8 V (**V_INT** = 2.8 V, if **VSEL** pin is left unconnected: see 1.5.3), the circuit should be implemented as described in Figure 38.

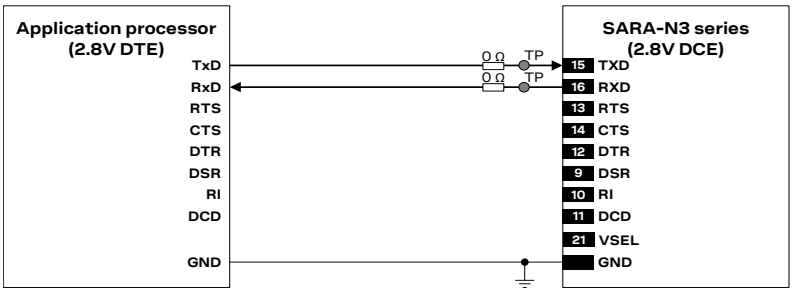

Figure 38: SARA-N3 series' UART application circuit with TXD and RXD lines connection (2.8 V DTE / 2.8 V DCE)

If a 3.0 V application processor is used and the generic digital interfaces of the module are configured to operate at 1.8 V (**V_INT** = 1.8 V, if **VSEL** pin is connected to GND: see 1.5.3), then the 1.8 V UART of the module (DCE) can be connected to the 3.0 V UART of the application processor (DTE) by means of an appropriate unidirectional voltage translators providing partial power down feature (thus the DTE 3.0 V supply can be also ramped up before the module **V_INT** 1.8 V supply), using the **V_INT** supply output of the module as the 1.8 V supply for the voltage translators on the module side, and the 3.0 V supply rail application processor on the application processor side.

Guidelines for SARA-N2 modules' UART lines connection

If RS-232 compatible signal levels are needed, an external voltage translators (e.g. Maxim MAX3237E) can be used to provide the translation from the **VCC** signal level of SARA-N2 modules' UART interface (3.3 ÷ 3.6 V) to RS-232 compatible signal level.

If a 3.3 V Application Processor (DTE) is used, which is the preferred solution, the UART interface of SARA-N2 module can be directly connected with the UART of the DTE as shown in Figure 39:

- Connect DTE TxD output line with the TXD input pin of SARA-N2 modules
- Connect DTE RxD input line with the RXD output pin of SARA-N2 modules
- RTS and CTS lines of the module can be left unconnected and floating, because hardware flow control is not supported by "02" product version of the SARA-N2 modules
- Use the same external supply rail (for example, at 3.3 V or 3.6 V) for both the SARA-N2 module and the Application Processor (DTE), so that the interface of both devices operates at the same level, considering that the UART interface of SARA-N2 modules operates at the VCC voltage level

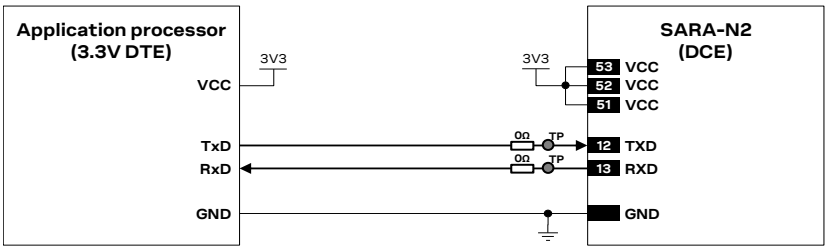

Figure 39: SARA-N2 series' UART interface application circuit with TXD and RXD lines connection to 3.3 V DTE

If a 1.8 V Application Processor (DTE) is used, then it is recommended to connect the UART interface of the module (DCE) by means of appropriate unidirectional voltage translators using the module **VCC** line as the supply for the voltage translators on the module side, as described in Figure 40.

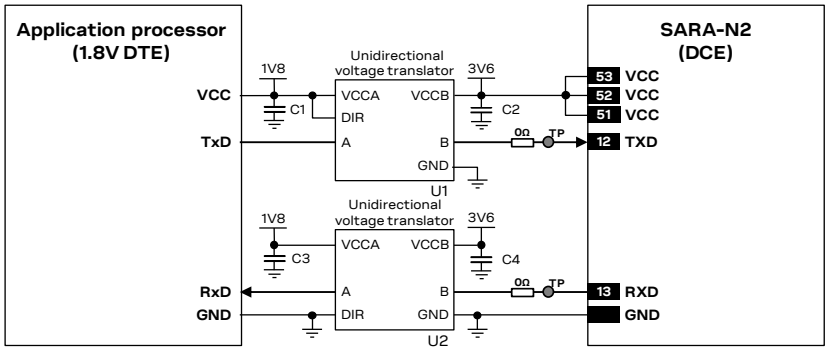

Figure 40: SARA-N2 series' UART interface application circuit with TXD and RXD lines connection to 1.8 V DTE

Reference	Description	Part Number - Manufacturer
C1, C2, C3, C4	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
U1, U2	Unidirectional Voltage Translator	SN74LVC1T45 - Texas Instruments

Table 23: Parts for SARA-N2 series' UART interface application circuit with TXD and RXD lines connection to 1.8 V DTE

☞ It is **not** recommended to use **V_INT** pin of the SARA-N2 module as control and/or supply line for the external voltage translator.

☞ It is recommended to provide a direct access to the **TXD** and **RXD** lines by means of accessible testpoints for diagnostic purpose.

If the application board requires a RING indication to get notifications when an URC or when new data is available, the **CTS** line of SARA-N2 modules can be used for such a functionality. In this case the circuit should be implemented as shown in Figure 41:

- Connect DTE TxD output line with the TXD input pin of SARA-N2 modules
- Connect DTE RxD input line with the RXD output pin of SARA-N2 modules
- Connect DTE RI input line with the CTS output pin of SARA-N2 modules
- Leave RTS line of the module unconnected and floating.
- Use the same external supply rail (for example, at 3.3 V or 3.6 V) for both the SARA-N2 module and the Application Processor (DTE), so that the interface of both devices operates at the same level, considering that the UART interface of SARA-N2 modules operates at the VCC voltage level

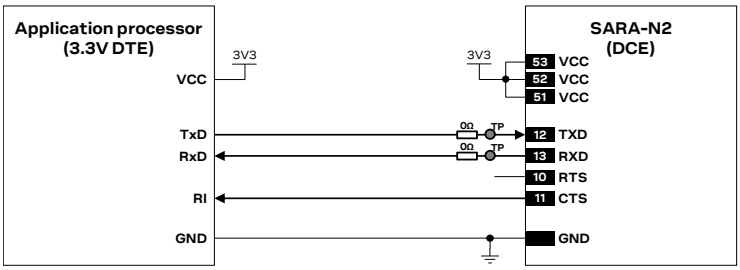

Figure 41: SARA-N2 series' UART interface application circuit with TXD, RXD and RING lines connection to 3.3 V DTE

Additional considerations

If a 1.8 V Application Processor (DTE) is used, the voltage scaling from any UART output of the module (DCE), working at **VCC** voltage level (3.6 V nominal), to the apposite 1.8 V input of the DTE can be implemented, as an alternative low-cost solution, by means of an appropriate voltage divider. Consider the value of the pull-up integrated at the input of the Application Processor (DTE), if any, for the correct selection of the voltage divider resistance values.

Mind that any DTE signal connected to the UART interface of the module has to be tri-stated or set low before the turn-on of the supply rail of the modules' UART interface (**VCC** for SARA-N2 modules, **V_INT** for SARA-N3 modules), to avoid latch-up of circuits and allow a proper boot of the module.

There is **no** internal pull-up / pull-down inside the **TXD** input line of the SARA-N2 module, which is assumed to be controlled by the external host once UART is initialized: to avoid an increase in current consumption, consider to add an external pull-up resistor of about 47 kΩ to 100 kΩ, biased by **VCC** module supply rail, if the **TXD** input is left floating by the external host in some scenario.

An internal pull-up is integrated inside the **TXD** input line of the SARA-N3 modules: an external pull-up resistor is not required.

ESD sensitivity rating of UART pins is 1 kV (HBM according to JESD22-A114). Higher protection level could be required if the lines are externally accessible on the application board. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor) close to accessible points.

2.6.1.2 Guidelines for main primary UART layout design

The UART serial interface requires the same consideration regarding electro-magnetic interference as any other digital interface. Keep the traces short and avoid coupling with RF line or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.

2.6.2 Secondary auxiliary UART interface

SARA-N2 modules do not include a secondary auxiliary UART interface.

SARA-N3 "00" product version do not support a secondary auxiliary UART interface.

2.6.2.1 Guidelines for secondary auxiliary UART circuit design

If RS-232 compatible signal levels are needed, two different external voltage translators (e.g. Maxim MAX3237E and Texas Instruments SN74AVC4T774) can be used. The Texas Instruments' chips provide the translation from 1.8 V / 2.8 V to 3.3 V, while the Maxim chip provides the translation from 3.3 V to RS-232 compatible signal level.

If a 1.8 V application processor (DTE) is used, and the generic digital interfaces of the module (DCE) are configured to operate at 1.8 V (**V_INT** = 1.8 V, if **VSEL** pin is connected to GND; see 1.5.3), the circuit should be implemented as described in Figure 42.

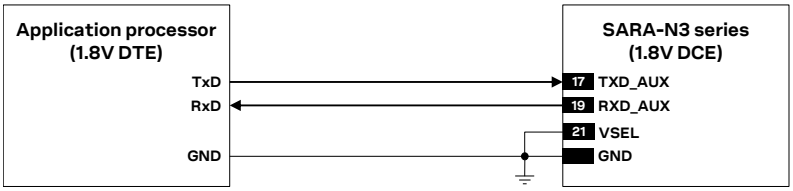

Figure 42: SARA-N3 series' UART AUX application circuit with TXD_AUX / RXD_AUX lines connection (1.8 V DTE / 1.8 V DCE)

If a 2.8 V application processor (DTE) is used, and the generic digital interfaces of the module (DCE) are configured to operate at 2.8 V (**V_INT** = 2.8 V, if **VSEL** pin is left unconnected: see 1.5.3), the circuit should be implemented as described in Figure 43.

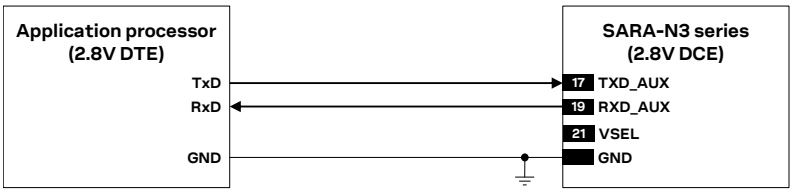

Figure 43: SARA-N3 series' UART AUX application circuit with TXD_AUX / RXD_AUX lines connection (2.8 V DTE / 2.8 V DCE)

If a 3.0 V application processor is used and the generic digital interfaces of the module are configure to operate at 1.8 V (**V_INT** = 1.8 V, if **VSEL** pin is connected to GND: see 1.5.3), then the 1.8 V UART of the module (DCE) can be connected to the 3.0 V UART of the application processor (DTE) by means of an appropriate unidirectional voltage translators providing partial power down feature (thus the DTE 3.0 V supply can be also ramped up before the module **V_INT** 1.8 V supply), using the **V_INT** supply output of the module as the 1.8 V supply for the voltage translators on the module side, and the 3.0 V supply rail application processor on the application processor side.

The ESD sensitivity rating of auxiliary UART pins is 1 kV (HBM according to JESD22-A114). Higher protection level could be required if the lines are externally accessible on the application board. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible points.

2.6.2.2 Guidelines for secondary auxiliary UART layout design

The UART serial interface requires the same consideration regarding electro-magnetic interference as any other digital interface. Keep the traces short and avoid coupling with RF line or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.

2.6.3 Additional UART interface

2.6.3.1 Guidelines for additional UART circuit design

The SARA-N2 modules include **GPIO1** pin, operating at **V_INT** voltage level (1.8 V) as additional UART interface for diagnostic purpose, to collect trace logs.

A suitable application circuit can be the one illustrated in Figure 44, where direct external access is provided for diagnostic purpose by means of Test-Points made available on the application board for **GPIO1** and **V_INT** lines.

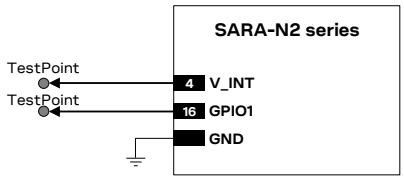

Figure 44: SARA-N2 modules' additional UART application circuit providing access for diagnostic purpose

☞ It is recommended to provide a direct access to the **GPIO1** pin of SARA-N2 module by means of accessible Test-Point for diagnostic purpose.

The SARA-N3 modules include the **RXD_FT** and **TXD_FT** pins, operating at the **V_INT** voltage level (1.8 V or 2.8 V, according to **VSEL** input pin external configuration: see 1.5.3) as additional UART interface for Firmware update and diagnostic Trace logs collection.

A suitable application circuit can be similar to the one illustrated in Figure 45, where direct external access is provided for Firmware update and diagnostic purpose by means of test-points made available on the application board for **RXD_FT**, **TXD_FT** and **V_INT** lines.

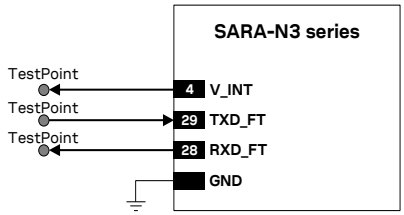

Figure 45: SARA-N3 modules' additional UART application circuit providing access for FW update and diagnostic purpose

☞ It is recommended to provide a direct access to the **RXD_FT** and **TXD_FT** pins of SARA-N3 module by means of accessible Test-Points for diagnostic purpose.

2.6.3.2 Guidelines for additional UART layout design

There are no specific layout design recommendations for additional UART.

2.6.4 DDC (I2C) interface

☞ The DDC (I2C) interface is not supported in the "02" product version of the SARA-N2 modules: the **SDA** and **SCL** lines can be left unconnected.

☞ The DDC (I2C) interface is not supported in the "00" product version of the SARA-N3 modules: the **SDA** and **SCL** lines can be left unconnected.

2.7 ADC

ADC interface is not available on the SARA-N2 modules.

2.7.1.1 Guidelines for ADC circuit design

The SARA-N3 modules include two Analog-to-Digital Converter input pins, **ANT_DET** and **ADC1**, configurable via a dedicated AT command (for further details, see the SARA-N2 / SARA-N3 series AT commands manual [4]). For example, the **ADC1** input pin can be connected to an external voltage divider for voltage measurement purpose as illustrated in Figure 46.

Figure 46: ADC application circuit example

The ESD sensitivity rating of the **ADC1** pin is 1 kV (HBM according to JESD22-A114). Higher protection level could be required if the line is externally accessible on the application board. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to an accessible point.

2.7.1.2 Guidelines for ADC layout design

The ADC circuit requires careful layout to perform proper measurements - ensure that no transient noise is coupled on this line; otherwise the measurements might be affected. It is recommended to keep the connection line to **ADC1** as short as possible.

2.8 General Purpose Input/Output (GPIO)

2.8.1.1 Guidelines for GPIO circuit design

A typical usage of SARA-N2/N3 series modules' GPIOs can be the following:

- **GPIO1** pin of SARA-N2 modules providing diagnostic trace log output: it is recommended to connect the **GPIO1** pin to a test-point accessible for diagnostic purposes (see section 2.6.3)
- **GPIO5** pin of SARA-N3 modules providing SIM card detection functionality (see section 2.5)
- **CTS** pin set as Network Indicator (see below) or Ring Indicator (see section 2.6.1)

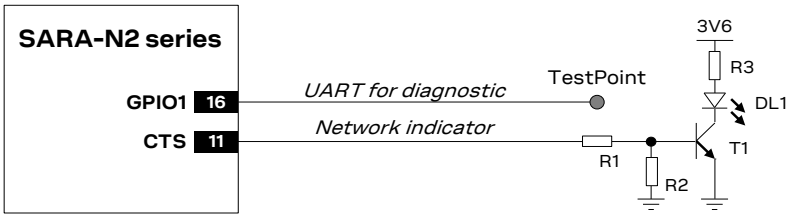

Figure 47: Application circuit for network indication provided over CTS

Reference	Description	Part Number - Manufacturer
R1	10 kΩ resistor 0402 5% 0.1 W	Various manufacturers
R2	47 kΩ resistor 0402 5% 0.1 W	Various manufacturers
R3	820 Ω resistor 0402 5% 0.1 W	Various manufacturers
DL1	LED red SMT 0603	LTST-C190KRKT - Lite-on Technology Corporation
T1	NPN BJT Transistor	BC847 - Infineon

Table 24: Components for network indication application circuit

Use transistors with at least an integrated resistor in the base pin or otherwise put a 10 kΩ resistor on the board in series to the GPIO of SARA-N2/N3 series modules.

Do not apply voltage to any GPIO of the module before the switch-on of the GPIO's supply (**V_INT**), to avoid latch-up of circuits and allow a proper boot of the module.

ESD sensitivity rating of the GPIO pins is 1 kV (HBM according to JESD22-A114). Higher protection level could be required if the lines are externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible points.

If GPIO pins are not used, they can be left unconnected on the application board, but it is recommended to provide direct access to the **GPIO1** pin by means of accessible test-points for diagnostic purposes.

2.8.1.2 Guidelines for GPIO layout design

There are no specific layout design recommendations for GPIOs lines.

2.9 Reserved pins (RSVD)

SARA-N2/N3 series modules have pins reserved for future use, marked as **RSVD**.

All the **RSVD** pins are to be left unconnected on the application board, except for the **RSVD** pin number **33** of SARA-N2 modules that can be externally connected to ground.

2.10 Module placement

Optimize placement for minimum length of RF line and closer path from DC source for **VCC**.

Make sure that the module, RF and analog parts / circuits are clearly separated from any possible source of radiated energy, including digital circuits that can radiate some digital frequency harmonics, which can produce Electro-Magnetic Interference affecting module, RF and analog parts / circuits' performance or implement proper countermeasures to avoid any possible Electro-Magnetic Compatibility issue.

Make sure that the module, RF and analog parts / circuits, high speed digital circuits are clearly separated from any sensitive part / circuit which may be affected by Electro-Magnetic Interference or employ countermeasures to avoid any possible Electro-Magnetic Compatibility issue.

Provide enough clearance between the module and any external part: clearance of at least 0.4 mm per side is recommended to permit suitable mounting of the parts.

2.11 Module footprint and paste mask

Figure 48 and Table 25 describe the suggested footprint (i.e. copper mask) and paste mask layout for SARA modules: the proposed land pattern layout reflects the modules' pins layout, while the proposed stencil apertures layout is slightly different (see the F'', H'', I'', J'', O'' parameters compared to the F', H', I', J', O' ones).

The Non Solder resist Mask Defined (NSMD) pad type is recommended over the Solder resist Mask Defined (SMD) pad type, implementing the solder resist mask opening 50 µm larger per side than the corresponding copper pad.

The recommended solder paste thickness is 150 µm, according to application production process requirements.

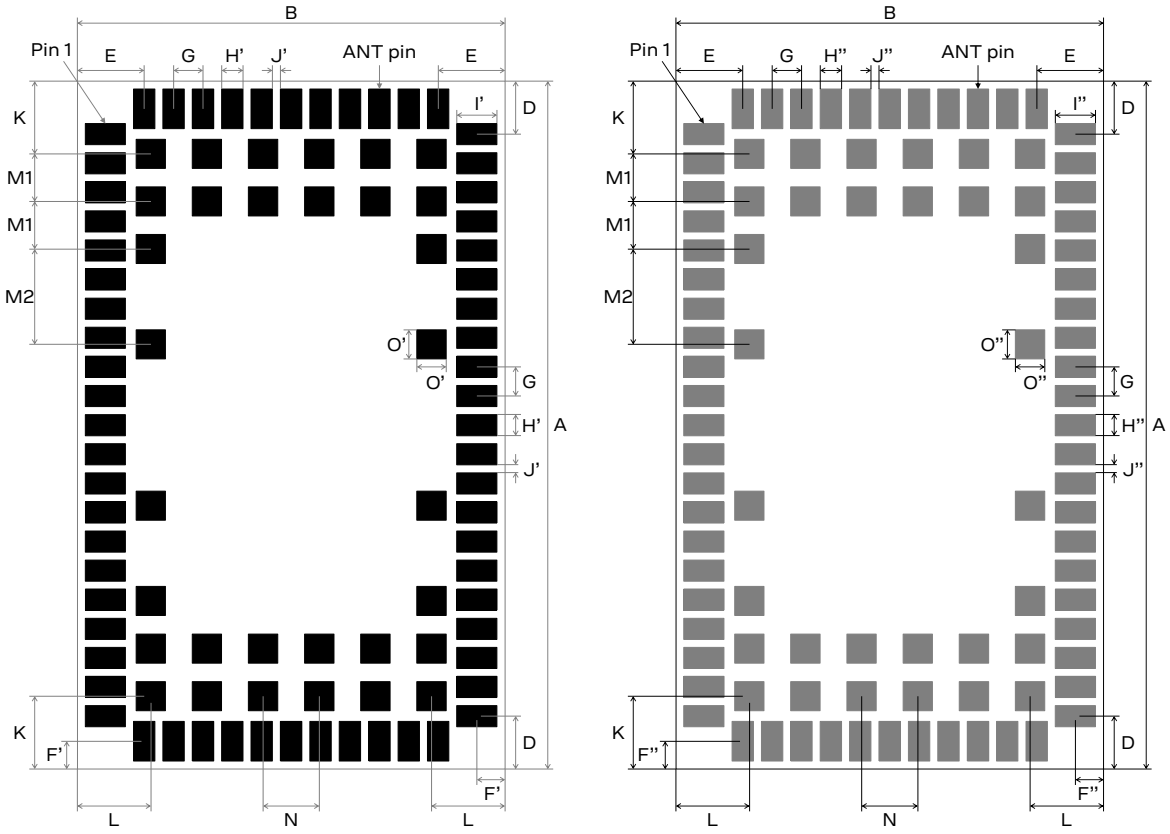

Figure 48: SARA-N2/N3 series modules suggested footprint and paste mask (application board top view)

Parameter	Value	Parameter	Value	Parameter	Value
A	26.0 mm	G	1.10 mm	K	2.75 mm
B	16.0 mm	H'	0.80 mm	L	2.75 mm
C	3.00 mm	H''	0.75 mm	M1	1.80 mm
D	2.00 mm	I'	1.50 mm	M2	3.60 mm
E	2.50 mm	I''	1.55 mm	N	2.10 mm
F'	1.05 mm	J'	0.30 mm	O'	1.10 mm
F''	1.00 mm	J''	0.35 mm	O''	1.05 mm

Table 25: SARA-N2/N3 series modules suggested footprint and paste mask dimensions

These are recommendations only and not specifications. The exact copper, solder and paste mask geometries, distances, stencil thicknesses and solder paste volumes must be adapted to the specific production processes (e.g. soldering etc.) of the customer.

2.12 SARA-N211 and SARA-N310 modules integration in devices intended for use in potentially explosive atmospheres

2.12.1 General guidelines

SARA-N211 and SARA-N310 modules are certified as components intended for use in potentially explosive atmospheres (see section 4.3 and see the "Approvals" section of the SARA-N2 series data sheet [1] for further details), with the following marking:

- Ⓔx II 1G Ex ia IIC for SARA-N211 modules
- Ⓔx II 1G Ex ia IIC Ga for SARA-N310 modules

According to the marking stated above, the modules are certified as electrical equipment of:

- group "II": intended for use in areas with explosive gas atmosphere other than mines susceptible to firedamp.
- category "1G": intended for use in zone 0 hazardous areas, in which an explosive atmospheres is caused by mixtures of air and gases, or when vapours or mists are continuously or frequently present for long periods. The modules are also suitable for applications intended for use in zone 1 and zone 2 hazardous areas.
- level of protection "ia": intrinsically safe apparatus with very high level of protection, not capable of causing ignition in normal operation and with the application of one countable fault or a combination of any two countable fault plus those non-countable faults which give the most onerous condition.
- subdivision "IIC": intended for use in areas where the nature of the explosive gas atmosphere is considered very dangerous based on the Maximum Experimental Safe Gap or the Minimum Ignition Current ratio of the explosive gas atmosphere in which the equipment may be installed (typical gases are hydrogen, acetylene, carbon disulphide), so that the modules are also suitable for applications intended for use in subdivision IIB (typical gases are ethylene, coke oven gas and other industrial gases) and subdivision IIA (typical gases are industrial methane, propane, petrol and the majority of industrial gases).
- equipment protection level "Ga": equipment for explosive gas atmospheres, having a very high level of protection, which is not a source of ignition in normal operation, during expected malfunctions or during rare malfunctions

The temperature range of the modules is defined in the "Operating temperature range" section of the SARA-N2 series data sheet [1] and the SARA-N3 series data sheet [2].

The modules are suitable for temperature class T4 applications, as long as the maximum input power

- does not exceed 2.0 W on SARA-N211 modules
- does not exceed 1.85 W on SARA-N310 modules

Even if the modules are certified as components intended for use in potentially explosive atmospheres as described above, the application device that integrates the module must be approved under all the certification schemes required by the specific application device that will be deployed in the market as apparatus intended for use in potentially explosive atmospheres.

The certification scheme approvals required for the application device integrating the module, intended for use in potentially explosive atmospheres, may differ depending on the following topics:

- the country or the region where the application device must be deployed
- the classification of the application device relative to the use in potentially explosive atmospheres
- the classification of the hazardous areas in which the application device is intended for use

☞ Any specific applicable requirement for the implementation of the apparatus integrating the module, intended for use in potentially explosive atmospheres, must be fulfilled according to the exact applicable standards: check the detailed requisites on the pertinent norms for the application, as for example the IEC 60079-0 [18], IEC 60079-11 [19], IEC 60079-26 [20] standards.

☞ The certification of the application device that integrates a the module and the compliance of the application device with all the applicable certification schemes, directives and standards required for use in potentially explosive atmospheres are the sole responsibility of the application device manufacturer.

The application device integrating a SARA-N211 and/or SARA-N310 module for use in potentially explosive atmospheres must be designed so that any circuit/part of the apparatus shall not invalidate the specific characteristics of the type of protection of the module.

The intrinsic safety "i" type of protection of SARA-N211 and SARA-N310 modules is based on the restriction of the electrical energy within equipment and of the interconnecting wiring exposed to the explosive atmosphere to a level below that which can cause ignition by either sparking or heating effects.

The following input and equivalent parameters must be considered integrating a SARA-N211 and/or SARA-N310 module in an application device intended for use in potentially explosive atmospheres:

- Total internal capacitance, Ci (see Table 26)
- Total internal inductance, Li (see Table 26)
- The module does not contain blocks which increase the voltage (e.g. like step-up, duplicators, boosters, etc.)

The nameplate of the modules is described in the "Product labeling" section of the SARA-N2 series data sheet [1] and the SARA-N3 series data sheet [2]. For additional info and modules' certificate of compliancy for use in potentially explosive atmospheres, see our website (www.u-blox.com) or contact the u-blox office or sales representative nearest you.

☞ The final enclosure of the application device integrating SARA-N211 and/or SARA-N310 modules, intended for use in potentially explosive atmospheres, must guarantee a minimum degree of ingress protection of IP20.

2.12.2 Guidelines for VCC supply circuit design

The power supply ratings, average and pulse, must be considered in the design of the **VCC** supply circuit on the application device integrating SARA-N211 and/or SARA-N310 module, implementing proper circuits providing adequate maximum voltage and current to the **VCC** supply input of the modules, according to the specific potentially explosive gas atmosphere category subdivision where the apparatus is intended for use.

Table 26 lists the maximum input and equivalent intrinsically safe parameters for the SARA-N211 and the SARA-N310 modules, which must be considered in the sub-division IIC, IIB and IIA.

Parameter	SARA-N211	SARA-N310
Ui	4.2 V	4.2 V
Ii	0.5 A	0.5 A
Ci	68.1 µF	42.2 µF
Li	8.5 µH	11.4 µH

Table 26: Maximum input and equivalent parameters for sub-division IIC

Primary and secondary cells and batteries

Cells and batteries incorporated into equipment with intrinsic safety "i" protection to potentially explosive gas atmosphere shall conform to the requirements of the IEC 60079-0 [18], IEC 60079-11 [19] ATEX standards.

Shunt voltage limiters

For Level of Protection "ia", the application of controllable semiconductor components as shunt voltage limiting devices, for example transistors, thyristors, voltage/current regulators, etc., may be permitted if both the input and output circuits are intrinsically safe circuits or where it can be shown that they cannot be subjected to transients from the power supply network. In circuits complying with the above, two devices are considered to be an infallible assembly.

For Level of Protection "ia", three independent active voltage limitation semiconductor circuits may be used in associated apparatus provided the transient conditions of the clause 7.5.1 of IEC 60079-11 standard are met. These circuits shall also be tested in accordance with the clause 10.1.5.3 of the IEC 60079-11 standard [19].

Series current limiters

The use of three series blocking diodes in circuits of Level of Protection "ia" is permitted, however, other semiconductors and controllable semiconductor devices shall be used as series current-limiting devices only in Level of Protection "ib" or "ic" apparatus. However, for power limitation purposes, Level of Protection "ia" apparatus may use series current limiters consisting of controllable and non-controllable semiconductor devices.

The use of semiconductors and controllable semiconductor devices as current-limiting devices for spark ignition limitation is not permitted for Level of Protection "ia" apparatus because of their possible use in areas in which a continuous or frequent presence of an explosive atmosphere may coincide with the possibility of a brief transient which could cause ignition. The maximum current that may be delivered may have a brief transient but will not be taken as Io, because the compliance with the spark ignition test of the clause 10.1 of IEC 60079-11 standard [19] would have established the successful limitation of the energy in this transient.

Protection against polarity reversal

Protection against polarity reversal shall be provided within intrinsically safe apparatus to prevent invalidation of the type of protection as a result of reversal of the polarity of supplies to that intrinsically safe apparatus or at connections between cells of a battery where this could occur. For this purpose, single diode shall be acceptable.

Other considerations

All the recommendations reported in section 2.12.1 must be considered for the implementation of the **VCC** supply circuit on application integrating SARA-N211 and/or SARA-N310 modules intended for use in potentially explosive atmospheres. Any specific applicable requirement for the **VCC** supply circuit design must be fulfilled according to all the exact applicable standards for the apparatus.

☞ Check the detailed requisites on the pertinent norms for the application apparatus, as for example the IEC 60079-0 [18], IEC 60079-11 [19], IEC 60079-26 [20] standards.

2.12.3 Guidelines for antenna RF interface design

The RF radiating power profile of the SARA-N211 and SARA-N310 modules is compliant to all the applicable 3GPP / ETSI standards, with a maximum of 250 mW RF average power according to the LTE Cat NB1 / NB2 Power Class stated in Table 2.

The RF threshold power of the application device integrating a SARA-N211 or SARA-N310 module is defined, according to the IEC 60079-0 ATEX standard [18], as the product of the effective output power of the module multiplied by the antenna gain (implemented/used on the application device).

The RF threshold power of the application device integrating a SARA-N211 or SARA-N310 module must not exceed the limits shown in Table 27, according to the IEC 60079-0 ATEX standard [18].

Gas group II subdivision	RF threshold power limits according to the IEC 60079-0 ATEX standard
IIA (a typical gas is propane)	6.0 W
IIB (a typical gas is ethylene)	3.5 W
IIC (a typical gas is hydrogen)	2.0 W

Table 27: RF threshold power limits for the different gas group II subdivisions according to the IEC 60079-0 ATEX standard [18]

☞ The system antenna(s) implemented/used on the application device integrating a SARA-N211 and/or SARA-N310 module must be designed/selected so that the antenna gain (i.e. the combined transmission line, connector, cable losses and radiating element gain) multiplied by the output power of the module does not exceed the limits shown in Table 27.

2.13 Schematic for SARA-N2/N3 series module integration

Figure 49 is an example of a schematic diagram where a SARA-N2 module “02” product version is integrated into an application board, using all the available interfaces and functions of the module.

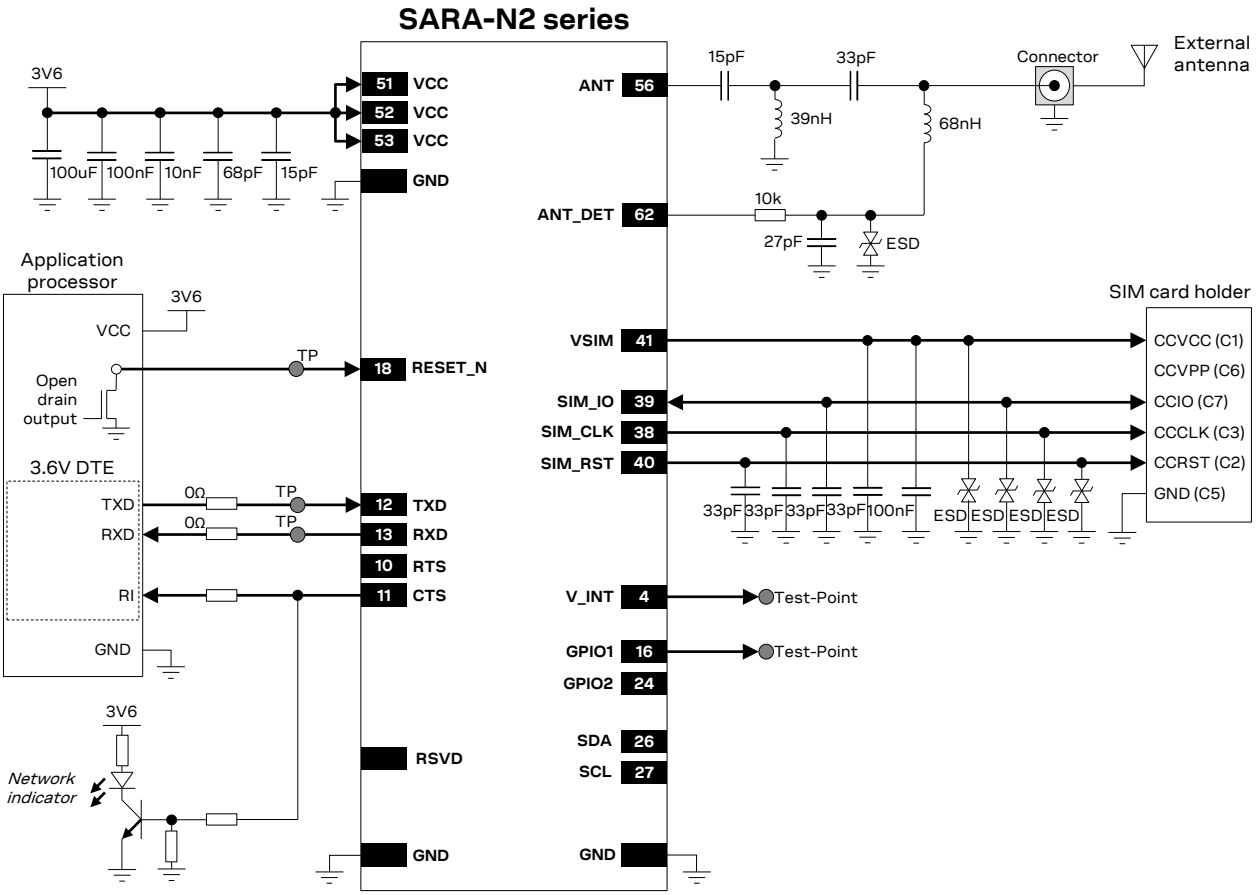

Figure 49: Example of schematic diagram to integrate a SARA-N2 module “02” product version using all available interfaces

Figure 50 shows an example of a schematic diagram where a SARA-N3 module “00” product version is integrated into an application board using most of the available interfaces and functions.

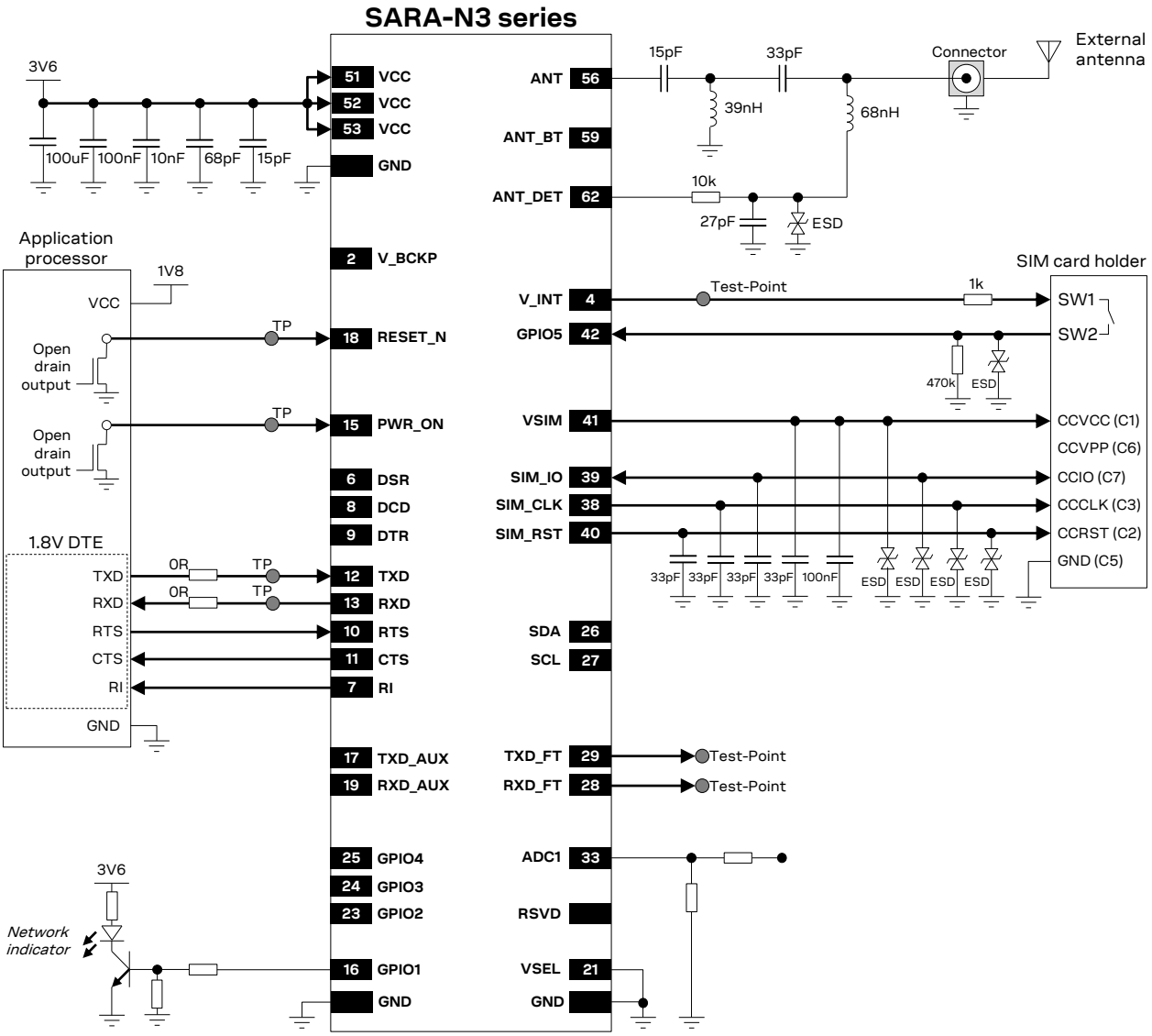

Figure 50: Sample schematic diagram to integrate a SARA-N3 module “00” product version using most of the interfaces

2.14 Design-in checklists

The following are the most important points for simple checks.

2.14.1 Schematic checklist

- ☑ The external DC supply circuit must provide a nominal voltage at **VCC** pins within the normal operating range limits.
- ☑ The external DC supply circuit must be capable of providing, at **VCC** pins, the specified average current during a transmission at maximum power with a voltage level above the minimum operating range limit.
- ☑ **VCC** supply should be clean, with very low ripple/noise.
- ☑ Do not apply loads that might exceed the maximum available current limit from **V_INT** supply.
- ☑ Check that voltage level of any connected pin does not exceed the relative operating range.
- ☑ Capacitance and series resistance must be limited on each SIM signal to match the SIM specifications.
- ☑ Insert the suggested capacitors on each SIM signal and low capacitance ESD protections if accessible.
- ☑ Check UART signals direction, since the signal names follow ITU-T V.24 recommendation [6].
- ☑ Provide accessible testpoints directly connected to the following pins: **TXD**, **RXD**, **TXD_FT**, **RXD_FT**, **GPIO1**, **V_INT**, **PWR_ON** and **RESET_N** for diagnostic and FW update purpose.
- ☑ Provide proper precautions for ESD immunity as required on the application board.
- ☑ Any external signal connected to the UART interface pin must be tri-stated or set low before applying **VCC** supply, to avoid latch-up of circuits and let a proper boot of the module.
- ☑ Any external signal connected to any generic digital interface pin must be tri-stated or set low when the module is not powered and during the module power-on sequence (at least until the activation of the **V_INT** output) to avoid latch-up of circuits and let a proper boot of the module.
- ☑ All unused pins can be left unconnected.

2.14.2 Layout checklist

- ☑ Check 50 Ω nominal characteristic impedance of the RF transmission line connected to the **ANT** pad (antenna RF input/output interface).
- ☑ Follow the recommendations of the antenna producer for correct antenna installation and deployment (PCB layout and matching circuitry).
- ☑ Ensure no coupling occurs between the RF interface and noisy or sensitive signals (like SIM signals and high-speed digital lines).
- ☑ **VCC** line should be wide and short.
- ☑ Route **VCC** supply line away from sensitive analog signals.
- ☑ Ensure proper grounding.
- ☑ Optimize placement for minimum length of RF line and closer path from DC source for **VCC**.
- ☑ Keep routing short and minimize parasitic capacitance on the SIM lines to preserve signal integrity.

2.14.3 Antenna checklist

- ☑ Antenna termination should provide 50 Ω characteristic impedance with V.S.W.R at least less than 3:1 (recommended 2:1) on operating bands in deployment geographical area.
- ☑ Follow the recommendations of the antenna producer for correct antenna installation and deployment (PCB layout and matching circuitry).
- ☑ Ensure compliance with any regulatory agency RF radiation requirement.

3 Handling and soldering

☞ No natural rubbers, no hygroscopic materials or materials containing asbestos are employed.

3.1 Packaging, shipping, storage and moisture preconditioning

For information pertaining to reels and tapes, Moisture Sensitivity levels (MSD), shipment and storage information, as well as drying for preconditioning see the SARA-N2 series data sheet [1], the SARA-N3 series data sheet [2] and the u-blox package information user guide [3].

3.2 Handling

The SARA-N2/N3 series modules are Electro-Static Discharge (ESD) sensitive devices.

⚠ Ensure ESD precautions are implemented during handling of the module.

Electrostatic discharge (ESD) is the sudden and momentary electric current that flows between two objects at different electrical potentials caused by direct contact or induced by an electrostatic field. The term is usually used in the electronics and other industries to describe momentary unwanted currents that may cause damage to electronic equipment.

The ESD sensitivity for each pin of SARA-N2/N3 series modules (as Human Body Model according to JESD22-A114F) is specified in the SARA-N2 series data sheet [1] and SARA-N3 series data sheet [2].

ESD prevention is based on establishing an Electrostatic Protective Area (EPA). The EPA can be a small working station or a large manufacturing area. The main principle of an EPA is that there are no highly charging materials near ESD sensitive electronics, all conductive materials are grounded, workers are grounded, and charge build-up on ESD sensitive electronics is prevented. International standards are used to define typical EPA and can be obtained for example from International Electrotechnical Commission (IEC) or American National Standards Institute (ANSI).

In addition to standard ESD safety practices, the following measures should be taken into account whenever handling the SARA-N2/N3 series modules:

- Unless there is a galvanic coupling between the local GND (i.e. the work table) and the PCB GND, then the first point of contact when handling the PCB must always be between the local GND and PCB GND.
- Before mounting an antenna patch, connect ground of the device.
- When handling the module, do not come into contact with any charged capacitors and be careful when contacting materials that can develop charges (e.g. patch antenna, coax cable, soldering iron,...).
- To prevent electrostatic discharge through the RF pin, do not touch any exposed antenna area. If there is any risk that such exposed antenna area is touched in non ESD protected work area, implement proper ESD protection measures in the design.
- When soldering the module and patch antennas to the RF pin, make sure to use an ESD safe soldering iron.

3.3 Soldering

3.3.1 Soldering paste

Use of "No Clean" soldering paste is strongly recommended, as it does not require cleaning after the soldering process has taken place. The paste listed in the example below meets these criteria.

Soldering Paste:	OM338 SAC405 / Nr.143714 (Cookson Electronics)
Alloy specification:	95.5% Sn / 3.9% Ag / 0.6% Cu (95.5% Tin / 3.9% Silver / 0.6% Copper)
	95.5% Sn / 4.0% Ag / 0.5% Cu (95.5% Tin / 4.0% Silver / 0.5% Copper)
Melting Temperature:	217 °C
Stencil Thickness:	150 µm for base boards

The final choice of the soldering paste depends on the approved manufacturing procedures.

The paste-mask geometry for applying soldering paste should meet the recommendations in section 2.11.

☞ The quality of the solder joints should meet the appropriate IPC specification.

3.3.2 Reflow soldering

A convection type-soldering oven is strongly recommended over the infrared type radiation oven. Convection heated ovens allow precise control of the temperature and all parts will be heated up evenly, regardless of material properties, thickness of components and surface color.

Consider the "IPC-7530 Guidelines for temperature profiling for mass soldering (reflow and wave) processes, published 2001".

Reflow profiles are to be selected according to the following recommendations.

⚠ Failure to observe these recommendations can result in severe damage to the device!

Preheat phase

Initial heating of component leads and balls. Residual humidity will be dried out. Note that this preheat phase will not replace prior baking procedures.

- Temperature rise rate: max 3 °C/s — If the temperature rise is too rapid in the preheat phase it may cause excessive slumping.
- Time: 60 to 120 s — If the preheat is insufficient, rather large solder balls tend to be generated. Conversely, if performed excessively, fine balls and large balls will be generated in clusters.
- End Temperature: 150 to 200 °C — If the temperature is too low, non-melting tends to be caused in areas containing large heat capacity.

Heating/ reflow phase

The temperature rises above the liquidus temperature of 217 °C. Avoid a sudden rise in temperature as the slump of the paste could become worse.

- Limit time above 217 °C liquidus temperature: 40 to 60 s
- Peak reflow temperature: 245 °C

Cooling phase

A controlled cooling avoids negative metallurgical effects (solder becomes more brittle) of the solder and possible mechanical tensions in the products. Controlled cooling helps to achieve bright solder fillets with a good shape and low contact angle.

- Temperature fall rate: max 4 °C/s

☞ To avoid falling off, modules should be placed on the topside of the motherboard during soldering.

The soldering temperature profile chosen at the factory depends on additional external factors like choice of soldering paste, size, thickness and properties of the base board, etc.

⚠ Exceeding the maximum soldering temperature and the maximum liquidus time limit in the recommended soldering profile may permanently damage the module.

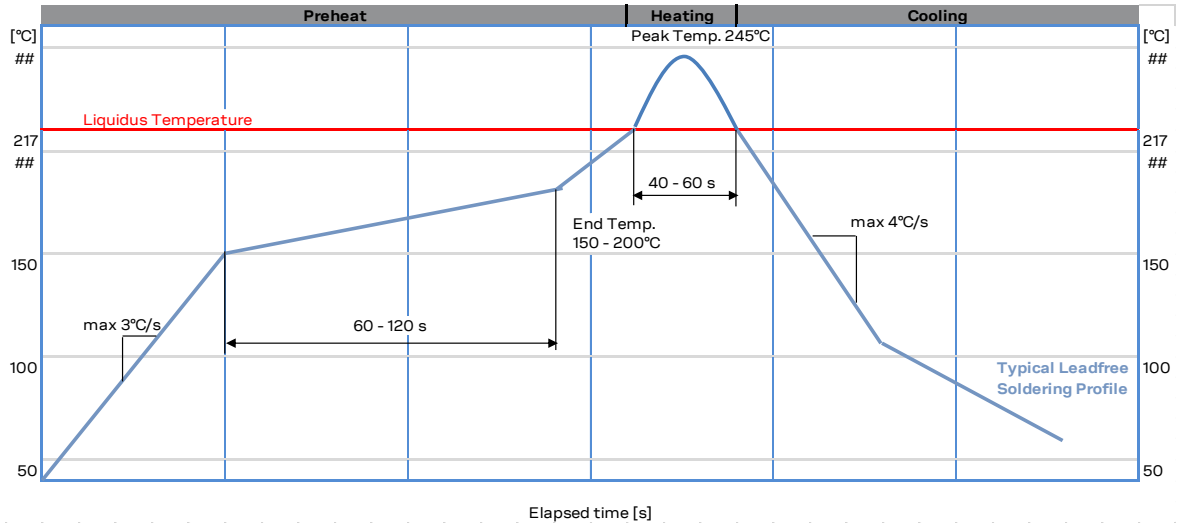

Figure 51: Recommended soldering profile

☞ SARA-N2/N3 series modules must not be soldered with a damp heat process.

3.3.3 Optical inspection

After soldering the module, inspect it optically to verify that the module is properly aligned and centered.

3.3.4 Cleaning

Cleaning the soldered modules is not recommended. Residues underneath the modules cannot be easily removed with a washing process.

- Cleaning with water will lead to capillary effects where water is absorbed in the gap between the baseboard and the module. The combination of residues of soldering flux and encapsulated water leads to short circuits or resistor-like interconnections between neighboring pads. Water will also damage the sticker and the ink-jet printed text.
- Cleaning with alcohol or other organic solvents can result in soldering flux residues flooding into the two housings, areas that are not accessible for post-wash inspections. The solvent will also damage the sticker and the ink-jet printed text.
- Ultrasonic cleaning will permanently damage the module, in particular the quartz oscillators.

For best results use a "no clean" soldering paste and eliminate the cleaning step after the soldering.

3.3.5 Repeated reflow soldering

Repeated reflow soldering processes and soldering the module upside down are not recommended.

Boards with components on both sides may require two reflow cycles. In this case, the module should always be placed on the side of the board that is submitted into the last reflow cycle. The reason for this (besides others) is the risk of the module falling off due to the significantly higher weight in relation to other components.

☞ u-blox gives no warranty against damages to the SARA-N2/N3 series modules caused by performing more than a total of two reflow soldering processes (one reflow soldering process to mount the SARA-N2/N3 series module, plus one reflow soldering process to mount other parts).

3.3.6 Wave soldering

SARA-N2/N3 series LGA modules must not be soldered with a wave soldering process.

Boards with combined through-hole technology (THT) components and surface-mount technology (SMT) devices require wave soldering to solder the THT components. No more than one wave soldering process is allowed for board with a SARA-N2/N3 series module already populated on it.

⚠ Performing a wave soldering process on the module can result in severe damage to the device!

☞ u-blox gives no warranty against damages to the SARA-N2/N3 series modules caused by performing more than a total of two soldering processes (one reflow soldering process to mount the SARA-N2/N3 series module, plus one wave soldering process to mount other THT parts on the application board).

3.3.7 Hand soldering

Hand soldering is not recommended.

3.3.8 Rework

Rework is not recommended.

☞ Never attempt a rework on the module itself, e.g. replacing individual components. Such actions immediately terminate the warranty.

3.3.9 Conformal coating

Certain applications employ a conformal coating of the PCB using HumiSeal® or other related coating products.

These materials affect the RF properties of the SARA-N2/N3 series modules and it is important to prevent them from flowing into the module.

The RF shields do not provide 100% protection for the module from coating liquids with low viscosity, therefore care is required in applying the coating.

☞ Conformal Coating of the module will void the warranty.

3.3.10 Casting

If casting is required, use viscose or another type of silicon pottant. The OEM is strongly advised to qualify such processes in combination with the SARA-N2/N3 series modules before implementing this in the production.

☞ Casting will void the warranty.

3.3.11 Grounding metal covers

Attempts to improve grounding by soldering ground cables, wick or other forms of metal strips directly onto the EMI covers is done at the customer's own risk. The numerous ground pins should be sufficient to provide optimum immunity to interferences and noise.

☞ u-blox gives no warranty for damages to the SARA-N2/N3 series modules caused by soldering metal cables or any other forms of metal strips directly onto the EMI covers.

3.3.12 Use of ultrasonic processes

SARA-N2/N3 series modules contain components which are sensitive to Ultrasonic Waves. Use of any Ultrasonic Processes (cleaning, welding etc.) may cause damage to the module.

☞ u-blox gives no warranty against damages to the SARA-N2/N3 series modules caused by any Ultrasonic Processes.

4 Approvals

4.1 Approvals overview

Product certification approval is the process of certifying that a product has passed all tests and criteria required by specifications, typically called “certification schemes”, which can be divided into three distinct categories:

- Regulatory certification
  - Country approvals required by local government in most regions and countries, such as:
    - CE (Conformité Européenne) marking for European Union
    - FCC (Federal Communications Commission) approval for United States
    - NCC (National Communications Commission) approval for Taiwan
- Conformance certification
  - Telecom industry approvals verifying the interoperability between devices and networks:
    - GCF (Global Certification Forum), partnership between device manufacturers and network operators to ensure and verify global interoperability between devices and networks
    - PTCRB (PCS Type Certification Review Board), created by United States network operators to ensure and verify interoperability between devices and North America networks
- Operator certification
  - Operator-specific approvals required by some mobile network operator, such as:
    - China Telecom network operator in China
    - AT&T network operator in United States

Table 28 lists the main approvals achieved or planned of SARA-N2/N3 series modules.

Certification scheme	SARA-N200	SARA-N201	SARA-N210	SARA-N211	SARA-N280	SARA-N300	SARA-N310
CE (Europe)	•		•	•			•
CCC (China)	•	•				•	
SRRC (China)	•	•				•	
NCC (Taiwan)	•			•	•		•
ANATEL (Brazil)					•		
RCM (Australia)					•		•
NBTC (Thailand)	•						•
IMDA (Singapore)	•						•
ATEX (Atmosphere Explosive)				•			•
GCF conformity				•			•
China Telecom		•					
China Unicom	•						
Deutsche Telekom	•		•	•			•
Vodafone							•

Table 28: SARA-N2/N3 series main certification approvals

☞ For all the certificates of compliance and for the complete list of approvals (including country, conformance and network operators’ approvals) of SARA-N2/N3 series modules, please contact the u-blox office or sales representative nearest you.

Even if SARA-N2/N3 series modules are approved under all major certification schemes, the application device that integrates SARA-N2/N3 series modules must also be approved under all the certification schemes required by the specific application device to be deployed in the market.

The required certification scheme approvals and relative testing specifications differ depending on the country or the region where the device that integrates SARA-N2/N3 series modules is intended to be deployed, on the relative vertical market of the device, on type, features and functionalities of the whole application device, and on the network operators where the device is intended to operate.

The u-blox cellular module's approval can be re-used for the approval of the integrating application device, but the possible re-use depends on the physical characteristics of the integrating application device, also considering the configuration used for the approvals of SARA-N2/N3 series modules, and it also depends on related certification scheme approvals required for the integrating application device as explained above.

☞ Check the appropriate applicability of SARA-N2/N3 series module's approvals while starting the certification process of the device integrating the module: the re-use of the u-blox module's approval can significantly reduce the cost and time to market of the end-device certification.

☞ The certification of the application device that integrates a SARA-N2/N3 series module and the compliance of the application device with all the applicable certification schemes, directives and standards are the sole responsibility of the application device manufacturer.

4.2 European Conformance CE mark

SARA-N200, SARA-N210 and SARA-N211 modules have been evaluated against the essential requirements of the Radio Equipment Directive 2014/53/EU.

In order to satisfy the essential requirements of the 2014/53/EU RED, the modules are compliant with the following standards:

- Radio Spectrum Efficiency (Article 3.2):
  - EN 301 908-1
  - EN 301 908-13
- Electromagnetic Compatibility (Article 3.1b):
  - EN 301 489-1
  - EN 301 489-52
- Health and Safety (Article 3.1a)
  - EN 62368-1
  - EN 62311

⚠ Radiofrequency radiation exposure Information: this equipment complies with radiation exposure limits prescribed for an uncontrolled environment for fixed and mobile use conditions. This equipment should be installed and operated with a minimum distance of 20 cm between the radiator and the body of the user or nearby persons. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except as authorized in the certification of the product.

⚠ The gain of the system antenna(s) used for the SARA-N200, SARA-N210 and SARA-N211 modules (i.e. the combined transmission line, connector, cable losses and radiating element gain) must not exceed the values stated in the Declaration of Conformity of the modules, for mobile and fixed or mobile operating configurations:

- 9.2 dBi in 800 MHz, i.e. LTE FDD-20 band
- 9.4 dBi in 900 MHz, i.e. LTE FDD-8 band

The conformity assessment procedure for SARA-N200 and SARA-N210 modules, referred to in Article 17 and detailed in Annex II of Directive 2014/53/EU, has been followed.

Thus, the following marking is included in the product:

CE

The conformity assessment procedure for SARA-N211 modules, referred to in Article 17 and detailed in Annex II of Directive 2014/53/EU, has been followed. According to the ATEX Directive 2014/34/EU, Article 13, Paragraph 1-3, the CE mark is not affixed to the product label.

The following marking is included in the product:

Ex 1304

4.3 ATEX conformance

SARA-N211 and SARA-N310 modules are certified as components intended for use in potentially explosive atmospheres compliant to the following standards:

- IEC 60079-0
- IEC 60079-11
- IEC 60079-26

The certification numbers[7] of the modules, according to ATEX directive 2014/34/EU, are:

- SIQ 18 ATEX 104 U for SARA-N211 modules
- SIQ 19 ATEX xxx U for SARA-N310 modules

The certification numbers[7] of the modules, according to IECEx conformity assessment system, are:

- IECEx SIQ 18.0004U for SARA-N211 modules
- IECEx SIQ 19.xxxxU for SARA-N310 modules

According to the standards listed above, the modules are certified with the following marking:

- Ex II 1G Ex ia IIC for SARA-N211 modules
- Ex II 1G Ex ia IIC Ga for SARA-N310 modules

The temperature range of the modules is defined in the “Operating temperature range” section of the SARA-N2 series data sheet [1] and the SARA-N3 series data sheet [2].

The modules are suitable for temperature class T4 applications, as long as the maximum input power

- does not exceed 2.0 W on SARA-N211 modules
- does not exceed 1.85 W on SARA-N310 modules

The RF radiating profile of the modules is compliant to all the applicable 3GPP / ETSI standards, with 250 mW maximum RF average power according to LTE Cat NB1/NB2 Power Class stated in Table 2.

The nameplate of the modules is described in the “Product labeling” section of the SARA-N2 series data sheet [1] and the SARA-N3 series data sheet [2].

[7] The exact ATEX and IECEx certification numbers of SARA-N310 modules are to be defined

Table 29 lists the maximum input and equivalent intrinsically safe parameters for the SARA-N211 and the SARA-N310 modules, which must be considered in the sub-division IIC, IIB and IIA.

Parameter	SARA-N211	SARA-N310
Ui	4.2 V	4.2 V
Ii	0.5 A	0.5 A
Ci	68.1 µF	42.2 µF
Li	8.5 µH	11.4 µH

Table 29: Maximum input and equivalent intrinsically safe parameters for sub-division IIC, IIB and IIA

4.4 Chinese conformance

SARA-N200 and SARA-N201 modules have the applicable regulatory approval for China:

- CMIIT ID: 2018CJ1113

4.5 Taiwanese conformance

SARA-N200, SARA-N211 and SARA-N280 modules have the applicable regulatory approval for Taiwan (National Communication Commission)

- SARA-N200 modules NCC ID: CCAI17Z10210T5

  CCAI17Z10210T5

- SARA-N211 modules NCC ID: CCAI17Z10270T0

  CCAI17Z10270T0

- SARA-N280 modules NCC ID: CCAI17Z10200T2

  CCAI17Z10200T2

5 Product testing

5.1 u-blox in-series production test

u-blox focuses on high quality for its products. All units produced are fully tested. Defective units are analyzed in detail to improve the production quality.

This is achieved with automatic test equipment, which delivers a detailed test report for each unit. The following measurements are done:

- Digital self-test (firmware download, flash firmware verification, IMEI programming)
- Measurement of voltages and currents
- Functional tests (serial interface communication, real time clock)
- Digital tests (GPIOs, digital interfaces)
- Measurement and calibration of RF characteristics in supported bands (receiver verification, frequency tuning of reference clock, calibration of transmitter and receiver power levels)
- Verification of RF characteristics after calibration (modulation accuracy, power levels and spectrum performance are checked to be within limits with calibration parameters applied)

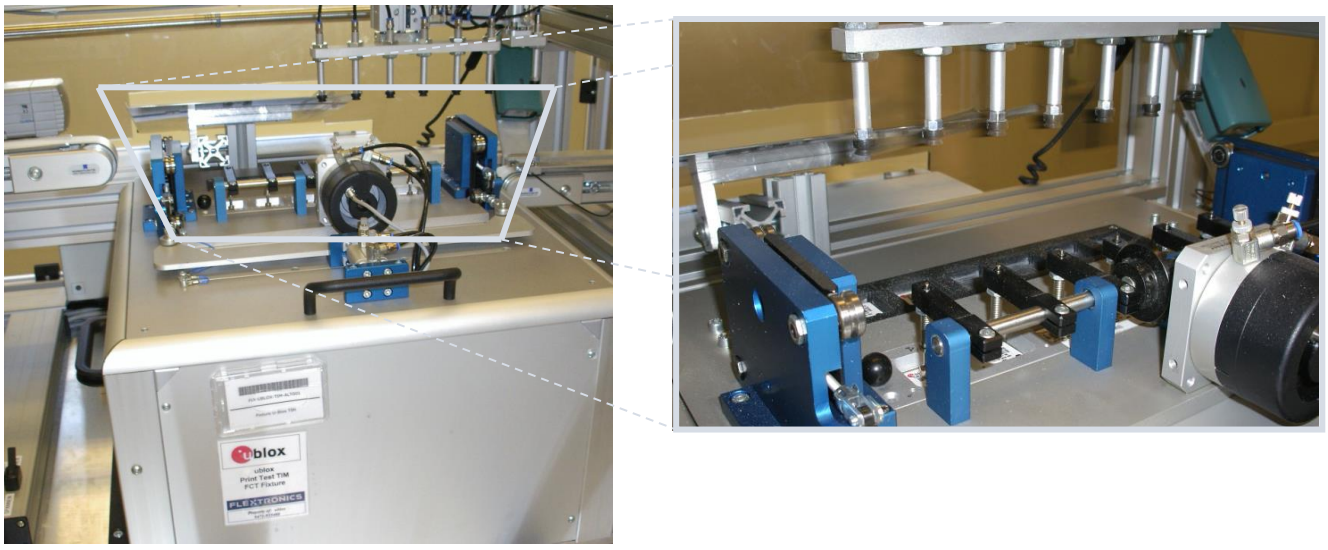

Figure 52: Automatic test equipment for module tests

5.2 Test parameters for OEM manufacturer

Because of the testing done by u-blox (with 100% coverage), an OEM manufacturer does not need to repeat firmware tests or measurements of the module RF performance or tests over analog and digital interfaces in their production test.

An OEM manufacturer should focus on:

- Module assembly on the device; it should be verified that:
  - Soldering and handling process did not damaged the module components
  - All module pins are well soldered on device board
  - There are no short circuits between pins
- Component assembly on the device; it should be verified that:
  - Communication with host controller can be established
  - The interfaces between module and device are working
  - Overall RF performance test of the device including antenna

Dedicated tests can be implemented to check the device. For example, AT commands can be used to perform functional tests on the digital interfaces (communication with the host controller, check the SIM interface, GPIOs, etc.) or to perform RF functional tests (see following section 5.2.2 for details).

5.2.1 "Go/No go" tests for integrated devices

A "Go/No go" test is typically used to compare the signal quality with a "Golden Device" in a location with excellent network coverage and known signal quality. This test should be performed after the data connection has been established. AT+CSQ is the typical AT command used to check signal quality in term of Received Signal Strength Indication (RSSI). See the SARA-N2/N3 series AT commands manual [4] for the AT+CSQ command syntax description and usage.

☞ These kinds of test may be useful as a "go/no go" test but not for RF performance measurements.

This test is suitable to check the functionality of communications with the host controller, the SIM card and the power supply. It is also a means to verify if components at the antenna interface are well-soldered.

5.2.2 RF functional tests

☞ RF functional testing by means of the AT+UTEST command is not supported by the "00" product version of SARA-N3 modules.

The overall RF functional test of the device including the antenna can be performed with basic instruments such as a spectrum analyzer (or an RF power meter) and a signal generator with the assistance of the AT+UTEST command over the AT command user interface.

The AT+UTEST command provides a simple interface to set the SARA-N2 module to Rx or Tx test modes ignoring the cellular signaling protocol. The command can set the module into:

- transmitting mode in a specified channel and power level in all supported bands
- receiving mode in a specified channel to return the measured power level in supported bands

This feature allows the measurement of the transmitter and receiver power levels to check the component assembly related to the module antenna interface and to check other device interfaces on which the RF performance depends.

☞ See the SARA-N2 / SARA-N3 series AT commands manual [4] for the description and usage of AT+UTEST command.

⚠ To avoid module damage during a transmitter test, a suitable antenna according to module specifications or a 50 Ω termination must be connected to the **ANT** port.

⚠ To avoid module damage during a receiver test, the maximum power level received at the **ANT** port must meet module specifications.

☞ The AT+UTEST command sets the module to emit RF power ignoring cellular signaling protocol. This emission can generate interference that can be prohibited by law in some countries. The use of this feature is intended for testing purposes in controlled environments by qualified users and must not be used during the normal module operation. Follow the instructions suggested in the u-blox documentation. u-blox assumes no responsibilities for the inappropriate use of this feature.

Figure 53 illustrates a typical test setup for such an RF functional test.

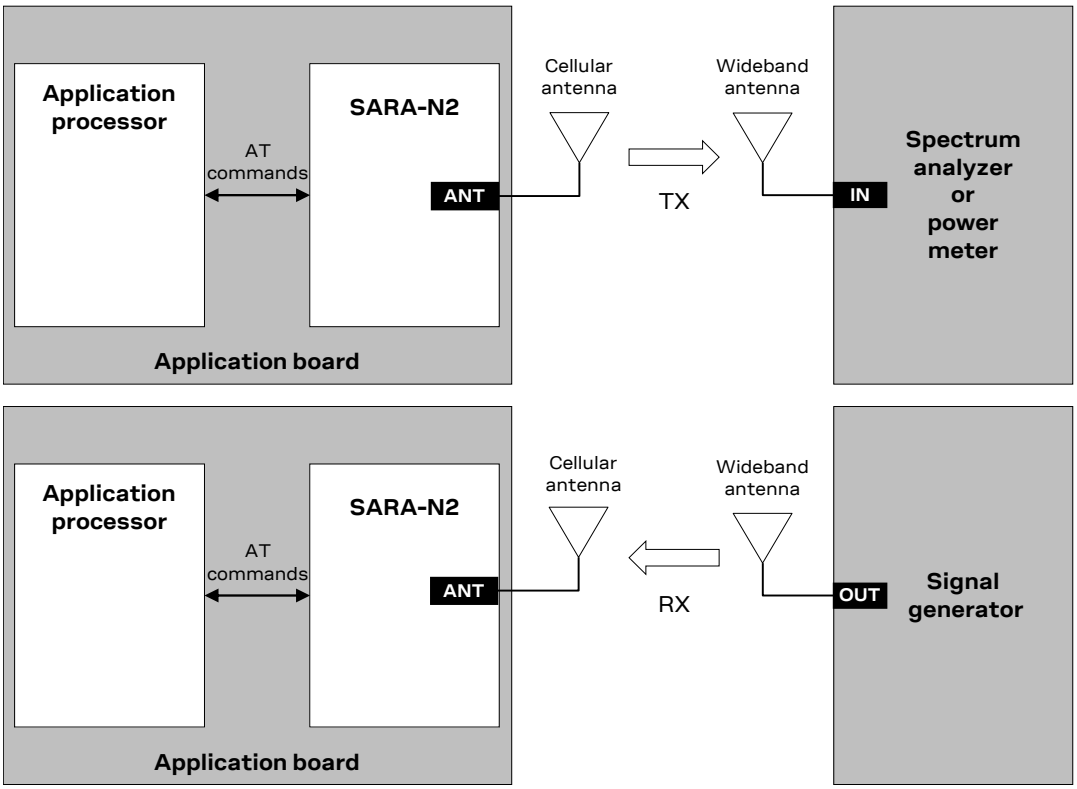

Figure 53: Setup with spectrum analyzer or power meter and signal generator for radiated measurements

Appendix

A Migration between SARA modules

A.1 Overview

The u-blox SARA form factor (26.0 x 16.0 mm, 96-pin LGA) include the following series of modules, with compatible pin assignment as described in Figure 54, so that the modules can be alternatively mounted on a single application PCB using exactly the same copper, solder resist and paste mask:

- SARA-N2 series modules supporting LTE Cat NB1 radio access technology
- SARA-N3 series modules supporting LTE Cat NB2 radio access technology
- SARA-N4 series modules supporting LTE Cat NB1 radio access technology
- SARA-R4 series modules supporting LTE Cat M1, LTE Cat NB1 and 2G radio access technology
- SARA-G3 series modules supporting 2G radio access technology
- SARA-G4 series modules supporting 2G radio access technology
- SARA-U2 series modules supporting 3G and 2G radio access technology

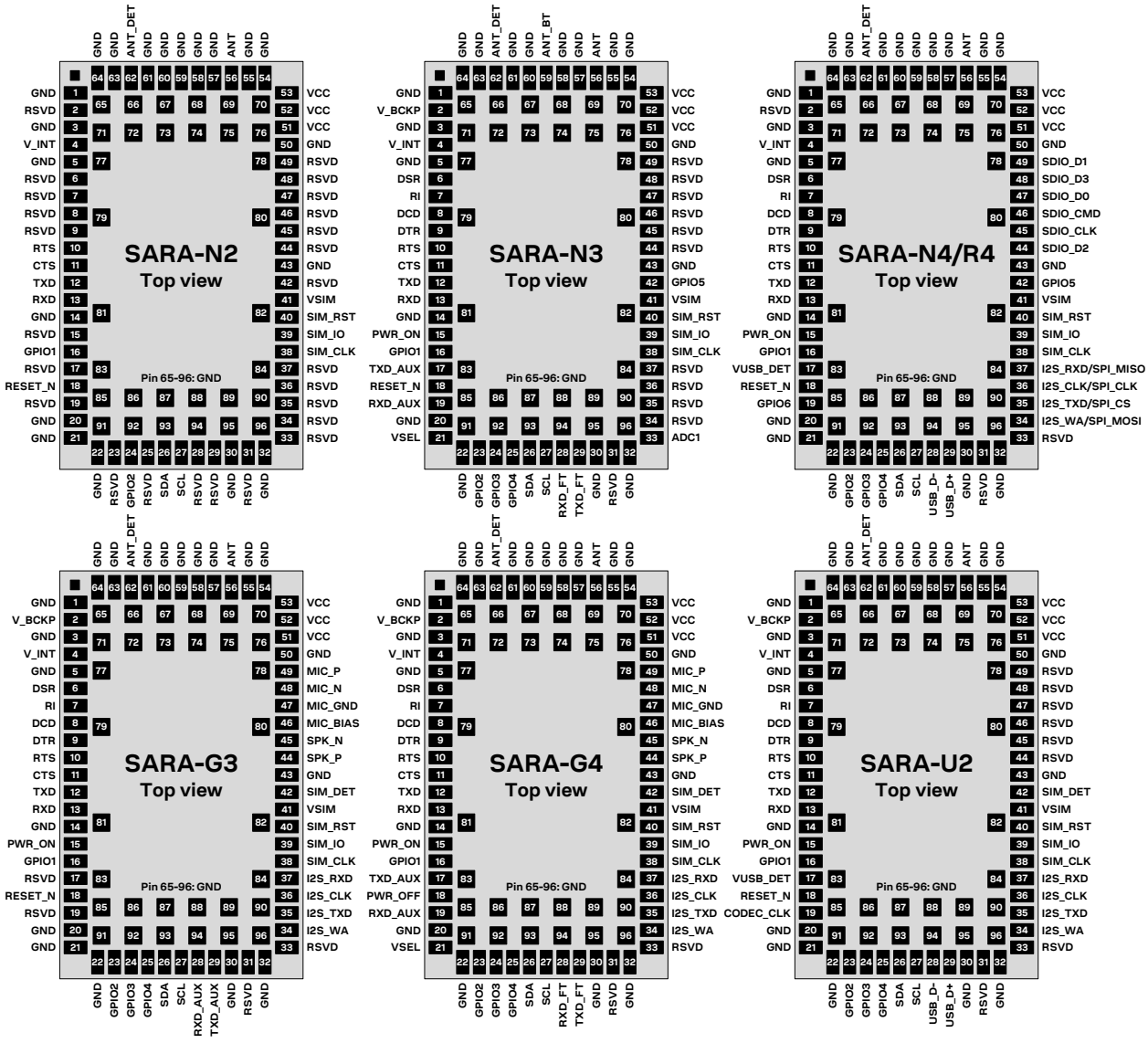

Figure 54: SARA-N2, SARA-N3, SARA-N4, SARA-R4, SARA-G3, SARA-G4 and SARA-U2 modules' layout and pin assignment

The SARA modules are also form-factor compatible with the u-blox LISA, LARA and TOBY cellular module families: although each has a different form factor, the footprints for the TOBY, LISA, SARA and LARA modules have been developed to ensure layout compatibility.

With the u-blox "nested design" solution, any TOBY, LISA, SARA or LARA module can be alternatively mounted on the same space of a single "nested" application board as described in Figure 55. Guidelines in order to implement a nested application board, description of the u-blox reference nested design and comparison between TOBY, LISA, SARA and LARA modules are provided in the nested design application note [8].

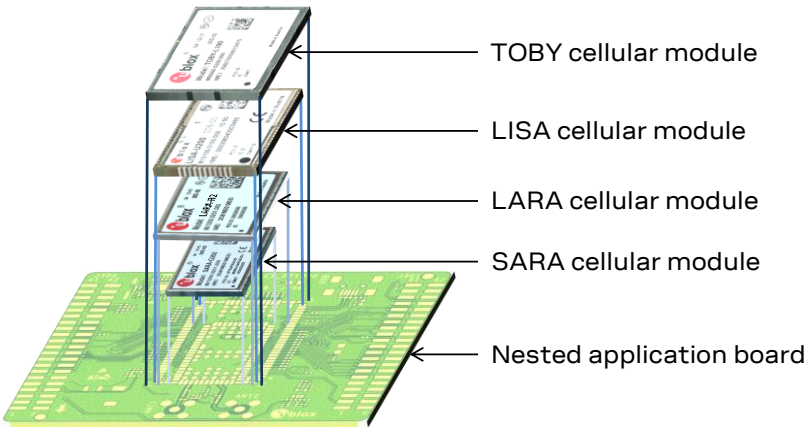

Figure 55: TOBY, LISA, SARA, LARA modules' layout compatibility: all modules can be mounted on the same nested footprint

Table 30 summarizes the interfaces provided by SARA modules:

Modules	RAT	Power			System			SIM		Serial						Audio			Other			
		RTC supply I/O	V_INT supply at 1.8V	V_INT supply configurable	Switch-on input pin	Switch-off input pin	Reset input pin	SIM interface	SIM detection	UART	UART AUX	SPI	USB	SDIO	DDC (I2C)	Analog audio	Digital audio	13/26 MHz output	GPIOs	Network indication	Antenna detection	GNSS via modem
SARA-N2	LTE NB1		●				●	●		●									●	●		
SARA-N3	LTE NB2	●	●	●	●	●	●	●	●	●	○				○				●	●	●	
SARA-N4	LTE NB1		●		●	●		●	●	●		○	●	○	●				●	●	●	●
SARA-R4	LTE M1 / NB1, 2G		●		●	●		●	●	●		○	●	○	●		○	○	●	●	●	●
SARA-G3	2G	●	●		●		●	●	●	●	●				●	●	●		●	●	●	●
SARA-G4	2G	●	●	●	●	●		●	●	●	○				○	○	○		●	●	●	○
SARA-U2	3G, 2G	●	●		●	●	●	●	●	●	●		●		●		●	●	●	●	●	●

● = supported by available product version ○ = supported by future product versions

Table 30: Summary of interfaces in SARA modules

Figure 56 summarizes the frequency ranges of the modules' operating bands.

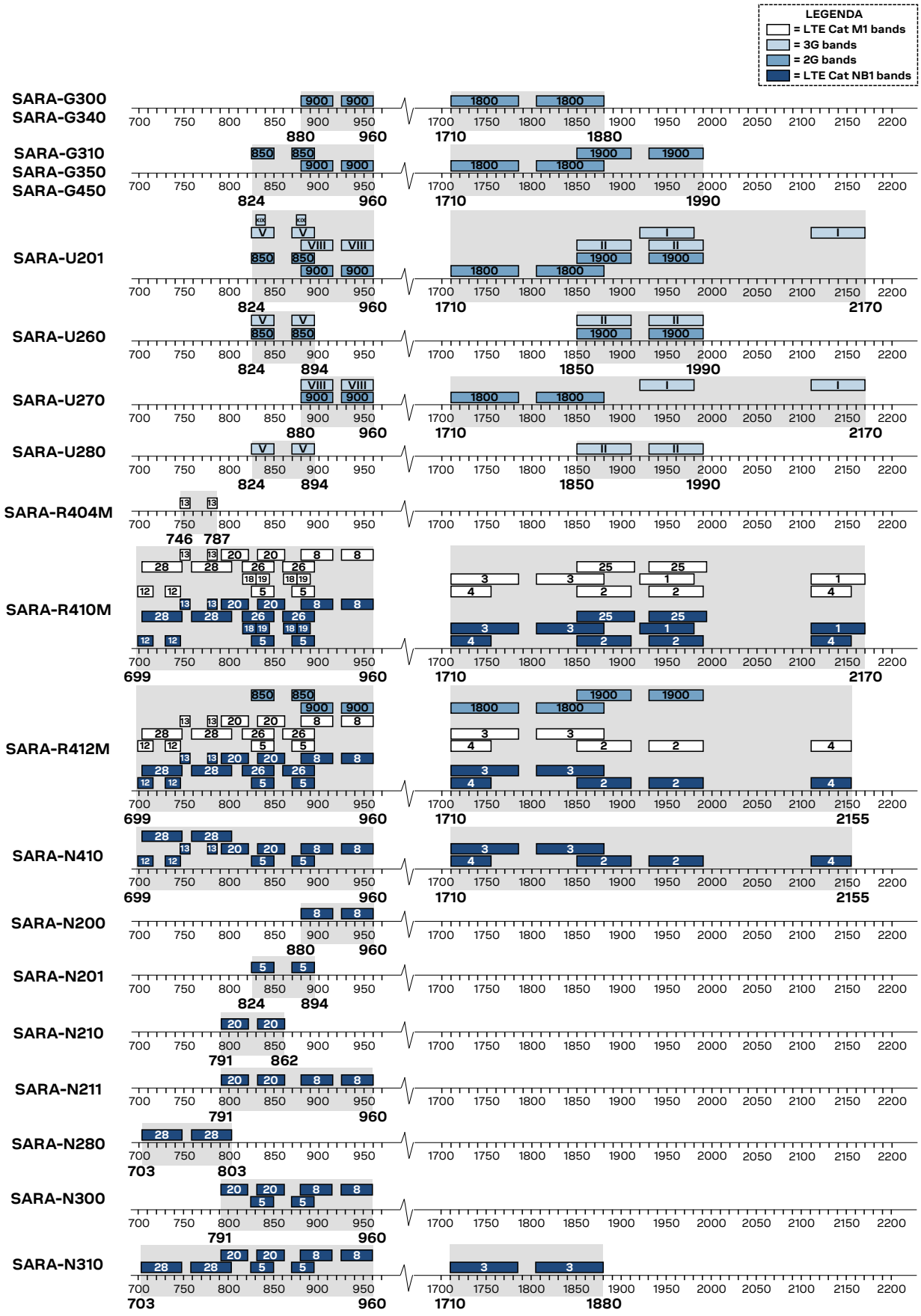

Figure 56: Summary of operating frequency bands supported by SARA modules

A.2 Pin-out comparison between SARA modules

	SARA-N2		SARA-N3		SARA-N4 / R4		SARA-G3		SARA-G4		SARA-U2	
No	**Pin name**	**Description**	**Pin name**	**Description**	**Pin name**	**Description**	**Pin name**	**Description**	**Pin name**	**Description**	**Pin name**	**Description**
1	GND	Ground	GND	Ground	GND	Ground	GND	Ground	GND	Ground	GND	Ground
2	RSVD	Reserved	V_BCKP	RTC Supply I/O	RSVD	Reserved	V_BCKP	RTC Supply I/O	V_BCKP	RTC Supply I/O	V_BCKP	RTC Supply I/O
3	GND	Ground	GND	Ground	GND	Ground	GND	Ground	GND	Ground	GND	Ground
4	V_INT	Supply Output: 1.8 V typ ON when radio is on TestPoint recommended	V_INT	Supply Output: 1.8 V typ / 2.8 V typ ON when SARA is on TestPoint recommended Voltage value set by VSEL	V_INT	Supply Output: 1.8 V typ ON when SARA is on	V_INT	Supply Output: 1.8 V typ ON when SARA is on TestPoint recommended	V_INT	Supply Output: 1.8 V typ / 3.0 V typ ON when SARA is on TestPoint recommended Voltage value set by VSEL	V_INT	Supply Output: 1.8 V typ ON when SARA is on
5	GND	Ground	GND	Ground	GND	Ground	GND	Ground	GND	Ground	GND	Ground
6	RSVD	Reserved	DSR	UART DSR Output[8] V_INT level (1.8 / 2.8 V)	DSR	UART DSR Output V_INT level (1.8 V) Driver strength: 2 mA	DSR	UART DSR Output V_INT level (1.8 V) Driver strength: 6 mA	DSR	UART DSR Output V_INT level (1.8 / 3.0 V) Driver strength: 3 mA	DSR	UART DSR Output V_INT level (1.8 V) Driver strength: 1 mA
7	RSVD	Reserved	RI	UART RI Output V_INT level (1.8 / 2.8 V) Driver strength: 3 mA Configurable as GPIO	RI	UART RI Output V_INT level (1.8 V) Driver strength: 2 mA	RI	UART RI Output V_INT level (1.8 V) Driver strength: 6 mA	RI	UART RI Output V_INT level (1.8 / 3.0 V) Driver strength: 3 mA	RI	UART RI Output V_INT level (1.8 V) Driver strength: 2 mA
8	RSVD	Reserved	DCD	UART DCD Output[8] V_INT level (1.8 / 2.8 V)	DCD	UART DCD Output V_INT level (1.8 V) Driver strength: 2 mA	DCD	UART DCD Output V_INT level (1.8 V) Driver strength: 6 mA	DCD	UART DCD Output V_INT level (1.8 / 3.0 V) Driver strength: 3 mA	DCD	UART DCD Output V_INT level (1.8 V) Driver strength: 2 mA
9	RSVD	Reserved	DTR	UART DTR Input[8] V_INT level (1.8 / 2.8 V)	DTR	UART DTR Input V_INT level (1.8 V) Internal pull-up: ~100 k To be set low for URCs	DTR	UART DTR Input V_INT level (1.8 V) Internal pull-up: ~33 k Must be low for greeting	DTR	UART DTR Input V_INT level (1.8 / 3.0 V) Internal pull-up: ~166 k	DTR	UART DTR Input V_INT level (1.8 V) Internal pull-up: ~14 k Must be low for greeting
10	RTS	UART RTS Input[9] VCC level (3.6 V typ.) Internal pull-up: ~78 k	RTS	UART RTS Input V_INT level (1.8 / 2.8 V) Internal pull-up: ~171 k Configurable as GPIO	RTS	UART RTS Input V_INT level (1.8 V) Internal pull-up: ~100 k Must be low to use UART on '00', '01' versions	RTS	UART RTS Input V_INT level (1.8 V) Internal pull-up:~58 k	RTS	UART RTS Input V_INT level (1.8 / 3.0 V) Internal pull-up: ~166 k	RTS	UART RTS Input V_INT level (1.8 V) Internal pull-up: ~8 k
11	CTS	UART CTS Output[11] VCC level (3.6 V typ.) Driver strength: 1 mA Configurable as RI or Network Indicator	CTS	UART CTS Output V_INT level (1.8 / 2.8 V) Driver strength: 3 mA Configurable as GPIO or Network Indicator	CTS	UART CTS Output V_INT level (1.8 V) Driver strength: 2 mA	CTS	UART CTS Output V_INT level (1.8 V) Driver strength: 6 mA	CTS	UART CTS Output V_INT level (1.8 / 3.0 V) Driver strength: 3 mA	CTS	UART CTS Output V_INT level (1.8 V) Driver strength: 6 mA
12	TXD	UART Data Input VCC level (3.6 V typ.) No internal pull-up/down	TXD	UART Data Input V_INT level (1.8 / 2.8 V) Internal pull-up: ~171 k	TXD	UART Data Input V_INT level (1.8 V) Inner pull-up/down ~100k	TXD	UART Data Input V_INT level (1.8 V) Internal pull-up:~18 k	TXD	UART Data Input V_INT level (1.8 / 3.0 V) Internal pull-up: ~166 k	TXD	UART Data Input V_INT level (1.8 V) Internal pull-up: ~8 k
13	RXD	UART Data Output VCC level (3.6 V typ.) Driver strength: 1 mA	RXD	UART Data Output V_INT level (1.8 / 2.8 V) Driver strength: 3 mA	RXD	UART Data Output V_INT level (1.8 V) Driver strength: 2 mA	RXD	UART Data Output V_INT level (1.8 V) Driver strength: 6 mA	RXD	UART Data Output V_INT level (1.8 / 3.0 V) Driver strength: 3 mA	RXD	UART Data Output V_INT level (1.8 V) Driver strength: 6 mA

[8] Not supported by "00" product versions
[9] Not supported by "02" product versions

	SARA-N2		SARA-N3		SARA-N4 / R4		SARA-G3		SARA-G4		SARA-U2	
No	**Pin name**	**Description**	**Pin name**	**Description**	**Pin name**	**Description**	**Pin name**	**Description**	**Pin name**	**Description**	**Pin name**	**Description**
14	GND	Ground	GND	Ground	GND	Ground	GND	Ground	GND	Ground	GND	Ground
15	RSVD	Reserved	PWR_ON	Power-on Input 90 k internal pull-up L-level: 0.00 ÷ 0.20 V H-level: 0.90 ÷ 1.10 V ON L-level pulse time: 1 s min OFF L-level pulse time: 1 s min TestPoint recommended	PWR_ON	Power-on Input 200 k internal pull-up L-level: -0.30 ÷ 0.35 V H-level: 1.17 ÷ 2.10 V ON L-level time: 0.15 s min – 3.2 s max OFF L-level pulse time: 1.5 s min TestPoint recommended	PWR_ON	Power-on Input No internal pull-up L-level: -0.10 ÷ 0.65 V H-level: 2.00 ÷ 4.50 V ON L-level time: 5 ms min OFF L-level pulse time: Not Available	PWR_ON	Power-on Input 28 k internal pull-up L-level: 0.00 ÷ 0.30 V H-level: 1.75 ÷ 2.50 V ON L-level time: 2 s min OFF L-level time: Not Available TestPoint recommended	PWR_ON	Power-on Input No internal pull-up L-level: -0.30 ÷ 0.65 V H-level: 1.50 ÷ 4.40 V ON L-level pulse time: 50 µs min / 80 µs max OFF L-level pulse time: 1 s min
16	GPIO1	Trace data output V_INT level (1.8 V) Driver strength: 1 mA TestPoint recommended	GPIO1	GPIO V_INT level (1.8 / 2.8 V) Driver strength: 3 mA	GPIO1	GPIO V_INT level (1.8 V) Driver strength: 2 mA	GPIO1 / RSVD	GPIO / Reserved V_INT level (1.8 V) Driver strength: 6 mA	GPIO1	GPIO V_INT level (1.8 / 3.0 V) Driver strength: 3 mA	GPIO1	GPIO V_INT level (1.8 V) Driver strength: 6 mA
17	RSVD	Reserved	TXD_AUX	AUX UART Data Input[10] V_INT level (1.8 / 2.8 V) Internal pull-up: ~171 k	VUSB_DET	5 V, USB Detect Input TestPoint recommended	RSVD	Reserved	TXD_AUX	AUX UART Data Input[10] V_INT level (1.8 / 3.0 V) Internal pull-up: ~166 k	VUSB_DET	5 V, USB Detect Input TestPoint recommended
18	RESET_N	Reset input Internal pull-up 78 k L-level: 0 ÷ 0.36*VCC H-level: 0.52*VCC ÷ VCC It triggers module reboot when toggled, without PMU shutdown when low. TestPoint recommended	RESET_N	Reset shutdown input Internal pull-up 70 k L-level: 0.00 ÷ 0.20 V H-level: 0.90 ÷ 1.10 V It triggers module (re)boot when toggled, with PMU shutdown when low. TestPoint recommended	RESET_N	Shutdown input Internal pull-up 37 k L-level: -0.30 ÷ 0.35 V H-level: 1.17 ÷ 2.10 V It triggers shutdown of the whole module when set low or toggled. TestPoint recommended	RESET_N	Reset input Internal diode & pull-up L-level: -0.30 ÷ 0.30 V H-level: 2.00 ÷ 4.70 V It triggers module reboot when toggled, without PMU shutdown when low. TestPoint recommended	PWR_OFF	Shutdown input Internal diode L-level: 0.00 ÷ 0.10 V H-level: 1.20 ÷ 1.50 V It triggers shutdown of the whole module when set low or toggled. TestPoint recommended	RESET_N	Reset shutdown input Internal pull-up 10 k L-level: -0.30 ÷ 0.51 V H-level: 1.32 ÷ 2.01 V It triggers module (re)boot when toggled, with PMU shutdown when low. TestPoint recommended
19	RSVD	Reserved	RXD_AUX	AUX UART Data Output[10] V_INT level (1.8 / 2.8 V) Driver strength: 3 mA	GPIO6	GPIO V_INT level (1.8 V) Driver strength: 2 mA	RSVD	Reserved	RXD_AUX	AUX UART Data Output[10] V_INT level (1.8 / 3.0 V) Driver strength: 3 mA	CODEC_CLK	13 or 26 MHz Output V_INT level (1.8 V) Driver strength: 4 mA
20	GND	Ground	GND	Ground	GND	Ground	GND	Ground	GND	Ground	GND	Ground
21	GND	Ground	VSEL	V_INT voltage selection VSEL connected to GND: V_INT = 1.8 V VSEL unconnected: V_INT = 2.8 V	GND	Ground	GND	Ground	VSEL	V_INT voltage selection VSEL connected to GND: V_INT = 1.8 V VSEL unconnected: V_INT = 3.0 V	GND	Ground
22	GND	Ground	GND	Ground	GND	Ground	GND	Ground	GND	Ground	GND	Ground
23	RSVD	Reserved	GPIO2	GPIO V_INT level (1.8 / 2.8 V) Driver strength: 3 mA	GPIO2	GPIO V_INT level (1.8 V) Driver strength: 2 mA	GPIO2 / RSVD	GPIO / Reserved V_INT level (1.8 V) Driver strength: 6 mA	GPIO2	GPIO V_INT level (1.8 / 3.0 V) Driver strength: 3 mA	GPIO2	GPIO V_INT level (1.8 V) Driver strength: 1 mA
24	GPIO2	GPIO[11] V_INT level (1.8 V) Driver strength: 1 mA	GPIO3	GPIO V_INT level (1.8 / 2.8 V) Driver strength: 3 mA	GPIO3	GPIO V_INT level (1.8 V) Driver strength: 2 mA	GPIO3 / 32K_OUT	GPIO / 32 kHz Output V_INT level (1.8 V) Driver strength: 5 mA	GPIO3	GPIO V_INT level (1.8 / 3.0 V) Driver strength: 3 mA	GPIO3	GPIO V_INT level (1.8 V) Driver strength: 6 mA

[10] Not supported by “00” product version
[11] Not supported by “02” product versions

	SARA-N2		SARA-N3		SARA-N4 / R4		SARA-G3		SARA-G4		SARA-U2	
No	**Pin name**	**Description**	**Pin name**	**Description**	**Pin name**	**Description**	**Pin name**	**Description**	**Pin name**	**Description**	**Pin name**	**Description**
25	RSVD	Reserved	GPIO4	GPIO V_INT level (1.8 / 2.8 V) Driver strength: 3 mA	GPIO4	GPIO V_INT level (1.8 V) Driver strength: 2 mA	GPIO4 / RSVD	GPIO / Reserved V_INT level (1.8 V) Driver strength: 6 mA	GPIO4	GPIO V_INT level (1.8 / 3.0 V) Driver strength: 3 mA	GPIO4	GPIO V_INT level (1.8 V) Driver strength: 6 mA
26	SDA	I2C Data[12] V_INT level (1.8 V) Open drain No internal pull-up	SDA	I2C Data[13] V_INT level (1.8 / 2.8 V) Open drain No internal pull-up	SDA	I2C Data[14] V_INT level (1.8 V) Open drain Internal 2.2 k pull-up	SDA / RSVD	I2C Data / Reserved V_INT level (1.8 V) Open drain No internal pull-up	SDA	I2C Data[13] V_INT level (1.8 / 3.0 V) Open drain No internal pull-up	SDA	I2C data / Aux UART in V_INT level (1.8 V) Open drain No internal pull-up
27	SCL	I2C Clock[12] V_INT level (1.8 V) Open drain No internal pull-up	SCL	I2C Clock[13] V_INT level (1.8 / 2.8 V) Open drain No internal pull-up	SCL	I2C Clock[14] V_INT level (1.8 V) Open drain Internal 2.2 k pull-up	SCL / RSVD	I2C Clock / Reserved V_INT level (1.8 V) Open drain No internal pull-up	SCL	I2C Clock[13] V_INT level (1.8 / 3.0 V) Open drain No internal pull-up	SCL	I2C clock / Aux UART out V_INT level (1.8 V) Open drain No internal pull-up
28	RSVD	Reserved	RXD_FT	FW update & Trace Out V_INT level (1.8 / 2.8 V) TestPoint recommended	USB_D-	USB Data I/O (D-) High-Speed USB 2.0 TestPoint recommended	RXD_AUX	Aux UART Data Out V_INT level (1.8 V) TestPoint recommended	RXD_FT	FW update & Trace Out V_INT level (1.8 / 3.0 V) TestPoint recommended	USB_D-	USB Data I/O (D-) High-Speed USB 2.0 TestPoint recommended
29	RSVD	Reserved	TXD_FT	FW update & Trace In V_INT level (1.8 / 2.8 V) TestPoint recommended	USB_D+	USB Data I/O (D+) High-Speed USB 2.0 TestPoint recommended	TXD_AUX	Aux UART Data In V_INT level (1.8 V) TestPoint recommended	TXD_FT	FW update & Trace In V_INT level (1.8 / 3.0 V) TestPoint recommended	USB_D+	USB Data I/O (D+) High-Speed USB 2.0 TestPoint recommended
30	GND	Ground	GND	Ground	GND	Ground	GND	Ground	GND	Ground	GND	Ground
31	RSVD	Reserved	RSVD	Reserved	RSVD	Reserved	RSVD / EXT32K	Reserved / 32kHz Input	RSVD	Reserved	RSVD	Reserved
32	GND	Ground	GND	Ground	GND	Ground	GND	Ground	GND	Ground	GND	Ground
33	RSVD	Reserved It can be grounded	ADC1	ADC input It can be grounded	RSVD	Reserved It can be grounded	RSVD	Reserved It must be grounded	RSVD	Reserved It can be grounded	RSVD	Reserved It must be grounded
34	RSVD	Reserved	RSVD	Reserved	I2S_WA / SPI_MOSI	I2S Align[14] / SPI MOSI[15] V_INT level (1.8 V) Driver strength: 2 mA	I2S_WA / RSVD	I2S Align / Reserved V_INT level (1.8 V) Driver strength: 6 mA	I2S_WA	I2S Word Alignment[13] V_INT level (1.8 V / 3.0 V) Driver strength: 3 mA	I2S_WA	I2S Word Alignment V_INT level (1.8 V) Driver strength: 2 mA
35	RSVD	Reserved	RSVD	Reserved	I2S_TXD / SPI_CS	I2S Out[14] / SPI chip sel[15] V_INT level (1.8 V) Driver strength: 2 mA	I2S_TXD / RSVD	I2S Out / Reserved V_INT level (1.8 V) Driver strength: 5 mA	I2S_TXD	I2S Data Output[13] V_INT level (1.8 V / 3.0 V) Driver strength: 3 mA	I2S_TXD	I2S Data Output V_INT level (1.8 V) Driver strength: 2 mA
36	RSVD	Reserved	RSVD	Reserved	I2S_CLK / SPI_CLK	I2S Clock[14] / SPI clock[15] V_INT level (1.8 V) Driver strength: 2 mA	I2S_CLK / RSVD	I2S Clock / Reserved V_INT level (1.8 V) Driver strength: 5 mA	I2S_CLK	I2S Clock[13] V_INT level (1.8 V / 3.0 V) Driver strength: 3 mA	I2S_CLK	I2S Clock V_INT level (1.8 V) Driver strength: 2 mA
37	RSVD	Reserved	RSVD	Reserved	I2S_RXD / SPI_MISO	I2S Input[14] / SPI MISO[15] V_INT level (1.8 V)	I2S_RXD / RSVD	I2S Input / Reserved V_INT level (1.8 V)	I2S_RXD	I2S Data Input[13] V_INT level (1.8 V / 3.0 V)	I2S_RXD	I2S Data Input V_INT level (1.8 V)
38	SIM_CLK	1.8V SIM Clock Output	SIM_CLK	1.8V/3V SIM Clock	SIM_CLK	1.8V/3V SIM Clock	SIM_CLK	1.8V/3V SIM Clock	SIM_CLK	1.8 V / 3 V SIM Clock	SIM_CLK	1.8V/3V SIM Clock
39	SIM_IO	1.8V SIM Data I/O Internal 4.7 k pull-up	SIM_IO	1.8V/3V SIM Data I/O Internal 4.7 k pull-up	SIM_IO	1.8V/3V SIM Data I/O Internal 4.7 k pull-up	SIM_IO	1.8V/3V SIM Data I/O Internal 4.7 k pull-up	SIM_IO	1.8 V / 3 V SIM Data I/O Internal 4.7 k pull-up	SIM_IO	1.8V/3V SIM Data I/O Internal 4.7 k pull-up
40	SIM_RST	1.8V SIM Reset Output	SIM_RST	1.8V/3V SIM Reset	SIM_RST	1.8V/3V SIM Reset	SIM_RST	1.8V/3V SIM Reset	SIM_RST	1.8 V / 3 V SIM Reset	SIM_RST	1.8V/3V SIM Reset
41	VSIM	1.8V SIM Supply	VSIM	1.8V/3V SIM Supply	VSIM	1.8V/3V SIM Supply	VSIM	1.8V/3V SIM Supply	VSIM	1.8 V / 3 V SIM Supply	VSIM	1.8V/3V SIM Supply

[12] Not supported by “02” product versions
[13] Not supported by “00” product version
[14] Not supported by “00” and “01” product versions
[15] Not supported by “00”, “01” and “x2” product version

	SARA-N2		SARA-N3		SARA-N4 / R4		SARA-G3		SARA-G4		SARA-U2	
No	**Pin name**	**Description**	**Pin name**	**Description**	**Pin name**	**Description**	**Pin name**	**Description**	**Pin name**	**Description**	**Pin name**	**Description**
42	RSVD	Reserved	GPIO5	SIM Detection Input V_INT level (1.8 / 2.8 V)	GPIO5	SIM Detection Input V_INT level (1.8 V)	SIM_DET	SIM Detection Input V_INT level (1.8 V)	SIM_DET	SIM Detection Input V_INT level (1.8 V / 3.0 V)	SIM_DET	SIM Detection Input V_INT level (1.8 V)
43	GND	Ground	GND	Ground	GND	Ground	GND	Ground	GND	Ground	GND	Ground
44	RSVD	Reserved	RSVD	Reserved	SDIO_D2	SDIO serial data [2][16]	SPK_P / RSVD	Analog Audio Out (+) / Reserved	SPK_P	Analog Audio Out (+)[17]	RSVD	Reserved
45	RSVD	Reserved	RSVD	Reserved	SDIO_CLK	SDIO serial clock[16]	SPK_N / RSVD	Analog Audio Out (-) / Reserved	SPK_N	Analog Audio Out (-)[17]	RSVD	Reserved
46	RSVD	Reserved	RSVD	Reserved	SDIO_CMD	SDIO command[16]	MIC_BIAS / RSVD	Microphone Supply / Reserved	MIC_BIAS	Microphone Supply[17]	RSVD	Reserved
47	RSVD	Reserved	RSVD	Reserved	SDIO_D0	SDIO serial data [0] [16]	MIC_GND / RSVD	Microphone Ground / Reserved	MIC_GND	Microphone Ground[17]	RSVD	Reserved
48	RSVD	Reserved	RSVD	Reserved	SDIO_D3	SDIO serial data [3] [16]	MIC_N / RSVD	Analog Audio In (-) / Reserved	MIC_N	Analog Audio In (-)[17]	RSVD	Reserved
49	RSVD	Reserved	RSVD	Reserved	SDIO_D1	SDIO serial data [1] [16]	MIC_P / RSVD	Analog Audio In (+) / Reserved	MIC_P	Analog Audio In (+)[17]	RSVD	Reserved
50	GND	Ground	GND	Ground	GND	Ground	GND	Ground	GND	Ground	GND	Ground
51-53	VCC	Module Supply Input Normal range: 3.10 ÷ 4.00 V Extended range: 2.75 ÷ 4.20 V Max current: ~0.3A during Tx Turn-on by VCC apply	VCC	Module Supply Input Normal range: 3.10 ÷ 4.20 V Extended range: 2.60 ÷ 4.20 V Max current: ~0.3A during Tx No turn-on by VCC apply	VCC	Module Supply Input Normal op. range: 3.20 ÷ 4.20 V Extended op. range: 3.00 ÷ 4.30 V Max current: ~2.0A during 2G Tx No turn-on by VCC apply	VCC	Module Supply Input Normal op. range: 3.35 ÷ 4.50 V Extended op. range: 3.00 ÷ 4.50 V Max current: ~2.0A during 2G Tx Turn-on by VCC apply	VCC	Module Supply Input Normal op. range: 3.40 ÷ 4.20 V Extended op. range: 3.10 ÷ 4.50 V Max current: ~2.0A during 2G Tx No turn-on by VCC apply	VCC	Module Supply Input Normal op. range: 3.30 ÷ 4.40 V Extended op. range: 3.10 ÷ 4.50 V Max current: ~2.0 A during 2G Tx Turn-on by VCC apply
54-55	GND	Ground	GND	Ground	GND	Ground	GND	Ground	GND	Ground	GND	Ground
56	ANT	Cellular RF I/O	ANT	Cellular RF I/O	ANT	Cellular RF I/O	ANT	Cellular RF I/O	ANT	Cellular RF I/O	ANT	Cellular RF I/O
57-58	GND	Ground	GND	Ground	GND	Ground	GND	Ground	GND	Ground	GND	Ground
59	GND	Ground	ANT_BT	Bluetooth RF I/O[17] It can be grounded	GND	Ground	GND	Ground	GND	Ground	GND	Ground
60-61	GND	Ground	GND	Ground	GND	Ground	GND	Ground	GND	Ground	GND	Ground
62	ANT_DET	Antenna Detection[18]	ANT_DET	Antenna Detection	ANT_DET	Antenna Detection	ANT_DET / RSVD	Antenna Detection / Reserved	ANT_DET / RSVD	Antenna Detection / Reserved	ANT_DET	Antenna Detection
63-96	GND	Ground	GND	Ground	GND	Ground	GND	Ground	GND	Ground	GND	Ground

Table 31: SARA-N2, SARA-N3, SARA-N4, SARA-R4, SARA-G3, SARA-G4 and SARA-U2 series modules pin assignment and description, with remarks for migration

For further details regarding the characteristics, capabilities, usage or settings applicable for each interface of the SARA-N2, SARA-N3, SARA-N4, SARA-R4, SARA-G3, SARA-G4 and SARA-U2 series modules, see the related data sheet [1], [2], [15], [9], [10], [11], the related system integration manual [12], [13], [16], the related AT commands manual [4], [14], [17], and the nested design application note [8].

[16] Not supported by “00”, “01” and “x2” product version
[17] Not supported by “00” product version
[18] Not supported by “02” product version

A.3 Schematic for SARA modules integration

Figure 57 shows an example of a simple schematic diagram where a SARA-N2, SARA-N3, SARA-N4, SARA-R4, SARA-G3, SARA-G4 and/or SARA-U2 module is integrated in the same application board, using the main available interfaces and functions of the modules.

The different mounting options for the external parts are highlighted in different colors as described in the legend, according to the interfaces supported by the each module, and related characteristics.

In the simple schematic diagram shown in Figure 57, the **VCC** supply of the SARA modules is provided by a suitable supply source, at 3.6 V nominal voltage, not illustrated in the diagram. The application processor controls the **VCC** supply of the modules by means of a high-side switch. Proper bypass capacitors and EMI filter parts are placed close to the **VCC** input pins of the modules.

While selecting the supply source for SARA cellular modules, consider with adequate safe design margin the maximum current consumption of each SARA cellular module (see the related data sheet [1], [2], [15], [9], [10], [11]), as it reflects the RATs supported. For additional specific design guidelines, see the **VCC** interface sections in the system integration manual [12], [13], [16]

The switch-on sequence of SARA-N2, SARA-G3 and SARA-U2 starts by applying a valid **VCC** supply.

Instead, SARA-N3, SARA-N4, SARA-R4 and SARA-G4 modules continue to be switched off even after a valid **VCC** supply has been applied: the **PWR_ON** line has to be properly toggled, with valid **VCC** supply present, to start the switch-on sequence of these modules. Proper toggling of the **RESET_N** line can be used as an alternative method, instead of the **PWR_ON** line toggling, to start the switch-on sequence of the SARA-N3 modules.

The application processor is connected to the SARA modules over main UART interface in the simple schematic diagram illustrated in Figure 57.

The design is implemented with the UART interface configured at the same voltage level on both sides (application processor and SARA module), without using voltage translators, as it is recommended in order to minimize any possible leakage and benefit from the extremely low current consumption of the u-blox LPWA modules, in particular in deep sleep Power Saving Mode.

Thus, the supply level of the application processor is selected to properly set its UART voltage level:

- at the **VCC** level of the module (3.6 V nominal), in case of SARA-N2
- at the **V_INT** level of the module (2.8 V nominal, with **VSEL** unconnected), in case of SARA-N3
- at the **V_INT** level of the module (3.0 V nominal, with **VSEL** unconnected), in case of SARA-G4
- at the **V_INT** level of the module (1.8 V nominal), for all the other SARA modules

The **TXD** and **RXD** data lines, supported by all the SARA modules for AT and data communication, are directly connected with the application processors. For additional specific design guidelines, see the UART sections in the system integration manual [12], [13], [16].

The **RTS**, **CTS** and **RI** lines are connected with the application processors by 0R jumpers for all the SARA modules except the SARA-N2 series, which does not support hardware flow control functionality and instead supports **RI** functionality over the **CTS** output pin.

The other UART lines are not implemented in the simple example of design shown in Figure 57, and the **DTR** input is grounded as required to have the greeting text and the URCs sent by the SARA-N4, SARA-R4 and SARA-U2 modules.

The application processor controls the **PWR_ON** line by means of an open drain driver in the circuit illustrated in Figure 57, with an external pull-up to **V_BCKP** for SARA-G3 and SARA-U2 modules. The whole circuit need not be populated for SARA-N2 modules, which do not provide **PWR_ON** input.

The application processor controls the **RESET_N** / **PWR_OFF** line by means of open drain driver too. Note that the assertion or toggling of this line causes different actions:

- the **RESET_N** line triggers an unconditional reboot of the module when toggled, without internal PMU shutdown when set low, in case of SARA-N2 and SARA-G3
- the **RESET_N** line triggers a boot of the module when toggled, in case the module is switched off, or an unconditional reboot of the module when toggled, in case the module is switched on, with internal PMU shutdown when set low, in case of SARA-N3 and SARA-U2
- the **RESET_N** / **PWR_OFF** line triggers an unconditional shutdown of the module when set low or toggled, in case of SARA-N4, SARA-R4 and SARA-G4

The timings for proper control of the **PWR_ON**, **RESET_N**, **PWR_OFF** lines of the SARA modules are reported in the related data sheet [1], [2], [15], [9], [10], [11].

The **ANT** cellular antenna circuit is implemented in Figure 57 with also the optional **ANT_DET** antenna detection circuit according to the design guidelines provided in the antenna interface sections of the system integration manual [12], [13], [16].

While selecting the antenna for SARA cellular modules, consider the frequency range supported by each SARA module, as illustrated in Figure 57.

Designers have to take care of the antenna from all perspective at the very start of the design phase, when the physical dimensions of the application board are under analysis/decision, since the RF compliance of the end-device integrating cellular modules with all the applicable required certification schemes depending on the antenna's radiating performance.

While implementing the RF antenna design for SARA cellular modules, consider providing the best possible return loss in the frequency range supported by the modules, and place the antenna far from **VCC** supply line and related parts, as well as far from any possible noise source.

The SIM interface circuit is implemented in Figure 57 with also the optional SIM detection function, according to the design guidelines provided in SIM interface sections of the system integration manual [12], [13], [16]: bypass capacitors with proper Self-Resonant Frequency are recommended to be placed close to the SIM connector, as well as ESD protections.

The **GPIO1** that controls an LED as shown in Figure 57, to provide the network status indication, is supported by all SARA modules except SARA-N2 series that can provide this function on the **CTS** pin. Other functions can be enabled on the GPIOs of the SARA modules, as described in the related data sheet [1], [2], [15], [9], [10], [11], and AT commands manual [4], [14], [17].

Test-Points for diagnostic access and/or FW upgrade purpose are provided in Figure 57 at the **V_INT**, **PWR_ON**, **RESET_N**, **GPIO1**, **TXD_FT**, **RXD_FT** and **VUSB_DET**, as recommended.

All the GND pins are intended to be externally connected to ground, while other interfaces are not implemented or not used in the simple example of design as shown in Figure 57.

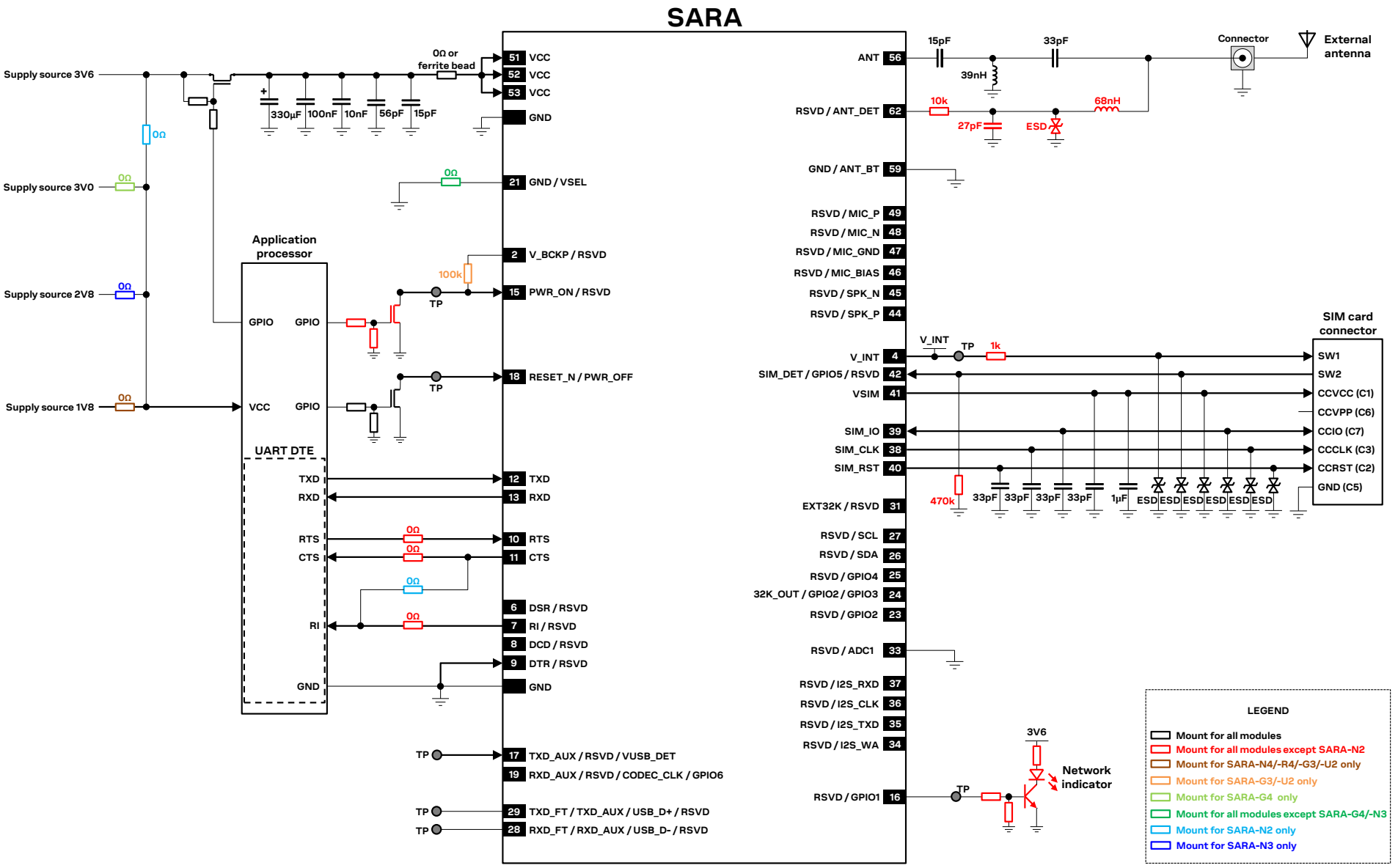

Figure 57: Example schematic to integrate a SARA-N2, SARA-N3, SARA-N4, SARA-R4, SARA-G3, SARA-G4 and/or SARA-U2 module in the same application PCB, using main interfaces

B Glossary

Abbreviation	Definition
3GPP	3rd Generation Partnership Project
ADC	Analog to Digital Converter
AP	Application Processor
APAC	Asia-Pacific
AT	AT Command Interpreter Software Subsystem, or attention
ATEX	EU Explosive Atmosphere Directive
Cat	Category
CoAP	Constrained Application Protocol
CTS	Clear To Send
DC	Direct Current
DCD	Data Carrier Detect
DCE	Data Communication Equipment
DDC	Display Data Channel interface
DL	Down-link (Reception)
DRX	Discontinuous Reception
DSP	Digital Signal Processing
DSR	Data Set Ready
DTE	Data Terminal Equipment
DTLS	Datagram Transport Layer Security
DTR	Data Terminal Ready
eDRX	Extended Discontinuous Reception
EMC	Electro-magnetic Compatibility
EMI	Electro-magnetic Interference
ESD	Electro-static Discharge
ESR	Equivalent Series Resistance
FEM	Front End Module
FOAT	Firmware (update) Over AT commands
FOTA	Firmware (update) Over-The-Air
FTP	File Transfer Protocol
FW	Firmware
GND	Ground
GNSS	Global Navigation Satellite System
GPIO	General Purpose Input Output
HF	Hands-free
HARQ	Hybrid Automatic Repeat Request
HTTP	HyperText Transfer Protocol
HW	Hardware
I/Q	In phase and Quadrature
I2C	Inter-Integrated Circuit interface
IP	Internet Protocol
LDO	Low-Dropout
LGA	Land Grid Array
LNA	Low Noise Amplifier

Abbreviation	Definition
LPWA	Low-Power Wide-Area
LwM2M	Lightweight Machine-to-Machine protocol
M2M	Machine-to-Machine
MQTT	Message Queuing Telemetry Transport
N/A	Not Applicable
N.A.	Not Available
NB-IoT	Narrow Band – Internet of Things
PA	Power Amplifier
PCM	Pulse Code Modulation
PCN	Sample Delivery Note / Information Note / Product Change Notification
PFM	Pulse Frequency Modulation
PMU	Power Management Unit
PSM	Power Saving Mode
PWM	Pulse Width Modulation
RAT	Radio Access Technology
RF	Radio Frequency
RI	Ring Indicator
RRC	Radio Resource Control
RTC	Real Time Clock
RTS	Request To Send
SAW	Surface Acoustic Wave
SSL	Secure Sockets Layer
SIM	Subscriber Identification Module
TBD	To Be Defined
TCP	Transmission Control Protocol
TLS	Transport Layer Security
TP	Test-Point
UART	Universal Asynchronous Receiver-Transmitter
UDP	User Datagram Protocol
UICC	Universal Integrated Circuit Card
UL	Up-link (Transmission)
URC	Unsolicited Result Code
VSWR	Voltage Standing Wave Ratio

Table 32: Explanation of the abbreviations and terms used

Related documents

[1] u-blox SARA-N2 series data sheet, doc. no. UBX-15025564
[2] u-blox SARA-N3 series data sheet, doc. no. UBX-18066692
[3] u-blox package information user guide, doc. no. UBX-14001652
[4] u-blox SARA-N2 / SARA-N3 series AT commands manual, doc. no. UBX-16014887
[5] u-blox NB-IoT application development guide, doc. no. UBX-16017368
[6] ITU-T recommendation V.24 - 02-2000 - List of definitions for interchange circuits between the Data Terminal Equipment (DTE) and the Data Circuit-terminating Equipment (DCE). http://www.itu.int/rec/T-REC-V.24-200002-I/en
[7] I2C-bus specification and user manual - Rev. 5 - 9 October 2012 - NXP semiconductors, http://www.nxp.com/documents/user_manual/UM10204.pdf
[8] u-blox nested design application note, doc. no. UBX-16007243
[9] u-blox SARA-G3 series data sheet, doc. no. UBX-13000993
[10] u-blox SARA-G4 series data sheet, doc. no. UBX-18006165
[11] u-blox SARA-U2 series data sheet, doc. no. UBX-13005287
[12] u-blox SARA-G3 / SARA-U2 series system integration manual, doc. no. UBX-13000995
[13] u-blox SARA-G4 series system integration manual, doc. no. UBX-18046432
[14] u-blox AT commands manual, doc. no. UBX-13002752
[15] u-blox SARA-R4 / SARA-N4 series data sheet, doc. no. UBX-16024152
[16] u-blox SARA-R4 / SARA-N4 series system integration manual, doc. no. UBX-16029218
[17] u-blox SARA-R4 / SARA-N4 series AT commands manual, doc. no. UBX-17003787
[18] IEC 60079-0 - Explosive atmospheres, part 0: equipment general requirements
[19] IEC 60079-11 - Explosive atmospheres, part 11: equipment protection by intrinsic safety “i”
[20] IEC 60079-26 - Explosive atmospheres, part 26: equipment with EPL Ga

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Revision history

Revision	Date	Name	Comments
R01	06-Jun-2017	sfal / sses	Initial release
R02	31-Oct-2017	sses	Updated VCC, V_INT, Power-on, Reset, ANT_DET, CTS and GPIO description. Updated main certification approvals.
R03	22-Feb-2018	sses	Extended document applicability to SARA-N211-02X and updated product status Updated VCC and switch-on info. Updated Antenna Detection, CTS and GPIO features info. Updated approvals info. Additional design-in examples, minor corrections and improvements.
R04	22-Jun-2018	sses	Extended the document applicability to SARA-N201-02B-01. Updated SARA-N211-02X product status. Added ATEX and approvals info. Updated TXD info. Minor corrections and clarifications.
R05	27-Aug-2018	lpah	Extended the document applicability to SARA-N200-02B-01, SARA-N210-02B-01, SARA-N211-02X-01, SARA-N280-02B-01.
R06	30-Nov-2018	lpah	SARA-N200-02B-01, SARA-N210-02B-01, SARA-N211-02X-01, SARA-N280-02B-01 product status update.
R07	08-Mar-2019	sses	Extended the document applicability to SARA-N300 and SARA-N310.
R08	18-Jul-2019	fvid	Improved description of SARA-N3 series modules operating modes.
R09	31-Jul-2019	lpah	Extended the document applicability to SARA-N200-02B-02, SARA-N210-02B-02, SARA-N211-02X-02.
R10	01-Oct-2019	lpah / sses	Update SARA-N300-00B / SARA-N310-00X product status. Added ATEX / IECEx approval info. Other minor changes.
R11	04-Nov-2019	lpah	SARA-N200-02B-02, SARA-N201-02B-01, SARA-N210-02B-02, SARA-N211-02X-02, SARA-N280-02B-01 product status update.

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