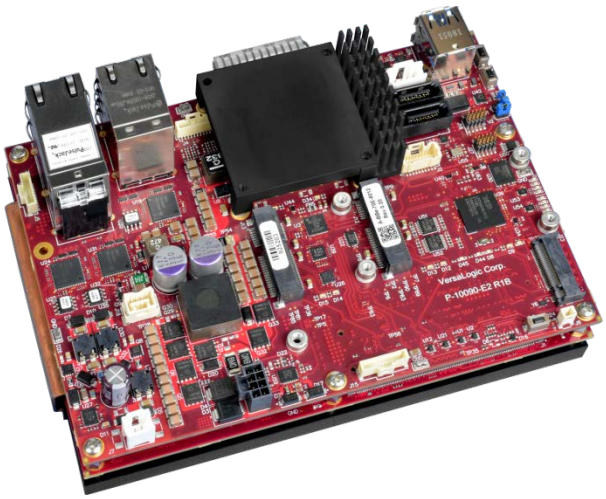
Hardware Reference Manual



REV. March 2020

Grizzly (VL-ESU-5070)

A rugged embedded server unit featuring the Intel® C3958 16-core micro-server processor and 10 GbE networking ports.

VERSALOGIC CORPORATION

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Product Release Notes

Rev. 1.00	• Initial draft
Rev. 1.10	• Added BIOS setup steps on page 15 • Added a note discussing replacing TIM after opening DIMM cover (page 43) • Several formatting changes • Added Figure 6."PoE Power Connector Pinout and Orientation"
Rev. 1.15	• Updated PoE information on page 26
Rev. 1.20	• Updated the "initial boot time" notes on pages 15 and 16.

Support Page

The Product Support Page contains additional information and resources for this product including:

- Operating system information and links to software drivers
- Data sheets and manufacturers' links for chips used in this product
- BIOS and PLD information and upgrades
- Links to KnowledgeBase articles and product advisories

VersaTech Knowledgebase

The VersaTech KnowledgeBase is a useful resource for resolving technical issues with your VersaLogic product.

Customer Support

If you are unable to solve a problem after reading this manual, visiting the product support page, or searching the KnowledgeBase, contact VersaLogic Technical Support at (503) 747-2261. VersaLogic support engineers are also available via e-mail at Support@VersaLogic.com.

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If your product requires service, you must obtain a Returned Material Authorization (RMA) number by calling (503) 747-2261. Please provide the following information:

- Your name, the name of your company, your phone number, and e-mail address
- The name of a technician or engineer that can be contacted if any questions arise
- The quantity of items being returned
- The model and serial number (barcode) of each item
- A detailed description of the problem
- Steps you have taken to resolve or recreate the problem

- The return shipping address

AS9100

All AS9100 products dispositioned for scrap shall be conspicuously and permanently marked, or positively controlled, until physically rendered unusable.

Material designated for scrap may be recycled in a manner that complies with applicable environmental regulations.

Note: VersaLogic recommends that all materials be disposed of in environmentally responsible manner i.e., recycling in compliance with applicable laws and regulations.

Warranty Repair

All parts and labor charges are covered, including return shipping charges for UPS Ground delivery to United States addresses.

Non-warranty Repair

All approved non-warranty repairs are subject to diagnosis and labor charges, parts charges and return shipping fees. Please specify the shipping method you prefer and provide a purchase order number for invoicing the repair.

Note: Please mark the RMA number clearly on the outside of the box before returning.

Contents

Tables

Figures

Introduction

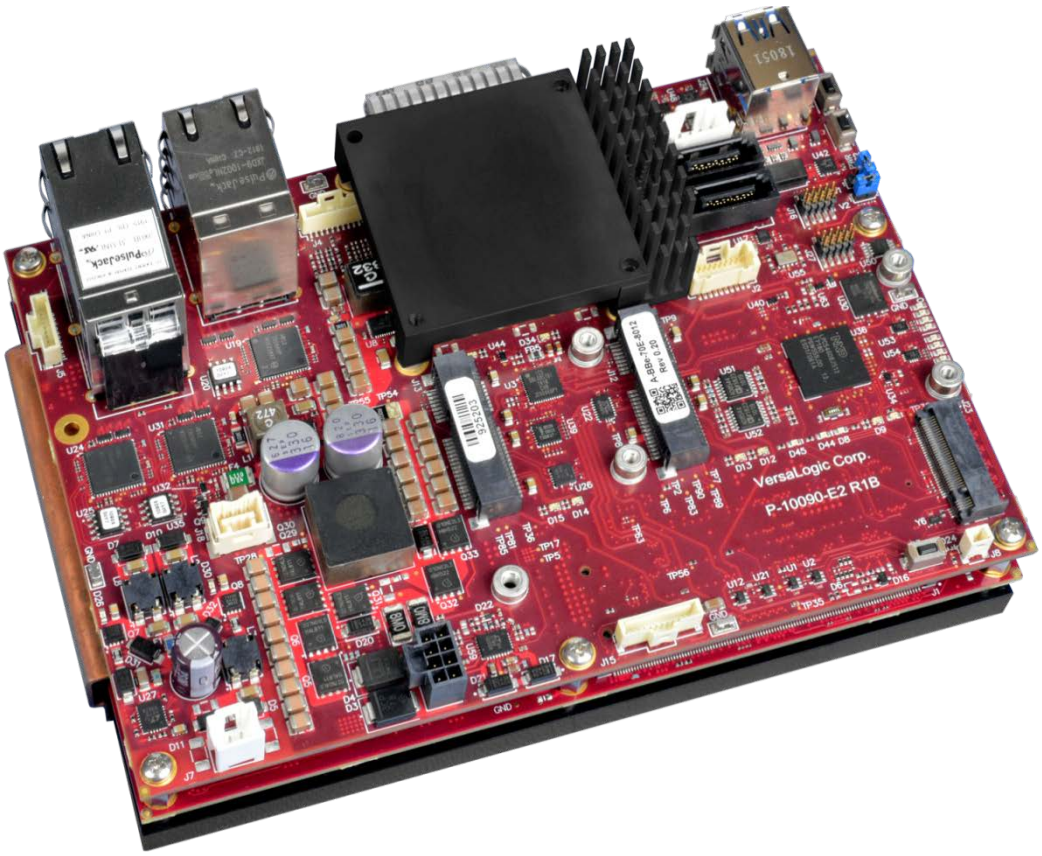
Description

The VL-ESU-5070 is a rugged embedded server unit (ESU) featuring an Intel 16-core processor, two 10 Gigabit Ethernet SFP+ ports, four Gigabit Ethernet ports, and up to 128 GB of ECC memory. This configuration is ideal for applications requiring high-performance processing using high data bandwidth. Additionally, two Mini PCIe sockets and a PCIe x4 M.2 site provide on-board I/O expansion and high speed read/write high-capacity storage. The VL-ESU-5070 also contains additional interfaces including USB, serial and digital I/O, and SATA.

The high-performance capabilities of the VL-ESU-5070 make it ideal for situations where local data gathering and processing are required for security or location-based cloud computing. A 16-core processor coupled with ECC memory enables the use of hypervisors supporting virtual machines. The 10 Gigabit SFP+ ports permit high speed connectivity. Networks can be created using plug-in copper, short-reach fiber, or long-reach fiber transceivers.

- **Intel* 16-core server-class processor**
  Very high performance computing and I/O processing
- **-40° to +85°C Operation**
  Operates over full industrial temperature range
- **MIL-STD-202H Shock and vibration**
  Ideal for Mil/Aero and other challenging environments
- **Error correcting RAM safeguards critical applications**
  Four slots support up to 128 GB of ECC memory
- **Two 10 Gigabit Ethernet (SFP+)**
  Supports very high speed copper and fiber connections
- **Four 1 GbE Ports. Two with Power Over Ethernet (POE)**
- **Mini PCIe Sockets. Add GPS and other options**
- **On-board data storage**
  M.2 expansion site supports up to 2 TB of storage
- **Compact size. Only 110 x 155 mm (4.33 x 6.1”)**

VL-ESU-5070 boards undergo 100% functional testing and are backed by a limited five-year warranty. Careful parts sourcing ensure the highest possible quality, reliability, and product longevity for this exceptional embedded server. A US-based technical support staff ensures quick, expert assistance.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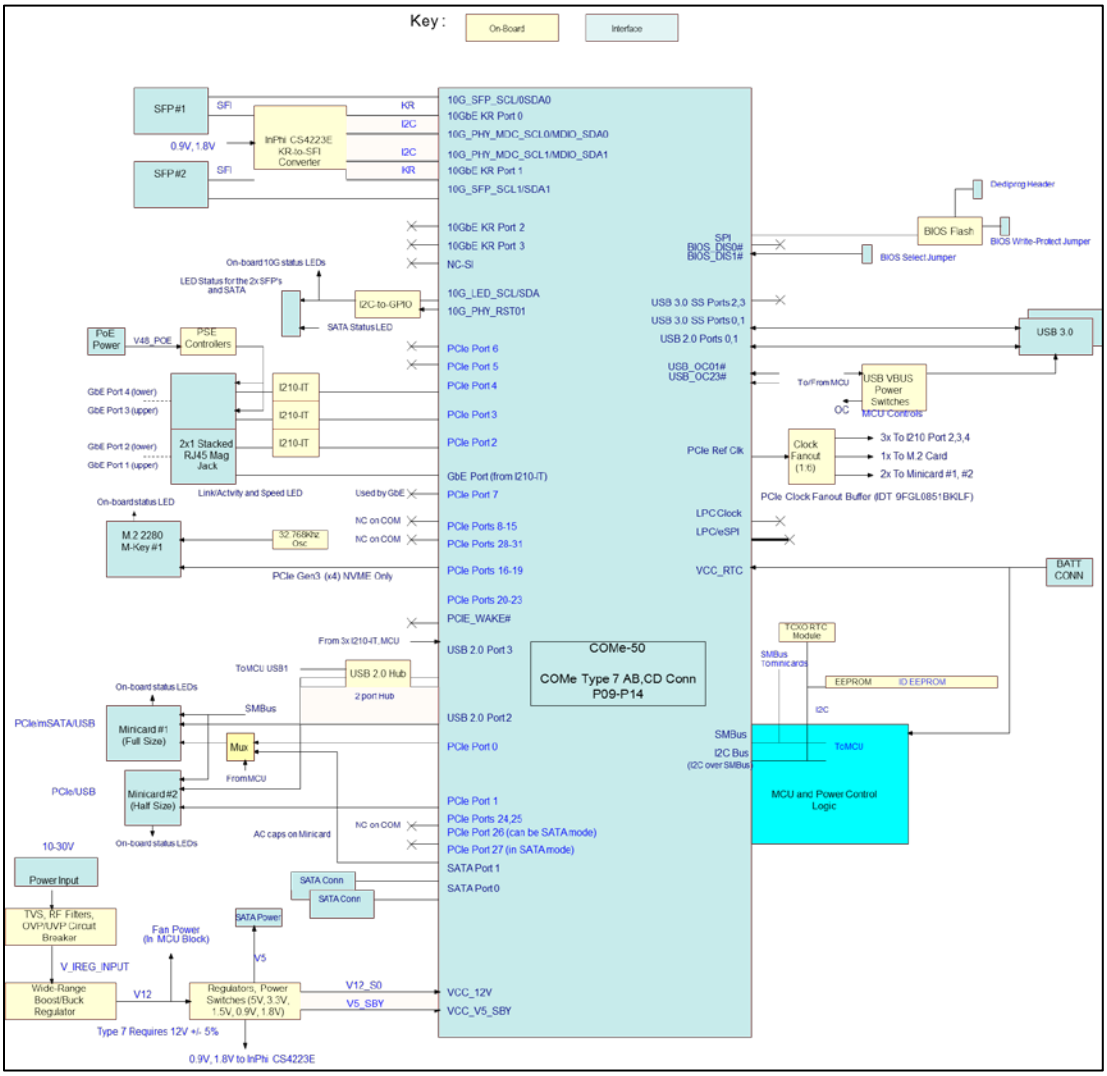
P-10090-E2 R1B

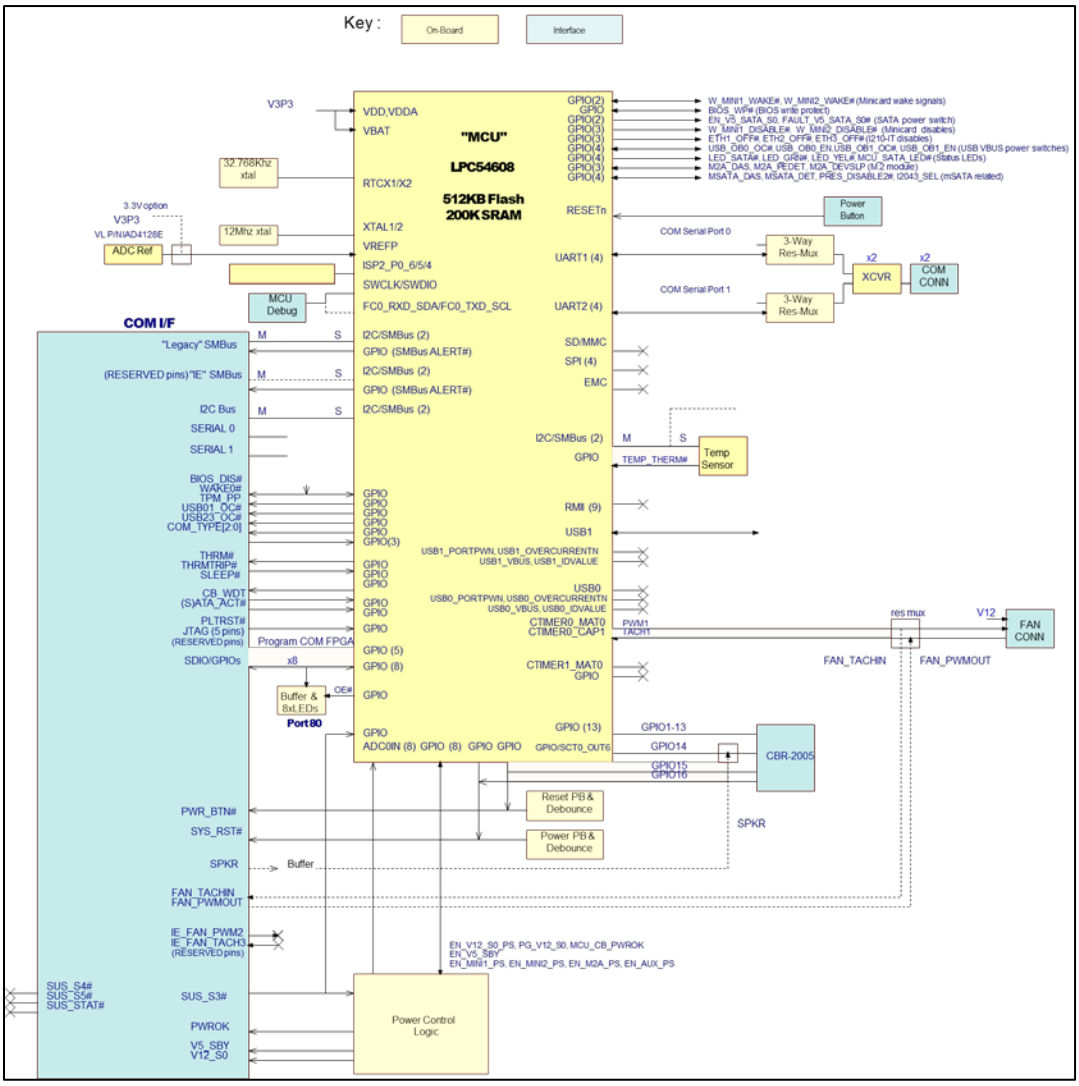
Technical Specifications

See the VL-ESU-5070 Data Sheet for complete specifications.

VL-ESU-5070 Block Diagram



VL-ESU-5070 MCU Block Diagram



Warnings

ELECTROSTATIC DISCHARGE

Electrostatic discharge (ESD) can damage circuit boards, disk drives and other components. The circuit board must only be handled at an ESD workstation. If an approved station is not available, some measure of protection can be provided by wearing a grounded antistatic wrist strap. Keep all plastic away from the board and do not slide the board over any surface.

After removing the board from its protective wrapper, place the board on a grounded, static-free surface, component side up. Use an antistatic foam pad if available.

The board should also be protected inside a closed metallic anti-static envelope during shipment or storage.

Note The exterior coating on some metallic antistatic bags is sufficiently conductive to cause excessive battery drain if the bag comes in contact with the bottom-side of the product.

Warning! To prevent shorting, premature failure or damage to the lithium battery, do not place the board on a conductive surface such as metal, black conductive foam or the outside surface of a metalized ESD protective pouch. The lithium battery may explode if mistreated. Do not recharge, disassemble or dispose of in fire. Dispose of used batteries promptly and in an environmentally suitable manner. VersaLogic recommends that the battery be disposed of in an environmentally responsible manner, i.e., recycling.

HANDLING CARE

Care must be taken when handling the board not to touch the exposed circuitry with your fingers. Though it will not damage the circuitry, it is possible that small amounts of oil or perspiration on the skin could have enough conductivity to cause the contents of BIOS RAM to become corrupted through careless handling, resulting in BIOS resetting to factory defaults.

EARTH GROUND REQUIREMENT

All mounting holes (eight on ESU, EBX and EPIC boards, four on PC/104 boards) should be connected to earth ground (chassis ground). This provides proper grounding for ESD and EMI purposes. In portable applications, the mounting holes should be connected to the ground reference of the system power supply

.

Configuration and Setup

Initial Configuration

The following components are recommended for a typical development system.

Configuration with Video

- VL-ESU-5070 computer
- VL-CBR-0812 power cable, 10 to 30V
- MPEe-V5E Mini PCIe video expansion module (installed at J12)
- VL-CBR-1204 VGA cable for MPEe-V5E
- VL-CBR-0203 battery (J8)
- SATA hard drive
- VL-CBR-0702 SATA cable
- VL-CBR-0407 SATA power cable
- USB keyboard and mouse

Configuration without Video

- VL-ESU-5070 computer
- VL-CBR-0812 power cable, 10 to 30V
- CBR-0203 battery (J8)
- Ethernet connection to host
- USB keyboard and mouse

Note: Air flow over the system is required for setup and configuration

You will also need an operating system installation media.

Basic Setup

The following steps outline the procedure for setting up a typical development system. The board should be handled at an ESD workstation or while wearing a grounded antistatic wrist strap.

Before you begin, unpack the product and accessories. Verify that you received all the items you ordered. Inspect the system visually for any damage that may have occurred in shipping. Contact Support@VersaLogic.com immediately if any items are damaged or missing.

Gather all the peripheral devices you plan to attach to the board and their interface and power cables.

It is recommended that you attach standoffs to the board.

1. Attach Cables and Peripherals

- Install MPEe-V5E Mini PCIe video expansion module (J12)
- Install VL-CBR-1204 VGA cable from the MPEe-V5E card to monitor
- Install VL-CBR-0203 battery (J8)
- Install keyboard and mouse
- Attach SATA hard drive using the VL-CBR-0702 SATA cable and VL-CBR-0407 SATA power cable

Note: Model VL-ESU-5070ECP-00X will require memory to be installed

2. Attach Power

- VL-CBR-0812 power cable to power connector (J6)

3. Review Configuration

- Before you power up the system, double-check all the connections. Make sure all cables are oriented correctly and that adequate power will be supplied to the board and peripheral devices.

4. Power On

- Turn on the power supply and the display. If the system is correctly configured, a video signal should be present.

Note: Initial boot time may be 5-12 minutes depending on memory module size, and this delay may occur again if memory modules are replaced.

Typically, the main POST code delays are 0x61 and 0x62. (Read and write training).

5. Enter BIOS Setup

- After video signal appears on monitor, press Esc repeatedly until the Front Page menu appears. Select the Setup Utility to enter BIOS Setup.

Note: There is a known issue in the 1.00 BIOS that may cause the system to reset after a few minutes if the F2 or Del hotkeys are used to enter BIOS Setup.

6. Configure Boot Priority

- On the Boot tab, configure the boot device priority. Then press F10 to Save and Exit.

Notes:

1. Setting Boot Type to UEFI only will prevent use of the MPEe-V5E video card in BIOS Setup.

2. To manually specify EFI device boot order, set “Add Boot Options” to First or Last.

7. Install Operating System

- Install the operating system according to the instructions provided by the OS manufacturer. (See Operating System Installation.)

Note: Initial boot time may be 5-12 minutes depending on memory module size, and this delay may occur again if memory modules are replaced or added.

It appears that the main POST code delays are 0x61 and 0x62. (Read and write training).

Operating System Installation

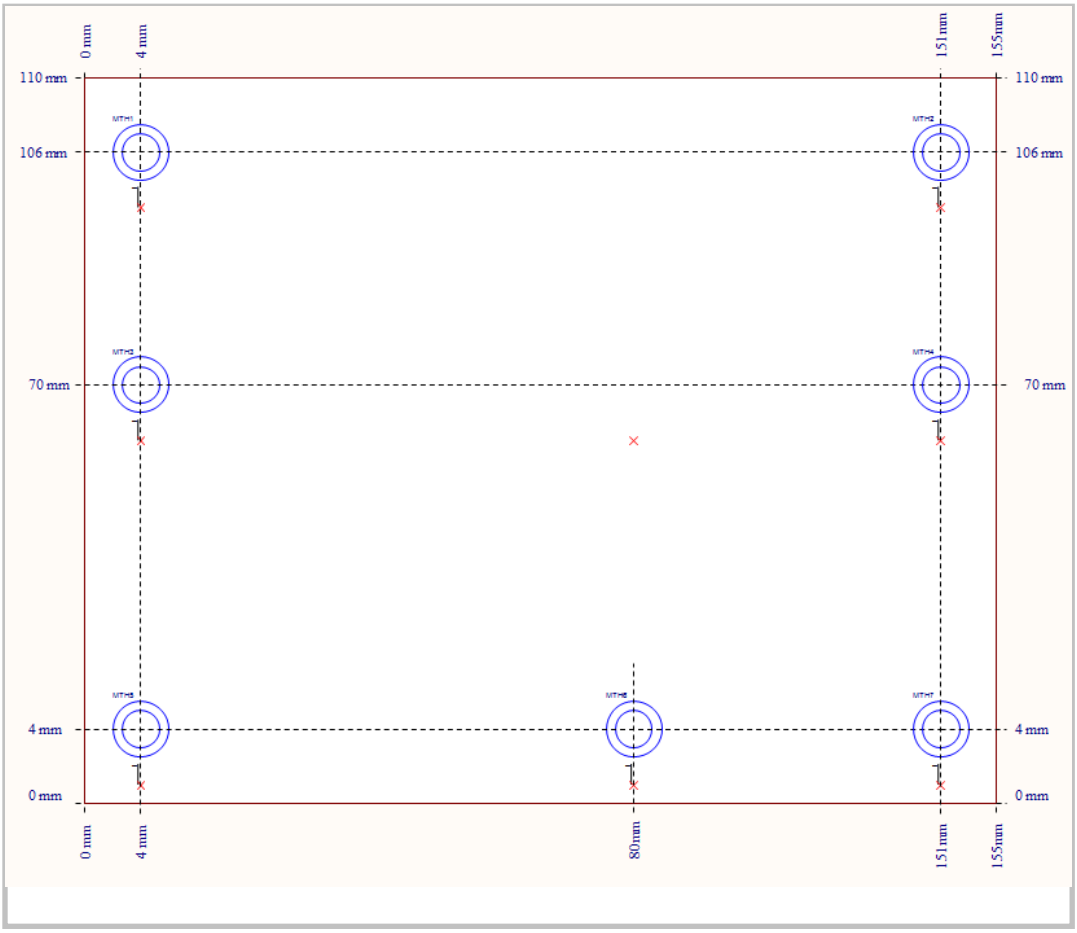
The standard PC architecture used on the VL-ESU-5070 make the installation and use of most of the standard x86 processor-based operating systems very simple. The operating systems listed on the Product Support Page use the standard installation procedures provided by the maker of the OS. Special optimized hardware drivers for a particular operating system, or a link to the drivers, are also available on the VL-ESU-5070 Support Page.

Physical Details

Dimensions and Mounting

The VL-ESU-5070 complies with all COM Express Extended standards which provide for specific mounting hole and stack locations as shown in the diagram below.

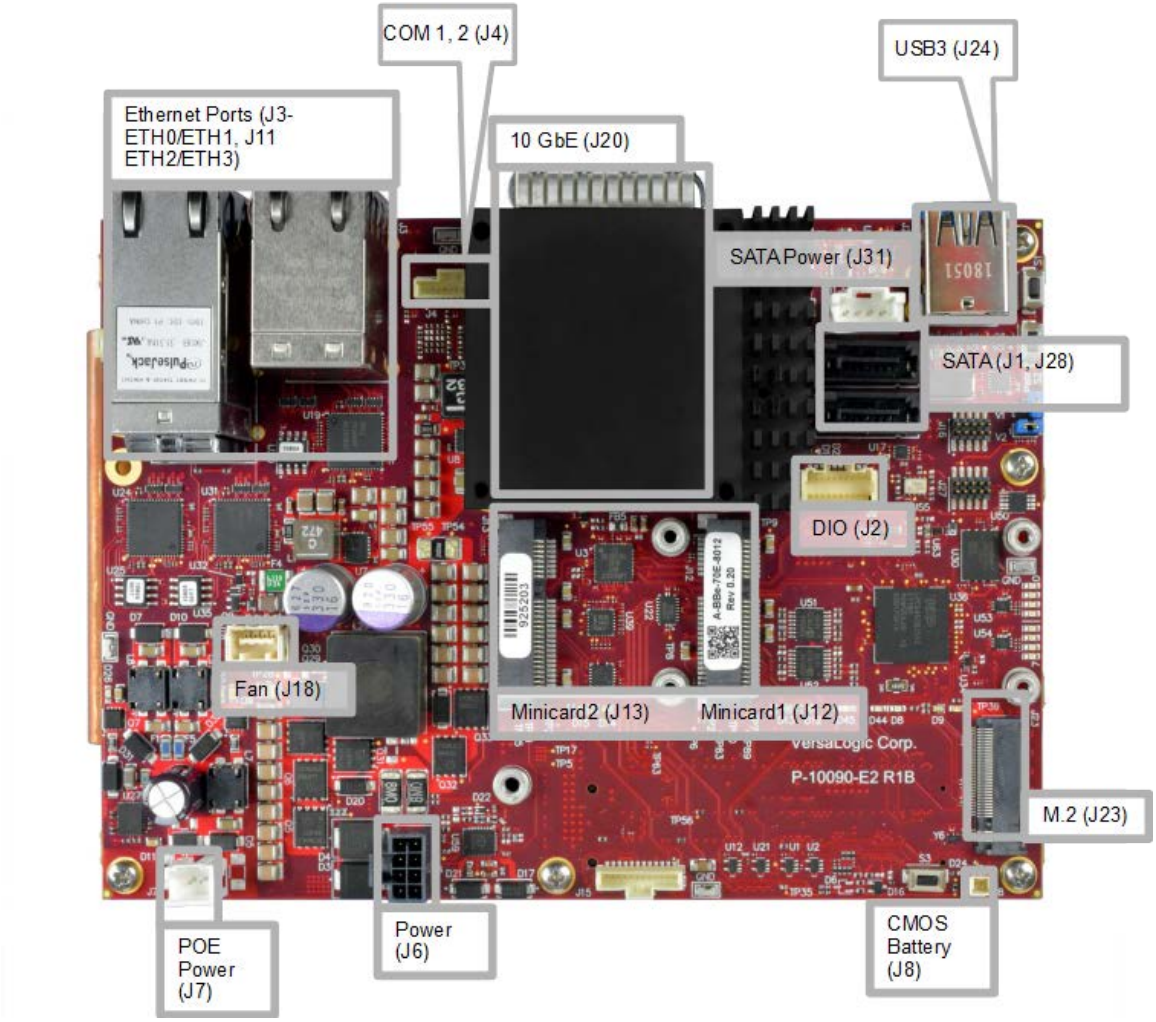
Figure 1. VL-ESU-5070 Dimensions and Mounting Holes
(Not to scale.)



External Connectors

VL-ESU-5070 Connector Locations – Top

Figure 2. VL-ESU-5070 Connector Locations – Top



ESU-5070 CONNECTOR FUNCTIONS AND INTERFACE CABLES

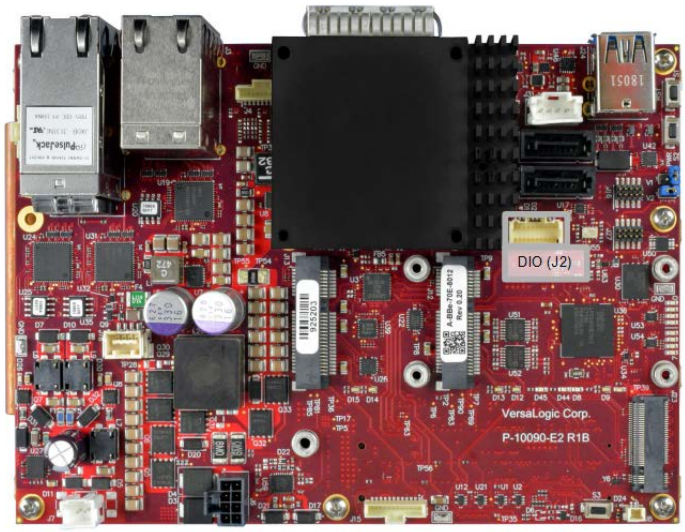
The following table notes the function of each connector, as well as mating connectors and cables, and the page where a detailed pinout or further information is available.

Table 1. Connector Functions and Interface Cables

Connector	Function	Mating Connector	Transition Cable	Cable Description
J1, J28	SATA	Molex 67800-8005	Standard - VL-CBR-0701 Latching - VL-CBR-0702	Standard SATA Cable - single latching vertical
J2	DIO	Molex 501190-2017	VL-CBR-2005	Connectors use the CBR-2004 Paddle Board
J3	RJ45 (ETH0, ETH1)	Pulse JXD9-1002NL		ETH0, ETH1 Ports uses non-PoE 2x vertical stacked magjack
J4	COM 1, 2	Molex 501331-1007	VL-CBR-1014	10-pin PicoClasp
J6	Power	Molex 105310-1208	VL-CBR-0812	2x4 vertical nanofit latching power connector
J7	PoE Power	Molex 55932-0230	VL-CBR-0206	1x2 vertical Micro-Clasp latching power connector
J8	Battery	Molex 501331-0207	VL-CBR-0203	2-pin PicoClasp
J11	RJ45 (ETH2, ETH3)	Pulse JX0B-3121NL		ETH2, ETH3 Ports uses PoE 2x vertical stacked magjack
J12	Minicard 1			Standard Minicard
J13	Minicard 2			Standard Minicard
J18	Fan	Molex 502584-0460	VL-CBR-0403	Support 3-wire or 4-wire fans (Pin 1 not used for 3-wire controlled fans since the FANCON MOSFET establishes this GND connection when the fan in on)
J20	10G SFP+ Cage and Connectors	TE Connectivity 2198230-2	N/A	Dual SFP+ Modules
J23	M.2	Amphenol MDT420M01001		Accepts an M-Key or an M+B-Key
J24	USB3	Molex 48406-0003		Right-Angle Dual-Stacked Type A USB 3.0 Connector
J31	SATA Power	Molex 53253-0470	VL- CBR-0407	A cable-adapter to 2x Molex 67582-0000 15-pin SATA power connectors

VL-CBR-2005 Connector Locations

Figure 3. VL-CBR-2005 Connectors



VL-CBR-2005 Connector Functions

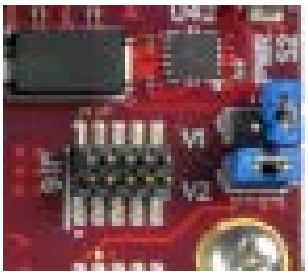
Table 2. VL-CBR-2005 Connector Functions

Connector	Function
J2	DIO

Jumper Blocks

Jumpers As-Shipped Configuration

Figure 4. Jumper Block Locations



Jumper Summary

Table 3. Jumper Summary

Jumper Block	Description
V1	Jumper used to select the back-up BIOS Not Installed – Use primary BIOS on the COM Express module (default) Installed – Use the backup BIOS on the COM Express carrier card
V2	Used to set the write-protect on the back-up BIOS flash (it currently has no function and can be in the installed or uninstalled position)

Power Supply

POWER CONNECTOR

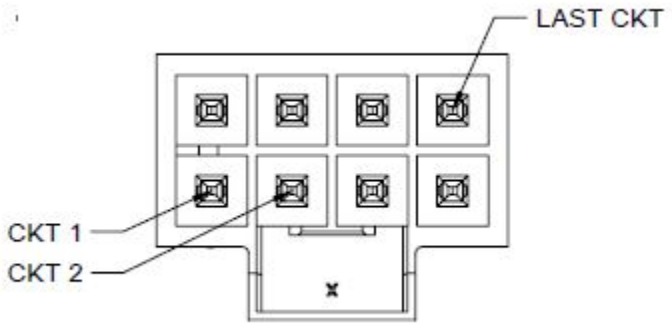
VersaLogic part number is VL-CBR-0812 adapter cable.

Warning! To prevent severe and possibly irreparable damage to the system, it is critical that the power connectors are wired correctly. Make sure to use all pins to prevent excess voltage drop.

Table 4. Main Power Connector Pinout (J6)

J6 Pins	Signal Name	Description
1,2,5,6	PWRIN_POS	Main input voltage (10V to 30V)
3,4,7,8	PWRIN_NEG	Power return

Figure 5. Power Connector Orientation and Pinout



POWER REQUIREMENTS

The input voltage range is 10V-30V. A Boost/Buck regulator is used to generate a 12V intermediate voltage used by the COM Express module and all other regulators.

POWER DELIVERY CONSIDERATIONS

The max current per pin is 6.5A. This limits the max current to 26 Amps. All power and return pins must be connected. The maximum gauge wire is 20 gauge.

CPU

Intel C3958 (16-core) server-class processor with 16 MB cache. Supports Intel 64-bit instructions, AES Instructions, Secure Key, Execute Disable Bit, Secure Boot, Virtualization Technology, and Integrated QuickAssist Technology.

Datasheet

System RAM

The VL-ESU-5070 accepts four SO-DIMM memory modules with the following characteristics:

SKU	Description
VL-MM10-8EDN	8 GB ECC SODIMM DDR4-2133, ET
VL-MM10-16EDN	16 GB ECC SODIMM DDR4-2133, ET
VL-MM10-32EDN	32 GB ECC SODIMM DDR4-2133, ET
VL-MM10-8EBN	8 GB PC4-17000 SODIMM DDR4-2133, ET
VL-MM10-16EBN	16 GB PC4-17000 SODIMM DDR4-2133, ET
VL-MM10-32EBN	32 GB PC4-17000 SODIMM DDR4-2133, ET

Note: The Intel C3958 processor supports x8 or x16 width for unbuffered memory SO-DIMM.

Microcontroller

The Microcontroller (MCU) is an NXP LPC54608 controller (Datasheet) with the following features:

- ARM Cortex-M4 processor, running at a frequency of up to 220 MHz
- The LPC5460x/61x devices operate at CPU frequencies of up to 180 MHz. The LPC54628 device operates at CPU frequencies of up to 220 MHz.
- Floating Point Unit (FPU) and Memory Protection Unit (MPU)
- ARM Cortex-M4 built-in Nested Vectored Interrupt Controller (NVIC)
- Non-maskable Interrupt (NMI) input with a selection of sources

Board Management

Board Management Controller (BMC).

- Out-of-band BMC connectivity via SFP+ 10 Gigabit Ethernet ports
- Cold system power-up without a push-button
- ESU reset, power on-off
- Monitor and log thermal protection signals
- Console UART port via an RS232 port

- Monitor major voltage rails and log out-of-bound conditions
- High reliability watchdog
- Power-up BMC self-test

Intelligent Platform Management Interface (IPMI)

The key characteristic of Intelligent Platform Management is that inventory, monitoring, logging and recovery control functions are available independent of the main processors, BIOS and operating system. Platform management functions may also be available when the system is in a powered down state.

The heart of IPMI architecture is a “microcontroller” called the Baseboard Management Controller (BMC). The BMC provides the intelligence behind Intelligent Platform Management. The BMC manages the interface between system management software and the platform management hardware, providing autonomous monitoring, event logging and recover controls.

IPMI messaging uses a request/response protocol. Access to monitor information such as temperature, voltages, and fan status is provided via the IPMI Sensor Model. Instead of providing direct access to the monitoring hardware, IPMI provides access by abstracted sensor commands, such as Get Sensor Reading, implemented via a management controller.

This same approach is applied to the generation and control of platform events. The BMC provides a centralized, non-volatile System Event Log (SEL) which has logging and control functions that helps to ensure that ‘post-mortem’ logging information is available should a failure occur that disables the system processor(s).

IPMI implementation and commands for the VL-ESU-5070 can be found in the *Remote Management User Guide*.

Expansion Busses

The following buses are found on the VL-ESU-5070.

ETHERNET

- Two SFP+ cages compatible with copper or fiber (SR and LR) 10 GbE modules. An SFP and adapter module (VL-CBR-SFPP1) is available
- Four autodetect 10BaseT/100BaseTX/1000BaseT ports (two with POE)

USB

Two USB 3.0 host ports with Type A connectors

SERIAL I/O

Two 4-wire serial ports via J4 connector.

DIGITAL I/O

Fourteen TTL I/O lines (3.3V) that are independently configurable.

GPIO lines are 3.3 V Low-voltage TTL (LVTTL) compatible DIOs capable of sourcing/sinking up to 4 mA of current. Level shifting or current limiting is necessary when connecting signals with different voltage rails. There are 51 ohm source terminators on each GPIO on board to improve signal integrity when they are used as outputs.

MINI PCIE

One full and one half-length Mini PCIe socket. Supports Wi-Fi modems, GPS receivers, non-volatile flash data storage with auto-detect mSATA support, and other plug-in modules.

M.2

M.2 M-key and B & M-key 2280 socket.

Interfaces and Connectors

Video Interfaces

A video interface is not included. A video card such as VL-MPEe-V5E minicard is suggested.

Ethernet

ETHERNET CONNECTORS

The ESU-5070 provides four on-board Intel I210-IT* Gigabit Ethernet controllers – two with Power-over-Ethernet (PoE). The standard controllers provide an Ethernet interface for 1000Base-T, 100Base-TX, and 10Base-T applications. The I210-IT Ethernet controller auto-negotiates connection speed. Drivers are available to support a variety of operating systems.

Intel Ethernet Controller I210 Datasheet

Two of the I210-IT Ethernet ports (ports 3 and 4) implement PoE PSE controllers. They support Type 1, 13W PoE.

Table 5. 1000Base-T, 100Base-TX, and 10Base-T Ethernet Connector Pinouts

J3 Upper ETH0 Pin #	Wire-Color (CAT5E)	10/100 Signals	10/100/1000 Signals
1	White/Orange	+ Auto Switch (can be either Tx or Rx)	BI_DA+
2	Orange	- Auto Switch (can be either Tx or Rx)	BI_DA-
3	White/Green	+ Auto Switch (can be either Tx or Rx)	BI_DB+
4	Blue	+ Auto Switch (can be either Tx or Rx)	BI_DC+
5	White/Blue	- Auto Switch (can be either Tx or Rx)	BI_DC-
6	Green	- Auto Switch (can be either Tx or Rx)	BI_DB-
7	White/Brown	+ Auto Switch (can be either Tx or Rx)	BI_DD+
8	Brown	- Auto Switch (can be either Tx or Rx)	BI_DD-
J3 Lower ETH1 Pin #	**Wire-Color (CAT5E)**	**10/100 Signals**	**10/100/1000 Signals**
1	White/Orange	+ Auto Switch (can be either Tx or Rx)	BI_DA+
2	Orange	- Auto Switch (can be either Tx or Rx)	BI_DA-
3	White/Green	+ Auto Switch (can be either Tx or Rx)	BI_DB+
4	Blue	+ Auto Switch (can be either Tx or Rx)	BI_DC+
5	White/Blue	- Auto Switch (can be either Tx or Rx)	BI_DC-
6	Green	- Auto Switch (can be either Tx or Rx)	BI_DB-
7	White/Brown	+ Auto Switch (can be either Tx or Rx)	BI_DD+
8	Brown	- Auto Switch (can be either Tx or Rx)	BI_DD-

ETHERNET CONNECTORS (POE)

Table 6. 1000Base-T, 100Base-TX, and 10Base-T Ethernet Connector Pinouts (PoE)

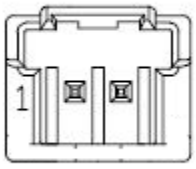
J11 Upper ETH2 Pin #	Wire-Color (CAT5E)	10/100 Signals	10/100/1000 Signals
1	White/Orange	+ Auto Switch (can be either Tx or Rx)	BI_DA+
2	Orange	- Auto Switch (can be either Tx or Rx)	BI_DA-
3	White/Green	+ Auto Switch (can be either Tx or Rx)	BI_DB+
4	Blue	+ Auto Switch (can be either Tx or Rx)	BI_DC+
5	White/Blue	- Auto Switch (can be either Tx or Rx)	BI_DC-
6	Green	- Auto Switch (can be either Tx or Rx)	BI_DB-
7	White/Brown	+ Auto Switch (can be either Tx or Rx)	BI_DD+
8	Brown	- Auto Switch (can be either Tx or Rx)	BI_DD-
J11 Lower ETH3 Pin #	**Wire-Color (CAT5E)**	**10/100 Signals**	**10/100/1000 Signals**
1	White/Orange	+ Auto Switch (can be either Tx or Rx)	BI_DA+
2	Orange	- Auto Switch (can be either Tx or Rx)	BI_DA-
3	White/Green	+ Auto Switch (can be either Tx or Rx)	BI_DB+
4	Blue	+ Auto Switch (can be either Tx or Rx)	BI_DC+
5	White/Blue	- Auto Switch (can be either Tx or Rx)	BI_DC-
6	Green	- Auto Switch (can be either Tx or Rx)	BI_DB-
7	White/Brown	+ Auto Switch (can be either Tx or Rx)	BI_DD+
8	Brown	- Auto Switch (can be either Tx or Rx)	BI_DD-

Note: PoE Power is applied to all four of the Ethernet Differential pairs.

Table 7. PoE Power Signals (J7)

Pin	Signal	Description
1	PoE Positive	PoE Positive Input Voltage: **Type 1** PoE Devices - 44V to 57V Type 2 PoE+ Devices – 50V to 57V **Note:** These are the voltage required at the connector. The lower end of these ranges must increase if there is any significant voltage drop on the power cable.
2	PoE Negative	PoE Negative Return Voltage

Figure 6. PoE Power Connector Pinout and Orientation



10GbE Ethernet

J20 cage – ports are J17 and J21

Table 8. 10 GbE Ethernet Connector Pinouts (J17, J21)

Pin	Signal	Description
1	VEET	Transmit Ground
2	TX_FAULT	Transmit Fault status signal.
3	TX_DIS	TX Disable
4	SDA	SFP I^2C data signal
5	SCL	SFP I^2C Clock data signal.
6	MOD_ABS	This is used for the SFP interrupt output.
7	RS0	Not used
8	RX_LOS	Receive loss-of-signal status
9	RS1	Not used.
10	VEER	Transmit Ground
11	VEER	Transmit Ground
12	RD-	SFP Receive data negative diff pair signal. .
13	**RD+**	SFP Receive data positive diff pair signal.
14	VEER	Transmit Ground
15	VCCR	3.3V Receiver Power
16	VCCT	3.3V Transmit Power
17	VEET	Transmit Ground
18	**TD+**	SFP Transmit data positive diff pair signal.
19	**TD-**	SFP Transmit data negative diff pair signal.
20	VEET	Transmit Ground

ETHERNET SOFTWARE DEFINED PINS (SDP)

The Intel I210-IT Gigabit Ethernet controllers have four software-defined pins (SDP pins) that can be used for IEEE1588 auxiliary device connections, enable/disable of the device, and for other miscellaneous hardware or software-control purposes. These pins can be individually configurable to act as either standard inputs, General-Purpose Interrupt (GPI) inputs or output pins

The connector (J15) is a vertical 12-pin pico-clasp connector – Molex 501331-1207. There are 6 SDP inputs. Three go to the I210-IT Ethernet controllers on the carrier board. One goes to the 1Gb Ethernet port on the COM I/F. The other two go to the first two 10G SDP pins on the COM I/F.

Serial Ports

The ESU-5070 provides two 4-wire serial interfaces (J4). They both support Legacy I/O mapped modes.

Table 9. COM Port Signals

Pin	Signal	Direction Relative to ESU-5070	Description
1	RTS1	Out	Usual signals for a COM1 port
2	TXD1	Out	
3	CTS1	In	
4	RXD1	In	
5	GND	--	Signal Ground
6	RTS2	Out	Usual signals for a COM2 port
7	TXD2	Out	
8	CTS2	In	
9	RXD2	In	
10	GND	--	Signal Ground

Note: Serial ports and one serial over LAN port can be used to install an OS without a video card if the OS supports it.

USB Interfaces

The VL-ESU-5070 supports two USB 3.0 SuperSpeed ports (J24). Two USB 3.0 SuperSpeed ports are paired with the first two USB 2.0 ports.

Table 10. USB Port Pinouts

Pin	Signal	Direction Relative to ESU-5070	Description
1	+5V	Out	VBUS Voltage (max 900mA)
2	**USB-**	I/O	USB 2.0 Diff pair negative
3	**USB+**	I/O	USB 2.0 Diff pair positive
4	Signal Ground	--	
5	**SSR-**	In	USB 3.0 Negative Rx Diff Pair
6	**SSR+**	In	USB 3.0 Positive Rx Diff Pair
7	Signal Ground	--	Called Ground-Drain in spec
8	**SST-**	Out	USB 3.0 Negative Tx Diff Pair
9	**SST+**	Out	USB 3.0 Positive Tx Diff Pair
10	+5V	Out	VBUS Voltage (max 900mA)
11	**USB-**	I/O	USB 2.0 Diff pair negative
12	**USB+**	I/O	USB 2.0 Diff pair positive
13	Signal Ground	--	
14	**SSR-**	In	USB 3.0 Negative Rx Diff Pair
15	**SSR+**	In	USB 3.0 Positive Rx Diff Pair
16	Signal Ground	--	Called Ground-Drain in spec
17	**SST-**	Out	USB 3.0 Negative Tx Diff Pair
18	**SST+**	Out	USB 3.0 Positive Tx Diff Pair

Mini PCIe Cards

Two minicards are supported. Minicard #1 (J12) is full-size and will support either a PCIe Minicard or an mSATA module. Minicard #2 (J13) is half-size and supports PCIe. Both minicards also support USB and SMBus interfaces.

Table 11. PCIe Full-Size Minicard #1 Pinouts (J12)

Pin	mSATA Signal	PCIe Minicard Signal	Pin	mSATA Signal	PCIe Minicard Signal
1	Reserved (NC)	WAKE#	2	+3.3V	+3.3V
3	Reserved (NC)	COEX1	4	GND	GND
5	Reserved (NC)	COEX2	6	+1.5V	+1.5V
7	Reserved (NC)	CLKREQ#	8	Reserved (NC)	UIM_PWR
9	GND	GND	10	Reserved (NC)	UIM_DATA
11	Reserved (NC)	REFCLK_N	12	Reserved (NC)	UIM_CLK
13	Reserved (NC)	REFCLK_P	14	Reserved (NC)	UIM_RESET
15	GND	GND	16	Reserved (NC)	UIM_SPU
17	Reserved (NC)	UIM_IC_DM	18	GND	GND
19	Reserved (NC)	UIM_IC_DP	20	Reserved (NC)	W_DISABLE1#
21	GND	GND	22	Reserved (NC)	PERST#
23	SATA_RX_**P**	PER0_**N**	24	+3.3V	+3.3V
25	SATA_RX_**N**	PER0_**P**	26	GND	GND
27	GND	GND	28	+1.5V	+1.5V
29	GND	GND	30	SMB_CLK	SMB_CLK
31	SATA_TX_N	PET0_N	32	SMB_DATA	SMB_DATA
33	SATA_TX_P	PET0_P	34	GND	GND
35	GND	GND	36	Reserved (NC)	USB_N
37	GND	GND	38	Reserved (NC)	USB_P
39	+3.3V	+3.3Vaux	40	GND	GND
41	+3.3V	+3.3Vaux	42	Reserved (NC)	LED_WWAN#
43	No Connect (some GND)	GND	44	Reserved (NC)	LED_WLAN#
45	Vendor Specific	Reserved	46	Reserved (NC)	LED_WPAN#
47	Vendor Specific	Reserved	48	+1.5V	+1.5V
49	DAS/DSS (or NC)	Reserved	50	GND	GND
51	Presence Detect (on NC)	W_DISABLE2#	52	+3.3V	+3.3V

Table 12. PCIe Half-Size Minicard #2 Pinouts (J13)

Pin	PCIe Minicard Signal	Pin	PCIe Minicard Signal
1	WAKE#	2	+3.3V
3	COEX1	4	GND
5	COEX2	6	+1.5V
7	CLKREQ#	8	UIM_PWR
9	GND	10	UIM_DATA
11	REFCLK_N	12	UIM_CLK
13	REFCLK_P	14	UIM_RESET
15	GND	16	UIM_SPU
17	UIM_IC_DM	18	GND
19	UIM_IC_DP	20	W_DISABLE1#
21	GND	22	PERST#
23	PER0_N	24	+3.3V
25	PER0_P	26	GND
27	GND	28	+1.5V
29	GND	30	SMB_CLK
31	PET0_N	32	SMB_DATA
33	PET0_P	34	GND
35	GND	36	USB_N
37	GND	38	USB_P
39	+3.3Vaux	40	GND
41	+3.3Vaux	42	LED_WWAN#
43	GND	44	LED_WLAN#
45	Reserved	46	LED_WPAN#
47	Reserved	48	+1.5V
49	Reserved	50	GND
51	Reserved	52	+3.3V

MINICARD LEDS

There are three LED outputs: WWAN, WLAN and WPAN. A fourth LED used to indicate when the Minicard is being powered (since the minicard power can be configured to either be always-on or on in S0). This power indicator is important as a warning to **Not** hot-plug the minicard.

Table 13. Minicard #1 and #2 LED Indicators

LED	Ref Des	State	Description
Green (WWAN)	**D12** (#1) **D14** (#2)	On	WWAN active
		Off	WWAN inactive
Yellow (WLAN)	**D12** (#1) **D14** (#2)	On	WLAN active
		Off	WLAN inactive
Green (WPAN)	**D13** (#1) **D15** (#2)	On	WPAN active
		Off	WPAN inactive
Yellow (Power On)	**D13** (#1) **D15** (#2)	On	Minicard Power is On
		Off	Minicard Power is Off

M.2

An M.2 M-Key 2280 socket is included that supports 4x PCIe Gen3 interfaces (x1 SATA M-Key modules are not supported). M-Key M.2 modules are commonly used for NVME Solid State Drives (SSD). B & M M.2 modules which support 2x PCIe Gen3 interfaces are also supported.

Notes:

1. M.2 modules are sold separately.
2. A heat-sink is required in rugged environments or where the ambient temperature is 85° C or greater.

Table 14. M.2 Pinouts (J23)

Pin	(x4 PCIE) on M-Key	(x2 PCIE) on M+B-Key	Pin	(x4 PCIE) on M-Key	(x2 PCIE) on M+B-Key
1	GND	GND	2	+3.3V	+3.3V
3	GND	GND	4	+3.3V	+3.3V
5	**PER3_N**	Reserved (NC)	6	Reserved (NC)	Reserved (NC)
7	**PER3_P**	Reserved (NC)	8	Reserved (NC)	Reserved (NC)
9	GND	GND	10	**DAS_LED#**	**DAS_LED#**
11	**PET3_N**	GND or NC	12	+3.3V or B-key	B-Key
13	**PET3_P**	B-Key	14	+3.3V or B-key	B-Key
15	GND	B-Key	16	+3.3V or B-key	B-Key
17	**PER2_N**	B-Key	18	+3.3V or B-key	B-Key
19	**PER2_P**	B-Key	20	Reserved (NC)	Reserved (NC)
21	GND	GND	22	Reserved (NC)	Reserved (NC)
23	**PET2_N**	Reserved (NC)	24	Reserved (NC)	Reserved (NC)
25	**PET2_P**	Reserved (NC)	26	Reserved (NC)	Reserved (NC)

Pin	(x4 PCIE) on M-Key	(x2 PCIE) on M+B-Key	Pin	(x4 PCIE) on M-Key	(x2 PCIE) on M+B-Key
27	GND	GND	28	Reserved (NC)	Reserved (NC)
29	**PER1_N**	**PER1_N**	30	Reserved (NC)	Reserved (NC)
31	**PER1_P**	**PER1_P**	32	Reserved (NC)	Reserved (NC)
33	GND	GND	34	Reserved (NC)	Reserved (NC)
35	**PET1_N**	**PET1_N**	36	Reserved (NC)	Reserved (NC)
37	**PET1_P**	**PET1_P**	38	**DEVSLP#** [1]	**DEVSLP#**
39	GND	GND	40	Reserved (NC)	Reserved (NC)
41	**PER0_N**	**PER0_N**	42	Reserved (NC)	Reserved (NC)
43	**PER0_P**	**PER0_P**	44	Reserved (NC)	Reserved (NC)
45	GND	GND	46	Reserved (NC)	Reserved (NC)
47	**PET0_N**	**PET0_N**	48	Reserved (NC)	Reserved (NC)
49	**PET0_P**	**PET0_P**	50	**PERST#**	**PERST#**
51	GND	GND	52	**CLKREQ#**	**CLKREQ#**
53	**REFCLK_N** [2]	**REFCLK_N**	54	**PEWAKE#** [3]	**PEWAKE#**
55	**REFCLK_P**	**REFCLK_P**	56	Reserved (NC)	Reserved (NC)
57	GND	GND	58	Reserved (NC)	Reserved (NC)
59	M-Key	M-Key	60	M-Key	M-Key
61	M-Key	M-Key	62	M-Key	M-Key
63	M-Key	M-Key	64	M-Key	M-Key
65	M-Key	M-Key	66	M-Key	M-Key
67	Reserved (NC)		68	**SUSCLK** [4]	**SUSCLK**
69	**PEDET** [5]	**PEDET**	70	+3.3V	+3.3V
71	GND	GND	72	+3.3V	+3.3V
73	GND	GND	74	+3.3V	+3.3V
75	GND	GND			

Notes:

+3.3V Power to the M.2 modules is always on. Turning power off in sleep modes is currently not supported and power reduction modes via host software should be used.

3. This signal is an input to the M.2 that can be used to reduce power in sleep modes. Since there are host software methods to do this, the signal is currently not supported.
4. This is a 100Mhz PCIe reference clock input to the M.2. It is turned off in processor sleep modes.
5. Some M.2 modules have wake-up support. Since the primary use of the M.2 slot is for solid state drives, it is not currently supported.
6. This is a 32.768Khz clock input to the M.2
7. This signal is used to determine if the M.2 is either a 4x PCIe or 1x SATA module. 1x SATA modules are not supported, so this signal is not used.

M.2 STATUS LEDS

Table 15. On-board M.2 Status LEDs

LED	Ref Des	State	Description
Blue (DAS)	D45	On	M.2 Plugged In (blink with activity)
		Off	M.2 not plugged in if always off or the M.2 doesn't support the DAS LED.
Yellow (Power On)	D46	On	M.2 Power is On

SATA Ports

The ESU-5070 supports two SATA 3.0 ports (J1 and J28) which use an on-board SATA vertical latching connector.

Table 16. SATA Pinouts (J1 and J28)

Pin	Signal
1	Signal Ground
2	SATA_TX_P
3	SATA_TX_N
4	Signal Ground
5	SATA_RX_N
6	SATA_RX_P
7	Signal Ground

If using Solid State Drives (SSD) (not disk drives) power is provided by the SATA power connector J31 to two SSD drives. The combined 5V current for both SATA drives is 1.1 Amps sustained with a peak power of 1.6 Amps. This should be adequate for 2.5" SSDs but always check the power requirements for the specific SSD drive being used.

At around 1.8A an electronic power switch will current-limit and disconnect power. The power will not come back on until the ESU-5070 is powered off. Power to the drives will go off when the host processor goes into a sleep mode such as S4 or S5 (SATA interfaces are not active in any sleep modes).

Table 17. SATA Power Signals (J31)

Pin	Signal	Description
1	+5V	5V SATA drive #1 power
2	GND	Ground Return for SATA drive #1 power
3	+5V	5V SATA drive #2 power
4	GND	Ground Return for SATA drive #2 power

SATA AND SFP STATUS LEDS (J5)

Note: LED outputs are not 5V compatible.

Table 18. SATA and SFP Status LEDS

Pin	Signal	Description
1	V3P3_LED1_RES	High Side power for SFP0_LINKSPEED_MAX_LED# LED cathode.
2	SFP0_LINKSPEED_MAX_LED#	Link Speed for SFP Port 0.
3	V3P3_LED2_RES	High Side power for SFP0_STATUS_ACT_LED# LED cathode
4	SFP0_STATUS_ACT_LED#	Status/Activity for SFP Port 0.
5	V3P3_LED3_RES	High Side power for SFP1_LINKSPEED_MAX_LED# LED cathode.
6	SFP1_LINKSPEED_MAX_LED#	Link Speed for SFP Port 1.
7	V3P3_LED4_RES	High Side power for SFP1_STATUS_ACT_LED# LED cathode
8	SFP1_STATUS_ACT_LED#	Status/Activity for SFP Port 1.
9	V3P3_LED5_RES	High Side power for LED_SATA# LED cathode.
10	LED_SATA#	Activity for SATA ports. It is intended to connect to the anode of an LED and will blink when there is SATA activity. There is also an on-board LED D8 used for this SATA activity. As a minimum this will correspond to the activity of the two on-board SATA ports J1, J28 but the MCU may also drive them based on the status of the mSATA module if installed.

CBR-2005 Paddleboard

To access the digital I/O lines on the ESU-5070 board, a paddleboard and 12-inch cable are available from VersaLogic, part number VL-CBR-2005.

CBR-2005 Connectors

The figure below shows the location and pin orientation of the connectors on the CBR-2005 paddleboard.

Figure 7. J4/J3/J2/J1 Digital I/O Terminal Block Pinouts

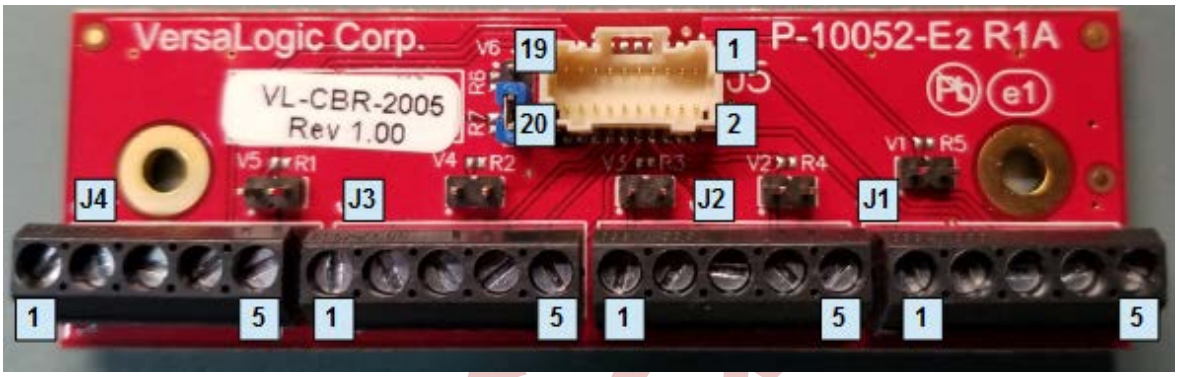


Table 19. ESU-5070 J21 and CBR-2005 J5 Connector Pinout

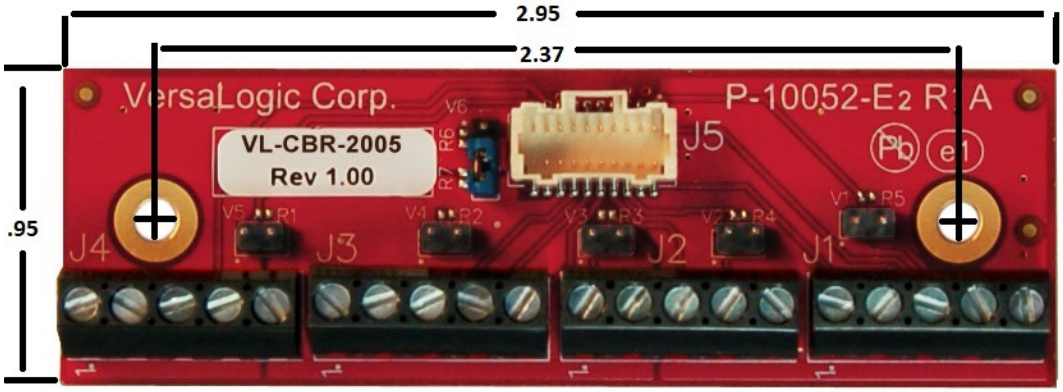
Pin on CBR-2005 Paddleboard End (J5)	Terminal Block	Terminal Block pin	Signal	Pin on ESU-5070 End (J2)
1	J1	5	DIO1	1
3		4	DIO2	2
2		3	DIO3	3
5		1	DIO4	4
4		2	DGND	5
7	J2	5	DIO5	6
6		4	DIO6	7
9		2	DIO7	8
11		1	DIO8	9
8		3	DGND	10
10	J3	5	DIO9	11
13		3	DIO10/TIMER1_OUT	12
15		2	DIO11/ TIMER1_IN	13
14		1	DIO12/ TIMER0_OUT	14
12		4	DGND	15

Pin on CBR-2005 Paddleboard End (J5)	Terminal Block	Terminal Block pin	Signal	Pin on ESU-5070 End (J2)
17	J4	4	DIO13/TIMER0_IN	16
18		3	DIO14	17
19		2	RST_BTN#	18
20		1	PWR_BTN#	19
16		5	DGND	20

Note: RST_BTN# and PWR_BTN# signals: The reset push-button input (RST_BTN#) and power push-button input (PWR_BTN#) are intended to be driven by 3.3V open-collector drivers or switches. They are ESD protected by TVS devices and there are switch debouncers on-board.

Dimensions and Mounting Holes

Figure 8. CBR-2005 Dimensions and Mounting Holes



Thermal Characterization

Selecting the Correct Thermal Solution for Your Application

This chapter discusses the following topics related to thermal issues:

- Selecting the correct thermal solution for your application
- VL-ESU-5070 thermal characterization
- Installing the active heat-sink and fan (HDW-421), and the heat-pipe block (HDW-422) thermal solutions available from VersaLogic

Selecting the Correct Thermal Solution for Your Application

This section provides guidelines for the overall system thermal engineering effort.

HEAT-PLATE

The heat-plate supplied with the VL-ESU-5070 is the basis of the thermal solution. The heat-plate draws heat away from the CPU chip as well as other critical components. Some components rely on the ambient air temperature at or below the maximum specified 85 ºC temperature.

The design of the heat-plate assumes that the user's thermal solution will maintain the top surface of the heat-plate at 80 ºC or less. If that temperature threshold is maintained, the CPU will remain safely within its operating temperature limits.

CAUTION:

By itself, the heat-plate is not a complete thermal solution. Integrators should either implement a thermal solution using the accessories available from VersaLogic or develop their own thermal solution that attaches to the heat-plate, suitable for environments in which the ESU-5070 will be used. As stated above, the thermal solution must be capable of keeping the top surface of the heat place at or below 80 ºC and the air surrounding the components in the assembly at or below 85 ºC.

The heat-plate is permanently affixed to the ESU-5070 and must not be removed. Removal of the heat-plate voids the product warranty. Attempting to operate the Raven without the heat-plate voids the product warranty and can damage the CPU.

SYSTEM-LEVEL CONSIDERATIONS

The ESU-5070 is often mounted directly to another thermally controlled surface via its heat-plate (that is, the inside surface of an enclosure). In this case, the user needs to maintain the heat-plate at or below 80 ºC by controlling the mounting surface temperature. The ESU-5070 thermal solutions available from VersaLogic – the HDW-421 heat-sink and fan or the HDW-422 heat-pipe block – can be used in the user's final system or only used during product development as a temporary bench-top solution. The operating temperature range of the HDW-421 heatsink and fan is -40° C to 70° C. The range for the HDW-422 heat-pipe block extends beyond 70° C.

The ambient air surrounding the ESU-5070 needs to be maintained at 85 ºC or below. This may prove to be challenging depending on how and where the SBC is mounted in the end user system.

The decision of which thermal solution to use relies on several factors including:

- Number of CPU cores on the SBC
- CPU and video processing utilization by the user application
- Temperature range within which the ESU-5070 will be operated
- Air movement (or lack of air movement)

Most of these factors involve the demands of the user application on the ESU-5070 and cannot be isolated from the overall thermal performance. Due to the interaction of the user application, the ESU-5070 thermal solution, and the overall environment of the end system, thermal performance cannot be rigidly defined.

The ambient air surrounding the ESU-5070 needs to be maintained at 85 ºC or below. This would include the space between the two main boards as well as the space beneath an installed Mini PCIe expansion board. Standard methods for addressing this requirement include the following:

- Provide a typical airflow of 100 linear feet per minute (LFM) / 0.5 linear meters per second.
- Position the ESU-5070 board to allow for convective airflow
- Lower the system level temperature requirement as needed

CPU THERMAL TRIP POINTS

The CPU cores in the ESU-5070 have their own thermal sensors. Coupled with these sensors are specific reactions to three thermal trip points. The table below describes the three thermal trip points. Note that these are internal temperatures that are about 10 ºC above the heat-plate temperature.

Table 20. CPU Thermal Trip Points

Trip Point	Description
Passive (Note 1)	At this temperature, the CPU cores throttle back to a lower speed. This reduces the power draw and heat dissipation, but lowers the processing speed.
Critical (Note 2)	At this temperature, the operating system typically puts the board into a sleep or other low-power state.
Maximum core temperature	The CPU turns itself off when this temperature is reached. This is a fixed trip point and cannot be adjusted.

Notes:

1. The default value in the BIOS Setup utility for this trip point is 80 ºC.
2. The default value in the BIOS Setup utility for this trip point is 100 ºC.

These trip points allow maximum CPU operational performance while maintaining the lowest CPU temperature possible. The long-term reliability of any electronic component degrades when it is continually run near its maximum thermal limit. Ideally, the CPU core temperatures will be kept well below 100 ºC with only brief excursions above.

THERMAL SPECIFICATIONS, RESTRICTIONS, AND CONDITIONS

Due to the unknown nature of the entire thermal system, or the performance requirement of the application, VersaLogic cannot recommend a particular thermal solution. This information is intended to provide guidance in the design of an overall thermal system solution.

Table 21. Absolute Minimum and Maximum Air Temperatures

Board	With Heat-plate	With Heat-sink and Fan (HDW-421)	Heat-pipe Adapter Plate (HDW-422)
VL-ESU-5070-ECP	-40 ° to +85 °C	-40 ° to +70 °C	-40 ° to +85 °C

OVERALL RESTRICTIONS AND CONDITIONS:

- Ranges shown assume less than 90% CPU utilization.
- Keep the maximum CPU core temperature below 100ºC.
- The ambient air surrounding the ESU-5070 needs to be maintained at 85 ºC or below. This includes the space between the two main boards as well as the space beneath an installed Mini PCIe expansion board. A recommended overall airflow of 100 linear feet per minute (LFM) / 0.5 linear meters per second (LMS) addresses this requirement. If this air flow is not provided, other means must be implemented to keep the adjacent air at 85 ºC or below.

HEAT-PLATE ONLY RESTRICTIONS AND CONDITIONS:

The heat-plate must be kept below 80 °C. This applies to a heat-plate mounted directly to another surface as well as when the HDW-422 heat-pipe block is used.

HEAT-SINK WITH FAN CONSIDERATIONS:

The heat-sink and fan combination cools the CPU when it is running in up to 70° C commercial environments, or when the application software is heavily utilizing the CPU or video circuitry. The fan assists in cooling the heat-sink and provides additional air movement within the system.

HEAT-PIPE CONSIDERATIONS:

The heat-pipe cools the CPU when it is running in industrial environments operating up to 85° C, or when the application software is heavily utilizing the CPU or video circuitry. The heat-pipe cools the heat-plate and moves the heat away from the system.

Thermal Characterization

Table 22. Product Thermal Testing Setup

Test Platform:	ESU-5070, aka Grizzly
Input Power:	30V
BIOS:	r11.006
BIOS Settings:	Default
Heat-sink Configuration 1:	HDW-421 fan sink
Heat-sink Configuration 2:	HDW-422 heat-pipe externally to powered external fan sink
Hardware Configuration:	4x MM10-32EDN, 2x POE network, 2x network, 2x SFP+ RJ45, 1x USB3.0 loopback, MPEe-V5E, 1x MPEe-W2E, 1x M.2, 2x SATA HDD (6Gb/s)
Memory:	Smart STI4097SO420893-SM 32GB
M.2 Module:	Viking VPFNP5240G5I5WT3 240GB with passive heat-sink
SFP+ Module:	10Gtek ASF-10G-T, RJ45
Software:	Windows 10 v1607, b14393.0; Passmark BurnIn Test v9.0 Pro

TEST RESULTS

The test results reflect the test environment within the temperature chamber used. The airflow of this particular chamber is about 0.5 linear meters per second (~100 linear feet per minute). Thermal performance improves by increasing the airflow beyond 0.5 linear meters per second.

The system power dissipation is primarily dependent on the application program; that is, its use of computing or I/O resources. The stress levels used in this testing are at the top of the range of a typical user's needs.

Table 23. Heat-sink Configuration 1

Ambient Temp (°C)	Average Core Temp (°C)	Speed (MHz)	Throttle	Power (W)
25	39	2000	No	59
70	81	2000	No	67

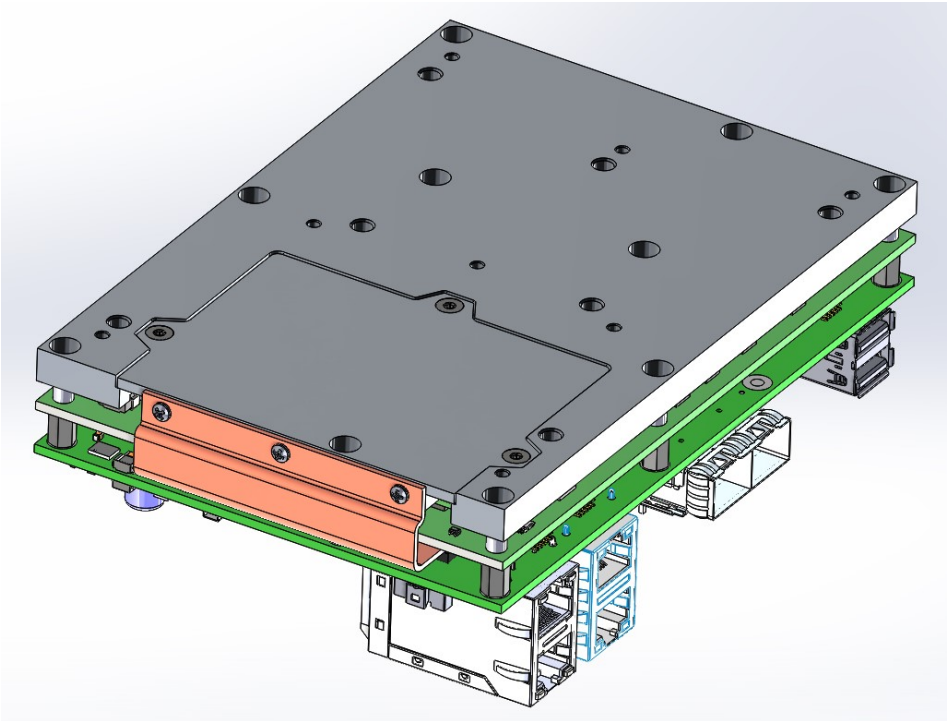
Table 24. Heat-sink Configuration 2

Ambient Temp (°C)	Average Core Temp (°C)	Speed (MHz)	Throttle	Power (W)
85	79	2000	No	59
90	81	2000	No	60

Installing ESU-5070 Thermal Solutions

The ESU-5070 is shipped with a heat spreader attached as shown here:

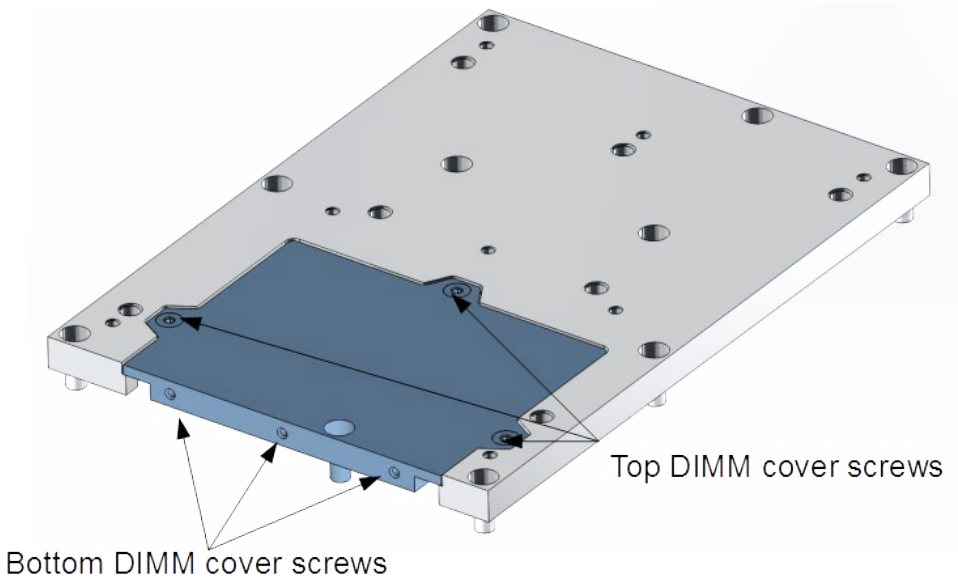
Figure 9. ESU-5070 Heat Spreader



The heat spreader serves to thermally couple ESU-5070 heat loads to various application cooling solutions described throughout this section.

Memory modules can be accessed through this plate by removing the top DIMM cover by removing screws in the following locations:

Figure 10. Removing the ESU-5070 Top DIMM Cover



Note: When installing additional memory in the customer accessible SODIMM slots, it is advisable to use a Thermal Interface Material (TIM) so that any heat from the SODIMM modules may be conducted to the Grizzly heat plate. The following is the specification of the recommended material.

- Thermal Conductivity:7.5 W/mK or better
- Hardness: 22 (Shore 00) or lower
- Volume Resistivity: 8.73 x 10^13 ohm-cm or higher
- Initial Thickness: 0.5mm
- Cut size: Upper module – 60mm x 20mm, Lower module 60mm x 10mm

Material used in production units: Laird TFLEX 90000 series.

If the SODIMM are replaced at some future date, it is also recommended to discard the old TIM pieces and to replace with new material.

INSTALLING THE HDW-421 HEAT-SINK AND FAN

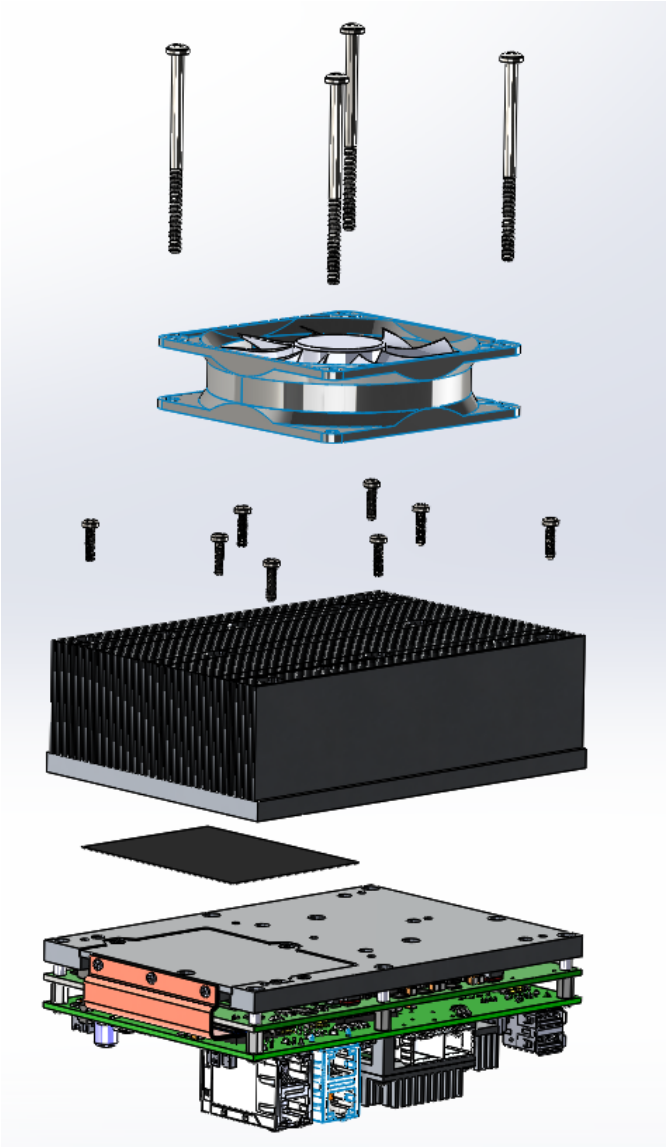
An optional heat-sink and fan assembly is available for the ESU-5070. This solution is designed for operating environments up 70° C.

Fans screws should be torqued to four inch pounds.

Skived heatsinks provide an extremely high fin to-gap aspect ratio for improved thermal performance in a forced airflow environment. The process for creating skived heatsinks by slicing and standing the fins up on end will cause some variation in fin spacing. Also, the fins will have a curved appearance. This will not impact performance.

Note: HDW-421 is intended for development use only – not for production environments.

Figure 11. HDW-421 – Installing the Fan-Sink Thermal Accessory (Bottom)



Errata Note: The following mounting screw and heat-plate mounting hole currently do not match.

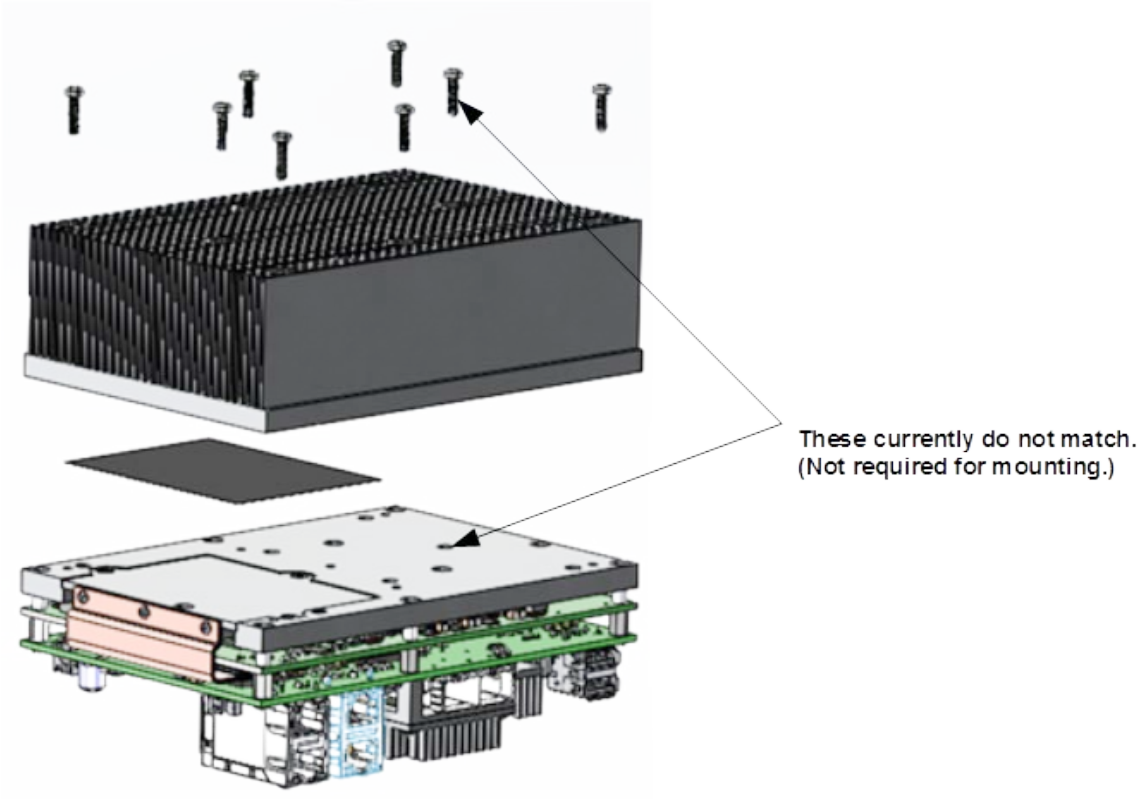
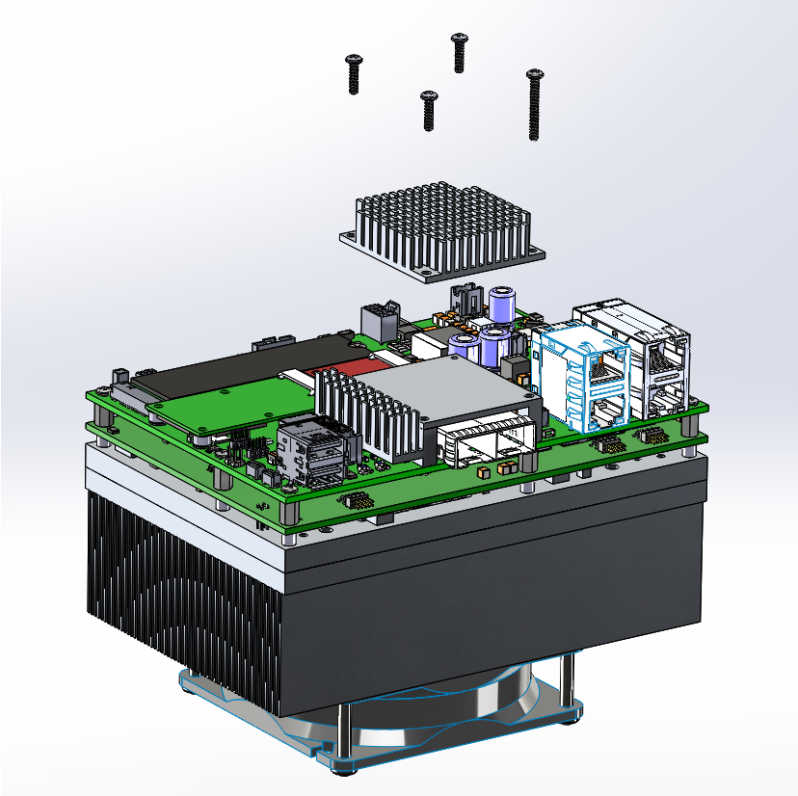
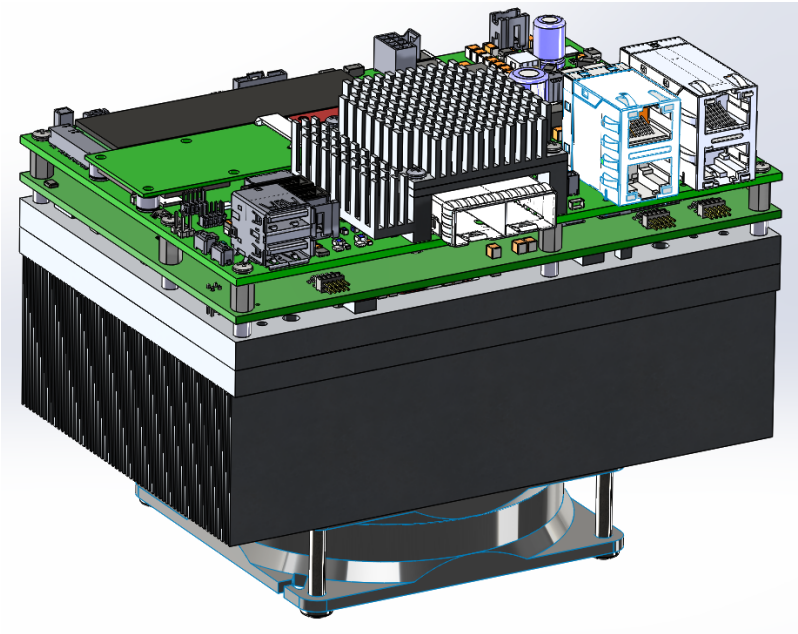


Figure 12. HDW-421 – Installing the Fan-Sink Thermal Accessory (Top)



Apply thermal compound to the SFP and heat-plate prior to attaching the heat-sink.

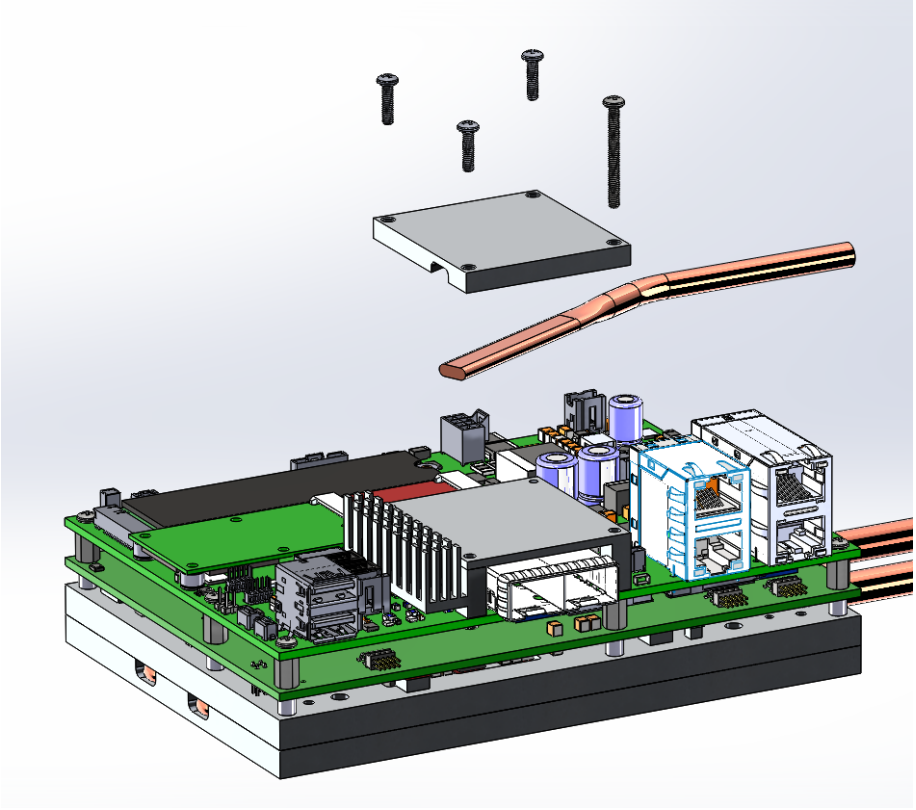
Figure 13. HDW-422 – Installed Fan Heat-sink Thermal Accessory



INSTALLING THE HDW-422 HEAT-PIPE THERMAL ASSEMBLY

The heat-pipe cools the CPU when it is running in industrial environments operating up to 85° C, or when the application software is heavily utilizing the CPU or video circuitry. The heat-pipe cools the heat-plate and moves the heat away from the system. The heat-pipes need to be connected chilled air to maintain 80° C on heat-plate.

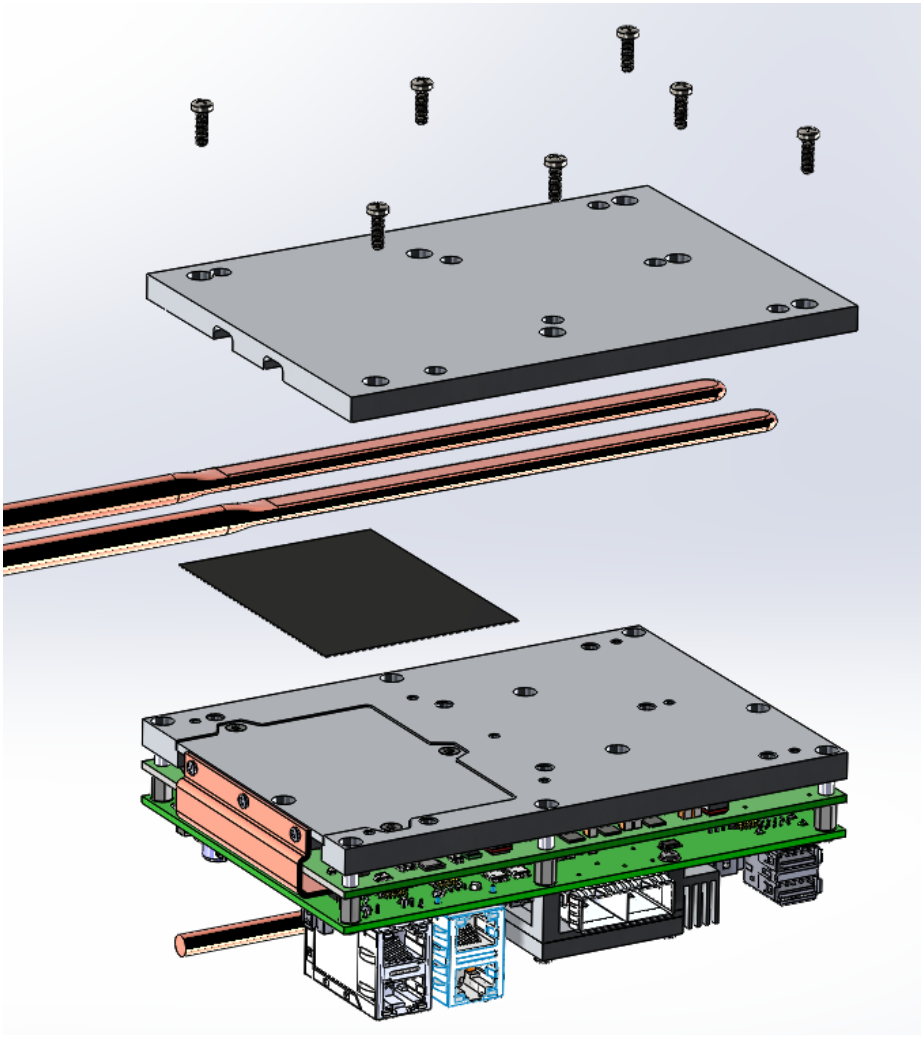
Figure 14. Installing the HDW-422 Heat-pipe Thermal Assembly (Top)



NOTES:

1. Remove screws as shipped on the SFP cage and replace as shown above
2. The heat-pipe will be supplied by the customer and is 6mm in diameter

Figure 15. Installing the HDW-422 Heat-pipe Thermal Assembly (Bottom)



Note: As shown above, HI-TP26 is placed over the DIMM cover. Thermal compound is used elsewhere on the heat-plate.

Figure 16. HDW-422 – Installed Heat-pipe Thermal Accessory