Product Specifications		
PART NO.:	VL33A1G63A-N6/M4/K2SD	REV: 0.03 PRELIMINARY

General Information

8GB 1Gx72 DDR4 SDRAM ECC REGISTERED RDIMM 288-PIN

Description

The VL33A1G63A is a 1Gx72 DDR4 SDRAM high density RDIMM. This dual rank memory module consists of eighteen CMOS 512Mx8 bits with 16 internal banks DDR4 Synchronous DRAMs in BGA packages, a 32-bit registered buffer/PLL clock in BGA package, and a 4K EEPROM in an 8-pin MLF package. This module is a 288-pin registered dual in-line memory module and is intended for mounting into an edge connector socket. Decoupling capacitors are mounted on the printed circuit board for each DDR4 SDRAM.

Features

- 288-pin, registered dual in-line memory module (RDIMM)
- Supports ECC error detection and correction
- Fast data transfer rate: PC4-17100, PC4-14900, PC4-12800
- VDD = VDDQ = 1.2V +/-0.060V
- VPP = 2.5V +/-0.125V
- VDDSPD = 3.0V to 3.6V
- 16 internal banks; 4 groups of 4 banks each
- Nominal and dynamic on-die termination (ODT)
- Low-power auto self refresh
- Programmable CAS# latency:
  15 (DDR4-2133), 13 (DDR4-1866), 11 (DDR4-1600)
- Programmable burst length (8)
- Asynchronous reset
- On-die VREFDQ generation and calibration
- Fly-by topology
- On board terminated command, address, and control bus
- Serial presence detect (SPD) EEPROM with thermal sensor
- Thermal sensor range: -40°C to +125°C (Max +/-3% accuracy)
- Lead-free, RoHS compliant
- JEDEC pinout
- Gold edge contacts
- PCB: Height 31.25mm (1.230"), double sided component
- Operating temperature (TOPER): - Commercial (0°C <= Tc <= 95°C)
  - Industrial (-40°C <= Tc <= 95°C)

Notes: Double refresh rate is required when 85°C < TOPER <= 95°C.
TOPER is DRAM case temperature (Tc).

Order Information:

VL33A1G63A - N6 S D - X

- X: OPERATING TEMPERATURE
  None: Commercial
  S1: Industrial screening
- D: DRAM DIE: D
- S: DRAM MANUFACTURER
  S - SAMSUNG
- N6: MODULE SPEED
  N6: PC4-17100 @ CL15
  M4: PC4-14900 @ CL13
  K2: PC4-12800 @ CL11
- VL: Lead-free/RoHS

DRAM component: K4A4G085WD-BCPB

Pin Description

Pin Name	Function
A0~A15	Address Inputs
A10/AP	Address Input/ Autoprecharge
A12/BC#	Address Input/ Burst Chop
ACT#	Activate input
RAS#/A16	Row Address Strobes/ Address Input
CAS#/A15	Column Address Strobes/ Address Input
WE#/A14	Write Enable/Address Input
BA0~BA1	Bank Address Inputs
BG0~BG1	Bank group address inputs
DQ0~DQ63	Data Input/Output
DQS0~DQS8	Data Strobes
DQS0#~DQS8#	Data Strobes Complement
TDQS9~TDQS17	Termination Data Strobes
TDQS9~DQS17#	Termination Data Strobes Complement
CB0~CB7	Data Check Bits I/O
PAR_IN	Parity Input
ALERT#	Alert output
CK0, CK0#	Clock Input
ODT0, ODT1	On-die Termination Control
CKE0, CKE1	Clock Enables
CS0#, CS1#	Chip Selects
RESET#	Register and SDRAM Control
VDD	Voltage Supply
VPP	DRAM Activating Voltage Supply
VSS	Ground
SA0~SA2	SPD Address
SDA	SPD Data Input/Output
SCL	SPD Clock Input
EVENT#	Temperature Event Output
VREFCA	Reference Voltage for CA
VDDSPD	SPD Voltage Supply
VTT	Termination Voltage
NC	No Connect

Pin Configuration

288-PIN DDR4 RDIMM FRONT SIDE

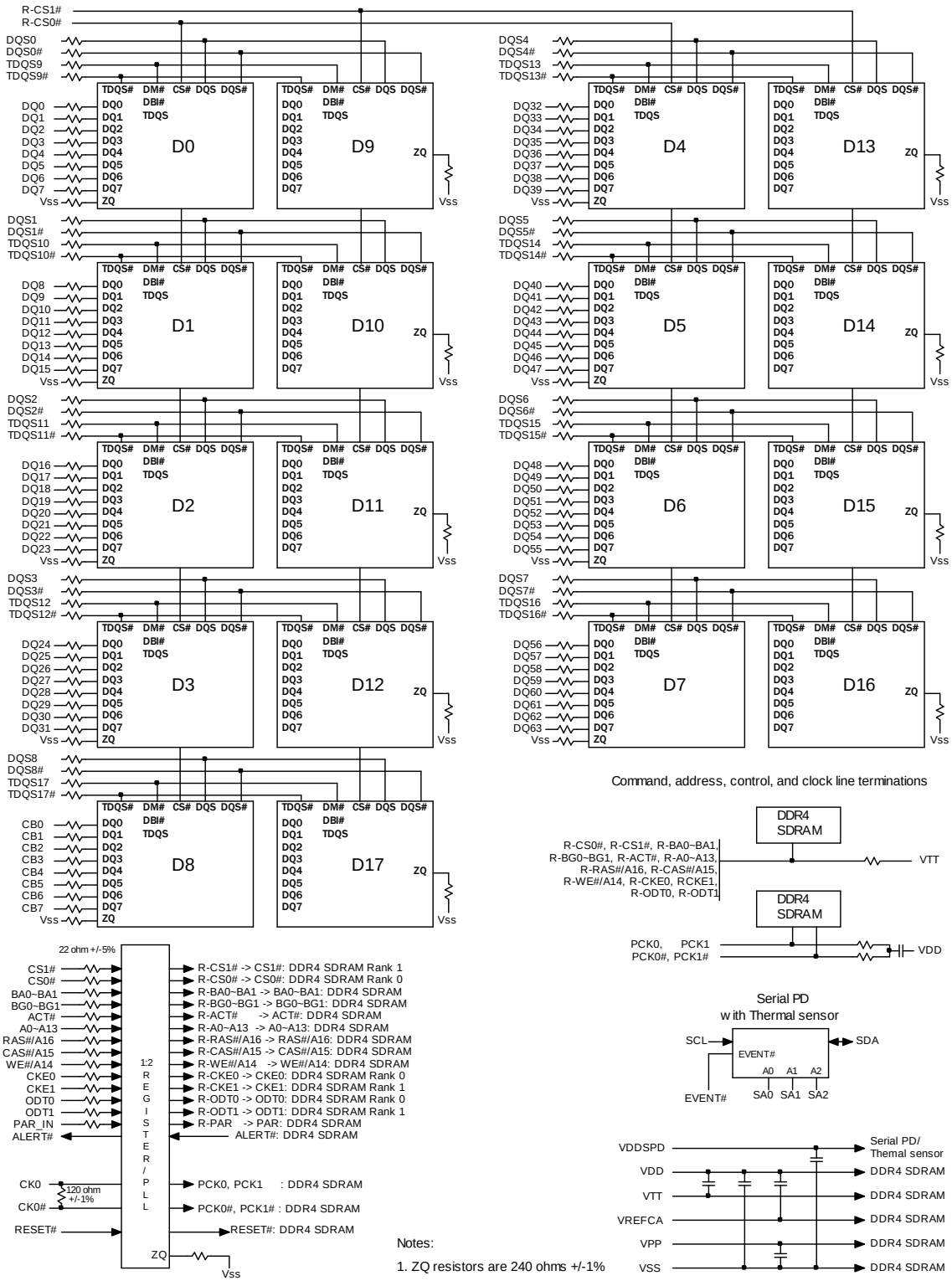
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	12V, NC*	37	VSS	73	VDD	109	VSS
2	VSS	38	DQ24	74	CK0	110	TDQS14
3	DQ4	39	VSS	75	CK0#	111	TDQS14#
4	VSS	40	TDQS12	76	VDD	112	VSS
5	DQ0	41	TDQS12#	77	VTT	113	DQ46
6	VSS	42	VSS	78	EVENT#	114	VSS
7	TDQS9	43	DQ30	79	A0	115	DQ42
8	TDQS9#	44	VSS	80	VDD	116	VSS
9	VSS	45	DQ26	81	BA0	117	DQ52
10	DQ6	46	VSS	82	RAS#/A16	118	VSS
11	VSS	47	CB4	83	VDD	119	DQ48
12	DQ2	48	VSS	84	CS0#	120	VSS
13	VSS	49	CB0	85	VDD	121	TDQS15
14	DQ12	50	VSS	86	CAS#/A15	122	TDQS15#
15	VSS	51	TDQS17	87	ODT0	123	VSS
16	DQ8	52	TDQS17#	88	VDD	124	DQ54
17	VSS	53	VSS	89	CS1#	125	VSS
18	TDQS10	54	CB6	90	VDD	126	DQ50
19	TDQS10#	55	VSS	91	ODT1	127	VSS
20	VSS	56	CB2	92	VDD	128	DQ60
21	DQ14	57	VSS	93	CS2#/C0*	129	VSS
22	VSS	58	RESET#	94	VSS	130	DQ56
23	DQ10	59	VDD	95	DQ36	131	VSS
24	VSS	60	CKE0	96	VSS	132	TDQS16
25	DQ20	61	VDD	97	DQ32	133	TDQS16#
26	VSS	62	ACT#	98	VSS	134	VSS
27	DQ16	63	BG0	99	TDQS13	135	DQ62
28	VSS	64	VDD	100	TDQS13#	136	VSS
29	TDQS11	65	A12/BC#	101	VSS	137	DQ58
30	TDQS11#	66	A9	102	DQ38	138	VSS
31	VSS	67	VDD	103	VSS	139	SA0
32	DQ22	68	A8	104	DQ34	140	SA1
33	VSS	69	A6	105	VSS	141	SCL
34	DQ18	70	VDD	106	DQ44	142	VPP
35	VSS	71	A3	107	VSS	143	VPP
36	DQ28	72	A1	108	DQ40	144	NC

288-PIN DDR4 RDIMM BACK SIDE

Pin	Name	Pin	Name	Pin	Name	Pin	Name
145	12V, NC*	181	DQ29	217	VDD	253	DQ41
146	VREFCA	182	VSS	218	CK1*	254	VSS
147	VSS	183	DQ25	219	CK1#*	255	DQS5#
148	DQ5	184	VSS	220	VDD	256	DQS5
149	VSS	185	DQS3#	221	VTT	257	VSS
150	DQ1	186	DQS3	222	PAR_IN	258	DQ47
151	VSS	187	VSS	223	VDD	259	VSS
152	DQS0#	188	DQ31	224	BA1	260	DQ43
153	DQS0	189	VSS	225	A10/AP	261	VSS
154	VSS	190	DQ27	226	VDD	262	DQ53
155	DQ7	191	VSS	227	NC	263	VSS
156	VSS	192	CB5	228	WE#/A14	264	DQ49
157	DQ3	193	VSS	229	VDD	265	VSS
158	VSS	194	CB1	230	SAVE/NC*	266	DQS6#
159	DQ13	195	VSS	231	VDD	267	DQS6
160	VSS	196	DQS8#	232	A13	268	VSS
161	DQ9	197	DQS8	233	VDD	269	DQ55
162	VSS	198	VSS	234	A17*	270	VSS
163	DQS1#	199	CB7	235	C2/NC*	271	DQ51
164	DQS1	200	VSS	236	VDD	272	VSS
165	VSS	201	CB3	237	CS3#/C1*	273	DQ61
166	DQ15	202	VSS	238	SA2	274	VSS
167	VSS	203	CKE1	239	VSS	275	DQ57
168	DQ11	204	VDD	240	DQ37	276	VSS
169	VSS	205	NC	241	VSS	277	DQS7#
170	DQ21	206	VDD	242	DQ33	278	DQS7
171	VSS	207	BG1	243	VSS	279	VSS
172	DQ17	208	ALERT#	244	DQS4#	280	DQ63
173	VSS	209	VDD	245	DQS4	281	VSS
174	DQS2#	210	A11	246	VSS	282	DQ59
175	DQS2	211	A7	247	DQ39	283	VSS
176	VSS	212	VDD	248	VSS	284	VDDSPD
177	DQ23	213	A5	249	DQ35	285	SDA
178	VSS	214	A4	250	VSS	286	VPP
179	DQ19	215	VDD	251	DQ45	287	VPP
180	VSS	216	A2	252	VSS	288	VPP

*: These pins are not used in this module.
NC: No Connect

Function Block Diagram



Absolute Maximum Ratings

Symbol	Parameter		Min	Max	Unit	Notes
VDD	Voltage on VDD pin relative to VSS		-0.4	1.5	V	1
VDDQ	Voltage on VDDQ pin relative to VSS		-0.4	1.5	V	1
VPP	Voltage on VPP pin relative to VSS		-0.4	3.0	V	1,2
VIN, VOUT	Voltage on any pin relative to VSS		-0.4	1.5	V	
TSTG	Storage temperature		-55	100	^{0}C	
IL	Input leakage current; Any input 0V<VIN<VDD; VREF input 0V<VIN<0.75V; (Other pins not under test = 0V)	Address inputs, BA RAS#, CAS#, WE#, CS#,CKE, ODT, BG	TBD	TBD	uA	3
		CK, CK#	TBD	TBD	uA	3
IOZ	Output leakage current; 0V<VOUT<VDDQ; DQs and ODT are disabled	DQ, DQS, DQS#, ALERT#	-10	10	uA	
IVREFCA	VREFCA leakage current; VREFCA = VDD/2, VDD at valid VREF level		-36	36	uA	

Notes:
1. VDD and VDDQ must be within 300mV of each other at all times; VREFCA must not be greater than 0.6 x VDDQ or less than 500mV; VREF may be less than or equal to 300mV.
2. VPP must be greater than or equal to VDD/VDDQ at all times when powered.
3. Inputs are terminated to VDD/2. Input current is dependent on terminating resistance se selected in register.

DC Operating Conditions

Symbol	Parameter	Min	Typical	Max	Unit	Notes
VDD	VDD Supply Voltage	1.14	1.2	1.26	V	1
VDDQ	VDDQ Supply Voltage for Input/Output	1.14	1.2	1.26	V	1
VPP	DRAM Activating Power Supply	2.375	2.5	2.750	V	2
VREFCA (DC)	Input reference voltage CMD/ADD bus	0.49 x VDD	0.5 x VDD	0.51 x VDD	V	4
VTT	Termination Reference Voltage	0.49 × VDD - 20mV	0.5 x VDDQ	0.49 × VDD + 20mV	V	3

Notes:
1. VDDQ tracks with VDD; VDDQ and VDD are tied together.
2. DC bandwidth is limited to 20 MHz.
3. VTT termination voltages in excess of specification limit will adversely affect command and address signals' voltage margins, and reduce timing margins.
4. The ac peak noise on VREF may not allow VREF to deviate from VREFCA(DC) by more than ±1% VDD (for reference: approx. ± 12 mV).

Operating Temperature Condition

Symbol	Parameter		Rating	Units	Notes
TOPER	Operating temperature	Commercial	0 to 95	^{0}C	1,2
		Industrial	-40 to +95		

Notes:
1. Operating temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC JESD51-2.
2. At -40 to +85^{o}C, operation temperature range, all DRAM specifications will be supported. The refresh rate is required to double when 85^{o}C < TOPER <= 95^{o}C.

Command/Address Input Levels

Symbol	Parameter	Min	Max	Unit	Note
VIH(DC)	DC Input High (Logic 1) Voltage	VREF + 0.075	VDD	V	1,2,3
VIL(DC)	DC Input Low (Logic 0) Voltage	VSS	VREF - 0.075	V	1,2
VIH(AC)	AC Input High (Logic 1) Voltage	VREF + 0.100	VDD	V	1,2
VIL(AC)	AC Input Low (Logic 0) Voltage	VSS	VREF - 0.100	V	1,2,3

Notes:

1. For input except RESET#. VREF = VREFCA(DC).
2. VREF = VREFCA(DC).
3. Input signal must meet VIL/VIH(AC) to meet tIS/tIH timings.

AC & DC Output Levels

Symbol	Parameter	Value	Unit	Note
VOH(DC)	DC output high measurement level (for IV curve linearity)	1.1 x VDDQ	V	
VOM(DC)	DC output mid measurement level (for IV curve linearity)	0.8 x VDDQ	V	
VOL(DC)	DC output low measurement level (for IV curve linearity)	0.5 x VDDQ	V	
VOH(AC)	AC output high measurement level (for output SR)	(0.7 + 0.15) x VDDQ	V	1
VOL(AC)	AC output low measurement level (for output SR)	(0.7 - 0.15) x VDDQ	V	1
VOHdiff(AC)	AC differential output high measurement level (for output SR)	+0.3 x VDDQ	V	2
VOLdiff(AC)	AC differential output low measurement level (for output SR)	-0.3 x VDDQ	V	2

Notes:

1. The swing of ± 0.15 × VDDQ is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of RZQ/7Ω and an effective test load of 50Ω to VTT = VDDQ.
2. The swing of ± 0.3 × VDDQ is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of RZQ/7Ω and an effective test load of 50Ω to VTT = VDDQ.

Input/Output Capacitance

TA=25^{0}C, f=100MHz

Parameter	Symbol	N6/M4/K2 (DDR4-2133/1866/1600)		Unit
		Min	Max	
Input capacitance (BA0~BA1, BG0~BG1, A0~A13, RAS#/A16, CAS#/A15, WE#/A14, ACT#)	CIN1	TBD	TBD	pF
Input capacitance (CKE0, CKE1, ODT0, ODT1, CS0#, CS1#)	CIN2	TBD	TBD	pF
Input capacitance (CK0, CK0#)	CIN3	TBD	TBD	pF
Input/Output capacitance (DQ, DQS, DQS#, TDQS, TDQS#, CB)	CIO	5.4	6.8	pF

IDD Specification

Parameter	Symbol	N6/M4/K2 (DDR4-2133/1866/1600)	Unit
Operating One Bank Active-Precharge Current (AL=0) CKE: HIGH; External clock: On; tCK, nRC, nRAS, CL: see the previous table; BL: 8; AL: 0; CS#: HIGH between ACT and PRE; Command, address, bank group address, bank address inputs: partially toggling according to the next table; Data I/O: VDDQ; DM#: stable at 0; Bank activity: cycling with one bank active at a time: 0, 0, 1, 1, 2, 2,...; Output buffer and RTT: enabled in mode registers; ODT signal: stable at 0	IDD0	496	mA
Operating One Bank Active-Read-Precharge Current (AL=0) CKE: HIGH; External clock: on; tCK, nRC, nRAS, nRCD, CL: see the previous table; BL: 8; AL: 0; CS#: HIGH between ACT, RD and PRE; Command, address, bank group address, bank address inputs, Data I/O: partially toggling according to the IDD1 Measurement-Loop Pattern table; DM#: stable at 0; Bank activity: cycling with one bank active at a time: 0, 0, 1, 1, 2, 2, ... ; Output buffer and RTT: enabled in mode registers; ODT Signal: stable at 0	IDD1	568	mA
Precharge Standby Current (AL=0) CKE: HIGH; External clock: On; tCK, CL: see the previous table; BL: 8; AL: 0; CS#: stable at 1; Command, address, bank group address, bank address Inputs: partially toggling according to the IDD2N and IDD3N Measurement-Loop Pattern table; Data I/O: VDDQ; DM#: stable at 1; Bank activity: all banks closed; Output buffer and RTT: enabled in mode registers; ODT signal: stable at 0	IDD2N	298	mA
Precharge Power-Down Current CKE: LOW; External clock: on; tCK, CL: see the previous table; BL: 8; AL: 0; CS#: stable at 1; Command, address, bank group address, bank address inputs: stable at 0; Data I/O: VDDQ; DM#: stable at 1; Bank activity: all banks closed; Output buffer and RTT: Enabled in mode registers; ODT signal: stable at 0	IDD2P	388	mA
Precharge Quiet Standby Current CKE: HIGH; External clock: on; tCK, CL: see the previous table; BL: 8; AL: 0; CS#: stable at 1; Command, address, bank group address, bank address inputs: stable at 0; Data I/O: VDDQ; DM#: stable at 1; Bank activity: all banks closed; Output buffer and RTT: Enabled in mode registers; ODT signal: stable at 0	IDD2Q	370	mA
Active Standby Current (AL=0) CKE: HIGH; External clock: on; tCK, CL: see the previous table; BL: 8; AL: 0; CS#: stable at 1; Command, address, bank group address, bank address inputs: partially toggling according to the IDD2N and IDD3N Measurement-Loop Pattern table; Data I/O: VDDQ; DM#: stable at 1; Bank activity: all banks open; Output buffer and RTT: Enabled in mode registers2; ODT signal: stable at 0	IDD3N	370	mA
Active Power-Down Current (AL=0) CKE: LOW; External clock: on; tCK, CL: see the previous table; BL: 8; AL: 0; CS#: stable at 1; Command, address, bank group address, bank address inputs: stable at 1; Data I/O: VDDQ; DM#: stable at 1; Bank activity: all banks open; Output buffer and RTT: Enabled in mode registers 2; ODT signal: stable at 0	IDD3P	640	mA
Operating Burst Read Current (AL=0) CKE: HIGH; External clock: on; tCK, CL: see the previous table; BL: 8; AL: 0; CS#: HIGH between RD; Command, address, bank group address, bank address inputs: partially toggling according to the IDD4R and IDDQ4R Measurement-Loop Pattern table; Data I/O: seamless read data burst with different data between one burst and the next one according to the IDD4R and IDDQ4R Measurement-Loop Pattern table; DM#: table at 1; Bankactivity: all banks open, RD commands cycling through banks: 0, 0, 1, 1, 2, 2, ...; Output buffer and RTT: Enabled in mode registers; ODT signal: stable at 0	IDD4R	946	mA
Operating Burst Write Current (AL=0) CKE: HIGH; External clock: on; tCK, CL: see the previous table; BL: 8; AL: 0; CS#: HIGH between WR; Command, address, bank group address, bank address inputs: partially toggling according to the IDD4W Measurement-Loop Pattern table; Data I/O: seamless write data burst with different data between one burst and the next one according to the IDD4W Measurement-Loop Pattern table; DM#: stable at 0; Bank activity: all banks open, WR commands cycling through banks: 0, 0, 1, 1, 2, 2, ...; Output buffer and RTT: enabled in mode registers; ODT signal: stable at HIGH	IDD4W	847	mA
Burst Refresh Current (1X REF) CKE: HIGH; External clock: on; tCK, CL, nRFC: see the previous table; BL: 8; AL: 0; CS#: HIGH between REF; Command, address, bank group address, bank address inputs: partially toggling according to the IDD5B Measurement-Loop Pattern table; Data I/O: VDDQ; DM#: stable at 1; Bank activity: REF command every nRFC; Output buffer and RTT: enabled in mode registers; ODT signal: stable at 0	IDD5B	2854	mA
Self Refresh Current: Normal Temperature Range TC: 0–85°C; Auto self refresh (ASR): disabled; Self refresh temperature range (SRT): normal; CKE: LOW; External clock: off; CK and CK#: LOW; CL: see the table above; BL: 8; AL: 0; CS#, command, address, bank group address, bank address, data I/O: VDDQ; DM#: stable at 1; Bank activity: SELF REFRESH operation; Output buffer and RTT: enabled in mode registers; ODT signal: mid-level	IDD6N	216	mA
Operating Bank Interleave Read Current CKE: HIGH; External clock: on; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: see the previous table; BL: 8; AL: CL -1; CS#: HIGH between ACT and RDA; Command, address, group bank adress, bank address inputs: partially toggling according to the IDD7 Measurement-Loop Pattern table; Data I/O: read data bursts with different databetween one burst and the next one according to the IDD7 Measurement-Loop Pattern table; DM: stable at 0; Bank activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing, see the IDD7 Measurement-Loop Pattern table; Output buffer and RTT: enabled in mode registers; ODT signal: stable at 0	IDD7	1441	mA

Note: IDD specification is based on Samsung D-die components.

AC TIMING PARAMETERS & SPECIFICATIONS

Parameter	Symbol	N6 (DDR4-2133)		M4 (DDR4-1866)		K2 (DDR4-1600)		Unit
		MIN	MAX	MIN	MAX	MIN	MAX	
Clock Timing								
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	-	8	-	8	-	ns
Average Clock Period	tCK(avg)	1.071	<1.25	1.25	<1.5	1.5	1.6	ps
Average high pulse width	tCH(avg)	0.48	0.52	0.48	0.52	0.48	0.52	nCK
Average low pulse width	tCL(avg)	0.48	0.52	0.48	0.52	0.48	0.52	nCK
Absolute Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)_tot min	tCK(avg)max + tJIT(per)_tot max	tCK(avg)min + tJIT(per)_tot min	tCK(avg)max + tJIT(per)_tot max	tCK(avg)min + tJIT(per)_tot min	tCK(avg)max + tJIT(per)_tot max	ps
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	0.45	-	0.45	-	tCK(avg)
Absolute clock LOW pulse width	tCL(abs)	0.45	-	0.45	-	0.45	-	tCK(avg)
Clock Period Jitter - total	tJIT(per)tot	-47	47	-54	54	-63	63	ps
Clock Period Jitter- deterministic	tJIT(per)_dj	-27	27	-27	27	-31	31	ps
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-43	43	-43	43	-50	50	ps
Cycle to Cycle Period Jitter - total	tJIT(cc) tot	94		107		125		ps
Cycle to Cycle Period Jitter -deterministic	tJIT(cc)_dj	47		54		63		ps
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	75		86		100		ps
Duty Cycle Jitter	tJIT(duty)	TBD	TBD	TBD	TBD	TBD	TBD	UI
Cumulative error across 2 cycles	tERR(2per)	-69	69	-79	79	-92	92	ps
Cumulative error across 3 cycles	tERR(3per)	-82	82	-94	94	-109	109	ps
Cumulative error across 4 cycles	tERR(4per)	-91	91	-104	104	-121	121	ps
Cumulative error across 5 cycles	tERR(5per)	-98	98	-112	112	-131	131	ps
Cumulative error across 6 cycles	tERR(6per)	-104	104	-119	119	-139	139	ps
Cumulative error across 7 cycles	tERR(7per)	-109	109	-124	124	-145	145	ps
Cumulative error across 8 cycles	tERR(8per)	-113	113	-129	129	-151	151	ps
Cumulative error across 9 cycles	tERR(9per)	-120	120	-134	134	-156	156	ps
Cumulative error across 10 cycles	tERR(10per)	-123	123	-137	137	-160	160	ps
Cumulative error across 11 cycles	tERR(11per)	-126	126	-141	141	-164	164	ps
Cumulative error across 12 cycles	tERR(12per)	-129	129	-144	144	-168	168	ps
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	tERR*n*per MIN = (1 + 0.68ln[*n*]) × tJITper MIN tERR*n*per MAX = (1 + 0.68ln[*n*]) × tJITper MAX						ps
Command Address Latency Timing								
CS# to Command Address Latency	tCAL	4	-	4	-	3	-	nCK
CS# to Command Address Latency in Gear-down mode	tCALg	4	-	4	-	4	-	nCK
DQ Input Timing								
Data setup time to DQS, DQS#	tDS (base)	TBD		TBD		TBD		-
Data hold time from DQS, DQS#	tDH (base)	TBD		TBD		TBD		-
DQ and DM minimum data pulse width for each input	tDIPW	0.58	-	0.58	-	0.58	-	UI_d
DQ Output Timing								
DQS ,DQS # to DQ skew, per group, per access	tDQSQ	-	0.16	-	0.16	-	0.16	UI_d
DQS ,DQS # to DQ Skew deterministic, per group, per access	$tDQSQ_d$	-	0.16	-	0.16	-	0.16	UI_d
DQS, DQS# to DQ skew, per group, per access, DBI enabled	$tDQSQ_{DBI}$	-	0.16	-	0.16	-	0.16	UI_d
DQ output hold time from DQS ,DQS #	tQH	0.76	-	0.76	-	0.76	-	UI_d

AC TIMING PARAMETERS & SPECIFICATIONS

Parameter	Symbol	N6 (DDR4-2133)		M4 (DDR4-1866)		K2 (DDR4-1600)		Unit
		MIN	MAX	MIN	MAX	MIN	MAX	
DQ output hold time deterministic from DQS , DQS #	tQH_d	0.76	-	0.76	-	0.76	-	UI_d
DQ output hold time total from DQS , DQS #; DBI enabled	tQH_{DBI}	0.76	-	0.76	-	0.76	-	UI_d
DQ to DQ offset , per group, per access referenced to DQS , DQS #	tDQSQ	TBD	TBD	TBD	TBD	TBD	TBD	UI
DQ Low-Z time from CK, CK#	tLZDQ	-360	180	-390	195	-450	225	ps
DQ High-Z time from CK, CK#	tHZDQ	-	180	-	195	-	225	ps
DQ Strobe Input Timing								
DQS, DQS# rising edge to CK, CK# rising edge	tDQSS	-0.27	0.27	-0.27	0.27	-0.27	0.27	nCK
DQS, DQS# differential input low pulse width	tDQSL	0.46	0.54	0.46	0.54	0.46	0.54	nCK
DQS, DQS# differential input high pulse width	tDQSH	0.46	0.54	0.46	0.54	0.46	0.54	nCK
DQS, DQS# falling edge setup to CK, CK# rising edge	tDSS	0.18	-	0.18	-	0.18	-	nCK
DQS, DQS# falling edge hold from CK, CK# rising edge	tDSH	0.18	-	0.18	-	0.18	-	nCK
DQS, DQS# differential WRITE preamble	tWPRE	0.9	-	0.9	-	0.9	-	nCK
DQS, DQS# differential WRITE postamble	tWPST	0.33	-	0.33	-	0.33	-	nCK
DQ Strobe Output Timing								
DQS, DQS# rising edge output access time from rising CK, CK#	tDQSCK	-180	180	-195	195	225	-225	ps
DQS ,DQS # differential output high time	tQSH	0.38	-	0.38	-	-	0.38	nCK
DQS ,DQS # differential output low time	tQSL	0.38	-	0.38	-	-	0.38	nCK
DQS, DQS# Low-Z time (RL - 1)	tLZDQS	-360	180	-390	195	225	-450	ps
DQS, DQS# High-Z time (RL + BL/2)	tHZDQS	-	180	-	195	225	-	ps
DQS, DQS# differential READ preamble	tRPRE	0.9	-	0.9	-	-	0.9	nCK
DQS, DQS# differential READ postamble	tRPST	0.33	-	0.33	-	-	0.33	nCK
MPSM Timing								
Command path disable delay upon MPSM entry	tMPED	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	nCK
Valid clock requirement after MPSM entry	tCKMPE	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	nCK
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX(min)	-	tCKSRX(min)	-	tCKSRX(min)	-	nCK
Exit MPSM to commands not requiring a locked DLL	tXMP	tXSmin	-	tXSmin	-	tXSmin	-	nCK
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP(min) + tXSDLL(min)	-	tXMP(min) + tXSDLL(min)	-	tXMP(min) + tXSDLL(min)	-	nCK
CS setup time to CKE	tMPX_S	tISmin + tIHmin	-	tISmin + tIHmin	-	tISmin + tIHmin	-	ns
CS# High hold time to CKE rising edge	tMPX_HH	tXP	-	tXP	-	tXP	-	ns
CS# Low hold time to CKE rising edge	tMPX_LH	12	tXMP-10ns	12	tXMP-10ns	12	tXMP-10ns	ns
Command and Address Timing								
DLL locking time	tDLLK	768	-	597	-	597	-	nCK
CMD, ADDR setup time toCK, CK# referenced to VIH(AC) and VIL(AC) levels	tIS	80	-	100	-	115	-	ps
CMD, ADDR setup time toCK, CK# referenced to VIH(AC) and VIL(AC) levels	tIS_{VREFCA}	180	-	200	-	215	-	ps
CMD, ADDR hold time to CK, CK# referenced to VIH(DC) and VIL(DC) levels	tIH	105	-	125	-	140	-	ps
CMD, ADDR hold time to CK, CK# referenced to VIH(DC) and VIL(DC) levels	tIH_{VREFCA}	180	-	200	-	215	-	ps
CTRL, ADDR pulse width for each input	tIPW	460	-	535	-	600	-	ps

AC TIMING PARAMETERS & SPECIFICATIONS

Parameter	Symbol	N6 (DDR4-2133)		M4 (DDR4-1866)		K2 (DDR4-1600)		Unit
		MIN	MAX	MIN	MAX	MIN	MAX	
ACTIVATE to internal READ or WRITE delay	tRCD	14.06	-	13.92	-	13.75	-	ns
PRECHARGE command period	tRP	14.06	-	13.92	-	13.75	-	ns
ACTIVATE-to-PRECHARGE command period	tRAS	33	9*tREFI	34	9*tREFI	35	9*tREFI	ns
ACTIVATE-to-ACTIVATE or REF command period	tRC	tRAS + tRP	-	tRAS + tRP	-	tRAS + tRP	-	ns
ACTIVATE-to-ACTIVATE command period to different bank groups for 1/2KB page size	tRRD_S (1/2KB)	Max(4nCK, 3.7ns)	-	Max(4nCK, 4.2ns)	-	Max(4nCK, 5ns)	-	nCK
ACTIVATE-to-ACTIVATE command period to different bank groups for 1KB page size	tRRD_S (1KB)	Max(4nCK, 3.7ns)	-	Max(4nCK, 4.2ns)	-	Max(4nCK, 5ns)	-	nCK
ACTIVATE-to-ACTIVATE command period to different bank groups for 2KB page size	tRRD_S (2KB)	Max(4nCK, 5.3ns)	-	Max(4nCK, 5.3ns)	-	Max(4nCK, 6ns)	-	nCK
ACTIVATE-to-ACTIVATE command period to same bank groups for 1/2KB page size	tRRD_L (1/2KB)	Max(4nCK, 5.3ns)	-	Max(4nCK, 5.3ns)	-	Max(4nCK, 6ns)	-	nCK
ACTIVATE-to-ACTIVATE command period to same bank groups for 1KB page size	tRRD_L (1KB)	Max(4nCK, 5.3ns)	-	Max(4nCK, 5.3ns)	-	Max(4nCK, 6ns)	-	nCK
ACTIVATE-to-ACTIVATE command period to same bank groups for 2KB page size	tRRD_L (2KB)	Max(4nCK, 6.4ns)	-	Max(4nCK, 6.4ns)	-	Max(4nCK, 7.5ns)	-	nCK
Four ACTIVATE windows for 1/2KB page size	tFAW (1/2KB)	Max(16nCK, 15ns)	-	Max(16nCK, 17ns)	-	Max(16nCK, 20ns)	-	ns
Four ACTIVATE windows for 1KB page size	tFAW (1KB)	Max(20nCK, 21ns)	-	Max(20nCK, 23ns)	-	Max(20nCK, 25ns)	-	ns
Four ACTIVATE windows for 1KB page size	tFAW (2KB)	Max(28nCK, 30ns)	-	Max(28nCK, 30ns)	-	Max(28nCK, 35ns)	-	ns
WRITE recovery time	tWR	15	-	15	-	15	-	ns
WRITE recovery time when CRC and DM are both enabled	tWR_CRC_DM	tWR+ Max(5nCK, 3.75ns)	-	tWR+ Max(5nCK, 3.75ns)	-	tWR+ Max(4nCK, 3.75ns)	-	nCK
Delay from start of internal WRITE transaction to internal READ command – Same bank group	tWTR_L	Max(5nCK, 7.5ns)	-	Max(5nCK, 7.5ns)	-	Max(4nCK, 7.5ns)	-	nCK
Delay from start of internal WRITE transaction to internal READ command – Same bank group when CRC and DM are both enabled	tWTR_L_CRC_DM	tWR+ Max(5nCK, 3.75ns)	-	tWR+ Max(5nCK, 3.75ns)	-	tWR+ Max(4nCK, 3.75ns)	-	nCK
Delay from start of internal WRITE transaction to internal READ command – Different bank group	tWTR_S	Max(2nCK, 2.5ns)	-	Max(2nCK, 2.5ns)	-	Max(2nCK, 2.5ns)	-	nCK
Delay from start of internal WRITE transaction to internal READ command – Different bank group when CRC and DM are both enabled	tWTR_S_CRC_DM	tWR+ Max(5nCK, 3.75ns)	-	tWR+ Max(5nCK, 3.75ns)	-	tWR+ Max(4nCK, 3.75ns)	-	nCK
READ-to-PRECHARGE time	tRTP	Max(4nCK, 7.5ns)	-	Max(4nCK, 7.5ns)	-	Max(4nCK, 7.5ns)	-	nCK
CAS#-to-CAS# command delay to different bank group	tCCD_S	4	-	4	-	4	-	nCK
CAS#-to-CAS# command delay to same bank group	tCCD_L	Max(5nCK, 5.355ns)	-	Max(5nCK, 5.355ns)	-	Max(5nCK, 6.25ns)	-	nCK
Auto precharge write recovery + precharge time	tDAL (MIN)	tWR+Round-UptRP/tCK (avg)	-	tWR+Round-UptRP/tCK (avg)	-	tWR+Round-UptRP/tCK (avg)	-	nCK
Refresh Timing								
4Gb REFRESH to REFRESH or REFRESH to ACTIVE command interval	tRFC1	260	-	260	-	260	-	ns
	tRFC2	160	-	160	-	160	-	ns
	tRFC4	110	-	110	-	110	-	ns
Average periodic refresh interval (0°C<= TCASE <= 85 °C)	tREFI	7.8	-	7.8	-	7.8	-	us
Average periodic refresh interval (85°C<= TCASE <= 95 °C)	tREFI	3.9	-	3.9	-	3.9	-	us
Calibration and V_{REFDQ} Train Timing								
Power-up and RESET calibration time	tZQinitI	1024	-	1024	-	1024	-	nCK
Normal operation Full calibration time	tZQoper	512	-	512	-	512	-	nCK
Normal operation Short calibration time	tZQCS	128	-	128	-	128	-	nCK
Enter VREFDQ training mode to the first write or VREFDQ MRS command delay	tVREFDQE	150	-	150	-	150	-	ns

AC TIMING PARAMETERS & SPECIFICATIONS

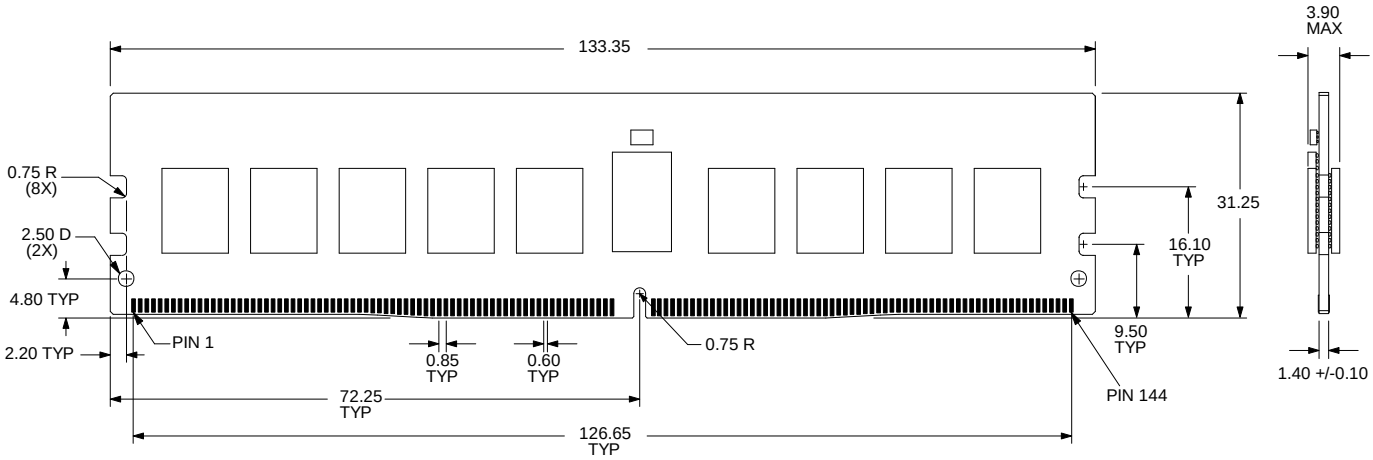
Parameter	Symbol	N6 (DDR4-2133)		M4 (DDR4-1866)		K2 (DDR4-1600)		Unit
		MIN	MAX	MIN	MAX	MIN	MAX	
Exit VREFDQ training mode to the first write command delay	tVREFDQX	150	-	150	-	150	-	ns
Reset/Self Refresh Timing								
Exit Reset from CKE HIGH to a valid command	tXPR	Max(5nCK, tRFC(min) + 10ns)	-	Max(5nCK, tRFC(min) + 10ns)	-	Max(5nCK, tRFC(min) + 10ns)	-	nCK
Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min)+ 10ns	-	tRFC(min)+ 10ns	-	tRFC(min)+ 10ns	-	ns
SRX to commands not requiring a locked DLL in Self Refresh ABORT	tXS_ABORT	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-	ns
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	tXS_FAST	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-	ns
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	nCK
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min)+ 1nCK	-	tCKE(min)+ 1nCK	-	tCKE(min)+ 1nCK	-	nCK
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	Max(5nCK, 10ns)	-	Max(5nCK, 10ns)	-	Max(5nCK, 10ns)	-	nCK
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	tCKSRE_PAR	Max(5nCK, 10ns)+PL	-	Max(5nCK, 10ns)+PL	-	Max(5nCK, 10ns)+PL	-	nCK
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	Max(5nCK, 10ns)	-	Max(5nCK, 10ns)	-	Max(5nCK, 10ns)	-	nCK
Power Down Timing								
Exit Power Down with DLL on to any valid command;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	Max(4nCK, 6ns)	-	Max(4nCK, 6ns)	-	Max(4nCK, 6ns)	-	nCK
CKE minimum pulse width	tCKE	Max(3nCK, 5ns)	-	Max(3nCK, 5ns)	-	Max(3nCK, 5ns)	-	nCK
Command pass disable delay	tCPDED	4	-	4	-	4	-	nCK
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	nCK
Timing of ACT command to Power Down entry	tACTPDEN	2	-	1	-	1	-	nCK
Timing of PRE or PREA command to Power Down entry	tPRPDEN	2	-	1	-	1	-	nCK
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	RL+4+1	-	RL+4+1	-	nCK
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(tWR/ tCK(avg))	-	WL+4+(tWR/ tCK(avg))	-	WL+4+(tWR/ tCK(avg))	-	nCK
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	nCK
Timing of WR command to Power Down entry (BC4MRS)	tWRPBC4DEN	WL+2+(tWR/ tCK(avg))	-	WL+2+(tWR/ tCK(avg))	-	WL+2+(tWR/ tCK(avg))	-	nCK
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPBC4DEN	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	nCK
Timing of REF command to Power Down entry	tREFPDEN	2	-	1	-	1	-	nCK
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	nCK
Mode Register Set (MRS) Command Timing								
MRS command cycle time	tMRD	8	-	8	-	8	-	nCK
MRS command cycle time in PDA mode	tMRD_PDA	Max(16nCK, 10ns)	-	Max(16nCK, 10ns)	-	Max(16nCK, 10ns)	-	nCK
MRS command cycle time in CAL mode	tMRD_CAL	tMOD + tCAL	-	tMOD + tCAL	-	tMOD + tCAL	-	nCK
MRS command update delay in PDA mode	tMOD	Max(24nCK, 15ns)	-	Max(24nCK, 15ns)	-	Max(24nCK, 15ns)	-	nCK
Mode Register Set command update delay in PDA mode	tMOD_PDA	tMOD	-	tMOD	-	tMOD	-	nCK
MRS command update delay in CAL mode	tMOD_CAL	tMOD + tCAL	-	tMOD + tCAL	-	tMOD + tCAL	-	nCK
MRS commandto DQS Drive in Preamble Training	tSDO	tMOD + 9ns	-	tMOD + 9ns	-	tMOD + 9ns	-	ns
Multipurpose Register (MPR) Command Timing								
MPR recovery time	tMPRR	1	-	1	-	1	-	nCK

AC TIMING PARAMETERS & SPECIFICATIONS

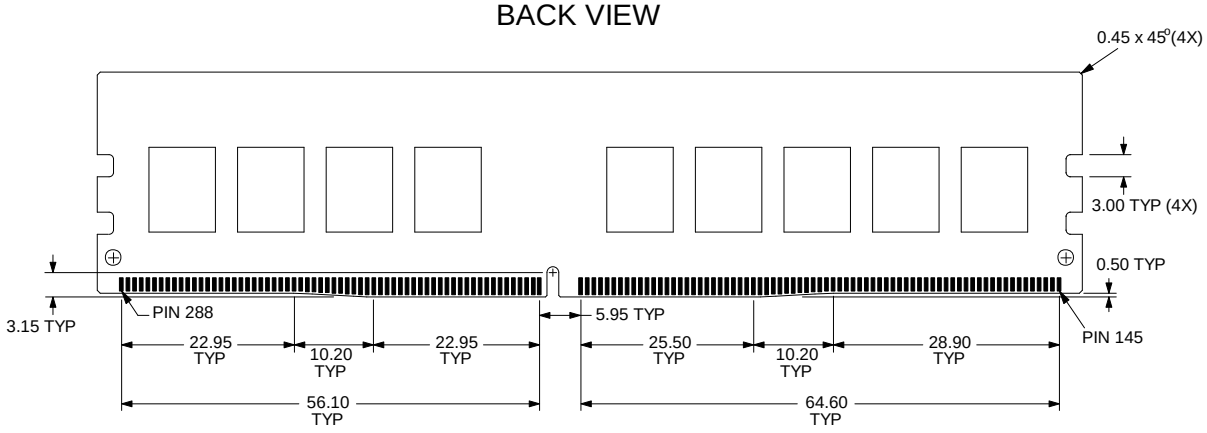
Parameter	Symbol	N6 (DDR4-2133)		M4 (DDR4-1866)		K2 (DDR4-1600)		Unit
		MIN	MAX	MIN	MAX	MIN	MAX	
MPR Write Recovery Time	tWR_MPRR	tMOD + AL + PL	-	tMOD + AL + PL	-	tMOD + AL + PL	-	nCK
ODT Timing								
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1.0	9.0	1.0	9.0	1.0	9.0	ns
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1.0	9.0	1.0	9.0	1.0	9.0	ns
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)
Write Leveling Timing								
First DQS /DQS# rising edge after write leveling	tWLMRD	40	-	40	-	40	-	nCK
mode is programmed	tWLDQSEN	25	-	25	-	25	-	nCK
DQS /DQS# delay after write leveling mode is	tWLS	0.13	-	0.13	-	0.13	-	tCK(avg)
Write leveling hold time from rising DQS /DQS# crossing to rising CK , CK # crossing	tWLH	0.13	-	0.13	-	0.13	-	tCK(avg)
Write leveling output delay	tWLO	0	9.5	0	9.5	0	9.5	ns
Write leveling output error	tWLOE	-	2	-	2	-	2	ns
CA Parity Timing								
Commands not guaranteed to be executed during this time	tPAR_ UNKNOWN	-	Max(2nCK, 3ns)	-	Max(2nCK, 3ns)	-	Max(2nCK, 3ns)	nCK
Delay from errant command to ALERT# assertion	tPAR_ ALERT_ON	-	PL+6ns	-	PL+6ns	-	PL+6ns	nCK
Pulse width of ALERT# signal when asserted	tPAR_ ALERT_PW	64	128	56	112	48	96	nCK
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ ALERT_RSP	-	57	-	50	-	43	nCK
Parity Latency	PL	4	-	4	-	4	-	nCK
CRC Error Reporting								
CRC error to ALERT# latency	tCRC_ALERT	3	13	3	13	3	13	ns
CRC ALERT# pulse width	tCRC_ALERT_ PW	6	10	6	10	6	10	nCK

Package Dimensions

FRONT VIEW



BACK VIEW



Notes: 1. All dimensions are in millimeters with tolerance +/- 0.15mm unless otherwise specified.
2. The dimensional diagram is for reference only.

Revision History:

Date	Rev.	Page	Changes
04/03/2014	0.01	All	Preliminary
05/13/2014	0.02	4-6	Preliminary: Update - DC Operating Conditions table - IDD Specification table - Add Command/Address Input Levels table - Add AC&DC Output Levels table
06/06/2014	0.03	1	Preliminary: - Changed “2K EEPROM” to “4K EEPROM” in Description section.