



Product Specifications

PART NO:

VL470T2863A-E6S/D5S/CCS

REV: 1.1

General Information

1GB 128Mx64 DDR2 SDRAM NON-ECC UNBUFFERED SODIMM 200-PIN

Description The VL470T2863A is a 128Mx64 DDR2 SDRAM high density SODIMM. This memory module consists of eight CMOS 128Mx8 bit with 8 banks DDR2 Synchronous DRAMs in BGA packages and a 2K EEPROM in an 8-pin TSSOP package. This module is a 200-pin small-outline dual in-line memory module and is intended for mounting into a connector socket. Decoupling capacitors are mounted on the printed circuit board for each DDR2 SDRAM.

Features

- . 200-pin, small-outline dual in-line memory module (SODIMM)
- . Fast data transfer rates: PC2-5300, PC2-4200, and PC2-3200
- . VDD = VDDQ = 1.8V
- . VDDSPD = 1.7V to 3.6V
- . JEDEC standard 1.8V I/O (SSTL_18 compatible)
- . Differential data strobe (DQS, DQS#) option
- . Four-bit prefetch architecture
- . DLL aligns DQ and DQS transition with CK
- . Programmable CAS# Latency (CL): 5 (DDR2-667), 4 (DDR2-533), 3 (DDR2-400)
- . Programmable burst; length (4, 8)
- . On-die termination (ODT)
- . Auto & Self refresh, (8K/64ms refresh)
- . Serial presence detect (SPD) with EEPROM
- . Gold edge PCB contacts
- . Lead-free, RoHS compliant
- . PCB: Height 30.00mm (1.181"), double sided components

Pin Name	Function
A0~A13	Address Inputs
BA0~BA2	Bank Address Inputs
DQ0~DQ63	Data Input/Output
DQS0~DQS7	Data Stobes
DQS0#~DQS7#	Data Stobes Complement
ODT0	On-die Termination Control
CK0,CK0#,CK1,CK1#	Clock Input
CKE0	Clock Enables
CS0#	Chip Selects
RAS#	Row Address Stobes
CAS#	Column Address Stobes
WE#	Write Enable
VDD	Voltage Supply 1.8V +/- 0.1V
VSS	Ground
SA0~SA1	SPD Address
SDA	SPD Data Input/Output
SCL	SPD Clock Input
DM0~DM7	Data Masks
A10/AP	Address Input/Autoprecharge
VREF	SSTL_18 Reference Voltage
VDDSPD	SPD Voltage Supply 1.7V to 3.6V
NC	No Connect

Order Information

VL470T2863A-E6 S X

DRAM DIE (option)

DRAM MANUFACTURER
S - SAMSUNG

MODULE SPEED
E6: PC2-5300 @ CL5
D5: PC2-4200 @ CL4
CC: PC2-3200 @ CL3

VL : Lead-free/RoHS

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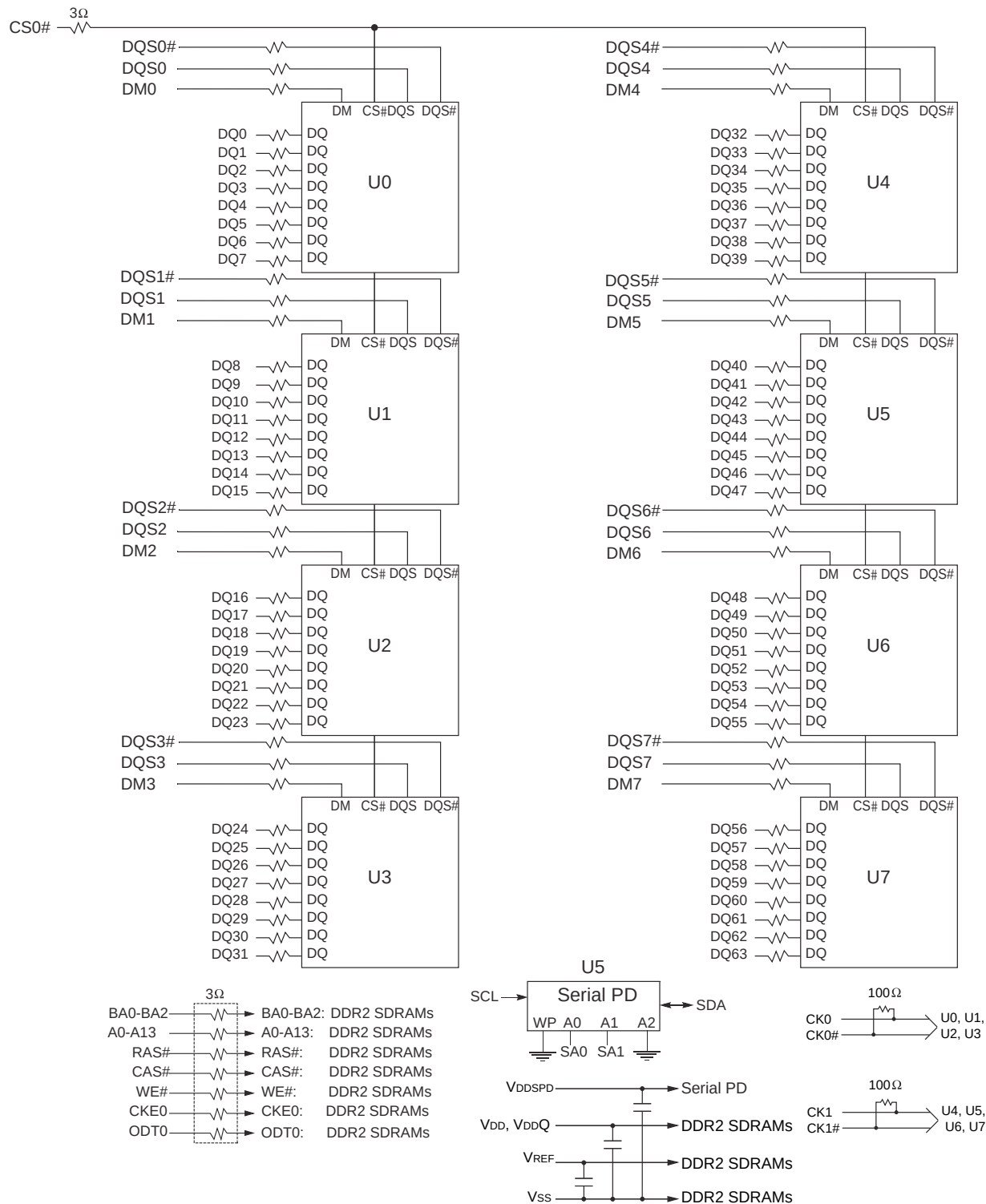
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Pin Configuration

200-PIN DDR2 SODIMM FRONT								200-PIN DDR2 SODIMM BACK							
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VREF	51	DQS2	101	A1	151	DQ42	2	VSS	52	DM2	102	A0	152	DQ46
3	VSS	53	VSS	103	VDD	153	DQ43	4	DQ4	54	VSS	104	VDD	154	DQ47
5	DQ0	55	DQ18	105	A10/AP	155	VSS	6	DQ5	56	DQ22	106	BA1	156	VSS
7	DQ1	57	DQ19	107	BA0	157	DQ48	8	VSS	58	DQ23	108	RAS#	158	DQ52
9	VSS	59	VSS	109	WE#	159	DQ49	10	DM0	60	VSS	110	CS0#	160	DQ53
11	DQS0#	61	DQ24	111	VDD	161	VSS	12	VSS	62	DQ28	112	VDD	162	VSS
13	DQS0	63	DQ25	113	CAS#	163	NC	14	DQ6	64	DQ29	114	OTD0	164	CK1
15	VSS	65	VSS	115	CS1#*	165	VSS	16	DQ7	66	VSS	116	A13	166	CK1#
17	DQ2	67	DM3	117	VDD	167	DQS6#	18	VSS	68	DQS3#	118	VDD	168	VSS
19	DQ3	69	NC	119	ODT1*	169	DQS6	20	DQ12	70	DQS3	120	NC	170	DM6
21	VSS	71	VSS	121	VSS	171	VSS	22	DQ13	72	VSS	122	VSS	172	VSS
23	DQ8	73	DQ26	123	DQ32	173	DQ50	24	VSS	74	DQ30	124	DQ36	174	DQ54
25	DQ9	75	DQ27	125	DQ33	175	DQ51	26	DM1	76	DQ31	126	DQ37	176	DQ55
27	VSS	77	VSS	127	VSS	177	VSS	28	VSS	78	VSS	128	VSS	178	VSS
29	DQS1#	79	CKE0	129	DQS4#	179	DQ56	30	CK0	80	CKE1*	130	DM4	180	DQ60
31	DQS1	81	VDD	131	DQS4	181	DQ57	32	CK0#	82	VDD	132	VSS	182	DQ61
33	VSS	83	NC	133	VSS	183	VSS	34	VSS	84	NC	134	DQ38	184	VSS
35	DQ10	85	BA2	135	DQ34	185	DM7	36	DQ14	86	NC	136	DQ39	186	DQS7#
37	DQ11	87	VDD	137	DQ35	187	VSS	38	DQ15	88	VDD	138	VSS	188	DQS7
39	VSS	89	A12	139	VSS	189	DQ58	40	VSS	90	A11	140	DQ44	190	VSS
41	VSS	91	A9	141	DQ40	191	DQ59	42	VSS	92	A7	142	DQ45	192	DQ62
43	DQ16	93	A8	143	DQ41	193	VSS	44	DQ20	94	A6	144	VSS	194	DQ63
45	DQ17	95	VDD	145	VSS	195	SDA	46	DQ21	96	VDD	146	DQS5#	196	VSS
47	VSS	97	A5	147	DM5	197	SCL	48	VSS	98	A4	148	DQS5	198	SA0
49	DQS2#	99	A3	149	VSS	199	VDDSPD	50	NC	100	A2	150	VSS	200	SA1

* These pins are not used in this module.

Functional Block Diagram



NOTE:

1. Unless otherwise noted, resistor values are 22

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Absolute Maximum Ratings

Absolute Maximum Ratings					
Symbol	Parameter		MIN	MAX	Unit
V _{DD}	Voltage on V _{DD} pin relative to V _{SS}		-1.0	2.3	V
V _{DDQ}	Voltage on V _{DDQ} pin relative to V _{SS}		-0.5	2.3	V
V _{DDL}	Voltage on V _{DDL} pin relative to V _{SS}		-0.5	2.3	V
V _{IN} , V _{OUT}	Voltage on any pin relative to V _{SS}		-0.5	2.3	V
T _{STG}	Storage temperature		-55	100	°C
I _L	Input leakage current; Any input 0V<V _{IN} <V _{DD} ; V _{REF} input 0V<V _{IN} <0.95V; Other pins not under test = 0V	Command/Address, RAS#, CAS#, WE#, CS#, CKE	-40	40	uA
		CK, CK#	-20	20	uA
		DM	-5	5	uA
I _{OZ}	Output leakage current; 0V<V _{OUT} <V _{DDQ} ; DQs and ODT are disabled	DQ, DQS, DQS#	-5	5	uA
I _{VREF}	V _{REF} leakage current; V _{REF} = Valid V _{REF} level		-16	16	uA

DC Operating Conditions

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Supply voltage	V _{DD}	1.7	1.8	1.9	V	1
IO Supply voltage	V _{DDQ}	1.7	1.8	1.9	V	4
VDDL Supply voltage	V _{DDL}	1.7	1.8	1.9	V	4
IO Reference voltage	V _{REF}	0.49 x V _{DDQ}	0.50 x V _{DDQ}	0.51 x V _{DDQ}	V	2
IO Termination voltage	V _{TT}	V _{REF} -0.04	V _{REF}	V _{REF} +0.04	V	3

- Notes:
1. V_{DD}, V_{DDQ} must track each other. V_{DDQ} must be less than or equal to V_{DD}.
 2. V_{REF} is expected to equal V_{DDQ}/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed +/-1percent of the DC value. Peak-to-peak AC noise on V_{REF} may not exceed +/-2 percent of V_{REF}. This measurement is to be taken at the nearest V_{REF} bypass capacitor.
 3. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
 4. V_{DDQ} tracks with V_{DD}; V_{DDL} tracks with V_{DD}.

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Operating Temperature Condition

Parameter	Symbol	Rating	Units	Notes
Operating temperature	T _{OPER}	0 to +95	°C	1,2

Notes:

- Operating temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC JESD51.2
- At 0 to +85°C, operation temperature range, all DRAM specifications will be supported. The refresh rate is required to double when 85°C < T_{OPER} ≤ 95 °C

Input DC Logic Level

All voltages referenced to VSS

Parameter	Symbol	Min	Max	Unit
Input High (Logic 1) Voltage	V _{IH} (DC)	V _{REF} + 0.125	V _{DDQ} + 0.300	V
Input Low (Logic 0) Voltage	V _{IL} (DC)	-0.300	V _{REF} - 0.125	V

Input AC Logic Level

All voltages referenced to VSS

Parameter	Symbol	Min	Max	Unit
AC Input High (Logic 1) Voltage DDR2-400 & DDR2-533	V _{IH} (AC)	V _{REF} + 0.250	-	V
AC Input High (Logic 1) Voltage DDR2-667	V _{IH} (AC)	V _{REF} + 0.200	-	V
AC Input Low (Logic 0) Voltage DDR2-400 & DDR2-533	V _{IL} (AC)	-	V _{REF} - 0.250	V
AC Input Low (Logic 0) Voltage DDR2-667	V _{IL} (AC)	-	V _{REF} - 0.200	V

Input/Output Capacitance

T_A=25°C, f=100MHz

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0~A13, BA0~BA2, RAS#, CAS#, WE#)	C _{IN1}	12	20	pF
Input capacitance (CKE0), (ODT0)	C _{IN2}	12	20	pF
Input capacitance (CS0#)	C _{IN3}	12	20	pF
Input capacitance (CK0, CK0#, CK1, CK1#)	C _{IN4}	8	12	pF
Input/Output capacitance (DQ, DQS, DQS#, DM)	C _{IO}	6.5	8	pF

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IDD Specification

IDD Specification						
Condition		Symbol	-E6	-D5	-CC	Unit
Operating one bank active-precharge; $t_{CK}=t_{CK(DD)}$; $t_{RC}=t_{RC(DD)}$; $t_{RAS}=t_{RAS\ MIN(DD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		IDD0	680	560	560	mA
Operating one bank active-read-precharge; IOUT = 0mA; BL = 4; CL = CL(DD); $t_{CK}=t_{CK(DD)}$; $t_{RC}=t_{RC(DD)}$; $t_{RAS}=t_{RAS\ MIN(DD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING; Data pattern is same as IDD4W.		IDD1	800	760	720	mA
Precharge power-down current; All banks idle; $t_{CK}=t_{CK(DD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		IDD2P	56	56	56	mA
Precharge quiet standby current; All banks idle; $t_{CK}=t_{CK(DD)}$; CKE is HIGH; CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		IDD2Q	320	320	280	mA
Precharge standby current; All banks idle; $t_{CK}=t_{CK(DD)}$; CKE is HIGH; CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are SWITCHING.		IDD2N	320	320	280	mA
Active power-down current; All banks open; $t_{CK}=t_{CK(DD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	Fast PDN Exit MRS(12) = 0	IDD3P	240	240	240	mA
	Slow PDN Exit MRS(12) = 1		80	80	80	mA
Active standby current; All banks open; $t_{CK}=t_{CK(DD)}$; $t_{RC}=t_{RC(DD)}$; $t_{RAS}=t_{RAS\ MIN(DD)}$; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		IDD3N	440	360	320	mA
Operating burst write current; All banks open; Continuous burst writes; BL = 4; CL = CL(DD); AL = 0; $t_{CK}=t_{CK(DD)}$; $t_{RAS}=t_{RAS\ MAX(DD)}$; $t_{RP}=t_{RP(DD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		IDD4W	1080	1000	840	mA
Operating burst read current; All banks open; Continuous burst reads; IOUT = 0mA; BL = 4; CL = CL(DD); AL = 0; $t_{CK}=t_{CK(DD)}$; $t_{RAS}=t_{RAS\ MAX(DD)}$; $t_{RP}=t_{RP(DD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W.		IDD4R	1080	1000	840	mA
Burst auto refresh current; $t_{CK}=t_{CK(DD)}$; Refresh command at every $t_{RFC(DD)}$ interval; CKE is HIGH; CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		IDD5	1720	1680	1640	mA
Self refresh current; CK and CK# at 0V; CKE < 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING.	Normal	IDD6	56	56	56	mA
Operating bank interleave read current; All bank interleaving reads; IOUT = 0mA; BL = 4; CL = CL(DD); AL = $t_{RCD(DD)} - 1 \cdot t_{CK(DD)}$; $t_{CK}=t_{CK(DD)}$; $t_{RC}=t_{RC(DD)}$; $t_{RRD}=t_{RRD(DD)}$; $t_{RCD}=1 \cdot t_{CK(DD)}$; CKE is HIGH; CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data bus inputs are SWITCHING.		IDD7	2240	2160	2080	mA
Note: IDD specification is based on Samsung components. Other DRAM Manufacturers specification may be different.						

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AC Timing Parameters & Specifications

Parameter			Symbol	-E6		-D5		-CC		Unit
				Min	Max	Min	Max	Min	Max	
Clock	Clock cycle time	CL=5	$t_{CK}(5)$	3000	8000	-	-	-	-	ps
		CL=4	$t_{CK}(4)$	-	-	3,750	8,000	-	-	ps
		CL=3	$t_{CK}(3)$	-	-	-	-	5,000	8,000	ps
	CK high-level width		$t_{CH(AVG)}$	0.48	0.52	0.48	0.52	0.48	0.52	t_{CK}
	CK low-level width		$t_{CL(AVG)}$	0.48	0.52	0.48	0.52	0.48	0.52	t_{CK}
	Half clock period		t_{HP}	MIN (t_{CH}, t_{CL})		MIN (t_{CH}, t_{CL})		MIN (t_{CH}, t_{CL})		ps
	Clock jitter		t_{JIT}	-125	125	-125	125	-125	125	ps
Data	DQ output access time from CK/CK#		t_{AC}	-450	+450	-500	+500	-600	+600	ps
	Data-out high impedance window from CK/CK#		t_{HZ}		$t_{AC(MAX)}$		$t_{AC(MAX)}$		$t_{AC(MAX)}$	ps
	Data-out low-impedance window from CK/CK#		t_{LZ}	$t_{AC(MIN)}$	$t_{AC(MAX)}$	$t_{AC(MIN)}$	$t_{AC(MAX)}$	$t_{AC(MIN)}$	$t_{AC(MAX)}$	ps
	DQ and DM input setup time relative to DQS		t_{DS}	100		100		150		ps
	DQ and DM input hold time relative to DQS		t_{DH}	175		225		275		ps
	DQ and DM input pulse width (for each input)		t_{DIPW}	0.35		0.35		0.35		t_{CK}
	Data hold skew factor		t_{QHS}		340		400		450	ps
	DQ-DQS hold, DQS to first DQ to go nonvalid, per access		t_{QH}	$t_{HP} - t_{QHS}$		$t_{HP} - t_{QHS}$		$t_{HP} - t_{QHS}$		ps
	Data valid output window (DVW)		t_{DVW}	$t_{QH} - t_{DQSQ}$		$t_{QH} - t_{DQSQ}$		$t_{QH} - t_{DQSQ}$		ns
Data Strobe	DQS input high pulse width		t_{DQSH}	0.35		0.35		0.35		t_{CK}
	DQS input low pulse width		t_{DQSL}	0.35		0.35		0.35		t_{CK}
	DQS output access time from CK/CK#		t_{DQSCK}	-400	+400	-450	+450	-500	+500	ps
	DQS falling edge to CK rising – setup time		t_{DSS}	0.2		0.2		0.2		t_{CK}
	DQS falling edge from CK rising – hold time		t_{DSH}	0.2		0.2		0.2		t_{CK}
	DQS-DQ skew, DQS to last DQ valid, per group, per access		t_{DQSQ}		240		300		350	ps
	DQS read preamble		t_{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}
	DQS read postamble		t_{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}
	DQS write preamble setup time		t_{WPRES}	0		0		0		ps
	DQS write preamble		t_{WPRE}	0.35		0.35		0.35		t_{CK}
	DQS write postamble		t_{WPST}	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}
	Write command to first DQS latching transition		t_{DQSS}	WL-0.25	WL+0.25	WL-0.25	WL+0.25	WL-0.25	WL+0.25	t_{CK}

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AC Timing Parameters & Specifications (cont')									
	Parameter	Symbol	-E6		-D5		-CC		Unit
			Min	Max	Min	Max	Min	Max	
Command and Address	Address and control input pulse width for each input	t_{PW}	0.6		0.6		0.6		t_{CK}
	Address and control input setup time	t_S	200		250		350		ps
	Address and control input hold time	t_H	275		375		475		ps
	CAS# to CAS# command delay	t_{CCD}	2		2		2		t_{CK}
	ACTIVE to ACTIVE (same bank) command	t_{RC}	60		60		55		ns
	ACTIVE bank a to ACTIVE bank b command	t_{RRD}	7.5		7.5		7.5		ns
	ACTIVE to READ or WRITE delay	t_{RCD}	15		15		15		ns
	Four Bank Activate period	t_{FAW}	37.5		37.5		37.5		ns
	ACTIVE to PRECHARGE command	t_{RAS}	45	70,000	45	70,000	40	70,000	ns
	Internal READ to precharge command delay	t_{RTP}	7.5		7.5		7.5		ns
	Write recovery time	t_{WR}	15		15		15		ns
	Auto precharge write recovery + precharge time	t_{DAL}	$t_{WR}+t_{RP}$		$t_{WR}+t_{RP}$		$t_{WR}+t_{RP}$		t_{CK}
	Internal WRITE to READ command delay	t_{WTR}	7.5		7.5		10		ns
	PRECHARGE command period	t_{RP}	15		15		15		ns
	LOAD MODE command cycle time	t_{MRD}	2		2		2		t_{CK}
	CKE low to CK,CK# uncertainty	t_{DELAY}	$t_S+t_{CK}+t_H$		$t_S+t_{CK}+t_H$		$t_S+t_{CK}+t_H$		ns
Self Refresh	REFRESH to Active or Refresh to Refresh command interval	t_{RFC}	127.5	70,000	127.5	70,000	127.5	70,000	ns
	Average periodic refresh interval	t_{REFI}		7.8		7.8		7.8	us
	Exit self refresh to non-READ command	t_{XSNR}	$t_{RFC(MIN)}+10$		$t_{RFC(MIN)}+10$		$t_{RFC(MIN)}+10$		ns
	Exit self refresh to READ	$t_{XS RD}$	200		200		200		t_{CK}
	Exit self refresh timing reference	t_{ISXR}	t_S		t_S		t_S		ps
ODT	ODT turn-on delay	t_{AOND}	2	2	2	2	2	2	t_{CK}
	ODT turn-on	t_{AON}	$t_{AC(MIN)}$	$t_{AC(MAX)}^{+700}$	$t_{AC(MIN)}$	$t_{AC(MAX)}^{+1000}$	$t_{AC(MIN)}$	$t_{AC(MAX)}^{+1000}$	ps
	ODT turn-off delay	t_{AOFD}	2.5	2.5	2.5	2.5	2.5	2.5	t_{CK}
	ODT turn-off	t_{AOF}	$t_{AC(MIN)}$	$t_{AC(MAX)}^{+600}$	$t_{AC(MIN)}$	$t_{AC(MAX)}^{+600}$	$t_{AC(MIN)}$	$t_{AC(MAX)}^{+600}$	ps
	ODT turn-on (power-down mode)	t_{AONPD}	$t_{AC(MIN)}^{+2000}$	$2 \times t_{CK}^{+} + t_{AC(MAX)}^{+1000}$	$t_{AC(MIN)}^{+2000}$	$2 \times t_{CK}^{+} + t_{AC(MAX)}^{+1000}$	$t_{AC(MIN)}^{+2000}$	$2 \times t_{CK}^{+} + t_{AC(MAX)}^{+1000}$	ps
	ODT turn-off (power-down mode)	$t_{AOF PD}$	$t_{AC(MIN)}^{+2000}$	$2.5 \times t_{CK}^{+} + t_{AC(MAX)}^{+1000}$	$t_{AC(MIN)}^{+2000}$	$2.5 \times t_{CK}^{+} + t_{AC(MAX)}^{+1000}$	$t_{AC(MIN)}^{+2000}$	$2.5 \times t_{CK}^{+} + t_{AC(MAX)}^{+1000}$	ps
	ODT to power-down entry latency	t_{ANPD}	3		3		3		t_{CK}
	ODT power-down exit latency	t_{AXPD}	8		8		8		t_{CK}
Power-Down	Exit active power-down to READ command, MR[bit12=0]	t_{XARD}	2		2		2		t_{CK}
	Exit active power-down to READ command, MR[bit12=1]	t_{XARDS}	7-AL		6-AL		6-AL		t_{CK}
	Exit precharge power-down to any non-READ command.	t_{XP}	2		2		2		t_{CK}
	CKE minimum high/low time	t_{CKE}	3		3		3		t_{CK}

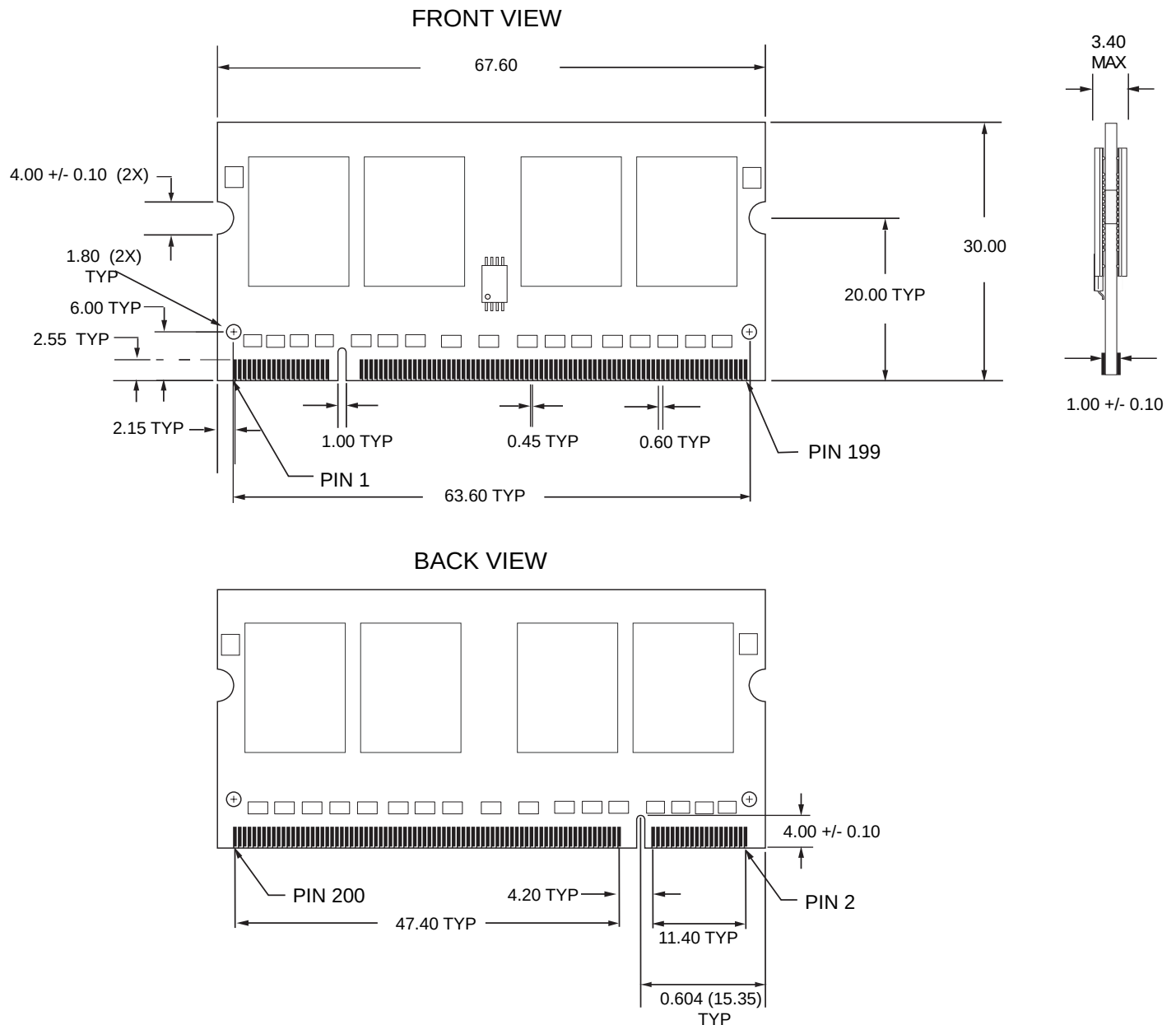
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Package Dimensions



NOTE:

All dimensions are in millimeters with tolerance +/- 0.15mm unless otherwise specified.



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Revision History:

Date	Rev.	Page	Changes
11/02/09	1.0	All	Spec release
08/23/10	1.1	1,9,5	Updated data