Product Specifications		
PART NO.:	VL47A1G63A-N6/M4/K2S	REV: 0.01 PRELIMINARY

General Information

8GB 1Gx64 DDR4 SDRAM NON-ECC UNBUFFERED SODIMM 260-PIN

Description

The VL47A1G63A is a 1Gx64 DDR4 SDRAM high density SODIMM. This dual rank memory module consists of sixteen CMOS 512Mx8 bits with 16 internal banks DDR4 Synchronous DRAMs in BGA packages, and a 4K EEPROM with thermal sensor in an 8-pin MLF package. This module is a 260-pin small out-line dual in-line memory module and is intended for mounting into an edge connector socket. Decoupling capacitors are mounted on the printed circuit board for each DDR4 SDRAM.

Features

- 260-pin, small out-line dual in-line memory module (SODIMM)
- Fast data transfer rates: PC4-17100, PC4-14900, PC4-12800
- VDD = VDDQ = 1.2V +/-0.060V
- VPP = 2.5V +/-0.125V
- VDDSPD = 3.0V to 3.6V
- 16 internal banks; 4 groups of 4 banks each
- Nominal and dynamic on-die termination (ODT)
- Low-power auto self refresh
- Programmable CAS# latency:
  15 (DDR4-2133), 13 (DDR4-1866), 11 (DDR4-1600)
- Programmable burst length (8)
- Asynchronous reset
- On-die VREFDQ generation and calibration
- Fly-by topology
- On board terminated command, address, and control bus
- Serial presence detect (SPD) EEPROM with thermal sensor
- Thermal sensor range: -40°C to +125°C (Max +/-3% accuracy)
- Lead-free, RoHS compliant
- JEDEC pinout
- Gold edge contacts
- PCB: Height 30.00mm (1.181”), double sided component
- Operating temperature (TOPER): - Commercial (0°C <= Tc <= 95°C)
  - Industrial (-40°C <= Tc <= 95°C)

Notes: Double refresh rate is required when 85°C < TOPER <= 95°C.
TOPER is DRAM case temperature (Tc)

Pin Description

Pin Name	Function
A0~A15	Row Address Inputs
A10/AP	Address Input/ Autoprecharge
A12/BC#	Address Input/ Burst Chop
ACT#	Activate input
RAS#/A16	Row Address Strobes/ Address Input
CAS#/A15	Column Address Strobes/ Address Input
WE#/A14	Write Enable/Address Input
BA0~BA1	Bank Address Inputs
BG0~BG1	Bank group address inputs
DQ0~DQ63	Data Input/Output
DQS0~DQS7	Data Strobes
DQS0#~DQS7#	Data Strobes Complement
DM0#~DM7#/ DBI0#~ DBI7#	Data Mask Input
	Data Bus Inversion I/O
PAR_IN	Parity Input
ALERT#	Alert output
CK0, CK0# CK1, CK1#	Clock Inputs
ODT0, ODT1	On-die Termination Controls
CKE0, CKE1	Clock Enables
CS0#, CS1#	Chip Selects
RESET#	Register and SDRAM Control
VDD	Voltage Supply
VPP	DRAM Activating Voltage Supply
VSS	Ground
SA0~SA2	SPD Address
SDA	SPD Data Input/Output
SCL	SPD Clock Input
EVENT#	Temperature Event Output
VREFCA	Reference Voltage for CA
VDDSPD	SPD Voltage Supply
VTT	Termination Voltage
NC	No Connect

Order Information:

VL47A1G63A - N6 S X - X

- OPERATING TEMPERATURE
  None: Commercial
  S1: Industrial screening
- DRAM DIE: (Option)
- DRAM MANUFACTURER
  S - SAMSUNG
- MODULE SPEED
  N6: PC4-17100 @ CL15
  M4: PC4-14900 @ CL13
  K2: PC4-12800 @ CL11
- VL: Lead-free/RoHS

Pin Configuration

260-PIN DDR4 SODIMM FRONT SIDE

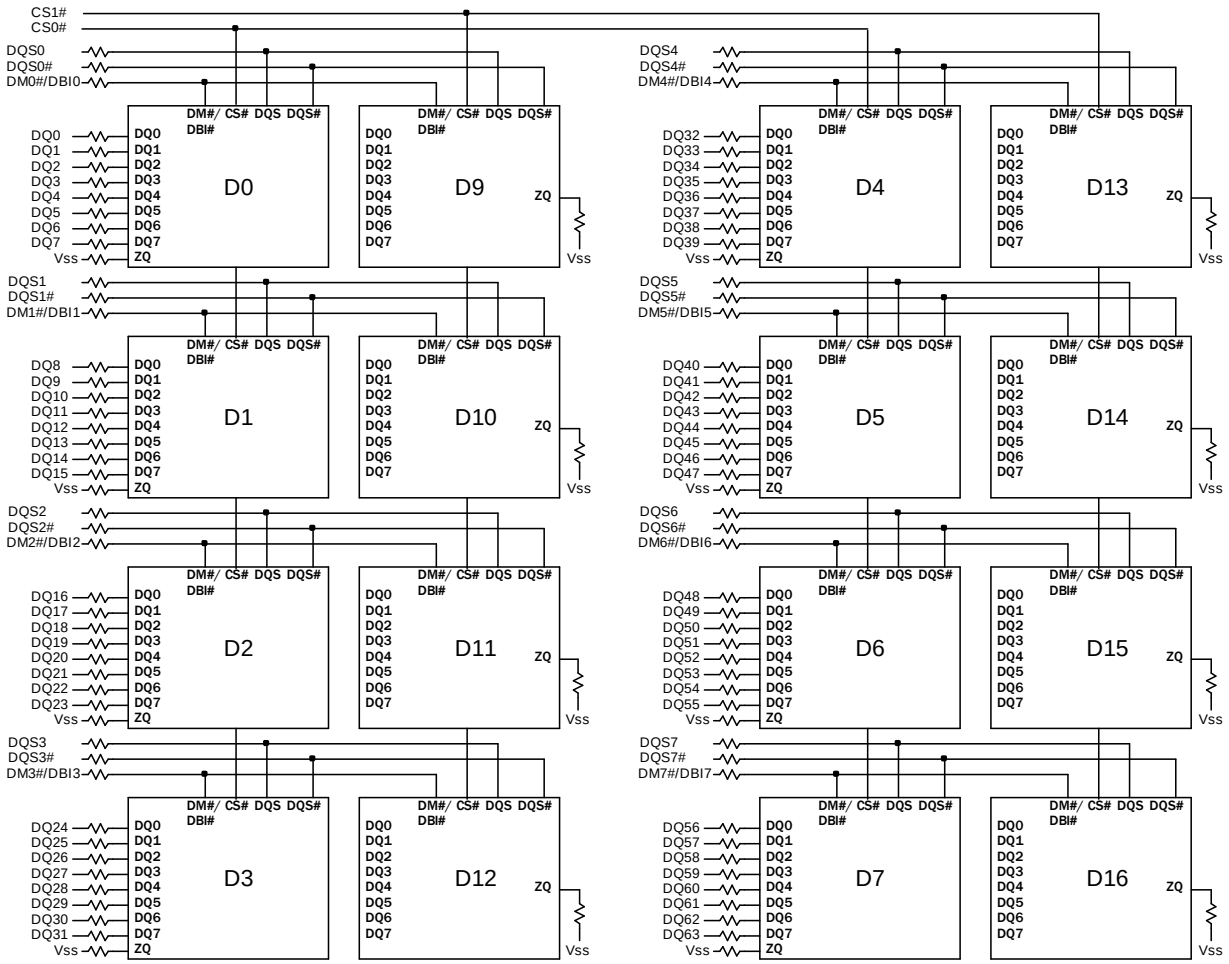
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VSS	67	DQ29	133	A1	195	DQ40
3	DQ5	69	VSS	135	VDD	197	VSS
5	VSS	71	DQ25	137	CK0	199	DM5#/ DBI5#
7	DQ1	73	VSS	139	CK0#	201	VSS
9	VSS	75	DM3#/ DBI3#	141	VDD	203	DQ46
11	DQS0#	77	VSS	143	PARITY	205	VSS
13	DQS0	79	DQ30	KEY		207	DQ42
15	VSS	81	VSS			209	VSS
17	DQ7	83	DQ26	145	BA1	211	DQ52
19	VSS	85	VSS	147	VDD	213	VSS
21	DQ3	87	CB5*	149	CS0#	215	DQ49
23	VSS	89	VSS	151	A14/WE#	217	VSS
25	DQ13	91	CB1*	153	VDD	219	DQS6#
27	VSS	93	VSS	155	ODT0	221	DQS6
29	DQ9	95	DQS8#	157	CS1#	223	VSS
31	VSS	97	DQS8	159	VDD	225	DQ55
33	DM1#/ DBI1#	99	VSS	161	ODT1	227	VSS
35	VSS	101	CB2*	163	VDD	229	DQ51
37	DQ15	103	VSS	165	NC, C1, CS3#	231	VSS
39	VSS	105	CB3*	167	VSS	233	DQ61
41	DQ10	107	VSS	169	DQ37	235	VSS
43	VSS	109	CKE0	171	VSS	237	DQ56
45	DQ21	111	VDD	173	DQ33	239	VSS
47	VSS	113	BG1	175	VSS	241	DM7#/ DBI7#
49	DQ17	115	BG0	177	DQS4#	243	VSS
51	VSS	117	VDD	179	DQS4	245	DQ62
53	DQS2#	119	A12	181	VSS	247	VSS
55	DQS2	121	A9	183	DQ38	249	DQ58
57	VSS	123	VDD	185	VSS	251	VSS
59	DQ23	125	A8	187	DQ34	253	SCL
61	VSS	127	A6	189	VSS	255	VDDSPD
63	DQ19	129	VDD	191	DQ44	257	VPP
65	VSS	131	A3	193	VSS	259	VPP

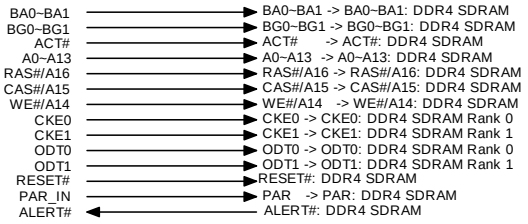
260-PIN DDR4 SODIMM BACK SIDE

Pin	Name	Pin	Name	Pin	Name	Pin	Name
2	VSS	68	VSS	134	EVENT#	196	VSS
4	DQ4	70	DQ24	136	VDD	198	DQS5#
6	VSS	72	VSS	138	CK1	200	DQS5
8	DQ0	74	DQS3#	140	CK1#	202	VSS
10	VSS	76	DQS3	142	VDD	204	DQ47
12	DM0#/ DBI0#	78	VSS	144	A0	206	VSS
14	VSS	80	DQ31	KEY		208	DQ43
16	DQ6	82	VSS			210	VSS
18	VSS	84	DQ27	146	A10/AP	212	DQ53
20	DQ2	86	VSS	148	VDD	214	VSS
22	VSS	88	CB4*	150	BA0	216	DQ48
24	DQ12	90	VSS	152	A16/RAS#	218	VSS
26	VSS	92	CB0*	154	VDD	220	DM6#/ DBI6#
28	DQ8	94	VSS	156	A15/CAS#	222	VSS
30	VSS	96	DM8#/ DBI8#*	158	A13	224	DQ54
32	DQS1#	98	VSS	160	VDD	226	VSS
34	DQS1	100	CB6*	162	NC, C0, CS2#,	228	DQ50
36	VSS	102	VSS	164	VREFCA	230	VSS
38	DQ14	104	CB7*	166	SA2	232	DQ60
40	VSS	106	VSS	168	VSS	234	VSS
42	DQ11	108	RESET#	170	DQ36	236	DQ57
44	VSS	110	CKE1	172	VSS	238	VSS
46	DQ20	112	VDD	174	DQ32	240	DQS7#
48	VSS	114	ACT#	176	VSS	242	DQS7
50	DQ16	116	ALERT#	178	DM4#/ DBI4#	244	VSS
52	VSS	118	VDD	180	VSS	246	DQ63
54	DM2#/ DBI2#	120	A11	182	DQ39	248	VSS
56	VSS	122	A7	184	VSS	250	DQ59
58	DQ22	124	VDD	186	DQ35	252	VSS
60	VSS	126	A5	188	VSS	254	SDA
62	DQ18	128	A4	190	DQ45	256	SA0
64	VSS	130	VDD	192	VSS	258	VTT
66	DQ28	132	A2	194	DQ41	260	SA1

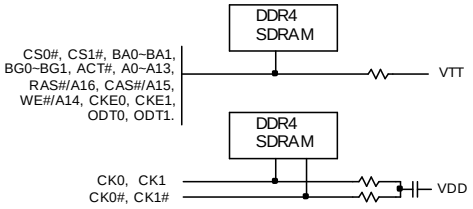
*: These pins are not used in this module.

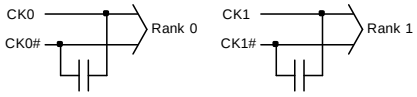
Function Block Diagram





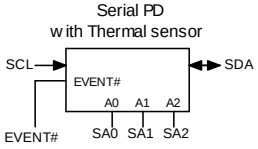
Command, address, control, and clock line terminations

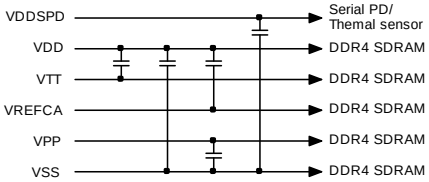




Notes:

1. ZQ resistors are 240 ohms +/-1%





Absolute Maximum Ratings

Symbol	Parameter		Min	Max	Unit	Notes
VDD	Voltage on VDD pin relative to VSS		-0.4	1.5	V	1
VDDQ	Voltage on VDDQ pin relative to VSS		-0.4	1.5	V	1
VPP	Voltage on VPP pin relative to VSS		-0.4	3.0	V	2
VIN, VOUT	Voltage on any pin relative to VSS		-0.4	1.5	V	
TSTG	Storage temperature		-55	100	^{0}C	
IL	Input leakage current; Any input 0V<VIN<VDD; VREF input 0V<VIN<0.75V; (Other pins not under test = 0V)	Address inputs, RAS#, CAS#, WE#, CS#, CKE, ODT, BA, BG, PAR_IN	-32	-32	uA	3
		CK, CK#	-16	-16	uA	3
		DM	-4	-4	uA	
IOZ	Output leakage current; 0V<VOUT<VDDQ; DQs and ODT are disabled	DQ, DQS, DQS#, ALERT#	-10	10	uA	
IVREF	VREF supply leakage current; VREF = Valid VREF level		-32	32	uA	

Notes:
1. VDD and VDDQ must be within 300mV of each other at all times; VREFCA must not be greater than 0.6 x VDDQ or less than 500mV; VREF may be less than or equal to 300mV.
2. VPP must be greater than or equal to VDD at all times.
3. Inputs are terminated to VDD/2. Input current is dependent on terminating resistance se selected in register.

DC Operating Conditions

Symbol	Parameter	Min	Typical	Max	Unit	Notes
VDD	VDD Supply Voltage	1.14	1.2	1.26	V	1
VDDQ	VDDQ Supply Voltage for Input/Output	1.14	1.2	1.26	V	1
VPP	DRAM Activating Power Supply	2.375	2.5	2.750	V	2
VREFCA (DC)	Input reference voltage CMD/ADD bus	0.49 x VDD	0.5 x VDD	0.51 x VDD	V	
VTT	Termination Reference Voltage	0.49 × VDD - 20mV	0.5 x VDDQ	0.49 × VDD + 20mV	V	3

Notes:
1. VDDQ tracks with VDD; VDDQ and VDD are tied together.
2. VPP must be greater than or equal to VDD at all times.
3. VTT termination voltages in excess of specification limit will adversely affect command and address signals' voltage margins, and reduce timing margins.

Operating Temperature Condition

Symbol	Parameter		Rating	Units	Notes
TOPER	Operating temperature	Commercial	0 to 95	^{0}C	1,2
		Industrial	-40 to +95		

Notes:
1. Operating temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC JESD51-2.
2. At -40 to +85^{o}C, operation temperature range, all DRAM specifications will be supported. The refresh rate is required to double when 85^{o}C < TOPER <= 95^{o}C.

Command/Address Input Levels

Symbol	Parameter	Min	Max	Unit	Note
VIH(DC)	DC Input High (Logic 1) Voltage	VREF + 0.075	VDD	V	1,2,3
VIL(DC)	DC Input Low (Logic 0) Voltage	VSS	VREF - 0.075	V	1,2
VIH(AC)	AC Input High (Logic 1) Voltage	VREF + 0.100	VDD	V	1,2
VIL(AC)	AC Input Low (Logic 0) Voltage	VSS	VREF - 0.100	V	1,2,3

Notes:

1. For input except RESET#. VREF = VREFCA(DC).
2. VREF = VREFCA(DC).
3. Input signal must meet VIL/VIH(AC) to meet tIS/tIH timings.

AC & DC Output Levels

Symbol	Parameter	Value	Unit	Note
VOH(DC)	DC output high measurement level (for IV curve linearity)	1.1 x VDDQ	V	
VOM(DC)	DC output mid measurement level (for IV curve linearity)	0.8 x VDDQ	V	
VOL(DC)	DC output low measurement level (for IV curve linearity)	0.5 x VDDQ	V	
VOH(AC)	AC output high measurement level (for output SR)	(0.7 + 0.15) x VDDQ	V	1
VOL(AC)	AC output low measurement level (for output SR)	(0.7 - 0.15) x VDDQ	V	1
VOHdiff(AC)	AC differential output high measurement level (for output SR)	+0.3 x VDDQ	V	2
VOLdiff(AC)	AC differential output low measurement level (for output SR)	-0.3 x VDDQ	V	2

Notes:

1. The swing of ± 0.15 × VDDQ is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of RZQ/7Ω and an effective test load of 50Ω to VTT = VDDQ.
2. The swing of ± 0.3 × VDDQ is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of RZQ/7Ω and an effective test load of 50Ω to VTT = VDDQ.

Input/Output Capacitance

TA=25^{0}C, f=100MHz

Parameter	Symbol	N6/M4/K2 (DDR4-2133/1866/1600)		Unit
		Min	Max	
Input capacitance (BA0~BA1, BG0~BG1, A0~A13, RAS#/A16, CAS#/A15, WE#/A14, ACT#)	CIN1	7.2	16.8	pF
Input capacitance (CKE0, CKE1), (ODT0, ODT1), (CS0#, CS1#)	CIN2	5.6	10.4	pF
Input capacitance (CK0, CK0#, CK1, CK1#)	CIN3	5.6	10.4	pF
Input/Output capacitance (DQ, DQS, DQS#, DM)	CIO	5.4	6.8	pF

IDD Specification

Parameter	Symbol	N6 (DDR4-2133)	M4 (DDR4-1866)	K2 (DDR4-1600)	Unit
Operating One Bank Active-Precharge Current (AL=0) CKE: HIGH; External clock: On; tCK, nRC, nRAS, CL: see the previous table; BL: 8; AL: 0; CS#: HIGH between ACT and PRE; Command, address, bank group address, bank address inputs: partially toggling according to the next table; Data I/O: VDDQ; DM#: stable at 0; Bank activity: cycling with one bank active at a time: 0, 0, 1, 1, 2, 2,...; Output buffer and RTT: enabled in mode registers; ODT signal: stable at 0	IDD0	352	352	352	mA
Operating One Bank Active-Read-Precharge Current (AL=0) CKE: HIGH; External clock: on; tCK, nRC, nRAS, nRCD, CL: see the previous table; BL: 8; AL: 0; CS#: HIGH between ACT, RD and PRE; Command, address, bank group address, bank address inputs, Data I/O: partially toggling according to the IDD1 Measurement-Loop Pattern table; DM#: stable at 0; Bank activity: cycling with one bank active at a time: 0, 0, 1, 1, 2, 2, ... ; Output buffer and RTT: enabled in mode registers; ODT Signal: stable at 0	IDD1	416	416	416	mA
Precharge Standby Current (AL=0) CKE: HIGH; External clock: On; tCK, CL: see the previous table; BL: 8; AL: 0; CS#: stable at 1; Command, address, bank group address, bank address Inputs: partially toggling according to the IDD2N and IDD3N Measurement-Loop Pattern table; Data I/O: VDDQ; DM#: stable at 1; Bank activity: all banks closed; Output buffer and RTT: enabled in mode registers; ODT signal: stable at 0	IDD2N	176	176	176	mA
Precharge Power-Down Current CKE: LOW; External clock: on; tCK, CL: see the previous table; BL: 8; AL: 0; CS#: stable at 1; Command, address, bank group address, bank address inputs: stable at 0; Data I/O: VDDQ; DM#: stable at 1; Bank activity: all banks closed; Output buffer and RTT: Enabled in mode registers; ODT signal: stable at 0	IDD2P	256	256	256	mA
Precharge Quiet Standby Current CKE: HIGH; External clock: on; tCK, CL: see the previous table; BL: 8; AL: 0; CS#: stable at 1; Command, address, bank group address, bank address inputs: stable at 0; Data I/O: VDDQ; DM#: stable at 1; Bank activity: all banks closed; Output buffer and RTT: Enabled in mode registers; ODT signal: stable at 0	IDD2Q	240	240	240	mA
Active Standby Current (AL=0) CKE: HIGH; External clock: on; tCK, CL: see the previous table; BL: 8; AL: 0; CS#: stable at 1; Command, address, bank group address, bank address inputs: partially toggling according to the IDD2N and IDD3N Measurement-Loop Pattern table; Data I/O: VDDQ; DM#: stable at 1; Bank activity: all banks open; Output buffer and RTT: Enabled in mode registers2; ODT signal: stable at 0	IDD3N	240	240	240	mA
Active Power-Down Current (AL=0) CKE: LOW; External clock: on; tCK, CL: see the previous table; BL: 8; AL: 0; CS#: stable at 1; Command, address, bank group address, bank address inputs: stable at 1; Data I/O: VDDQ; DM#: stable at 1; Bank activity: all banks open; Output buffer and RTT: Enabled in mode registers 2; ODT signal: stable at 0	IDD3P	480	480	480	mA
Operating Burst Read Current (AL=0) CKE: HIGH; External clock: on; tCK, CL: see the previous table; BL: 8; AL: 0; CS#: HIGH between RD; Command, address, bank group address, bank address inputs: partially toggling according to the IDD4R and IDDQ4R Measurement-Loop Pattern table; Data I/O: seamless read data burst with different data between one burst and the next one according to the IDD4R and IDDQ4R Measurement-Loop Pattern table; DM#: table at 1; Bankactivity: all banks open, RD commands cycling through banks: 0, 0, 1, 1, 2, 2, ...; Output buffer and RTT: Enabled in mode registers; ODT signal: stable at 0	IDD4R	752	752	752	mA
Operating Burst Write Current (AL=0) CKE: HIGH; External clock: on; tCK, CL: see the previous table; BL: 8; AL: 0; CS#: HIGH between WR; Command, address, bank group address, bank address inputs: partially toggling according to the IDD4W Measurement-Loop Pattern table; Data I/O: seamless write data burst with different data between one burst and the next one according to the IDD4W Measurement-Loop Pattern table; DM#: stable at 0; Bank activity: all banks open, WR commands cycling through banks: 0, 0, 1, 1, 2, 2, ...; Output buffer and RTT: enabled in mode registers; ODT signal: stable at HIGH	IDD4W	664	664	664	mA
Burst Refresh Current (1X REF) CKE: HIGH; External clock: on; tCK, CL, nRFC: see the previous table; BL: 8; AL: 0; CS#: HIGH between REF; Command, address, bank group address, bank address inputs: partially toggling according to the IDD5B Measurement-Loop Pattern table; Data I/O: VDDQ; DM#: stable at 1; Bank activity: REF command every nRFC; Output buffer and RTT: enabled in mode registers; ODT signal: stable at 0	IDD5B	2448	2448	2448	mA
Self Refresh Current: Normal Temperature Range TC: 0–85°C; Auto self refresh (ASR): disabled; Self refresh temperature range (SRT): normal; CKE: LOW; External clock: off; CK and CK#: LOW; CL: see the table above; BL: 8; AL: 0; CS#, command, address, bank group address, bank address, data I/O: VDDQ; DM#: stable at 1; Bank activity: SELF REFRESH operation; Output buffer and RTT: enabled in mode registers; ODT signal: mid-level	IDD6N	192	192	192	mA
Operating Bank Interleave Read Current CKE: HIGH; External clock: on; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: see the previous table; BL: 8; AL: CL -1; CS#: HIGH between ACT and RDA; Command, address, group bank adress, bank address inputs: partially toggling according to the IDD7 Measurement-Loop Pattern table; Data I/O: read data bursts with different databetween one burst and the next one according to the IDD7 Measurement-Loop Pattern table; DM: stable at 0; Bank activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing, see the IDD7 Measurement-Loop Pattern table; Output buffer and RTT: enabled in mode registers; ODT signal: stable at 0	IDD7	1192	1192	1192	mA

Note: IDD specification is based on Samsung D-die components.

AC TIMING PARAMETERS & SPECIFICATIONS

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Units
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	
Clock Timing										
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	-	8	-	8	-	8	-	ns
Average Clock Period	tCK(avg)	1.25	<1.5	1.071	<1.25	0.938	<1.071	0.833	<0.938	ns
Average high pulse width	tCH(avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)
Average low pulse width	tCL(avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)
Absolute Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min_tot	tCK(avg)max + tJIT(per)max_tot	tCK(avg)min + tJIT(per)min_tot	tCK(avg)max + tJIT(per)max_tot	tCK(avg)min + tJIT(per)min_tot	tCK(avg)max + tJIT(per)max_tot	tCK(avg)min + tJIT(per)min_tot	tCK(avg)max + tJIT(per)max_tot	tCK(avg)
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	0.45	-	0.45	-	0.45	-	tCK(avg)
Absolute clock LOW pulse width	tCL(abs)	0.45	-	0.45	-	0.45	-	0.45	-	tCK(avg)
Clock Period Jitter- total	JIT(per)_tot	-63	63	-54	54	-47	47	-42	42	ps
Clock Period Jitter- deterministic	JIT(per)_dj	-31	31	-27	27	-23	23	-21	21	ps
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-50	50	-43	43	-38	38	-33	33	ps
Cycle to Cycle Period Jitter	tJIT(cc)_total	125		107		94		83		ps
Cycle to Cycle Period Jitter determin- istic	tJIT(cc)_dj	63		54		47		42		ps
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	100		86		75		67		ps
Duty Cycle Jitter	tJIT(duty)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ps
Cumulative error across 2 cycles	tERR(2per)	-92	92	-79	79	-69	69	-61	61	ps
Cumulative error across 3 cycles	tERR(3per)	-109	109	-94	94	-82	82	-73	73	ps
Cumulative error across 4 cycles	tERR(4per)	-121	121	-104	104	-91	91	-81	81	ps
Cumulative error across 5 cycles	tERR(5per)	-131	131	-112	112	-98	98	-87	87	ps
Cumulative error across 6 cycles	tERR(6per)	-139	139	-119	119	-104	104	-92	92	ps
Cumulative error across 7 cycles	tERR(7per)	-145	145	-124	124	-109	109	-97	97	ps
Cumulative error across 8 cycles	tERR(8per)	-151	151	-129	129	-113	113	-101	101	ps
Cumulative error across 9 cycles	tERR(9per)	-156	156	-134	134	-117	117	-104	104	ps
Cumulative error across 10 cycles	tERR(10per)	-160	160	-137	137	-120	120	-107	107	ps
Cumulative error across 11 cycles	tERR(11per)	-164	164	-141	141	-123	123	-110	110	ps
Cumulative error across 12 cycles	tERR(12per)	-168	168	-144	144	-126	126	-112	112	ps
Cumulative error across 13 cycles	tERR(13per)	-172	172	-147	147	-129	129	-114	114	ps
Cumulative error across 14 cycles	tERR(14per)	-175	175	-150	150	-131	131	-116	116	ps
Cumulative error across 15 cycles	tERR(15per)	-178	178	-152	152	-133	133	-118	118	ps
Cumulative error across 16 cycles	tERR(16per)	-180	189	-155	155	-135	135	-120	120	ps
Cumulative error across 17 cycles	tERR(17per)	-183	183	-157	157	-137	137	-122	122	ps
Cumulative error across 18 cycles	tERR(18per)	-185	185	-159	159	-139	139	-124	124	ps
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	^{t}ERR(nper)min = ((1 + 0.68ln(n)) * ^{t}JIT(per)_total min) ^{t}ERR(nper)max = ((1 + 0.68ln(n)) * ^{t}JIT(per)_total max)								ps
Command and Address setup time to CK_t, CK_c referenced to Vih(ac) / Vil(ac) levels	tIS(base)	115	-	100	-	80	-	62	-	ps
Command and Address setup time to CK_t, CK_c referenced to Vref levels	tIS(Vref)	215	-	200	-	180	-	162	-	ps
Command and Address hold time to CK_t, CK_c referenced to Vih(dc) / Vil(dc) levels	tIH(base)	140	-	125	-	105	-	87	-	ps
Command and Address hold time to CK_t, CK_c referenced to Vref levels	tIH(Vref)	215	-	200	-	180	-	162	-	ps

AC TIMING PARAMETERS & SPECIFICATIONS

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Units
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	
Control and Address Input pulse width for each input	tIPW	600	-	525	-	460	-	410	-	ps
Command and Address Timing										
CAS_n to CAS_n command delay for same bank group	tCCD_L	5	-	5	-	6	-	6	-	nCK
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	4	-	4	-	4	-	nCK
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nCK,6ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(1K)	Max(4nCK,5ns)	-	Max(4nCK,4.2ns)	-	Max(4nCK,3.7ns)	-	Max(4nCK,3.3ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to different bank group for 1/ 2KB page size	tRRD_S(1/ 2K)	Max(4nCK,5ns)	-	Max(4nCK,4.2ns)	-	Max(4nCK,3.7ns)	-	Max(4nCK,3.3ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK,7.5ns)	-	Max(4nCK,6.4ns)	-	Max(4nCK,6.4ns)	-	Max(4nCK,6.4ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nCK,6ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,4.9ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L(1/ 2K)	Max(4nCK,6ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,4.9ns)	-	nCK
Four activate window for 2KB page size	tFAW_2K	Max(28nCK,35ns)	-	Max(28nCK,30ns)	-	Max(28nCK,30ns)	-	Max(28nCK, 30ns)	-	ns
Four activate window for 1KB page size	tFAW_1K	Max(20nCK,25ns)	-	Max(20nCK,23ns)	-	Max(20nCK,21ns)	-	Max(20nCK, 21ns)	-	ns
Four activate window for 1/2KB page size	tFAW_1/2K	Max(16nCK,20ns)	-	Max(16nCK,17ns)	-	Max(16nCK,15ns)	-	Max(16nCK, 13ns)	-	ns
Delay from start of internal write transaction to internal read command for different bank group	tWTR_S	max(2nCK,2.5ns)	-	max(2nCK,2.5ns)	-	max(2nCK,2.5ns)	-	max (2nCK, 2.5ns)	-	
Delay from start of internal write transaction to internal read command for same bank group	tWTR_L	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	max (4nCK,7.5ns)	-	
Internal READ Command to PRE-CHARGE Command delay	tRTP	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	max (4nCK,7.5ns)	-	
WRITE recovery time	tWR	15	-	15	-	15	-	15	-	ns
Write recovery time when CRC and DM are enabled	tWR_CRC_DM	tWR+max (4nCK,3.75ns)	-	tWR+max (5nCK,3.75ns)	-	tWR+max (5nCK,3.75ns)	-	tWR+max (5nCK,3.75 ns)	-	ns
delay from start of internal write transaction to internal read command for different bank group with both CRC and DM enabled	tWTR_S_CRC_DM	tWTR_S+max (4nCK,3.75ns)	-	tWTR_S+max (5nCK,3.75ns)	-	tWTR_S+max (5nCK,3.75ns)	-	tWTR_S+max (5nCK,3.75ns)	-	ns
delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	tWTR_L_CRC_DM	tWTR_L+max (4nCK,3.75ns)	-	tWTR_L+max (5nCK,3.75ns)	-	tWTR_L+max (5nCK,3.75ns)	-	tWTR_L+max (5nCK,3.75ns)	-	ns
DLL locking time	tDLLK	597	-	597	-	768	-	768	-	nCK
Mode Register Set command cycle time	tMRD	8	-	8	-	8	-	8	-	nCK
Mode Register Set command update delay	tMOD	max(24nCK,15ns)	-	max(24nCK,15ns)	-	max(24nCK,15ns)	-	max(24nCK, 15ns)	-	
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	1	-	nCK
Multi Purpose Register Write Recov- ery Time	tWR_MPR	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	-
Auto precharge write recovery + pre-charge time	tDAL(min)	Programmed WR + roundup (tRP / tCK(avg))								nCK
CS_n to Command Address Latency										
CS_n to Command Address Latency	tCAL	3	-	4	-	4	-	5	-	nCK

AC TIMING PARAMETERS & SPECIFICATIONS

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Units
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	
DRAM Data Timing										
DQS_t,DQS_c to DQ skew, per group, per access	tDQSQ	-	TBD	-	TBD	-	TBD	-	TBD	tCK(avg) /2
DQS_t,DQS_c to DQ Skew determin- istic, per group, per access	tDQSQ	-	TBD	-	TBD	-	TBD	-	TBD	tCK(avg) /2
DQ output hold time from DQS_t,DQS_c	tQH	TBD	-	TBD	-	TBD	-	TBD	-	tCK(avg) /2
DQ output hold time deterministic from DQS_t, DQS_c	tQH	TBD	-	TBD	-	TBD	-	TBD	-	UI
DQS_t,DQS_c to DQ Skew total, per group, per access; DBI enabled	tDQSQ	-	TBD	-	TBD	-	TBD	-	TBD	UI
DQ output hold time total from DQS_t, DQS_c; DBI enabled	tQH	TBD	-	TBD	-	TBD	-	TBD	-	UI
DQ to DQ offset , per group, per ac- cess referenced to DQS_t, DQS_c	tDQSQ	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	UI
Data Strobe Timing										
DQS_t, DQS_c differential READ Pre- amble (2 clock preamble)	tRPRE	0.9	TBD	0.9	TBD	0.9	TBD	0.9	TBD	tCK
DQS_t, DQS_c differential READ Postamble	tRPST	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	tCK
DQS_t,DQS_c differential output high time	tQSH	0.4	-	0.4	-	0.4	-	0.4	-	tCK
DQS_t,DQS_c differential output low time	tQSL	0.4	-	0.4	-	0.4	-	0.4	-	tCK
DQS_t, DQS_c differential WRITE Preamble	tWPRE	0.9	-	0.9	-	0.9	-	0.9	-	tCK
DQS_t, DQS_c differential WRITE Postamble	tWPST	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	tCK
DQS_t and DQS_c low-impedance time (Referenced from RL-1)	tLZ(DQS)	-450	225	-390	195	-360	180	-300	150	ps
DQS_t and DQS_c high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	225	-	195	-	180	-	150	ps
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble)	tDQSS	-0.27	0.27	-0.27	0.27	-0.27	0.27	-0.27	0.27	tCK
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	0.18	-	0.18	-	0.18	-	tCK
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	tDSH	0.18	-	0.18	-	0.18	-	0.18	-	tCK
MPSM Timing										
Command path disable delay upon MPSM entry	tMPED	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCP- DED(min)	-	
Valid clock requirement after MPSM entry	tCKMPE	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCP- DED(min)	-	
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX(min)		tCKSRX(min)		tCKSRX(min)		tCK- SRX(min)	-	
Exit MPSM to commands not requir- ing a locked DLL	tXMP	TBD		TBD		TBD		TBD	-	
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP(min) + tXSDLL(min)		tXMP(min) + tXSDLL(min)		tXMP(min) + tXSDLL(min)		tXMP(min) + tXS- DLL(min)	-	
CS setup time to CKE	tMPX_S	TBD	-	TBD	-	TBD	-	TBD	-	
CS hold time to CKE	tMPX_H	TBD	-	TBD	-	TBD	-	TBD	-	
Calibration Timing										
Power-up and RESET calibration time	tZQinit	1024	-	1024	-	1024	-	1024	-	nCK

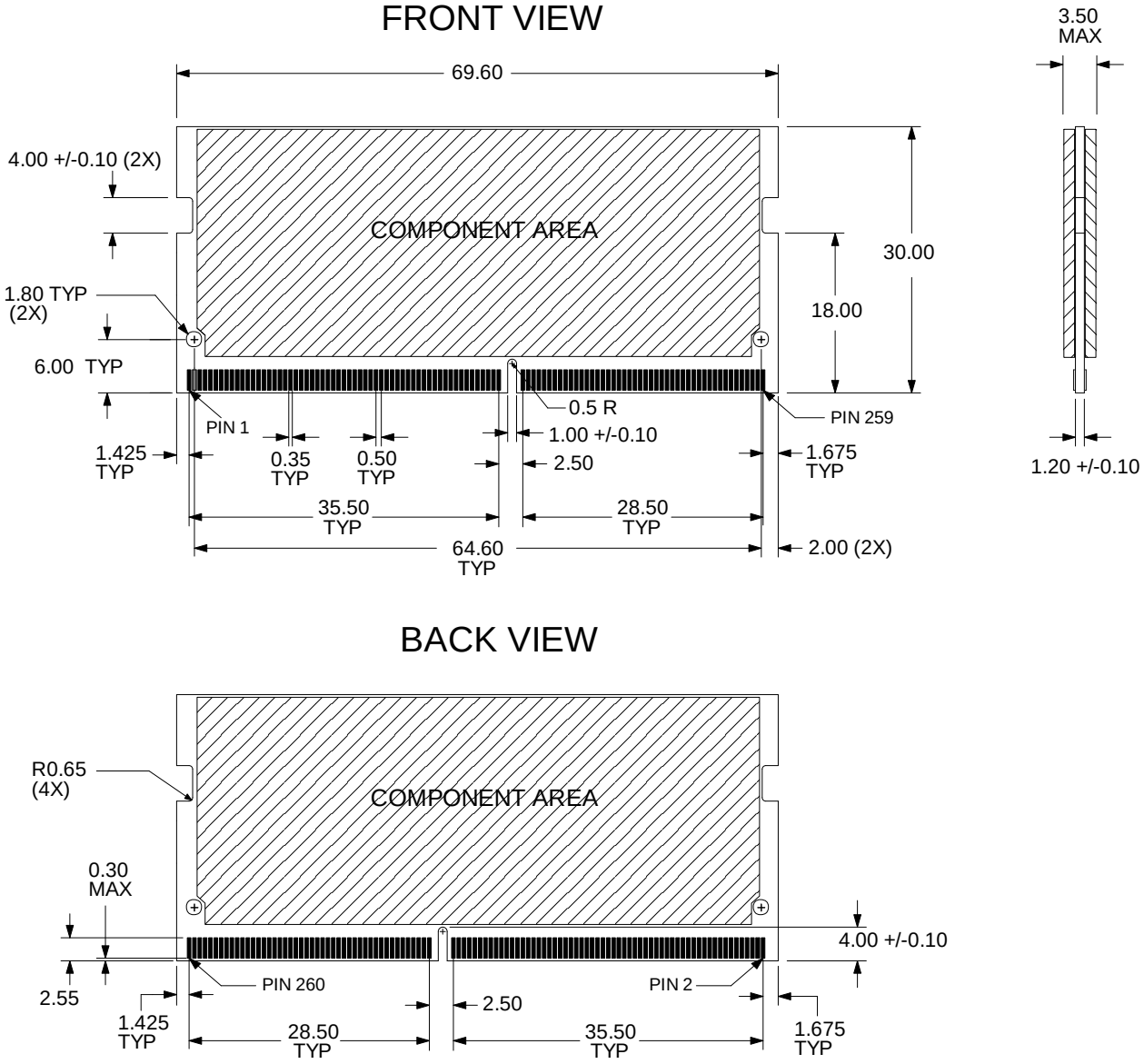
AC TIMING PARAMETERS & SPECIFICATIONS

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Units
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	
Normal operation Full calibration time	tZQoper	512	-	512	-	512	-	512	-	nCK
Normal operation Short calibration time	tZQCS	128	-	128	-	128	-	128	-	nCK
Reset/Self Refresh Timing										
Exit Reset from CKE HIGH to a valid command	tXPR	max (5nCK,tRFC(min)+ 10ns)	-	max (5nCK,tRFC(min)+ 10ns)	-	max (5nCK,tRFC(min)+ 10ns)	-	max (5nCK,tRFC (min)+10ns)	-	
Exit Self Refresh to commands not re- quiring a locked DLL	tXS	tRFC(min)+1 0ns	-	tRFC(min)+1 0ns	-	tRFC(min)+1 0ns	-	tRFC(min)+ 10ns	-	
SRX to commands not requiring a locked DLL in Self Refresh ABORT	tXS_ABORT (min)	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-	tRFC4(min) +10ns	-	
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	tXS_FAST (min)	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-	tRFC4(min) +10ns	-	
Exit Self Refresh to commands requir- ing a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	
Minimum CKE low width for Self re- fresh entry to exit timing	tCKESR	tCKE(min)+1 nCK	-	tCKE(min)+1 nCK	-	tCKE(min)+1 nCK	-	tCKE(min)+ 1nCK	-	
Minimum CKE low width for Self re- fresh entry to exit timing with CA Pari- ty enabled	tCKESR_ PAR	tCKE(min)+ 1nCK+PL	-	tCKE(min)+ 1nCK+PL	-	tCKE(min)+ 1nCK+PL	-	tCKE(min)+ 1nCK+PL	-	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nCK,10 ns)	-	max(5nCK,10 ns)	-	max(5nCK,10 ns)	-	max (5nCK,10ns)	-	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	tCKSRE_PA R	max (5nCK,10ns) +PL	-	max (5nCK,10ns) +PL	-	max (5nCK,10ns) +PL	-	max (5nCK,10ns) +PL	-	
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK,10 ns)	-	max(5nCK,10 ns)	-	max(5nCK,10 ns)	-	max (5nCK,10ns)	-	
Power Down Timing										
Exit Power Down with DLL on to any valid command;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max (4nCK,6ns)	-	max (4nCK,6ns)	-	max (4nCK,6ns)	-	max (4nCK,6ns)	-	
CKE minimum pulse width	tCKE	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	
Command pass disable delay	tCPDED	4	-	4	-	4	-	4	-	nCK
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	
Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-	2	-	2	-	nCK
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	1	-	2	-	2	-	nCK
Timing of RD/RDA command to Pow- er Down entry	tRDPDEN	RL+4+1	-	RL+4+1	-	RL+4+1	-	RL+4+1	-	nCK
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(tWR/ tCK(avg))	-	WL+4+(tWR/ tCK(avg))	-	WL+4+(tWR/ tCK(avg))	-	WL+4+(tWR /tCK(avg))	-	nCK
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+ 1	-	nCK
Timing of WR command to Power Down entry (BC4MRS)	tWRPBC4D EN	WL+2+(tWR/ tCK(avg))	-	WL+2+(tWR/ tCK(avg))	-	WL+2+(tWR/ tCK(avg))	-	WL+2+(tWR /tCK(avg))	-	nCK
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPBC4 DEN	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+ 1	-	nCK
Timing of REF command to Power Down entry	tREFPDEN	1	-	1	-	2	-	2	-	nCK
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	

AC TIMING PARAMETERS & SPECIFICATIONS

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Units
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	
PDA Timing										
Mode Register Set command cycle time in PDA mode	tMRD_PDA	max(16nCK,10ns)		max(16nCK,10ns)		max(16nCK,10ns)		max(16nCK, 10ns)		
Mode Register Set command update delay in PDA mode	tMOD_PDA	tMOD		tMOD		tMOD		tMOD		
ODT Timing										
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	ns
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	ns
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)
Write Leveling Timing										
First DQS_t/DQS_n rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	40	-	40	-	nCK
DQS_t/DQS_n delay after write level- ing mode is programmed	tWLDQSEN	25	-	25	-	25	-	25	-	nCK
Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/ DQS_n crossing	tWLS	0.13	-	0.13	-	0.13	-	0.13	-	tCK(avg)
Write leveling hold time from rising DQS_t/DQS_n crossing to rising CK_t, CK_ crossing	tWLH	0.13	-	0.13	-	0.13	-	0.13	-	tCK(avg)
Write leveling output delay	tWLO	0	9.5	0	9.5	0	9.5	0	9.5	ns
Write leveling output error	tWLOE									ns
CA Parity Timing										
Commands not guaranteed to be exe- cuted during this time	tPAR_UNKNOWN	-	PL	-	PL	-	PL	-	PL	
Delay from errant command to ALERT_n assertion	tPAR_ALERT_ON	-	PL+6ns	-	PL+6ns	-	PL+6ns	-	PL+6ns	
Pulse width of ALERT_n signal when asserted	tPAR_ALERT_PW	48	96	56	112	64	128	72	144	nCK
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALERT_RSP	-	43	-	50	-	57	-	64	nCK
Parity Latency	PL	4		4		4		5		nCK
CRC Error Reporting										
CRC error to ALERT_n latency	tCRC_ALERT	3	13	3	13	3	13	3	13	ns
CRC ALERT_n pulse width	CRC_ALERT_PW	6	10	6	10	6	10	6	10	nCK
tREFI										
tRFC1 (min)	2Gb	160	-	160	-	160	-	160	-	ns
	4Gb	260	-	260	-	260	-	260	-	ns
	8Gb	350	-	350	-	350	-	350	-	ns
	16Gb	TBD	-	TBD	-	TBD	-	TBD	-	ns
tRFC2 (min)	2Gb	110	-	110	-	110	-	110	-	ns
	4Gb	160	-	160	-	160	-	160	-	ns
	8Gb	260	-	260	-	260	-	260	-	ns
	16Gb	TBD	-	TBD	-	TBD	-	TBD	-	ns
tRFC4 (min)	2Gb	90	-	90	-	90	-	90	-	ns
	4Gb	110	-	110	-	110	-	110	-	ns
	8Gb	160	-	160	-	160	-	160	-	ns
	16Gb	TBD	-	TBD	-	TBD	-	TBD	-	ns

Package Dimensions



Note: 1. All dimensions are in millimeters with tolerance +/- 0.15mm unless otherwise specified.
2. The dimensional diagram is for reference only.

Revision History:

Date	Rev.	Page	Changes
06/05/2014	0.01	All	Preliminary