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Jameco Part Number 890939

Improved Quad CMOS Analog Switches

FEATURES

- ± 22 -V Supply Voltage Rating
- TTL and CMOS Compatible Logic
- Low On-Resistance— $r_{DS(on)}$: 50 Ω
- Low Leakage— $I_{D(on)}$: 20 pA
- Single Supply Operation Possible
- Extended Temperature Range
- Fast Switching— t_{ON} : 120 ns
- Low Charge Injection—Q: 1 pC

BENEFITS

- Wide Analog Signal Range
- Simple Logic Interface
- Higher Accuracy
- Minimum Transients
- Reduced Power Consumption
- Superior to DG211/212
- Space Savings (TSSOP)

APPLICATIONS

- Industrial Instrumentation
- Test Equipment
- Communications Systems
- Disk Drives
- Computer Peripherals
- Portable Instruments
- Sample-and-Hold Circuits

DESCRIPTION

The DG211B/212B analog switches are highly improved versions of the industry-standard DG211/212. These devices are fabricated in Vishay Siliconix' proprietary silicon gate CMOS process, resulting in lower on-resistance, lower leakage, higher speed, and lower power consumption.

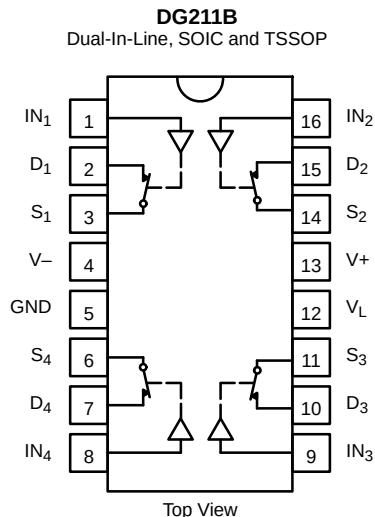
These quad single-pole single-throw switches are designed for a wide variety of applications in telecommunications, instrumentation, process control, computer peripherals, etc. An improved charge injection compensation design minimizes switching transients. The DG211B and DG212B can handle

up to ± 22 V, and have an improved continuous current rating of 30 mA. An epitaxial layer prevents latchup.

All devices feature true bi-directional performance in the on condition, and will block signals to the supply levels in the off condition.

The DG211B is a normally closed switch and the DG212B is a normally open switch. (See Truth Table.)

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE		
Logic	DG211B	DG212B
0	ON	OFF
1	OFF	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

ORDERING INFORMATION		
Temp Range	Package	Part Number
-40 to 85°C	16-Pin Plastic DIP	DG211BDJ
		DG212BDJ
	16-Pin Narrow SOIC	DG211BDY
		DG212BDY
	16-Pin TSSOP	DG211BDQ
		DG212BDQ

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V-

V+ 44 V

GND 25 V

Digital Inputs^a V_S, V_D (V-) -2 V to (V+) +2 V
or 30 mA, whichever occurs first

Current, Any Terminal 30 mA

Peak Current, S or D

(Pulsed at 1 ms, 10% duty cycle max) 100 mA

Storage Temperature -65 to 125°C

Power Dissipation (Package)^b

16-Pin Plastic DIP^c 470 mW

16-Pin Narrow SOIC and TSSOP^d 640 mW

Notes:

a. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

b. All leads welded or soldered to PC Board.

c. Derate 6.5 mW/°C above 75°C

d. Derate 7.6 mW/°C above 75°C

SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

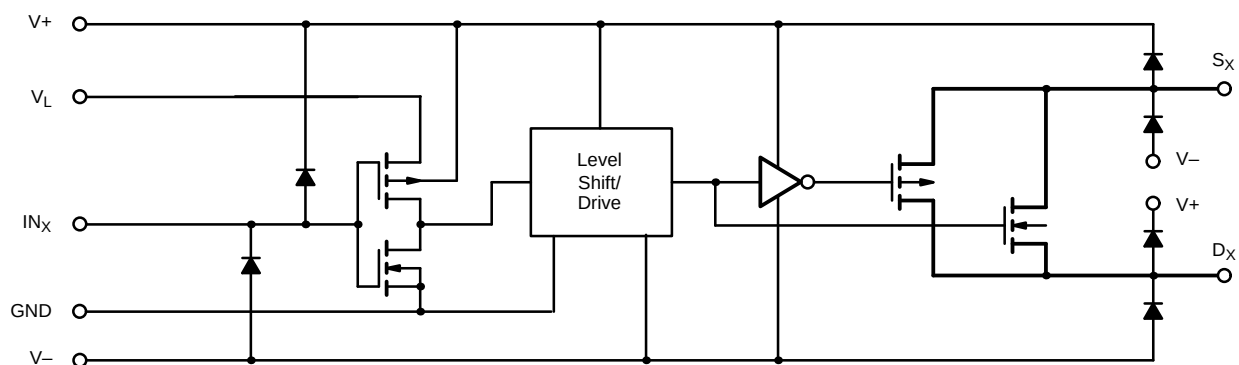


FIGURE 1.



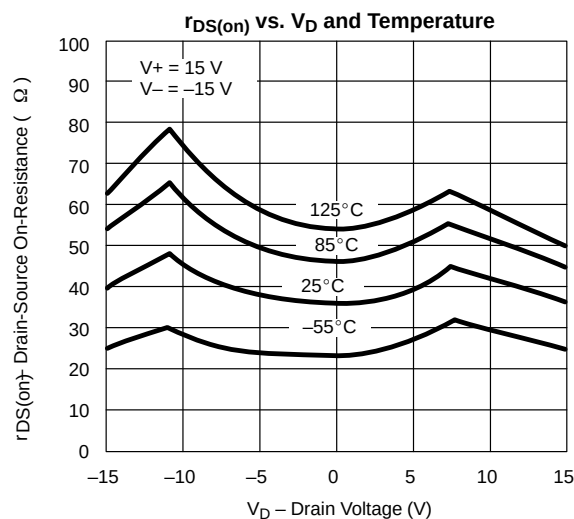
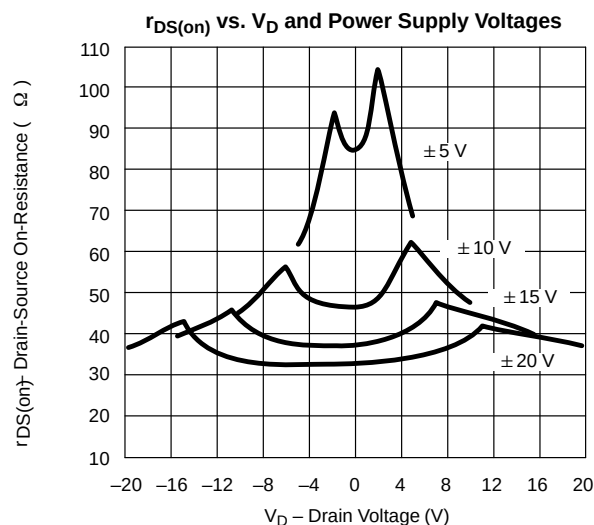
SPECIFICATIONS							
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V VL = 5 V, VIN = 2.4 V, 0.8 V ^e	Temp ^a	D Suffix −40 to 85°C			Unit
				Min ^b	Typ ^c	Max ^b	
Analog Switch							
Analog Signal Range ^d	V _{ANALOG}		Full	−15		15	V
Drain-Source On-Resistance	r _{DS(on)}	V _D = ± 10 V, I _S = 1 mA	Room Full		45	85 100	Ω
r _{DS(on)} Match	Δr _{DS(on)}		Room		2		
Source Off Leakage Current	I _{S(off)}	V _S = ± 14 V, V _D = ∓ 14 V	Room Full	−0.5 −5	± 0.01	0.5 5	nA
Drain Off Leakage Current	I _{D(off)}	V _D = ± 14 V, V _S = ∓ 14 V	Room Full	−0.5 −5	± 0.01	0.5 5	
Drain On Leakage Current	I _{D(on)}	V _S = V _D = ± 14 V	Room Full	−0.5 −10	± 0.02	0.5 10	
Digital Control							
Input Voltage High	V _{INH}		Full	2.4			V
Input Voltage Low	V _{INL}		Full			0.8	
Input Current	I _{INH} or I _{INL}	V _{INH} or V _{INL}	Full	−1		1	μA
Input Capacitance	C _{IN}		Room		5		pF
Dynamic Characteristics							
Turn-On Time	t _{ON}	V _S =10 V See Figure 2	Room			300	ns
Turn-Off Time	t _{OFF}		Room			200	
Charge Injection	Q	C _L = 1000 pF, V _g = 0 V, R _g = 0 Ω	Room		1		pC
Source-Off Capacitance	C _{S(off)}	V _S = 0 V, f = 1 MHz	Room		5		pF
Drain-Off Capacitance	C _{D(off)}		Room		5		
Channel On Capacitance	C _{D(on)}	V _D = V _S = 0 V, f = 1 MHz	Room		16		
Off Isolation	OIRR	C _L = 15 pF, R _L = 50 Ω V _S = 1 V _{RMS} , f = 100 kHz	Room		90		dB
Channel-to-Channel Crosstalk	X _{TALK}		Room		95		
Power Supply							
Positive Supply Current	I ₊	V _{IN} = 0 or 5 V	Room Full			10 50	μA
Negative Supply Current	I _−		Room Full	−10 −50			
Logic Supply Current	I _L		Room Full			10 50	
Power Supply Range for Continuous Operation	V _{OP}		Full	± 4.5		± 22	V

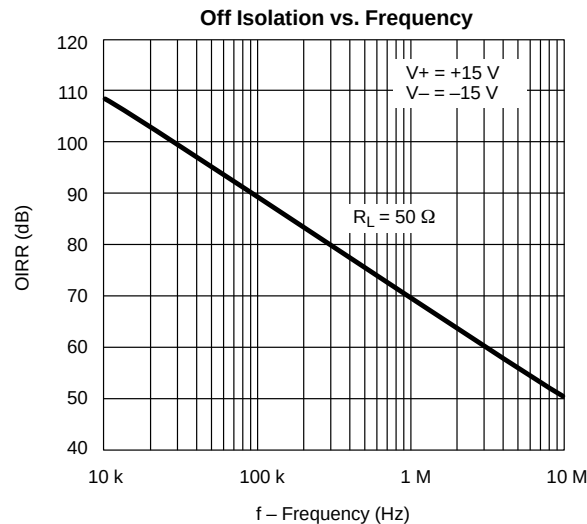
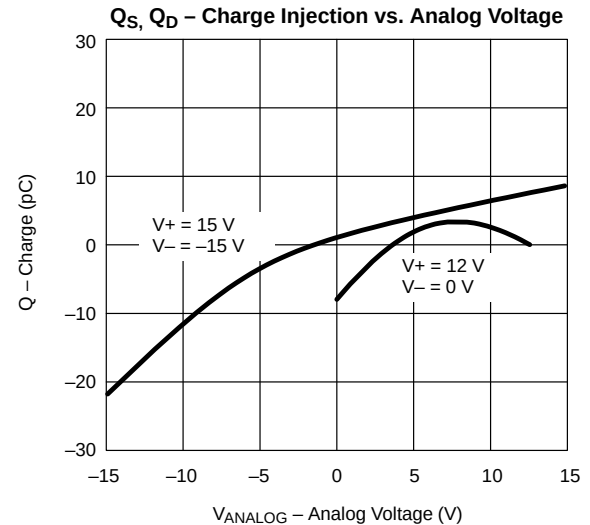
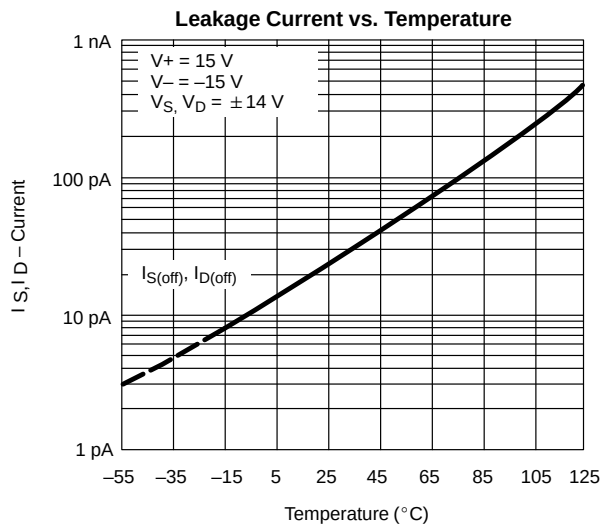
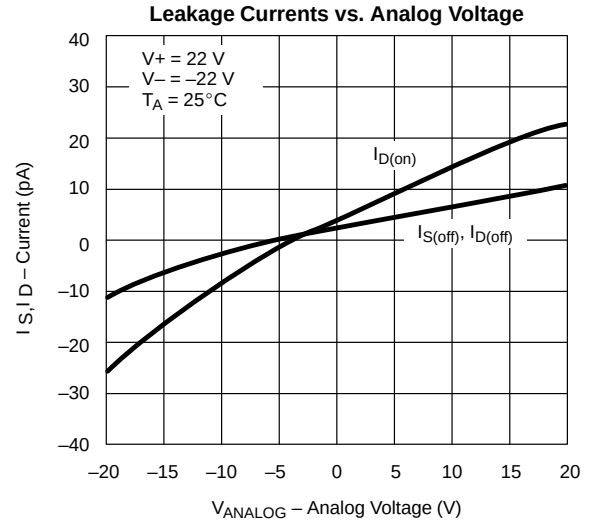
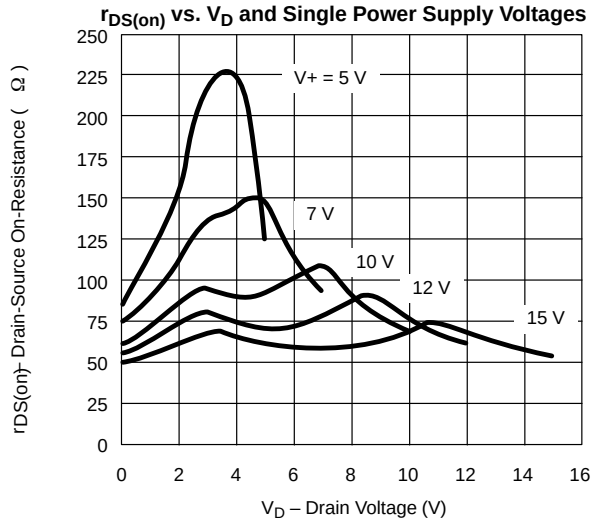
SPECIFICATIONS FOR SINGLE SUPPLY

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 12 V, V− = 0 V VL = 5 V, VIN = 2.4 V, 0.8 V ^e	Temp ^a	D Suffix −40 to 85°C			Unit
				Min ^b	Typ ^c	Max ^b	
Analog Switch							
Analog Signal Range ^d	VANALOG		Full	0		12	V
Drain-Source On-Resistance	rDS(on)	VD = 3 V, 8 V, IS = 1 mA	Room Full		90	160 200	Ω
Dynamic Characteristics							
Turn-On Time	tON	VS = 8 V See Figure 2	Room			300	ns
Turn-Off Time	tOFF		Room			200	
Charge Injection	Q	CL = 1 nF, Vgen= 6 V, Rgen = 0 Ω	Room		4		pC
Power Supply							
Positive Supply Current	I+	VIN = 0 or 5 V	Room Full			10 50	μA
Negative Supply Current	I−		Room Full	−10 −50			
Logic Supply Current	IL	Room Full			10 50		
Power Supply Range for Continuous Operation	VOP		Full	+4.5		+25	V

Notes:

- Room = 25°C, Full = as determined by the operating temperature suffix.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- Guaranteed by design, not subject to production test.
- V_{IN} = input voltage to perform proper function.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)


TEST CIRCUITS

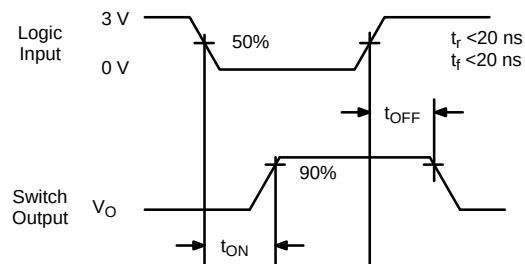
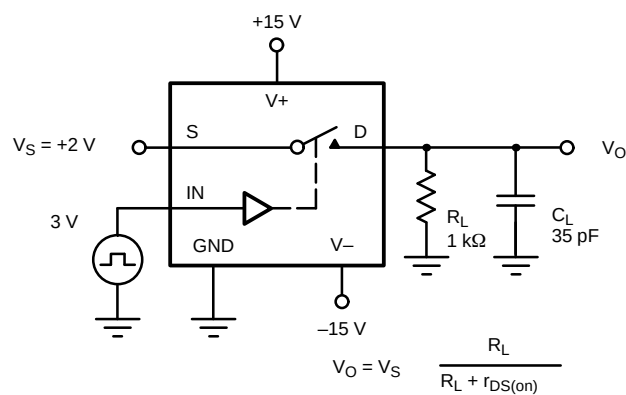


FIGURE 2. Switching Time

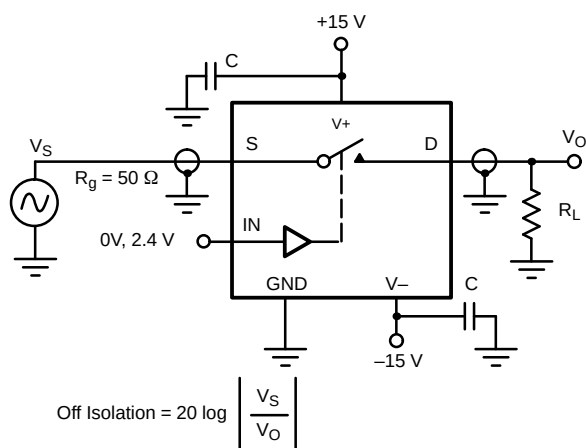


FIGURE 3. Off Isolation

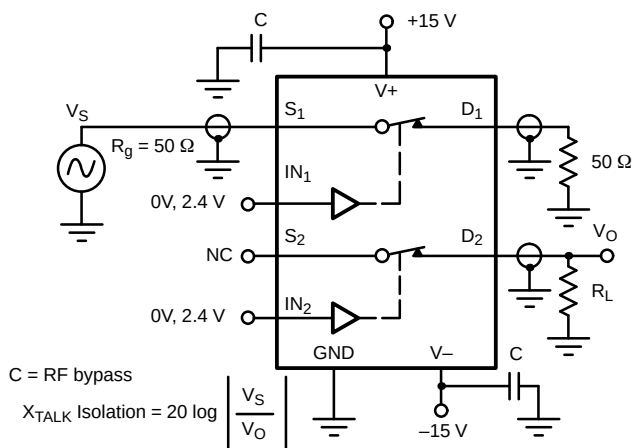
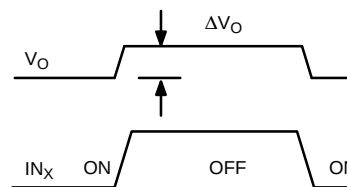
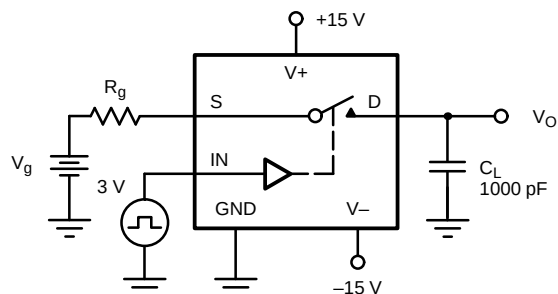
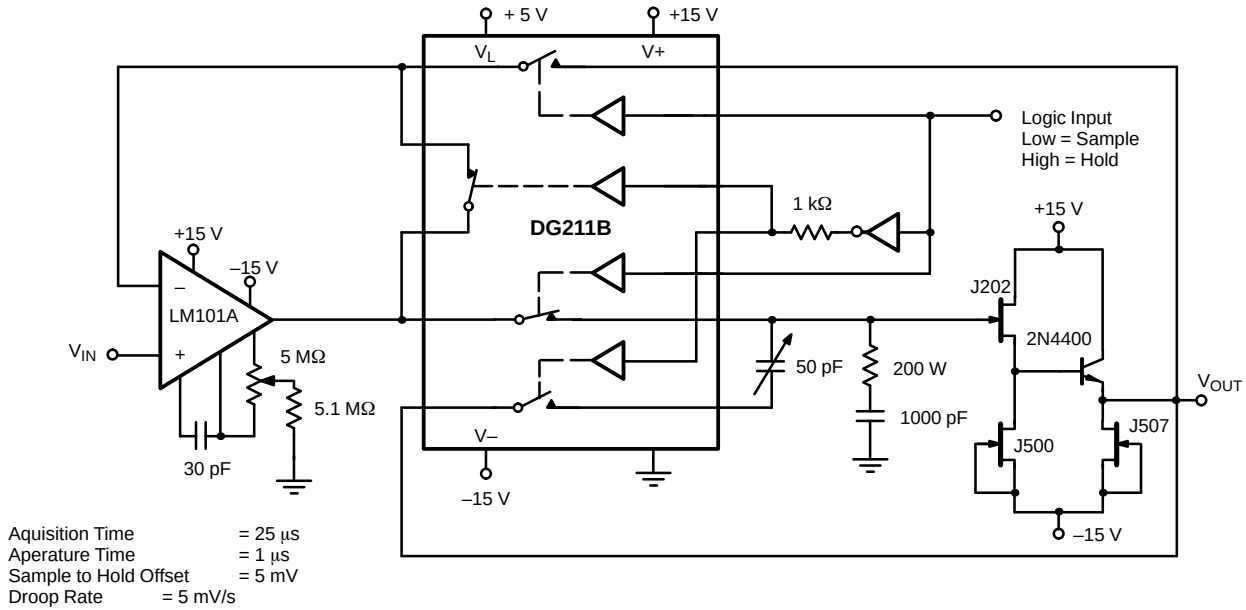
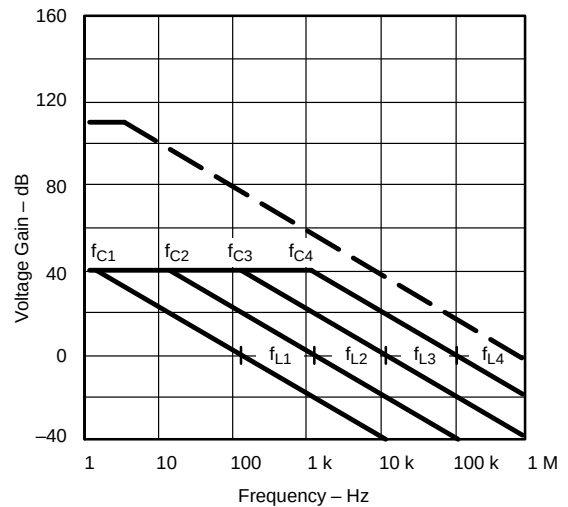
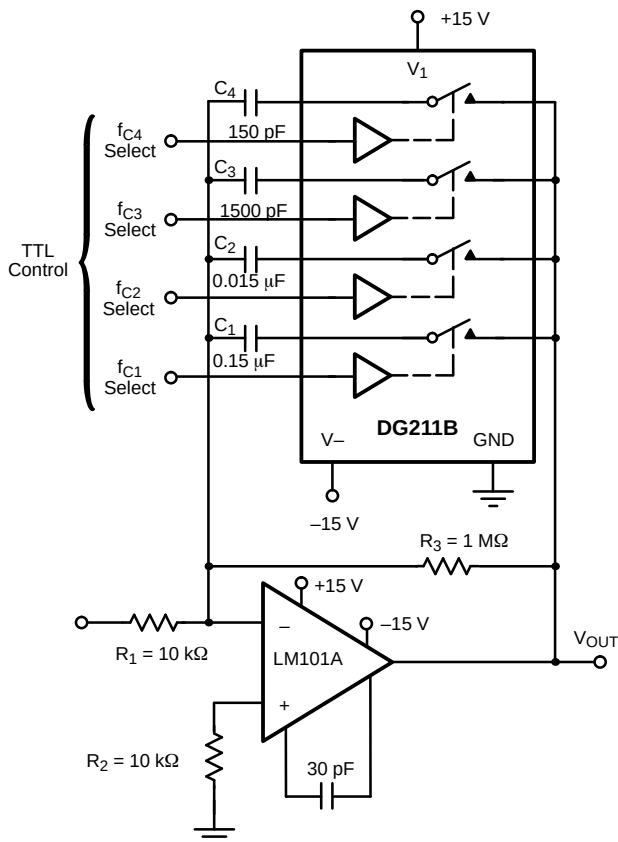


FIGURE 4. Channel-to-Channel Crosstalk



ΔV_O = measured voltage error due to charge injection
 The charge injection in coulombs is $Q = C_L \times \Delta V_O$

FIGURE 5. Charge Injection

APPLICATIONS

FIGURE 6. Sample-and-Hold


$$\begin{aligned}
 A_L \text{ (Voltage Gain Below Break Frequency)} &= \frac{R_3}{R_1} = 100 \text{ (40 dB)} \\
 f_C \text{ (Break Frequency)} &= \frac{1}{2\pi R_3 C_X} \\
 f_L \text{ (Unity Gain Frequency)} &= \frac{1}{2\pi R_1 C_X} \\
 \text{Max Attenuation} &= \frac{f_{DS(on)}}{10 \text{ k}\Omega} \approx -47 \text{ dB}
 \end{aligned}$$

FIGURE 7. Active Low Pass Filter with Digitally Selected Break Frequency

APPLICATIONS

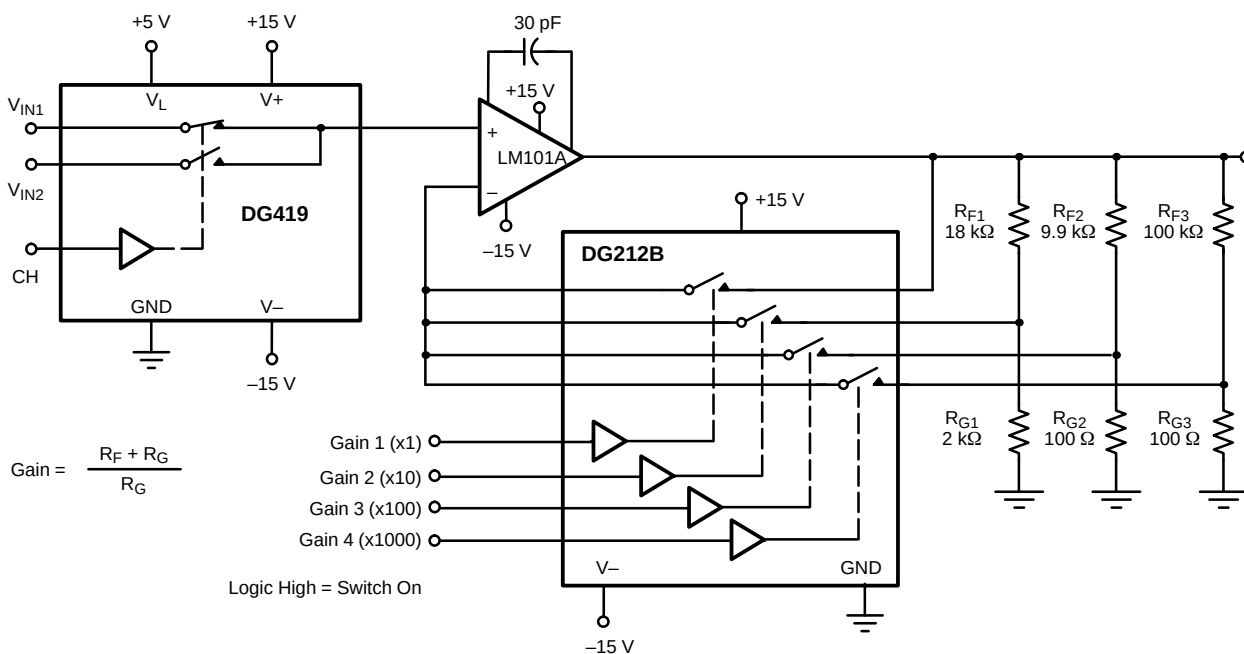


FIGURE 8. A Precision Amplifier with Digitally Programable Input and Gains



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