

16-Ch/Dual 8-Ch High-Performance CMOS Analog Multiplexers

DESCRIPTION

The DG406 is a 16 channel single-ended analog multiplexer designed to connect one of sixteen inputs to a common output as determined by a 4-bit binary address. The DG407 selects one of eight differential inputs to a common differential output. Break-before-make switching action protects against momentary shorting of inputs.

An on channel conducts current equally well in both directions. In the off state each channel blocks voltages up to the power supply rails. An enable (EN) function allows the user to reset the multiplexer/demultiplexer to all switches off for stacking several devices. All control inputs, address (A_x) and enable (EN) are TTL compatible over the full specified operating temperature range.

Applications for the DG406, DG407 include high speed data acquisition, audio signal switching and routing, ATE systems, and avionics. High performance and low power dissipation make them ideal for battery operated and remote instrumentation applications.

Designed in the 44 V silicon-gate CMOS process, the absolute maximum voltage rating is extended to 44 V, allowing operation with ± 20 V supplies. Additionally single (12 V) supply operation is allowed. An epitaxial layer prevents latchup.

For applications information please request documents 70601 and 70604.

FEATURES

- Low on-resistance - $R_{DS(on)}$: 50 Ω
- Low charge injection - Q: 15 pC
- Fast transition time - t_{TRANS} : 200 ns
- Low power: 0.2 mW
- Single supply capability
- 44 V supply max. rating

BENEFITS

- Higher accuracy
- Reduced glitching
- Improved data throughput
- Reduced power consumption
- Increased ruggedness
- Wide supply ranges: ± 5 V to ± 20 V

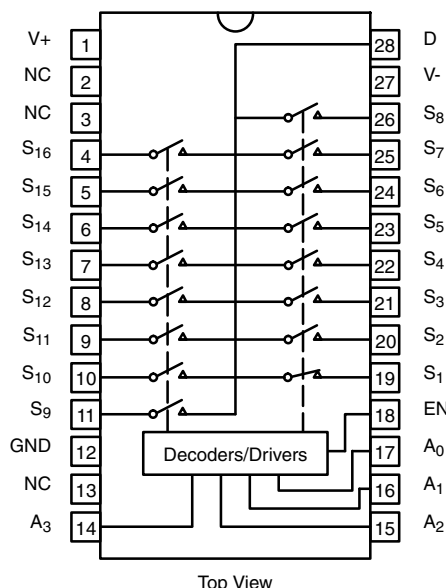
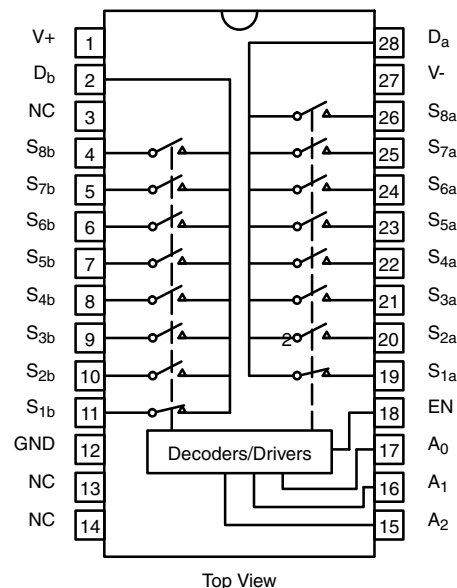
APPLICATIONS

- Data acquisition systems
- Audio signal routing
- Medical instrumentation
- ATE systems
- Battery powered systems
- High-rel systems
- Single supply systems



RoHS*
COMPLIANT

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

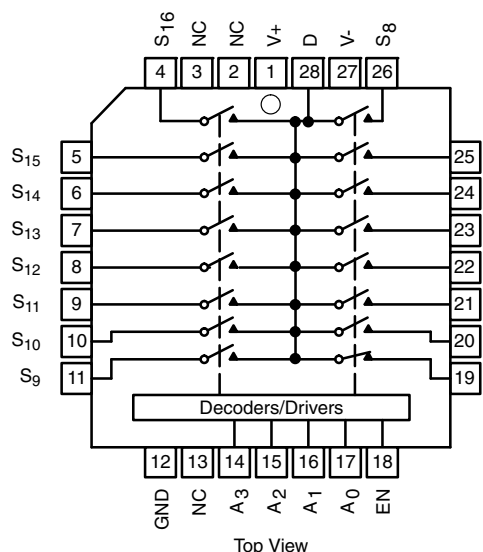
DG406
Dual-In-Line and SOIC Wide-Body

DG407
Dual-In-Line and SOIC Wide-Body


* Pb containing terminations are not RoHS compliant, exemptions may apply

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

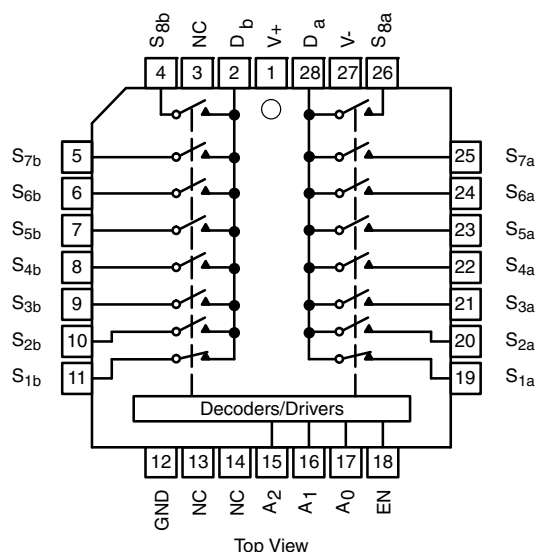
DG406

PLCC and LCC



DG407

PLCC and LCC



TRUTH TABLE (DG406)

A ₃	A ₂	A ₁	A ₀	EN	On Switch
X	X	X	X	0	None
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

TRUTH TABLE (DG407)

A ₂	A ₁	A ₀	EN	On Switch Pair
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Logic "0" = $V_{AL} \leq 0.8 V$
 Logic "1" = $V_{AH} \geq 2.4 V$
 X = Do not Care

ORDERING INFORMATION (DG406)

Temp. Range	Package	Part Number
- 40 °C to 85 °C	28-Pin Plastic DIP	DG406DJ DG406DJ-E3
	28-Pin PLCC	DG406DN DG406DN-T1-E3
	28-Pin Widebody SOIC	DG406DW DG406DW-E3

ORDERING INFORMATION (DG407)

Temp. Range	Package	Part Number
- 40 °C to 85 °C	28-Pin Plastic DIP	DG407DJ DG407DJ-E3
	28-Pin PLCC	DG407DN DG407DN-T1-E3
	28-Pin Widebody SOIC	DG407DW DG407DW-E3



ABSOLUTE MAXIMUM RATINGS			
Parameter		Limit	Unit
Voltages Referenced to V-	V+	44	V
	GND	25	
Digital Inputs ^a , V _S , V _D		(V-) - 2 to (V+) + 2 V or 20 mA, whichever occurs first	
Current (Any terminal)		30	mA
Peak Current, S or D (Pulsed at 1 ms, 10 % duty cycle max.)		100	
Storage Temperature	(AK, AZ Suffix)	- 65 to 150	°C
	(DJ, DN Suffix)	- 65 to 125	
Power Dissipation (Package) ^b	28-Pin Plastic DIP ^b	625	mW
	28-Pin CerDIP ^d	1.2	W
	28-Pin Plastic PLCC ^c	450	mW
	LCC-28 ^e	1.35	W
	28-Pin Widebody SOIC	450	mW

Notes:

- a. Signals on SX, DX or INX exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads soldered or welded to PC board.
- c. Derate 6 mW/°C above 75°C.
- d. Derate 12 mW/°C above 75°C.
- e. Derate 13.5 mW/°C above 75°C .

SPECIFICATIONS ^a											
Parameter	Symbol	Test Conditions Unless Otherwise Specified V ₊ = 15 V, V ₋ = - 15 V V _{AL} = 0.8 V, V _{AH} = 2.4 V ^f		Temp. ^b	Typ. ^c	A Suffix - 55 °C to 125 °C		D Suffix - 40 °C to 85 °C		Unit	
						Min. ^d	Max. ^d	Min. ^d	Max. ^d		
Analog Switch											
Analog Signal Range ^e	V _{ANALOG}			Full		- 15	15	- 15	15	V	
Drain-Source On-Resistance	R _{DS(on)}	V _D = ± 10 V, I _S = - 10 mA sequence each switch on		Room Full	50		100 125		100 125	Ω	
R _{DS(on)} Matching Between Channels ^g	ΔR _{DS(on)}	V _D = ± 10 V		Room	5					%	
Source Off Leakage Current	I _{S(off)}	V _{EN} = 0 V V _D = ± 10 V V _S = ± 10 V		Room Full	0.01	- 0.5 - 50	0.5 50	- 0.5 - 5	0.5 5	nA	
Drain Off Leakage Current	I _{D(off)}			DG406	Room Full	0.04	- 1 - 200	1 200	- 1 - 40		1 40
				DG407	Room Full	0.04	- 1 - 100	1 100	- 1 - 20		1 20
Drain On Leakage Current	I _{D(on)}			DG406	Room Full	0.04	- 1 - 200	1 200	- 1 - 40		1 40
		DG407	Room Full	0.04	- 1 - 100	1 100	- 1 - 20	1 20			
Digital Control											
Logic High Input Voltage	V _{INH}			Full		2.4		2.4		V	
Logic Low Input Voltage	V _{INL}			Full			0.8		0.8		
Logic High Input Current	I _{AH}	V _A = 2.4 V, 15 V		Full		- 1	1	- 1	1	μA	
Logic Low Input Current	I _{AL}	V _{EN} = 0 V, 2.4 V, V _A = 0 V		Full		- 1	1	- 1	1		
Logic Input Capacitance	C _{in}	f = 1 MHz		Room	7					pF	
Dynamic Characteristics											
Transition Time	t _{TRANS}	see figure 2		Room Full	200		350 450		350 450	ns	
Break-Before-Make Interval	t _{OPEN}	see figure 4		Room Full	50	25 10		25 10			
Enable Turn-On Time	t _{ON(EN)}	see figure 3		Room Full	150		200 400		200 400		
Enable Turn-Off Time	t _{OFF(EN)}			Room Full	70		150 300		150 300		
Charge Injection	Q	V _S = 0 V, C _L = 1 nF, R _S = 0 Ω		Room	15					pC	
Off Isolation ^h	OIRR	V _{EN} = 0 V, R _L = 1 kΩ f = 100 kHz		Room	- 69					dB	
Source Off Capacitance	C _{S(off)}	V _{EN} = 0 V, V _S = 0 V, f = 1 MHz		Room	8					pF	
Drain Off Capacitance	C _{D(off)}	V _{EN} = 0 V V _D = 0 V f = 1 MHz		Room	130						
				DG407	Room	65					
DG406	Room			140							
DG407	Room			70							
Power Supplies											
Positive Supply Current	I ₊	V _{EN} = V _A = 0 or 5 V		Room Full	13		30 75		30 75	μA	
Negative Supply Current	I ₋			Room Full	- 0.01	- 1 - 10		- 1 - 10			
Positive Supply Current	I ₊	V _{EN} = 2.4 V, V _A = 0 V		Room Full	50		500 900		500 700		
Negative Supply Current	I ₋			Room Full	- 0.01	- 20 - 20		- 20 - 20			



SPECIFICATIONS ^a (for Single Supply)										
Parameter	Symbol	Test Conditions Unless Otherwise Specified V ⁺ = 12 V, V ⁻ = 0 V V _{AL} = 0.8 V, V _{AH} = 2.4 V ^f		Temp. ^b	Typ. ^c	A Suffix - 55 °C to 125 °C		D Suffix - 40 °C to 85 °C		Unit
		Min. ^d	Max. ^d			Min. ^d	Max. ^d			
Analog Switch										
Analog Signal Range ^e	V _{ANALOG}	V _D = 3 V, 10 V, I _S = - 1 mA sequence each switch on		Full		0	12	0	12	V
Drain-Source On-Resistance	R _{DS(on)}			Room	90		120		120	Ω
R _{DS(on)} Matching Between Channels ^g	ΔR _{DS(on)}			Room	5					%
Source Off Leakage Current	I _{S(off)}	V _{EN} = 0 V		Room	0.01				nA	
Drain Off Leakage Current	I _{D(off)}	V _D = 10 V or 0.5 V		DG406	Room	0.04				
		V _S = 0.5 V or 10 V		DG407	Room	0.04				
Drain On Leakage Current	I _{D(on)}	V _S = V _D = ± 10		DG406	Room	0.04				
		sequence each switch on		DG407	Room	0.04				
Dynamic Characteristics										
Switching Time of Multiplexer	t _{OPEN}	V _{S1} = 8 V, V _{S8} = 0 V, V _{IN} = 2.4 V		Room	300		450		450	ns
Enable Turn-On Time	t _{ON(EN)}	V _{INH} = 2.4 V, V _{INL} = 0 V		Room	250		600		600	
Enable Turn-Off Time	t _{OFF(EN)}	V _{S1} = 5 V		Room	150		300		300	
Charge Injection	Q	C _L = 1 nF, V _S = 6 V, R _S = 0		Room	20					pC
Power Supplies										
Positive Supply Current	I ⁺	V _{EN} = 0 V or 5 V, V _A = 0 V or 5 V		Room Full	13		30 75		30 75	μA
Negative Supply Current	I ⁻			Room Full	- 0.01	- 20 -20		- 20 -20		

Notes:

a. Refer to PROCESS OPTION FLOWCHART.

b. Room = 25 °C, Full = as determined by the operating temperature suffix.

c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.

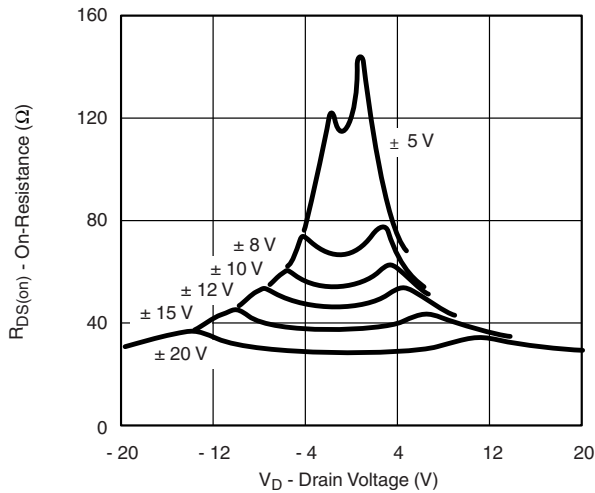
e. Guaranteed by design, not subject to production test.

f. V_{IN} = input voltage to perform proper function.g. $\Delta R_{DS(on)} = R_{DS(on)} \text{ max.} - R_{DS(on)} \text{ min.}$

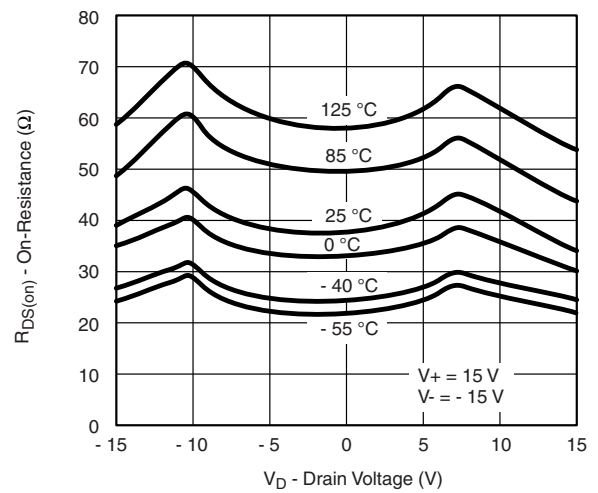
h. Worst case isolation occurs on Channel 4 due to proximity to the drain pin.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

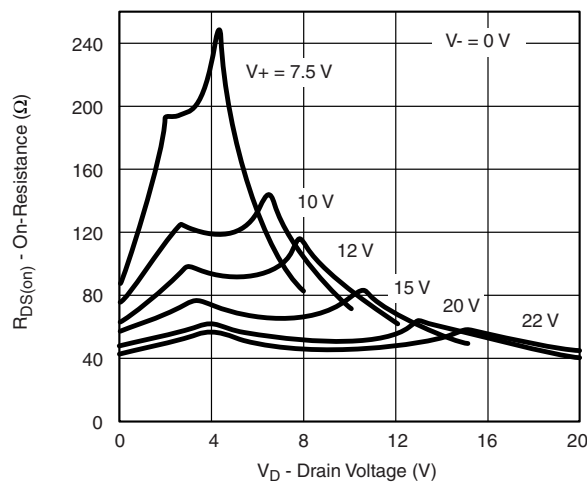
TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)



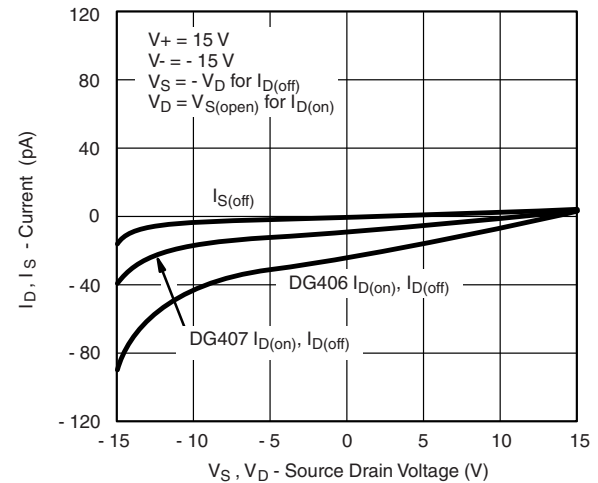
$R_{DS(on)}$ vs. V_D and Supply



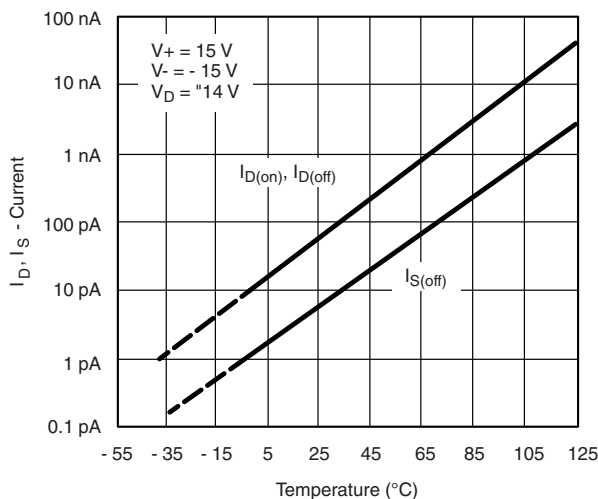
$R_{DS(on)}$ vs. V_D and Temperature



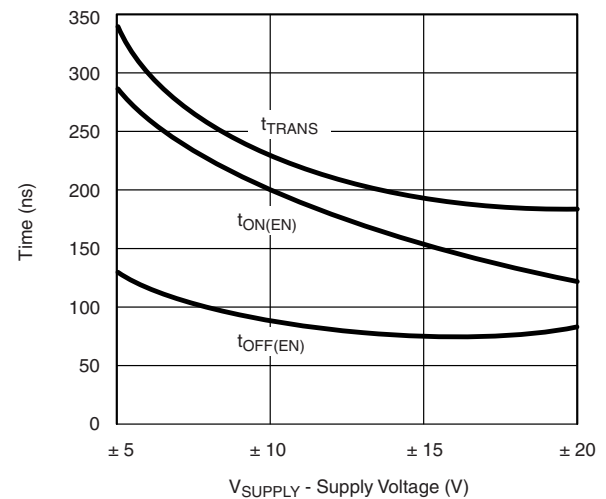
$R_{DS(on)}$ vs. V_D and Supply



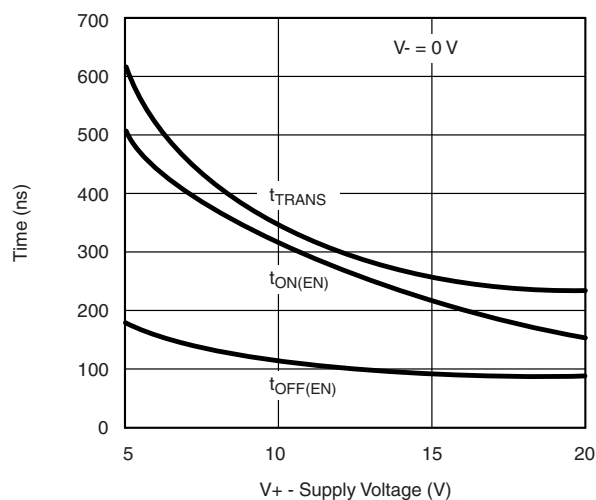
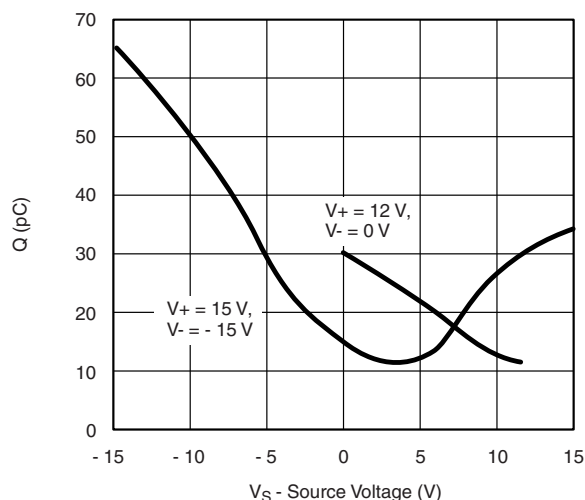
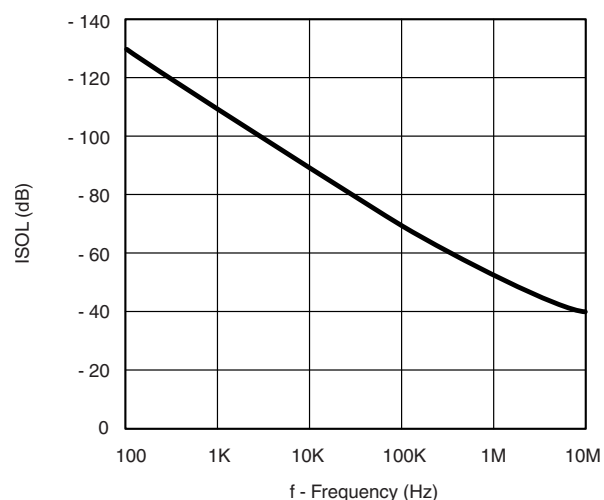
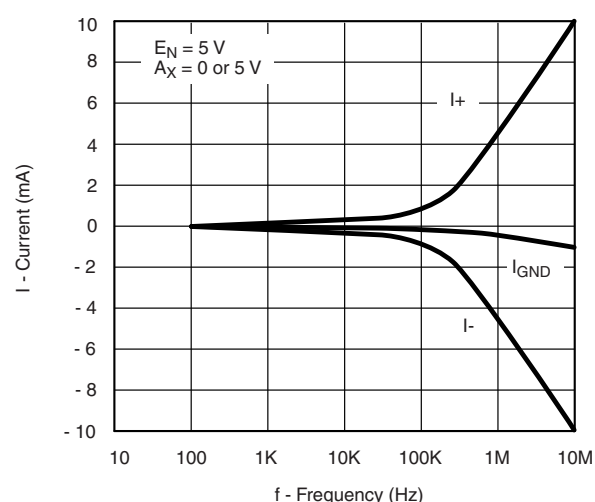
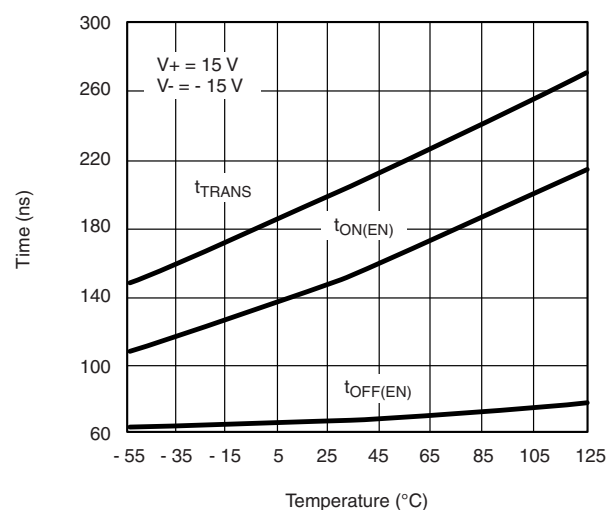
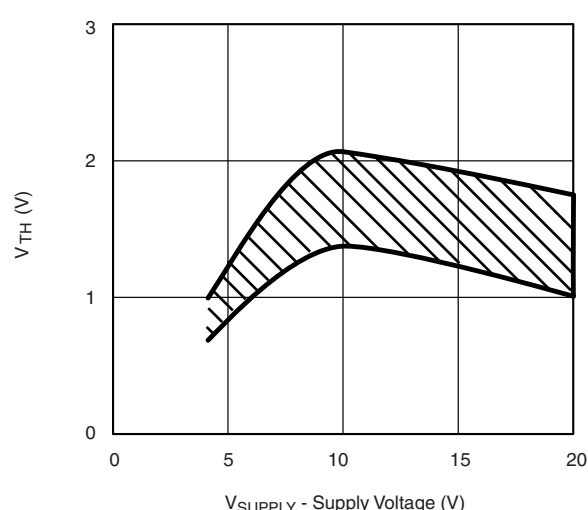
I_D , I_S Leakage Currents vs. Analog Voltage



I_D , I_S Leakages vs. Temperature



Switching Times vs. Bipolar Supplies

TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Switching Times vs. Single Supply

Charge Injection vs. Analog Voltage

Off-Isolation vs. Frequency

Supply Currents vs. Switching Frequency

 $t_{\text{ON}}/t_{\text{OFF}}$ vs. Temperature

Switching Threshold vs. Supply Voltage

SCHEMATIC DIAGRAM (Typical Channel)

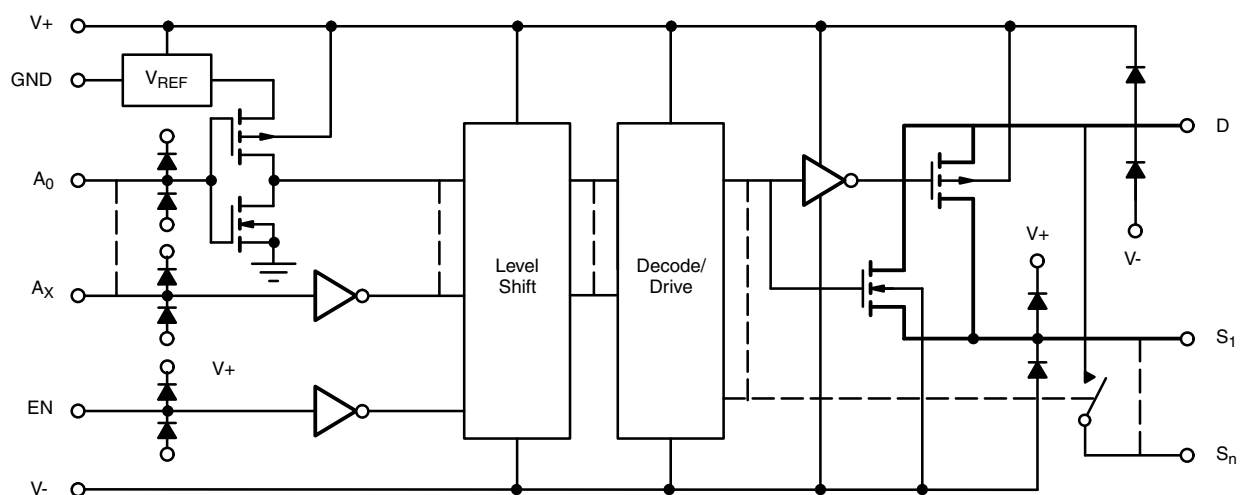
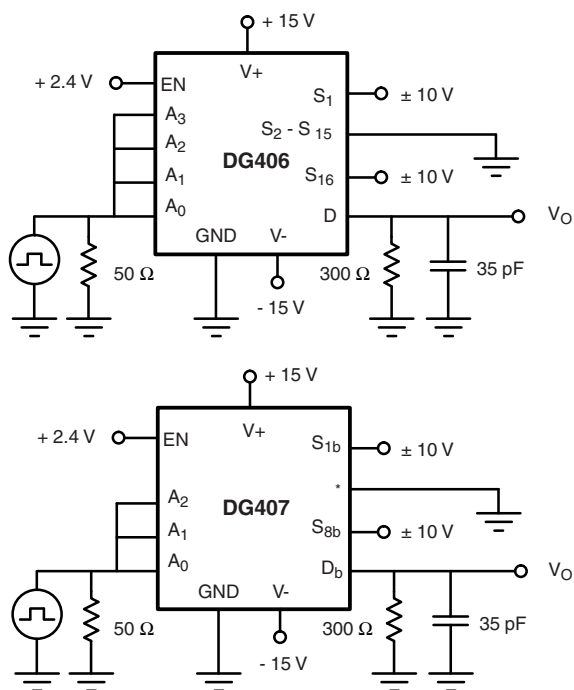


Figure 1.

TEST CIRCUITS



* = S_{1a} - S_{8a}, S_{2b} S_{±7b}, D_a

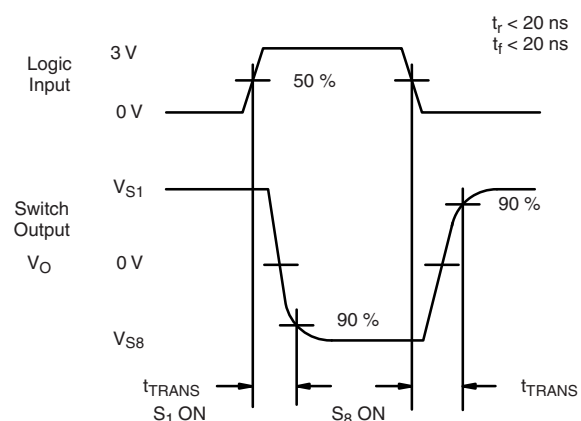


Figure 2. Transition Time

TEST CIRCUITS

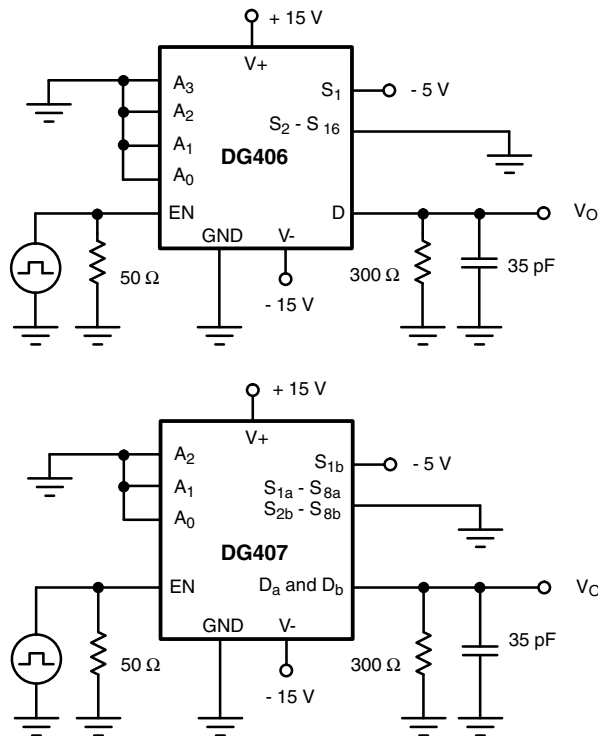


Figure 3. Enable Switching Time

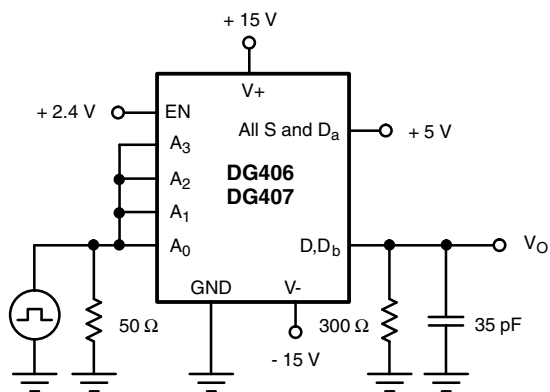
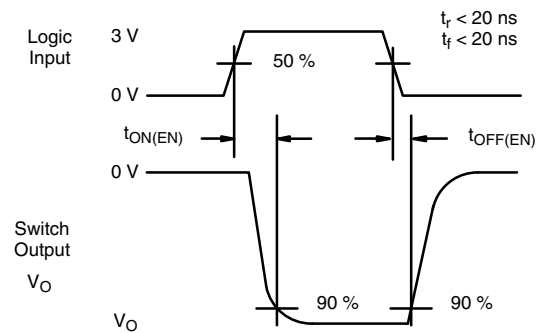
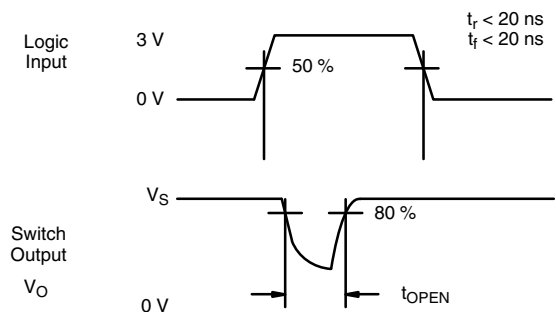


Figure 4. Break-Before-Make Interval



APPLICATIONS HINTS

Sampling speed is limited by two consecutive events: the transition time of the multiplexer, and the settling time of the sampled signal at the output.

t_{TRANS} is given on the data sheet. Settling time at the load depends on several parameters: $R_{\text{DS(on)}}$ of the multiplexer, source impedance, multiplexer and load capacitances, charge injection of the multiplexer and accuracy desired.

The settling time for the multiplexer alone can be derived from the model shown in figure 5. Assuming a low impedance signal source like that presented by an op amp or a buffer amplifier, the settling time of the RC network for a given accuracy is equal to $n\tau$:

% ACCURACY	# BITS	N
0.25	8	6
0.012	12	9
0.0017	15	11

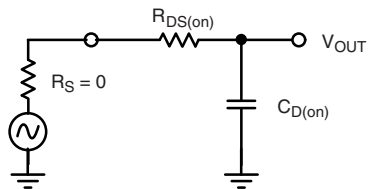


Figure 5. Simplified Model of One Multiplexer Channel

The maximum sampling frequency of the multiplexer is:

$$f_s = \frac{1}{N(t_{\text{SETTLING}} + t_{\text{TRANS}})} \quad (1)$$

where N = number of channels to scan

$t_{\text{SETTLING}} = n\tau = n \times R_{\text{DS(on)}} \times C_{\text{D(on)}}$

For the DG406 then, at room temp and for 12-bit accuracy, using the maximum limits:

$$f_s = \frac{1}{16 (9 \times 100 \Omega \times 10^{-12} \text{F}) + 300 \times 10^{-12} \text{s}} \quad (2)$$

or

$$f_s = 694 \text{ kHz} \quad (3)$$

From the sampling theorem, to properly recover the original signal, the sampling frequency should be more than twice the maximum component frequency of the original signal. This assumes perfect bandlimiting. In a real application sampling at three to four times the filter cutoff frequency is a good practice.

Therefore from equation 2 above:

$$f_c = \frac{1}{4} \times f_s = 173 \text{ kHz} \quad (4)$$

From this we can see that the DG406 can be used to sample 16 different signals whose maximum component frequency can be as high as 173 kHz. If for example, two channels are used to double sample the same incoming signal then its cutoff frequency can be doubled.

The block diagram shown in Figure 6 illustrates a typical data acquisition front end suitable for low-level analog signals. Differential multiplexing of small signals is preferred since this method helps to reject any common mode noise. This is especially important when the sensors are located at a distance and it may eliminate the need for individual amplifiers. A low $R_{\text{DS(on)}}$, low leakage multiplexer like the DG407 helps to reduce measurement errors. The low power dissipation of the DG407 minimizes on-chip thermal gradients which can cause errors due to temperature mismatch along the parasitic thermocouple paths. Please refer to Application Note AN203 for additional information.

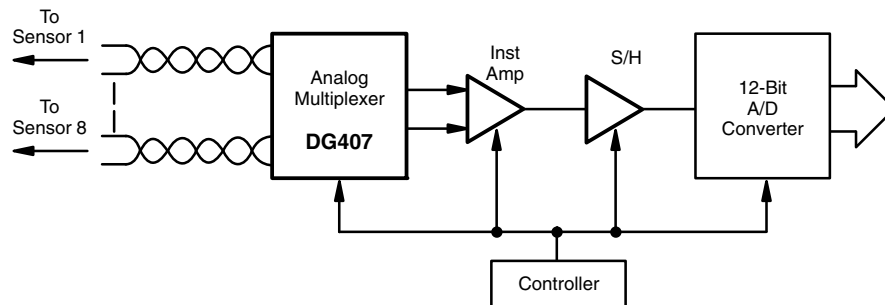


Figure 6. Measuring low-level analog signals is more accurate when using a differential multiplexing technique

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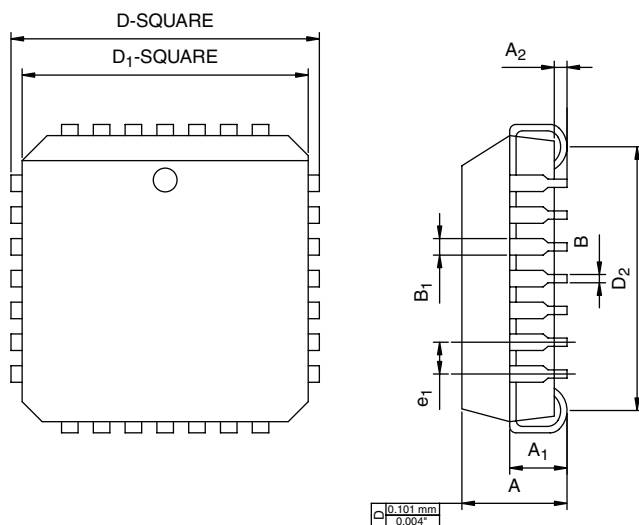
PDIP: 28-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	2.29	5.08	0.090	0.200
A₁	0.39	1.77	0.015	0.070
B	0.38	0.56	0.015	0.022
B₁	0.89	1.65	0.035	0.065
C	0.204	0.30	0.008	0.012
D	35.10	39.70	1.380	1.565
E	15.24	15.88	0.600	0.625
E₁	13.21	14.73	0.520	0.580
e₁	2.29	2.79	0.090	0.110
e_A	14.99	15.49	0.590	0.610
L	2.60	5.08	0.100	0.200
Q₁	0.95	2.345	0.0375	0.0925
S	0.995	2.665	0.0375	0.105

ECN: S-03946—Rev. F, 09-Jul-01
DWG: 5488

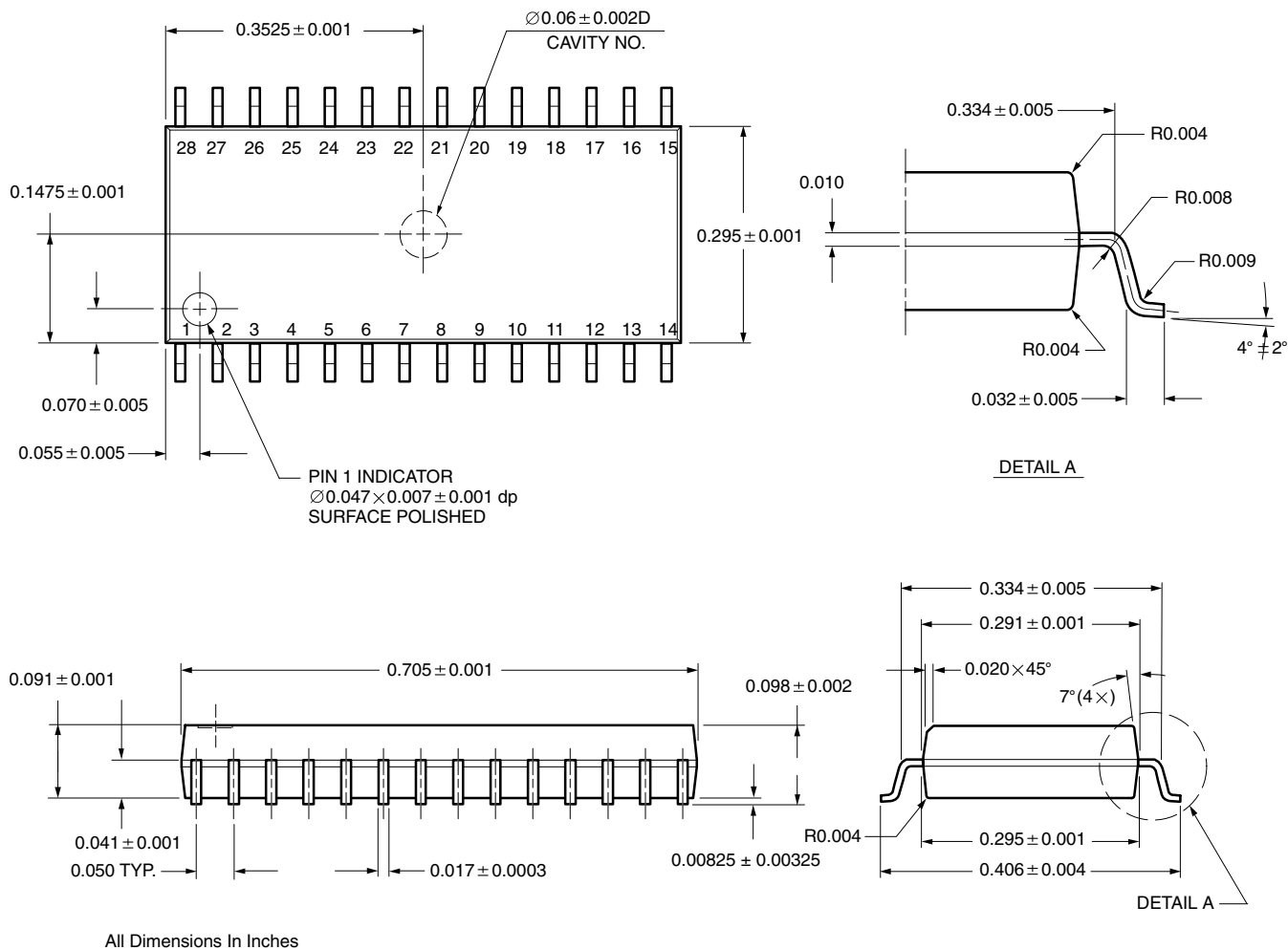
PLCC: 28-LEAD



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.20	4.57	0.165	0.180
A ₁	2.29	3.04	0.090	0.120
A ₂	0.51	-	0.020	-
B	0.331	0.553	0.013	0.021
B ₁	0.661	0.812	0.026	0.032
D	12.32	12.57	0.485	0.495
D ₁	11.430	11.582	0.450	0.456
D ₂	9.91	10.92	0.390	0.430
e ₁	1.27 BSC		0.050 BSC	
ECN: T09-0766-Rev. D, 28-Sep-09 DWG: 5491				



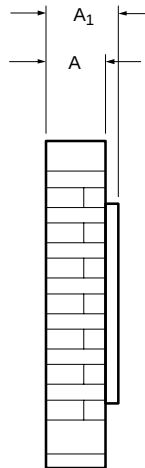
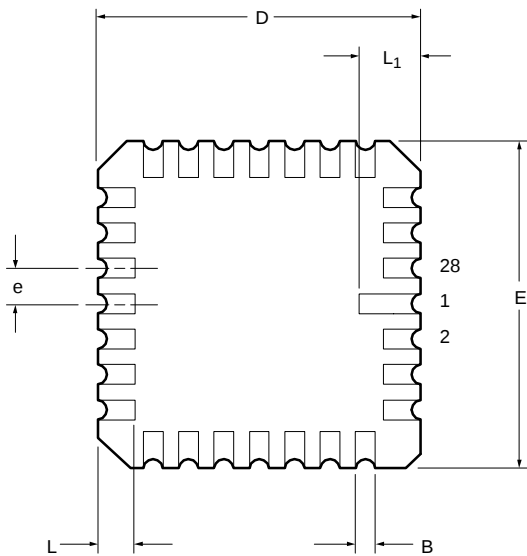
SOIC (WIDE-BODY): 28-LEADS



ECN: E11-2209-Rev. D, 01-Aug-11
DWG: 5850



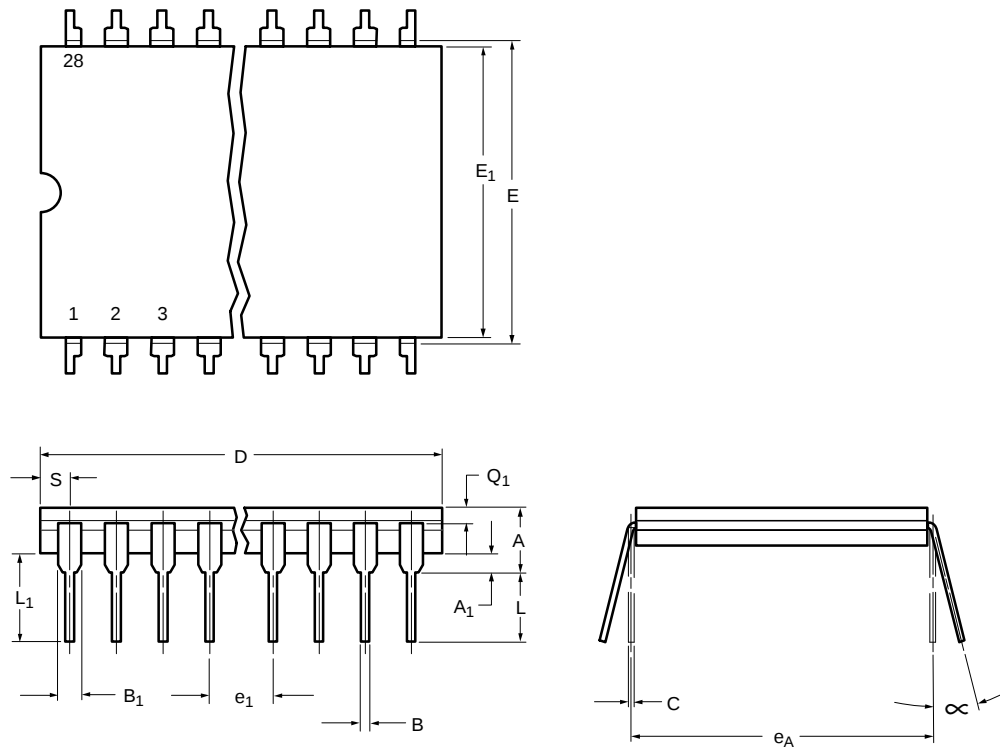
28-LEAD LCC



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.37	2.24	0.054	0.088
A₁	1.63	2.54	0.064	0.100
B	0.56	0.71	0.022	0.028
D	11.23	11.63	0.442	0.458
E	11.23	11.63	0.442	0.458
e	1.27 BSC		0.050 BSC	
L	1.14	1.40	0.045	0.055
L₁	1.96	2.36	0.077	0.093
ECN: S-03946—Rev. B, 09-Jul-01 DWG: 5319				



CERDIP: 28-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	4.06	5.92	0.160	0.232
A ₁	0.38	1.52	0.015	0.060
B	0.38	0.51	0.015	0.020
B ₁	1.14	1.65	0.045	0.065
C	0.20	0.30	0.008	0.012
D	36.58	37.08	1.440	1.460
E	15.24	15.88	0.600	0.625
E ₁	12.95	13.46	0.510	0.530
e ₁	2.54 BSC		0.100 BSC	
e _A	15.24 BSC		0.600 BSC	
L	3.18	3.81	0.125	0.150
L ₁	3.81	5.08	0.150	0.200
Q ₁	1.27	2.16	0.050	0.085
S	1.52	2.29	0.060	0.090
∞	0°	15°	0°	15°
ECN: S-03946—Rev. E, 09-Jul-01 DWG: 5434				



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