

Low-Voltage Dual SPST Analog Switch

DESCRIPTION

The DG9232/9233 is a single-pole/single-throw monolithic CMOS analog device designed for high performance switching of analog signals. Combining low power, high speed (t_{ON} : 35 ns, t_{OFF} : 20 ns), low on-resistance ($r_{DS(on)}$: 20 Ω) and small physical size, the DG9232/9233 is ideal for portable and battery powered applications requiring high performance and efficient use of board space.

The DG9232/9233 is built on Vishay Siliconix's low voltage BCD-15 process. Minimum ESD protection, per Method 3015.7 is 2000 V. An epitaxial layer prevents latchup. Break-before -make is guaranteed for DG9232/9233.

Each switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

BENEFITS

- Reduced Power Consumption
- Simple Logic Interface
- High Accuracy
- Reduce Board Space

FEATURES

- Low Voltage Operation (+ 2.7 to + 5 V)
- Low On-Resistance - $r_{DS(on)}$: 20 Ω
- Fast Switching - t_{ON} : 35 ns, t_{OFF} : 20 ns
- Low Leakage - $I_{COM(on)}$: 200 pA max
- Low Charge Injection - Q_{INJ} : 1 pC
- Low Power Consumption
- TTL/CMOS Compatible
- ESD Protection > 2000 V (Method 3015.7)
- Available in MSOP-8 and SOIC-8

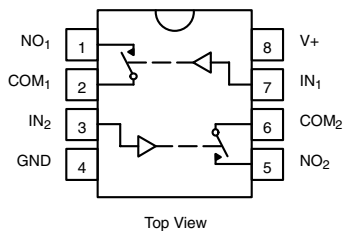
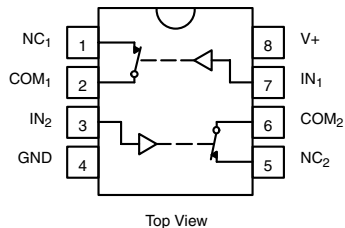


Available
RoHS*
COMPLIANT

APPLICATIONS

- Battery Operated Systems
- Portable Test Equipment
- Sample and Hold Circuits
- Cellular Phones
- Communication Systems
- Military Radio
- PBX, PABX Guidance and Control Systems

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE - DG9232

Logic	Switch
0	ON
1	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

TRUTH TABLE - DG9233

Logic	Switch
0	OFF
1	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

ORDERING INFORMATION

Temp Range	Package	Part Number
- 40 to 85 $^{\circ}$ C	SOIC-8	DG9232DY DG9232DY-E3 DG9232DY-T1 DG9232DY-T1-E3
		DG9233DY DG9233DY-E3 DG9233DY-T1 DG9233DY-T1-E3
	MSOP-8	DG9232DQ-T1-E3
		DG9233DQ-T1-E3

* Pb containing terminations are not RoHS compliant, exemptions may apply

ABSOLUTE MAXIMUM RATINGS

Parameter	Limit	Unit
Reference V+ to GND	- 0.3 to + 13	V
IN, COM, NC, NO ^a	- 0.3 to (V+ + 0.3)	
Continuous Current (Any terminal)	± 20	mA
Peak Current (Pulsed at 1 ms, 10 % duty cycle)	± 40	
ESD (Method 3015.7)	> 2000	V
Storage Temperature	D Suffix	°C
Power Dissipation (Packages) ^b	8-Pin Narrow Body SOIC ^c	mW

Notes:

a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

b. All leads welded or soldered to PC Board.

c. Derate 6.5 mW/°C above 70 °C.

SPECIFICATIONS (V+ = 3 V)

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ± 10 %, V _{IN} = 0.8 V or 2.4 V ^e	Temp ^a	D Suffix - 40 to 85 °C			Unit
				Min ^c	Typ ^b	Max ^c	
Analog Switch							
Analog Signal Range ^d	V _{ANALOG}		Full	0		3	V
Drain-Source On-Resistance	r _{DS(on)}	V _{NO} or V _{NC} = 1.5 V, V+ = 2.7 V I _{COM} = 5 mA	Room Full		30	50 80	Ω
r _{DS(on)} Match ^d	Δr _{DS(on)}	V _{NO} or V _{NC} = 1.5 V	Room		0.4	2	
r _{DS(on)} Flatness ^d	r _{DS(on)} Flatness	V _{NO} or V _{NC} = 1 and 2 V	Room		4	8	
NO or NC Off Leakage Current ^g	I _{NO/NC(off)}	V _{NO} or V _{NC} = 1 V/2 V, V _{COM} = 2 V/1 V	Room Full	- 100 - 5000	5	100 5000	pA
COM Off Leakage Current ^g	I _{COM(off)}	V _{COM} = 1 V/2 V, V _{NO} or V _{NC} = 2 V/1 V	Room Full	- 100 - 5000	5	100 5000	
Channel-On Leakage Current ^g	I _{COM(on)}	V _{COM} = V _{NO} or V _{NC} = 1 V/2 V	Room Full	- 200 - 10000	10	200 10000	
Digital Control							
Input Current	I _{INL} or I _{INH}		Full		1		μA
Dynamic Characteristics							
Turn-On Time	t _{ON}	V _{NO} or V _{NC} = 1.5 V	Room Full		50	120 200	ns
Turn-Off Time	t _{OFF}		Room Full		20	50 120	
Charge Injection ^d	Q _{INJ}	C _L = 1 nF, V _{GEN} = 0 V, R _{GEN} = 0 Ω	Room		1	5	pC
Off-Isolation	OIRR	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz	Room		- 74		dB
Crosstalk	X _{TALK}		Room		- 90		
NC and NO Capacitance	C _{S(off)}	f = 1 MHz	Room		7		pF
Channel-On Capacitance	C _{COM(on)}		Room		20		
COM-Off Capacitance	C _{COM(off)}		Room		13		
Power Supply							
Positive Supply Range	V+			2.7		12	V
Power Supply Current	I+	V+ = 3.3 V, V _{IN} = 0 or 3.3 V				1	μA

Notes:

a. Room = 25 °C, Full = as determined by the operating suffix.

b. Typical values are for design aid only, not guaranteed nor subject to production testing.

c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.

d. Guarantee by design, nor subjected to production test.

e. V_{IN} = input voltage to perform proper function.

f. Difference of min and max values.

g. Guaranteed by 5-V leakage tests, not production tested.



SPECIFICATIONS (V+ = 5 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 5 V, ± 10 %, VIN = 0.8 V or 2.4 V ^e	Temp ^a	D Suffix - 40 to 85°C			Unit
				Min ^c	Typ ^b	Max ^c	
Analog Switch							
Analog Signal Range ^d	VANALOG		Full	0		5	V
Drain-Source On-Resistance	rDS(on)	VNO or VNC = 3.5 V, V+ = 4.5 V ICOM = 5 mA	Room Full		20	30 50	Ω
rDS(on) Match ^d	ΔrDS(on)	VNO or VNC = 3.5 V	Room		0.4	2	
rDS(on) Flatness ^d	rDS(on) Flatness	VNO or VNC = 1, 2 and 3 V	Room		2	6	
NO or NC Off Leakage Current ^g	INO/NC(off)	VNO or VNC = 1 V/4 V, VCOM = 4 V/1 V	Room Full	- 100 - 5000	10	100 5000	pA
COM Off Leakage Current	ICOM(off)	VCOM = 1 V/4 V, VNO or VNC = 4 V/1 V	Room Full	- 100 - 5000	10	100 5000	
Channel-On Leakage Current	ICOM(on)	VCOM = VNO or VNC = 1 V/4 V	Room Full	- 200 - 10000		200 10000	
Digital Control							
Input Current	IINL or IINH		Full		1		μA
Dynamic Characteristics							
Turn-On Time	tON	VNO or VNC = 3.0 V	Room Full		35	75 150	ns
Turn-Off Time	tOFF		Room Full		20	50 100	
Charge Injection ^d	QINJ	CL = 1 nF, VGEN = 0 V, RGEN = 0 Ω	Room		2	5	pC
Off-Isolation	OIRR	RL = 50 Ω, CL = 5 pF, f = 1 MHz	Room		- 74		dB
Crosstalk	XTALK		Room		- 90		
NC and NO Capacitance	C(off)	f = 1 MHz	Room		7		pF
Channel-On Capacitance	CD(on)		Room		20		
COM-Off Capacitance	CD(off)		Room		13		
Power Supply							
Positive Supply Range	V+			2.7		12	V
Power Supply Current	I+	V+ = 5.5 V, VIN = 0 or 5.5 V				1	μA

Notes:

a. Room = 25 °C, Full = as determined by the operating suffix.

b. Typical values are for design aid only, not guaranteed nor subject to production testing.

c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.

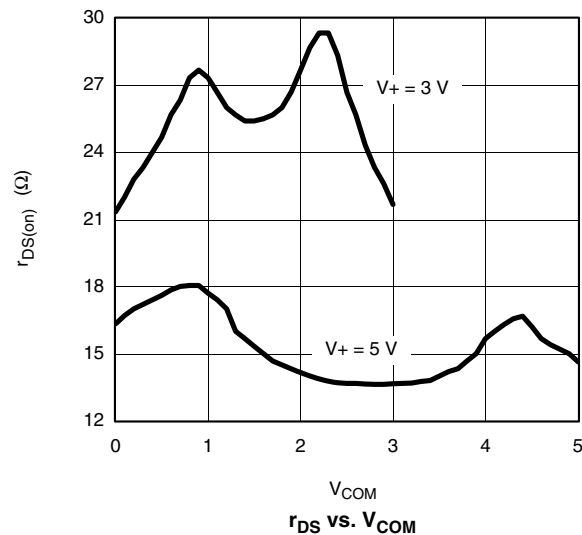
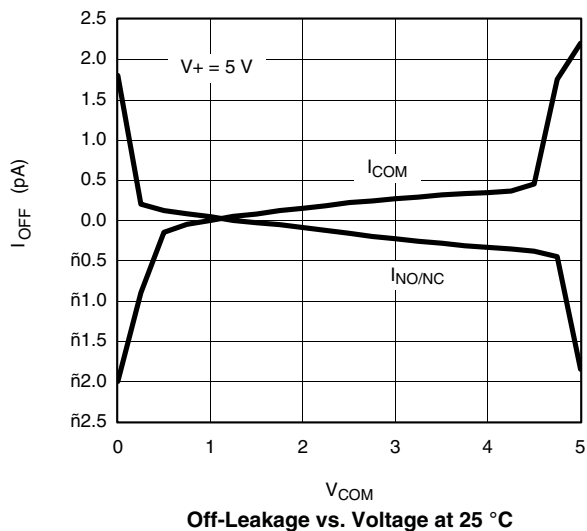
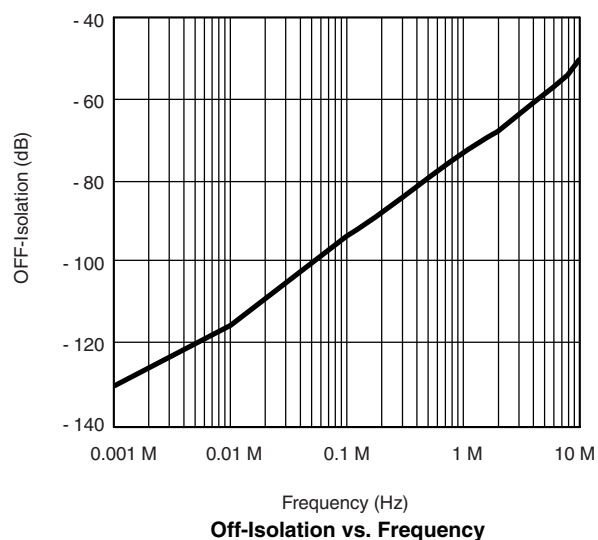
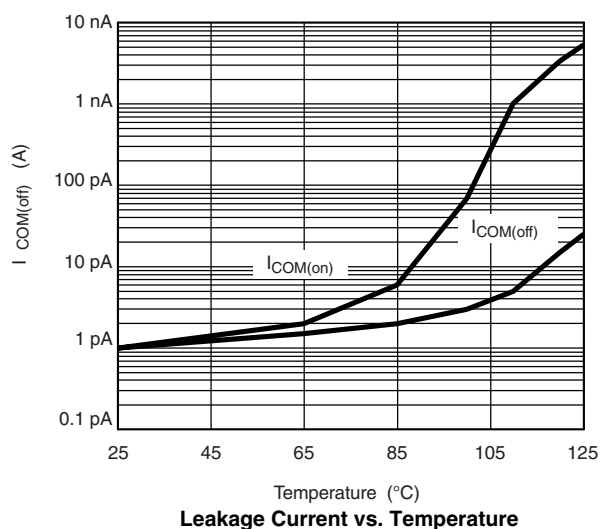
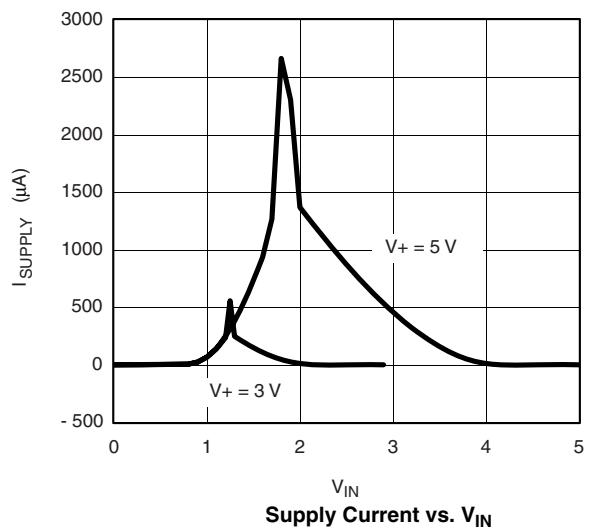
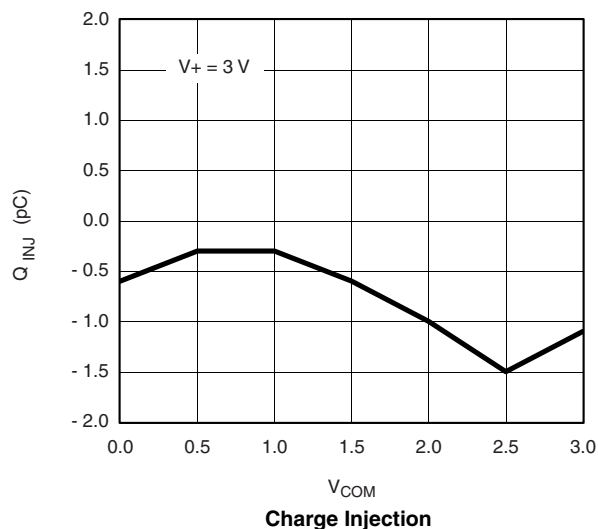
d. Guarantee by design, nor subjected to production test.

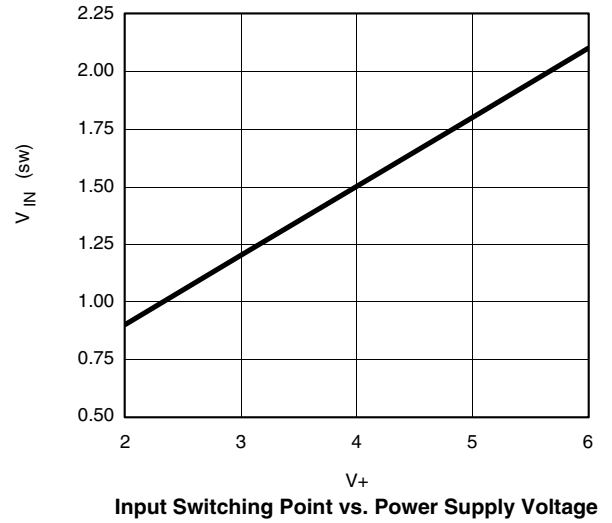
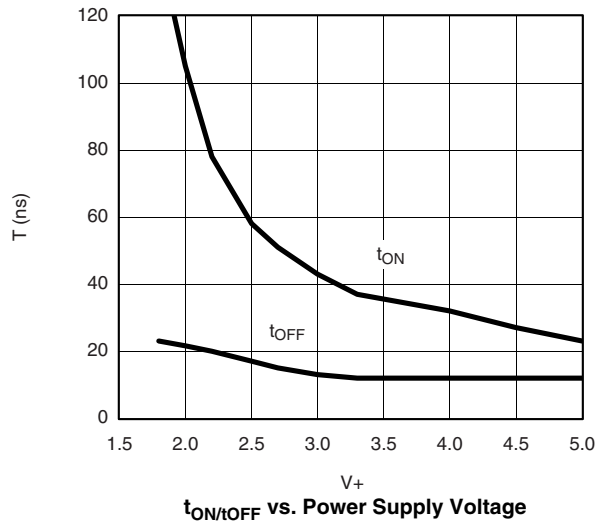
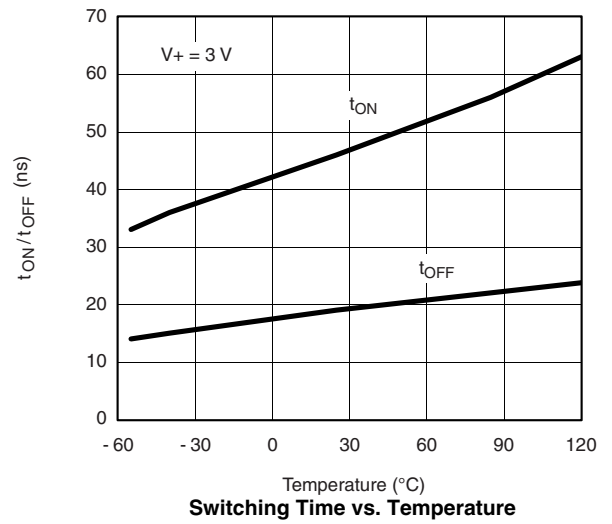
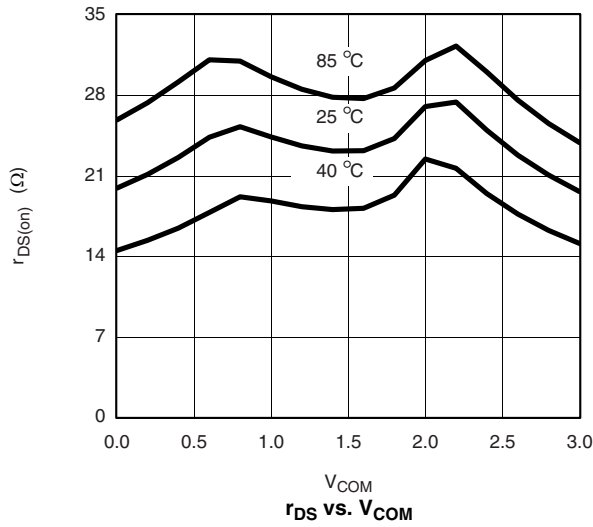
e. V_{IN} = input voltage to perform proper function.

f. Difference of min and max values.

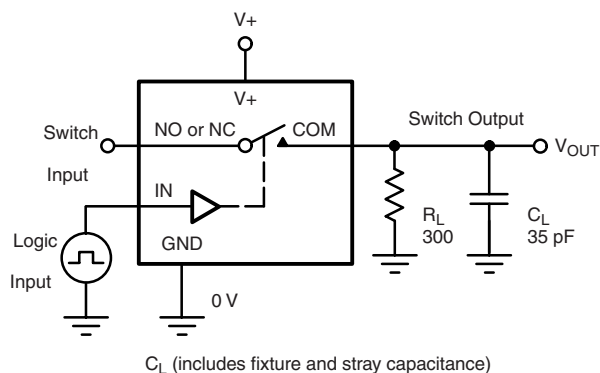
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, unless otherwise noted

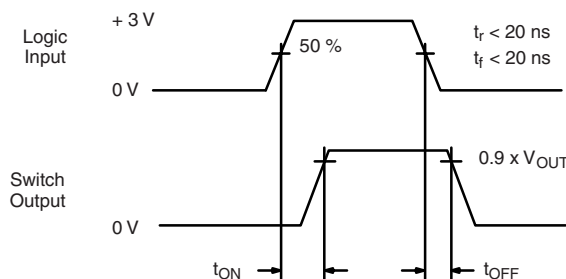


TYPICAL CHARACTERISTICS $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted


TEST CIRCUITS



$$V_{OUT} = V_{COM} \left(\frac{R_L}{R_L + R_{ON}} \right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

Figure 1. Switching Time

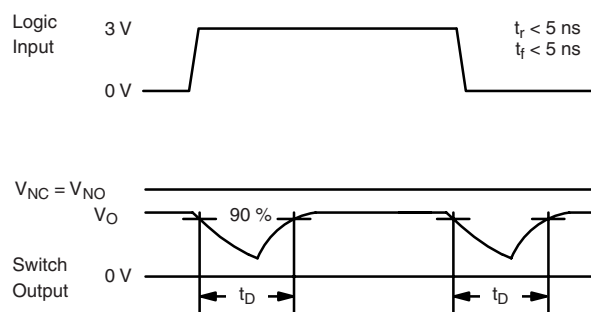
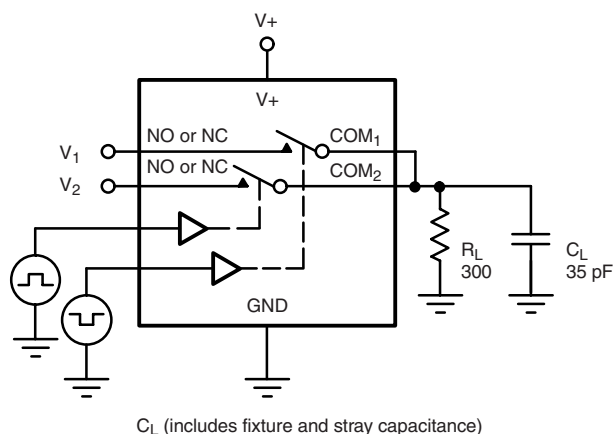
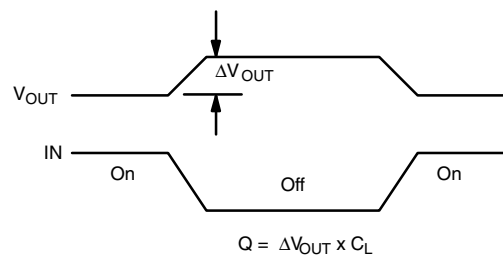
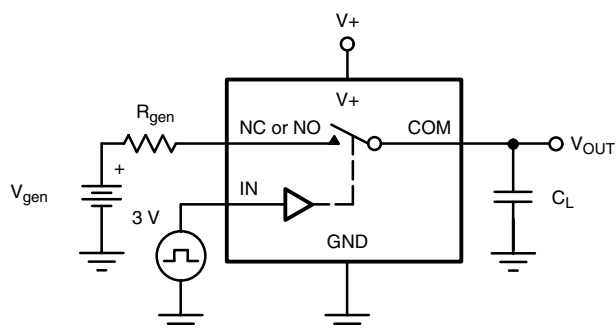
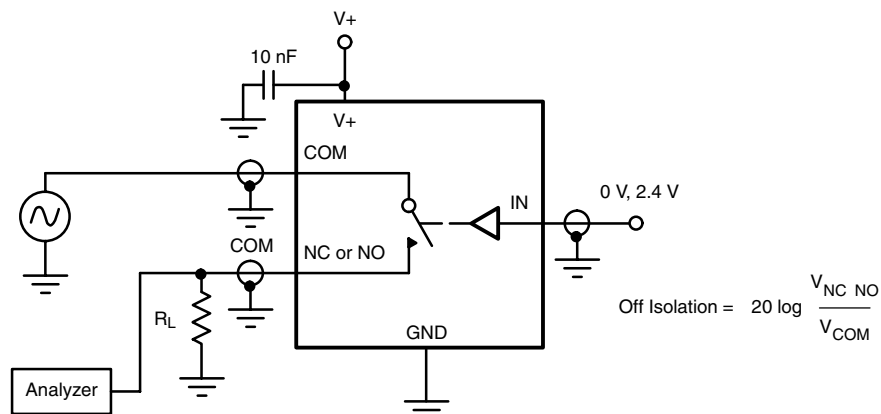
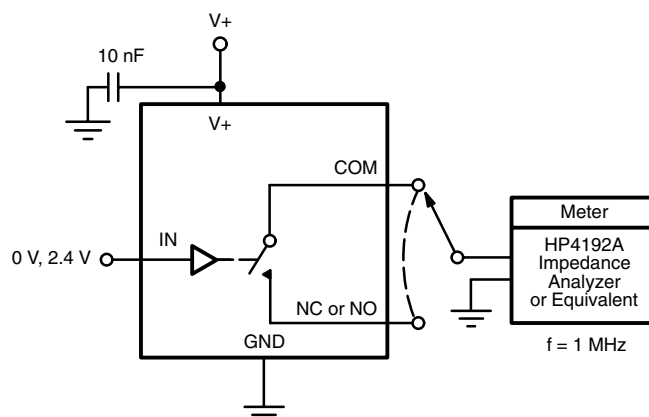


Figure 2. Break-Before-Make Interval



IN depends on switch configuration: input polarity determined by sense of switch.

Figure 3. Charge Injection

TEST CIRCUITS

Figure 4. Off-Isolation

Figure 5. Channel Off/On Capacitance

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